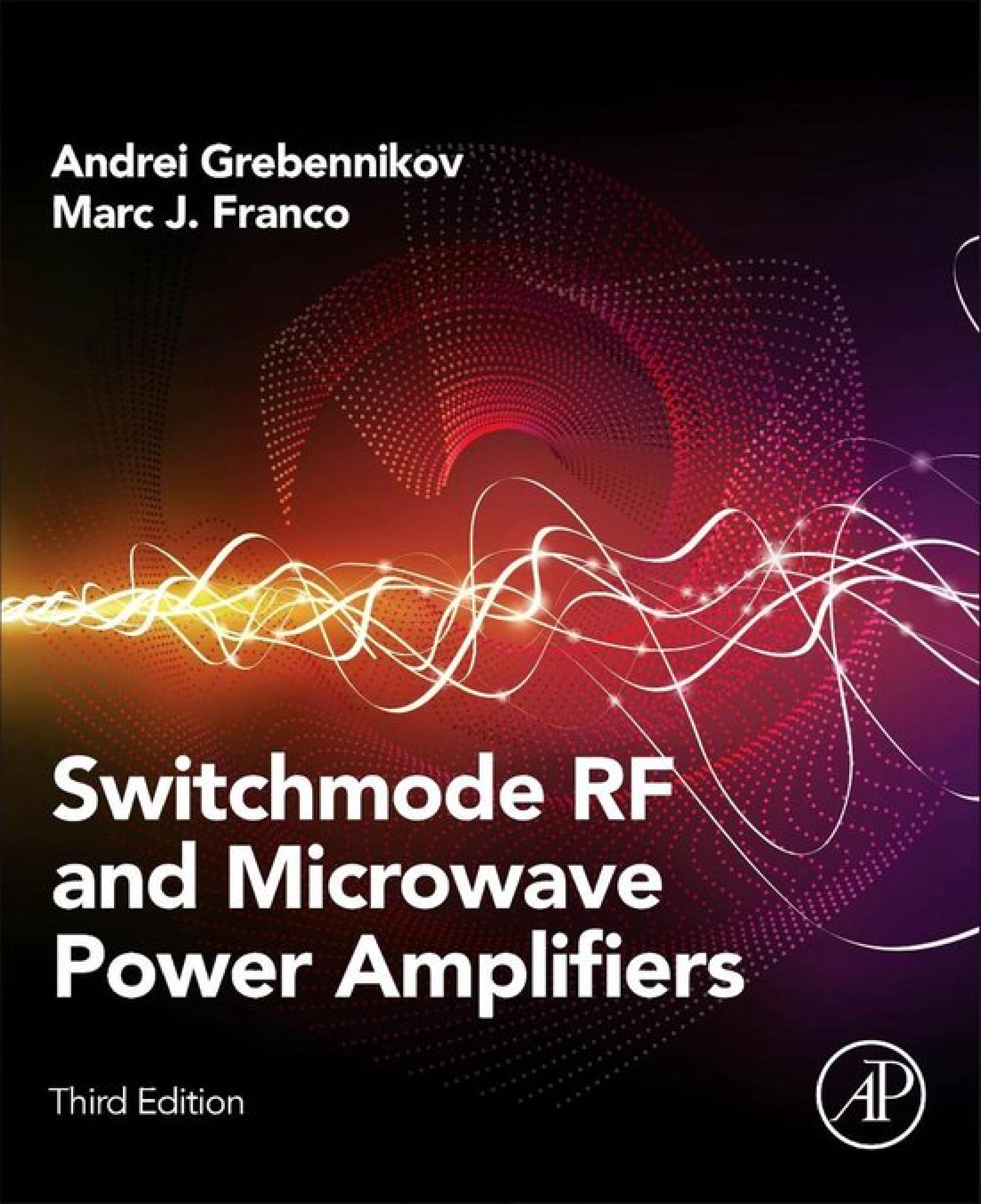

Andrei Grebennikov
Marc J. Franco

Switchmode RF and Microwave Power Amplifiers

Third Edition

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Preface

The main objective of this book is to present all relevant information required to design high efficiency RF and microwave power amplifiers, including well-known and novel theoretical approaches and practical design techniques. Regardless of the different operation classes like Class-D, Class-E, or Class-F, and their combination, an efficiency improvement is achieved by providing the nonlinear operation conditions when an active device can subsequently operate in pinch-off, active, and saturation regions resulting in nonsinusoidal collector current and voltage waveforms, for example, symmetrical for Class-F and asymmetrical for Class-E modes. As a result, the power amplifiers operated in Class-F can be analyzed explicitly in the frequency domain when the harmonic load impedances are optimized by short-circuit and open-short terminations to control the voltage and current waveforms at the collector to obtain maximum efficiency. However, the power amplifier operated in Class-E can be fully analyzed analytically in the time domain when an efficiency improvement is achieved by realizing the ideal on-to-off active device operation in only pinch-off and voltage-saturation modes only so that high voltage and high current at the collector do not occur at the same time. Unlike the single-ended power amplifiers operated in Class-F or Class-E modes, a Class-D power amplifier represents a switching-mode power amplifier using two switching-mode active devices driven on and off that one of the switches is turned on when the other is turned off, and vice versa. Since the transmitting signal is characterized by a high peak-to-average power ratio in modern wireless communication systems with increased bandwidth and high data rate when improving efficiency and linearity simultaneously have become critical, several analog and digital techniques are described to minimize the distortion of high-efficiency RF and microwave power amplifier.

Generally, this book is intended for and can be recommended to practicing RF circuit designers and engineers as an anthology of a wide family of high efficiency RF and microwave power amplifiers based on both well-known and novel switched-mode operation conditions with detailed description of their operational principles and applications and clear practical demonstration of theoretical results. To bridge the theoretical idealized results with real practical implementation, the theory is supported by design examples, in which the optimum design approaches combine effectively analytical calculations and simulation, resulting in practical schematics of high efficiency power amplifier circuits using different types of field-effect or bipolar transistors.

The third edition of the book is a continuation of its first edition entitled *Switchmode RF Power Amplifiers* (published in 2007) and the extended second edition entitled *Switchmode RF and Microwave Power Amplifiers* (published in 2012), which were written together with Nathan Sokal who is well known for introducing the Class-E high-efficiency power amplifier to RF and microwave community in the mid-1970s, with his priceless contribution to our books. To our great regret, Nathan Sokal died on May 8, 2016, therefore we dedicated the recollections notes to honor his memory written by his close friend and colleague Dr. Frederick Raab, which are preceding the main material of the book.

The introductory Chapter 1 describes the basic principles of power amplifiers design procedures. Based on the spectral-domain analysis, the concept of a conduction angle is introduced with simple and clear analyses of the basic Classes-A, AB, B, and C of the power-amplifier operation. Nonlinear models are given for MOSFET, MESFET, HEMT, and bipolar devices (including HBTs), which have good prospects for power amplifiers using modern microwave monolithic integrated circuits. The effect of the device input parameters on the conduction angle at high frequencies is explained. The concept and design of push-pull amplifiers using balanced transistors are presented. The possibility of the maximum power gain for a stable power amplifier is discussed and analytically derived. The parasitic parametric effect due to the nonlinear collector capacitance and measures for its cancellation in practical power amplifier are discussed. Finally the basics of the load-pull characterization and distortion fundamentals are presented.

In Chapter 2, the voltage- and current-switching configurations of Class-D power amplifiers are presented, the increased efficiency of which is a result of operating the active devices as switches. The basic switched-mode power amplifiers with resistive load of different configurations as well as the current- and voltage-switching configurations based on complementary and transformer-coupled topologies are analyzed. The effects of the transistor saturation resistance, rectangular and sinusoidal driving signals, nonzero switching transition times, and parasitic shunt capacitance and series inductance are demonstrated. Practical design examples of voltage- and current-switching Class-D power amplifiers that are intended to operate at high frequencies and microwaves are described. Finally, a high-frequency Class-S amplification architecture using a switching-mode Class-D power amplifier to efficiently amplify digitally modulated transmitting signal is shown and discussed.

Highly efficient operation of the power amplifier can be obtained by applying biharmonic or polyharmonic modes when an additional single-resonant or multiresonant circuit tuned to the odd harmonics of the fundamental frequency is added to the load network. An infinite number of odd-harmonic resonators results in an idealized Class-F mode with a square voltage waveform and a half-sinusoidal current waveform at the device output terminal providing ideally 100% collector (or drain) efficiency. Chapter 3 describes the different Class-F techniques using lumped and transmission-line elements including a quarterwave transmission line. The effects of the transistor saturation resistance and parasitic shunt capacitance are demonstrated. Design examples and practical RF and microwave Class-F power amplifiers are given and discussed.

An inverse Class-F mode can be obtained by using a single-resonant or a multiresonant circuit tuned to the even harmonics of the fundamental frequency added to the load network. An infinite number of even-harmonic resonators results in an idealized inverse Class-F mode with a half-sinusoidal voltage waveform and a square current waveform at the device output terminal. Chapter 4 describes the different inverse Class-F techniques using lumped and transmission-line elements including a quarterwave transmission line. Design examples and practical RF and microwave inverse Class-F power amplifiers are presented.

The switchmode Class-E tuned power amplifiers with a shunt capacitance have found widespread application due to their design simplicity and high efficiency operation. In a Class-E power amplifier, the transistor operates as an on/off switch and the shapes and relative timing of the current and voltage waveforms are such that high current and high voltage do not occur simultaneously. That minimizes the power dissipation and maximizes the power-amplifier efficiency. Chapter 5 presents the historical aspect and modern trends of Class-E power amplifier design. Different circuit configurations and load-network techniques using the push-pull mode, with lumped and transmission-line elements are analyzed. The effects of the device saturation resistance, finite switching times, and nonlinear shunt capacitance are described. Practical RF and microwave Class-E power amplifiers and their applications are given and discussed.

In Chapter 6, we discuss and analyze the switchmode second-order Class-E configurations with one capacitor and one inductor and generalized load network including the finite dc-feed inductance, shunt capacitance and series reactance. The results of the Fourier analysis and derivation of the equations for the idealized operation of the circuit are presented. Effects of the device output bondwire inductance on the optimum circuit parameters are demonstrated. The possibilities to realize a Class-E approximation with transmission lines and broadband Class-E load networks are shown and discussed. The operating power gain of a parallel-circuit Class-E power amplifier is evaluated and compared with the operating power gain of a conventional Class-B power amplifier. Circuit design examples and practical implementations of CMOS Class-E power amplifiers are also given.

Chapter 7 presents the results of exact time-domain analysis of the switched-mode tuned Class-E power amplifiers with a quarterwave transmission line. The load-network parameters are derived analytically. The idealized collector voltage and current waveforms demonstrate the possibility of 100% efficiency. Different load-network implementations are considered, including output matching circuit at RF and microwave frequencies, using lumped and transmission-line elements. Accurate derivation of the matching circuit parameters is provided. Switchmode Class-E power amplifiers with a quarterwave transmission line offer a new challenge for RF and microwave power amplification, providing high efficiency and harmonic suppression.

An analysis of a Class-E mode with shunt capacitance and shunt filter with explicit derivation of the idealized optimum voltage and current waveforms and load-network parameters with their verification by frequency-domain simulations is presented in Chapter 8. The ideal collector voltage and current waveforms demonstrate a possibility of 100% efficiency. A multiplicity of solutions for the load-network parameters can be achieved for Class-E with shunt capacitance and shunt filter when an additional reactance is introduced between the shunt filter and the load, which can generally have inductive, zero, or capacitive reactance. Several practical implementations of the Class-E power amplifier with shunt filter and series reactance with load networks based on lumped elements and transmission lines at different operating frequencies are described.

In Chapter 9, the reactance compensation technique applied to the circuits with lumped elements and transmission lines to provide a broadband operation of Class-E power amplifiers is introduced and analyzed. This technique can be directly used to design a parallel-circuit Class-E power amplifier because its load network configuration has the same structure with shunt and series resonant circuits. Different circuit configurations and Class-E load-network techniques corresponding to broadband high-power RF power amplifiers operating in VHF and UHF bands, microwave monolithic integrated circuits of power amplifiers, and CMOS power amplifiers operating in a wide frequency range with high efficiency are given and described.

Chapter 10 presents alternative and mixed-mode configurations of high-efficiency power amplifiers. The Class-DE power amplifier is the combination of a voltage-switching Class-D mode and Class-E switching conditions, and thus extending the switching Class-D operation to higher frequencies. The switchmode Class-E/F power amplifier can provide lower peak voltage on the switch, while providing the Class-E zero voltage and zero voltage-derivative switching conditions required to eliminate capacitor-discharge power dissipation. This is achieved by harmonic tuning using resonant circuits tuned to selected harmonic frequencies, realizing Class-F mode. Also described is the biharmonic Class-E_M mode, which can reduce the switching power dissipation of a Class-E circuit operating at higher frequencies, at which the turn-off switching time occupies a larger fraction of the RF period. The requirements of jumpless voltage and current waveforms and sinusoidal load waveform, with nonzero output power delivered to the load, can be provided by using nonlinear reactive elements in the load network to convert fundamental-frequency power to a desired harmonic frequency or by injecting the harmonic-frequency power into the load network from an external source. The inverse Class-E power amplifier is the dual of the classical Class-E power amplifier with a shunt capacitor, in which the load-network inductor and capacitor replace each other. However, this dual circuit is limited to low operating frequencies or low output powers because the transistor must discharge its output capacitance from the peak voltage to zero, in every RF cycle. As a result, the transistor must be sufficiently small to reduce the capacitor-discharge power dissipation to an acceptable level. Harmonic-control techniques for designing microwave power amplifiers are given, with a description of a systematic procedure of multiharmonic load-pull simulation using the harmonic balance method and active load-pull measurement system. Finally, outphasing modulation systems are considered where a variable envelope output is created by the sum of two constant-envelope signals with varying phases which therefore can be amplified by highly efficient power amplifier operated in a switching Class-D, Class-E, or Class-F operation mode, or their combinations.

Chapter 11 describes the historical aspect of the Doherty approach to the power amplifier design and modern trends in Doherty amplifier design techniques using multistage and asymmetric multiway architectures. To increase efficiency over the power-backoff range, the switchmode Class-E, conventional Class-F, or inverse Class-F operation mode by controlling the second and third harmonics can be used in the load network. The Doherty amplifier with a series connected load, inverted, balanced, push-pull, and dual Doherty architectures are also described and discussed. Finally, examples of the lumped Doherty amplifier implemented in monolithic microwave integrated circuits, digitally driven Doherty technique, and broadband capability of the Doherty amplifier are given.

Several techniques can be used to minimize the distortion of an RF power amplifier, since the RF power amplifier remains the major contributor of distortion in the communication channel. Among the simplest is to provide an operation of the power amplifier within its linear region. The predistortion is the most popular due to its ease of use and possibility to be implemented utilizing analog or digital techniques. Chapter 12 treats the power amplifier from a system perspective, introducing a simple black-box model. Then it continues describing the fundamentals of predistortion linearization, including the sensitivity of the method to various parameters, and presenting practical predistorters implemented using analog and digital techniques. Finally, memory effects are described and how they can diminish the effectiveness of a memoryless predistorter.

Nonlinear circuit simulation in the frequency and time domains is the most important tool for analysis, design, and optimization of highly efficient switchmode power amplifiers of Classes-D, DE, and E. The advantages are the significantly reduced development time and final product cost, better understanding of the circuit behavior and faster obtaining of the optimum design. It is especially important at very high frequencies, including microwaves, and for MMIC development, where the transistor and circuit parasitics can significantly affect the overall power amplifier performance. Therefore, it is important to incorporate into the simulator as accurate a transistor model as possible to approximate correctly the device behavior, at the fundamental frequency, and at the second and higher harmonics of the operating frequency. Chapter 13 focuses on five CAD programs for analyzing the time-domain and frequency-domain behaviors of the switched-mode high-efficiency power amplifiers in frequency ranges from high frequencies to microwaves: HB-PLUS and SPICE CAD tools for Class-D and Class-DE circuits, and HEPA-PLUS, SPICE and ADS CAD tools for Class-E circuits.

Recollections of Nathan Sokal

Frederick H. Raab
Green Mountain Radio Research, Boone, IA, United States

Introduction

Nathan O. Sokal (Fig. 1) is best known for introducing the Class-E high-efficiency power amplifier to our RF/microwave community. My interactions with Nat Sokal began in the early 1970s. Both of us were working on high-efficiency RF power amplifiers and found out about each other through literature searches. This led to exchanges of papers, manuscripts, and anything else we could find about power amplifiers. That in turn led to meeting each other and collaborations on a number of papers and projects.

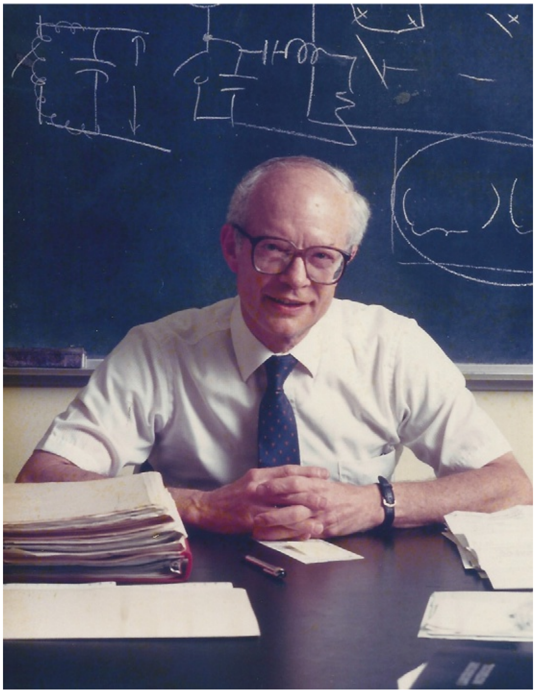

FIG. 1

Nat Sokal at his desk.

Courtesy of Sokal Family.

Early years

Nat Sokal was born in Brooklyn in 1929. His parents and older siblings had emigrated from Poland 5 years earlier. Nat's parents came to the United States from the city Lvov, which was in the Galicia region of Poland (Austro-Hungarian Empire) and is now in the Ukraine. Nat received BS and MS degrees in electrical engineering from MIT in 1950. During his junior and senior years, he was a coop student and worked alternate semesters for Philco Corp. (Philadelphia) on industrial projects.

Nat's wife Zelda Kaufman Sokal was a fellow New Yorker and a student at Radcliffe College when they met. They were married in 1952 and had three children: Alan Sokal (London, England), Karen Sokal-Gutierrez (Piedmont, CA), and Diane Sokal (Brookline, MA).

Career

Nat worked as an electronics engineer for over 60 years. At the start of his career, Nat helped to design an equipment for an atomic weapons test site in the Marshall Islands and then served with the US Air Force at MIT Lincoln Laboratory working on the US air defense system. This work was very diverse and included radar devices and systems, low-noise amplifiers, control devices, and more and ranged from components, to systems, to field installations.

In 1965, Nat founded Design Automation, Inc.(DAI), which was located on Massachusetts Avenue in Lexington. DAI provided electronics engineering design, consulting, and design review. He also described this work (Fig. 2) as "emergency fixes" and "solving unsolvable problems." This work was performed for equipment manufacturers, government agencies, and technical consulting attorneys.

Much of that work was related to high-efficiency switching-mode power conversion and power amplification, at frequencies from dc to 2.5 GHz. Sokal held eight patents in power electronics, including the Class-E switching-mode high-efficiency RF power amplifier. He was the author or coauthor of

FIG. 2

Nat Sokal working in DAI laboratory.

Courtesy of Sokal Family.

two books and over a hundred technical papers. Mostly in high-efficiency generation of RF power and dc power.

High-efficiency amplifiers

In the early 1970s, both Nat and I were working on high-efficiency power amplifiers. At the time, there was a good deal of interest in solid-state RF power, but not many others were interested in efficiency. Our interest was motivated in part by our interest in amateur radio and the desire to get the most RF-output power within the legal limit on the dc-input power.

The Class-D amplifier offered a high efficiency. However, as the frequency increased, it became difficult to synchronize the two transistors, and losses due to discharge of the collector capacitance increased. The Class-F amplifier also offered a high efficiency. However, its multiple resonators complicated the circuit, frequencies were not easily changed, nor was it amenable to broad banding.

A few papers suggested that single-ended amplifiers could be made fairly efficient. None had credible theory; hence none really determined the limits nor how to optimize the efficiency. Nat and his son Alan discovered that with judicious choices of components, the collector voltage would drop to zero at the time the transistor turned on. This eliminated the capacitor-discharge losses of the Class-D amplifier and resulted in an efficiency of 100% for an "ideal" transistor (no on-state resistance nor voltage). They further discovered that the components could be chosen to produce a collector voltage with zero slope at the time of turn-on. This made the amplifier somewhat insensitive to variations in its components as well as the frequency of operation.

I became aware of Nat's work through an obscure paper that he presented at a conference.[1] He similarly became aware of my work after finding my PhD dissertation. We began exchanging notes. We subsequently collaborated on several papers and projects. The Sokals' original analysis[2] determined load reactance experimentally. I subsequently provided a more complete mathematical analysis.[3]

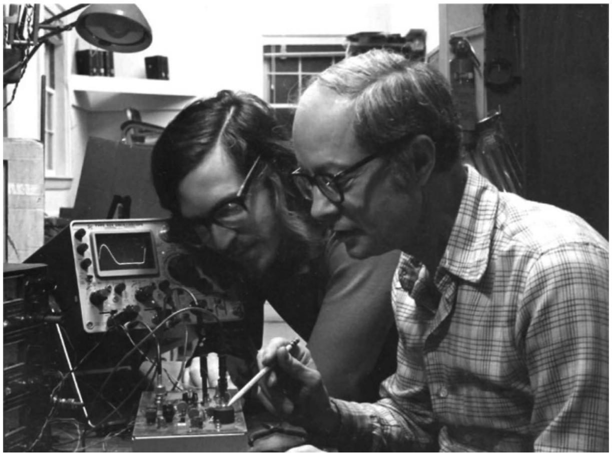

FIG. 3

Nat and Alan Sokal working with demonstrator (Raab collection).

Using Class-E in a linear amplifier requires a technique such as envelope elimination and restoration,[4] which is fundamentally an open-loop system. Varying the collector voltage causes the collector capacitance to vary, and this introduces an unwanted phase modulation. The use of feedback for linearizing the envelope had been developed by Bruene.[5] The Sokals added phase feedback (lock) to clean-up the amplitude-to-phase conversion, thus creating the "polar loop."[6]

In the mid-1970s, Nat put together a "Class-E Demonstrator" (Fig. 3). This was a self-contained box that allowed a potential user to see Class-E operation firsthand in his own laboratory. It produced 3–4 W at 30 MHz. DAI sold the computer program "HB Plus" that facilitated the design of Class-E amplifiers. It included not only the classic theory but empirical adjustments as well.

We initially used the term "optimum" for the condition in which the collector voltage reaches zero with zero slope at the time of turn-on. Nat later decided this was not appropriate. Optimum can refer to various different combinations of things. It also turned out that with nonzero on-state resistance in a FET, the best efficiency is often obtained with a small nonzero voltage at the time of turn-on. Nat decided that we should call the zero-voltage/zero slope condition "nominal."

Power electronics

Nat was also heavily involved in power electronics technology. His work at DAI included dc-dc converters. He attended the Power Electronics Specialist and Applied Power Electronics conferences and gave seminars on power converters all over the world.

Nat reasoned that if the operating frequency of a dc-dc converter could be increased significantly, the sizes of its components (especially inductors) could be decreased significantly. His prototype was a

FIG. 4

Nat Sokal receiving the MTT Pioneer award.

Courtesy: Ed Niehenke.

14-MHz Class-E amplifier that drove a rectifier through a matching transformer. This work led to converters that operate at frequencies of up to several GHz.

MTT and other activities

Nat Sokal was a frequent presenter at the RF Expo and IMS conferences.

Nat gave a workshop on high-efficiency amplifiers at several of the International Microwave Symposia. His workshops were always filled to and over capacity. He also participated in the MTT Speakers Bureau. He was one of the contributors to the MTT 50th anniversary paper on RF power amplifiers.[7] He presented long and short versions of the tutorial course "RF Power Amplifiers, Classes A-S: How the Circuits Operate, How to Design Them, and When to Use Each" to both industry and academia.

Nat Sokal (amateur call sign WA1HQC) was a Technical Adviser to the American Radio Relay League, in the area of RF power amplification and dc power conversion. He was also a member of Eta Kappa Nu, Sigma Xi, and The Electromagnetics Academy honorary professional societies.

Nat became an IEEE fellow in 1989. At IMS 2007 in Hawaii, MTT presented Nat Sokal (Fig. 4) with the Pioneer Award "in recognition of a major, lasting contribution of the development of the Class-E high efficiency switching mode, RF power amplifier." The Polytechnic University of Madrid (Spain) in 2011 awarded him an honorary doctoral degree (*Doctor Honors Causa*) for inventing and developing the Class-E high-efficiency switching mode RF power amplifier.

Retirement and passing

Nat closed the Design Automation office on Massachusetts Avenue in Lexington but continued to work from home through his seventies. Nathan Sokal died on May 8, 2016, at the age of 87 years. He is survived by his wife, three children, and seven grandchildren.

Acknowledgment

This note is condensed from an article in the IEEE Microwave Magazine and published with permission from the IEEE.[8]

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CHAPTER

Power amplifier design principles

1

This introductory chapter presents the basic principles for understanding the power amplifiers design procedure in principle. Based on the spectral-domain analysis, the concept of conduction angle is introduced, by which the basic Classes-A,AB,B, and C of the power-amplifier operation are analyzed and illustrated in a simple and clear form. The frequency-domain analysis is less ambiguous because a relatively complex circuit often can be reduced to one or more sets of immittances at each harmonic component. Classes of operation based upon a finite number of harmonics are discussed and described. The different nonlinear models for various types of MOSFET, MESFET, HEMT, and BJT devices, including HBTs, which are very prospective for modern microwave monolithic integrated circuits of power amplifiers, are given. The effect of the input device parameters on the conduction angle at high frequencies is explained. The design and concept of push-pull amplifiers using balanced transistors are presented. The possibility of the maximum power gain for a stable power amplifier is discussed and analytically derived. The device bias conditions and required bias circuits depend on the classes of operations and type of the active device. The parasitic parametric effect due to the nonlinear collector capacitance and measures for its cancellation in practical power amplifier are discussed. In addition, the basics of the load-pull characterization and distortion fundamentals are presented.

1.1 Spectral-domain analysis

The best way to understand the electrical behavior of a power amplifier and the fastest way to calculate its basic electrical characteristics such as output power, power gain, efficiency, stability, or harmonic suppression is to use a spectral-domain analysis. Generally, such an analysis is based on the determination of the output response of the nonlinear active device when applying the multiharmonic signal to its input port, which analytically can be written as

$$i(t) = f\,[v(t)], \tag{1.1}$$

where $i(t)$ is the output current, $v(t)$ is the input voltage, and $f(v)$ is the nonlinear transfer function of the device. Unlike the spectral-domain analysis, time-domain analysis establishes the relationships between voltage and current in each circuit element in the time domain when a system of equations is obtained applying Kirchhoff's law to the circuit to be analyzed. Generally, such a system will be composed of nonlinear integro-differential equations in a nonlinear circuit. The solution to this system can be found by applying the numerical integration methods.

The voltage $v(t)$ in the frequency domain generally represents the multiple frequency signal at the device input, which is written as

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$$v(t) = V_0 + \sum_{k=1}^{N} V_k \cos(\omega_k t + \phi_k), \tag{1.2}$$

where V_0 is the constant voltage, V_k is the voltage amplitude, ϕ_k is the phase of the k-order harmonic component ω_k, $k = 1, 2, \ldots, N$, and N is the number of harmonics.

The spectral-domain analysis, based on substituting Eq. (1.2) into Eq. (1.1) for a particular nonlinear transfer function of the active device, determines the output spectrum as a sum of the fundamental-frequency and higher-order harmonic components, the amplitudes and phases of which will determine the output signal spectrum. Generally, it is a complicated procedure that requires a harmonic-balance technique to numerically calculate an accurate nonlinear circuit response. However, the solution can be found analytically in a simple way when it is necessary to only estimate the basic performance of a power amplifier in terms of the output power and efficiency. In this case, a technique based on a piecewise linear approximation of the device transfer function can provide a clear insight to the basic behavior of a power amplifier and its operation modes. It can also serve as a good starting point for a final computer-aided design and optimization procedure.

The piecewise-linear approximation of the active device current-voltage transfer characteristic is a result of replacing the actual nonlinear dependence $i = f(v_{\text{in}})$, where v_{in} the voltage applied to the device input, by an approximated one that consists of the straight lines tangent to the actual dependence at the specified points. Such a piecewise linear approximation for the case of two straight lines is shown in Fig. 1.1A.

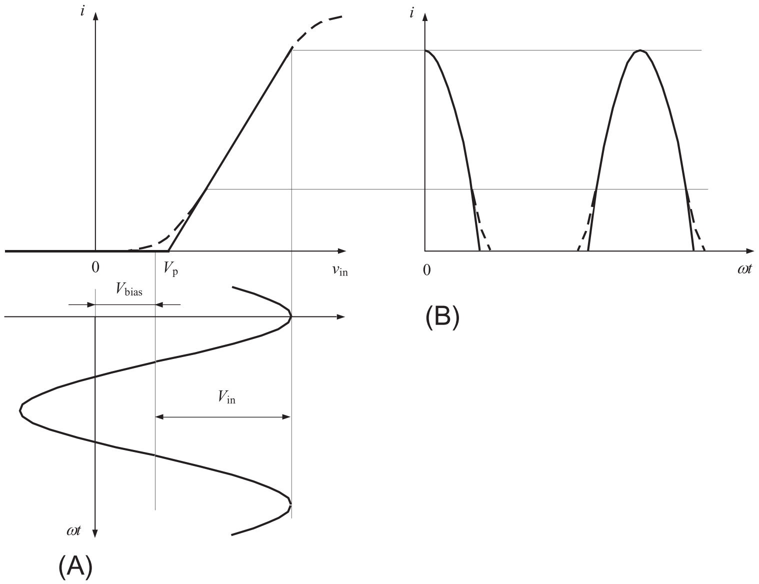


FIG. 1.1

Piecewise linear approximation technique.

The output current waveforms for the actual current-voltage dependence (dashed curve) and its piecewise linear approximation by two straight lines (solid curve) are plotted in Fig. 1.1B. Under a large-signal operation mode, the waveforms corresponding to these two dependences are practically the same for the most part, with negligible deviation for small values of the output current close to the pinch-off region of the device operation and significant deviation close to the saturation region of the device operation. However, the latter case results in a significant nonlinear distortion and is used only for high-efficiency operation modes when the active period of the device operation is minimized. Hence at least two first output current components, DC and fundamental, can be calculated through a Fourier-series expansion enough accurately. Therefore such a piecewise linear approximation with two straight lines can be effective for a quick estimate of the output power and efficiency of the linear power amplifier.

The piecewise linear active device current-voltage characteristic is defined as

$$i = \begin{cases} 0 & v_{\mathrm{in}} \le V_{\mathrm{p}} \\ g_{\mathrm{m}}\left(v_{\mathrm{in}} - V_{\mathrm{p}}\right) & v_{\mathrm{in}} \ge V_{\mathrm{p}} \end{cases}, \tag{1.3}$$

where g_{m} is the device transconductance and V_{p} is the pinch-off voltage.

Let us assume the input signal to be in a cosine form,

$$v_{\mathrm{in}} = V_{\mathrm{bias}} + V_{\mathrm{in}} \cos \omega t, \tag{1.4}$$

where V_{bias} the input DC bias voltage.

At the point on the plot when the voltage $v_{\mathrm{in}}(\omega t)$ becomes equal to a pinch-off voltage V_{p} and where $\omega t = \theta$, the output current $i(\theta)$ takes a zero value. At this moment,

$$V_{\mathrm{p}} = V_{\mathrm{bias}} + V_{\mathrm{in}} \cos \theta, \tag{1.5}$$

and the angle θ can be calculated from

$$\cos \theta = -\frac{V_{\mathrm{bias}} - V_{\mathrm{p}}}{V_{\mathrm{in}}}. \tag{1.6}$$

As a result, the output current represents a periodic pulsed waveform described by the cosinusoidal pulses with maximum amplitude $I_{\max}$ and width 2θ as

$$i = \begin{cases} I_{\mathrm{q}} + I \cos \omega t & -\theta \le \omega t < \theta \\ 0 & \theta \le \omega t < 2\pi - \theta \end{cases}, \tag{1.7}$$

where the conduction angle 2θ indicates the part of the RF current cycle, within which the device conduction period occurs, as shown in Fig. 1.2. When the output current $i(\omega t)$ takes a zero value, one can write

$$i = I_{\mathrm{q}} + I \cos \theta = 0. \tag{1.8}$$

Taking into account that $I = g_{\mathrm{m}} V_{\mathrm{in}}$ for a piecewise linear approximation, Eq. (1.7) can be rewritten for $i > 0$ by

$$i = g_{\mathrm{m}} V_{\mathrm{in}} (\cos \omega t - \cos \theta). \tag{1.9}$$

When $\omega t = 0$, then $i = I_{\max}$ and

$$I_{\max} = I(1 - \cos \theta). \tag{1.10}$$

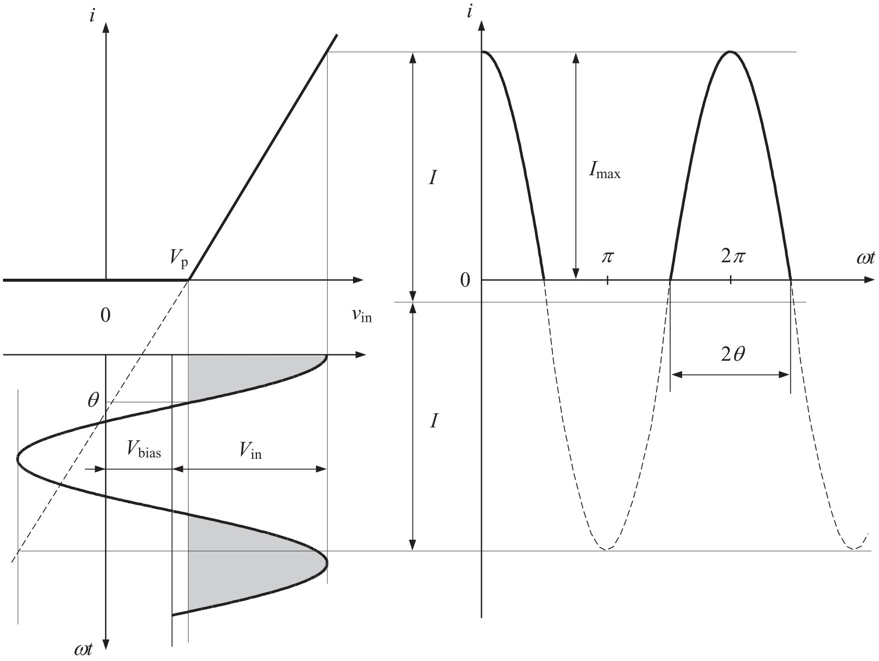


FIG. 1.2

Schematic definition of conduction angle.

The Fourier-series expansion of the even function when $i(\omega t) = i(-\omega t)$ contains only even components of this function and can be written as

$$i(\omega t) = I_0 + I_1 \cos \omega t + I_2 \cos 2\omega t + \cdots + I_n \cos n\omega t, \tag{1.11}$$

where the DC, fundamental-frequency, and nth harmonic components are calculated by

$$I_0 = \frac{1}{2\pi} \int_{-\theta}^{\theta} g_m V_{in} (\cos \omega t - \cos \theta) d\omega t = I\gamma_0(\theta), \tag{1.12}$$

$$I_1 = \frac{1}{\pi} \int_{-\theta}^{\theta} g_m V_{in} (\cos \omega t - \cos \theta) \cos \omega t d\omega t = I\gamma_1(\theta), \tag{1.13}$$

$$I_n = \frac{1}{\pi} \int_{-\theta}^{\theta} g_m V_{in} (\cos \omega t - \cos \theta) \cos n\omega t d\omega t = I\gamma_n(\theta), \tag{1.14}$$

where $\gamma_n(\theta)$ are called the coefficients of expansion of the output current cosine waveform or the current coefficients.[1, 2] They can be analytically defined as

$$\gamma_0(\theta) = \frac{1}{\pi} (\sin \theta - \theta \cos \theta), \tag{1.15}$$

$$\gamma_1(\theta) = \frac{1}{\pi}\left(\theta - \frac{\sin 2\theta}{2}\right), \tag{1.16}$$

$$\gamma_n(\theta) = \frac{1}{\pi}\left[\frac{\sin(n-1)\theta}{n(n-1)} - \frac{\sin(n+1)\theta}{n(n+1)}\right], \tag{1.17}$$

where $n = 2, 3, \ldots$

The dependences of $\gamma_n(\theta)$ for the DC, fundamental-frequency, second-, and higher-order current components are shown in Fig. 1.3. The maximum value of $\gamma_n(\theta)$ is achieved when $\theta = 180$ degrees/n. Special case is $\theta = 90$ degrees, when odd current coefficients are equal to zero, that is, $\gamma_3(\theta) = \gamma_5(\theta) = \cdots = 0$. The ratio between the fundamental-frequency and DC components $\gamma_1(\theta)/\gamma_0(\theta)$ varies from 1 to 2 for any values of the conduction angle, with a minimum value of 1 for $\theta = 180$ degrees and a maximum value of 2 for $\theta = 0$ degrees, as shown in Fig. 1.3A. Besides, it is necessary to pay attention to the fact that the current coefficient $\gamma_3(\theta)$ becomes negative within the interval of 90 degrees $< \theta < 180$ degrees, as shown in Fig. 1.3B. This implies the proper phase changes of the third current harmonic component when its values are negative. Consequently, if the harmonic components, for which $\gamma_n(\theta) > 0$, achieve positive maximum values at the time moments corresponding to the middle points of the current waveform, the harmonic components, for which $\gamma_n(\theta) < 0$, can achieve negative maximum values at these time moments too. As a result, a combination of different harmonic components with proper loading will result in flattening of the current or voltage waveforms, thus improving the efficiency of the power amplifier. The amplitude of corresponding current harmonic component can be obtained by

$$I_n = \gamma_n(\theta) g_\mathrm{m} V_\mathrm{in} = \gamma_n(\theta) I. \tag{1.18}$$

In some cases, it is necessary to provide a constant value of I_max at any values of θ that requires an appropriate variation of the input voltage amplitude V_in. In this case, it is more convenient to use the coefficients α_n defined as a ratio of the nth current harmonic amplitude I_n to the maximum current waveform amplitude I_max,

$$\alpha_n = \frac{I_n}{I_\mathrm{max}}. \tag{1.19}$$

From Eqs. (1.10), (1.18), (1.19), it follows that

$$\alpha_n = \frac{\gamma_n(\theta)}{1 - \cos\theta}, \tag{1.20}$$

and maximum value of $\alpha_n(\theta)$ is achieved when $\theta = 120$ degrees/n.

1.2 Basic classes of operation: A, AB, B, and C

As it was established at the end of 1910s, the amplifier efficiency may reach quite high values when suitable adjustments of the grid and anode voltages are made.[3] With resistive load, the anode current is in phase with the grid voltage, whereas it leads with the capacitive load and lags with the inductive load. On the assumption that the anode current and anode voltage both have sinusoidal variations, the maximum possible output of the amplifying device would be just a half the DC supply power, resulting in an anode efficiency of 50%. However, by using a pulsed-shaped anode current, it is possible to achieve

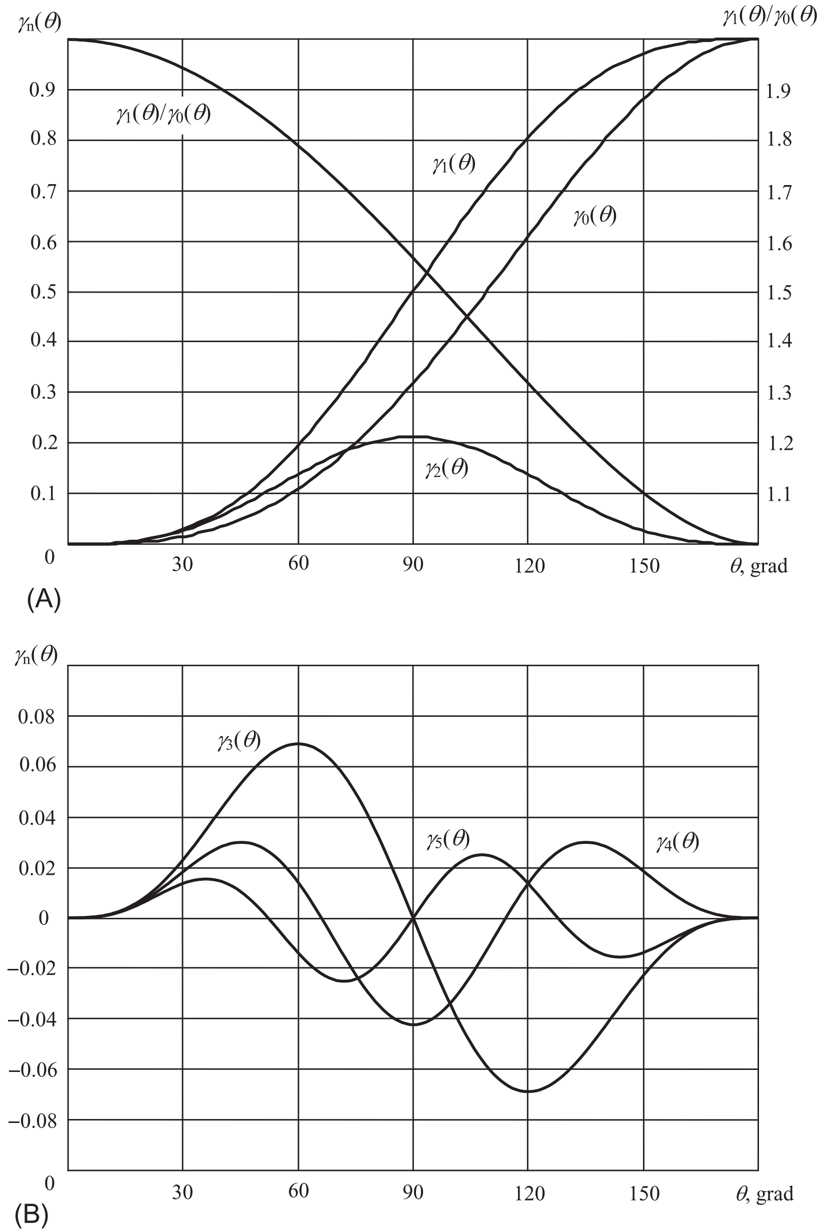


FIG. 1.3

Dependences of $\gamma_n(\theta)$ for DC, fundamental, and higher-order current components.

anode efficiency considerably in excess of 50%, potentially as high as 90%, by choosing the proper operation conditions. By applying the proper negative bias voltage to the grid terminal to provide the pulsed anode current of different width with the angle θ, the anode current becomes equal to zero, where the double angle 2θ represents a conduction angle of the amplifying device.[4] In this case, a theoretical anode efficiency approaches 100% when the conduction angle, within which the anode current flows, reduces to zero starting from 50%, which corresponds to the conduction angle of 360 degrees or 100% duty ratio.

Generally, power amplifiers can be classified into three classes according to their mode of operation: *linear mode* when its operation is confined to the substantially linear portion of the active device characteristic curve; *critical mode* when the anode current ceases to flow but operation extends beyond the linear portion up to the saturation and cutoff regions; and *nonlinear mode* when the anode current ceases to flow during a portion of each cycle, with a duration that depends on the grid bias.[5] When a high efficiency is required, power amplifiers of the third class are employed because the presence of harmonics contributes to the attainment of high efficiencies. In order to suppress the harmonics of the fundamental frequency to deliver a sinusoidal signal to the load, a parallel resonant circuit can be used in the load network, which bypasses harmonics through a low-impedance path and, by virtue of its resonance to the fundamental, receives energy at that frequency. At the very beginning of 1930s, the power amplifiers operating in the first two classes with 100% duty ratio were called the Class-A power amplifiers, whereas the power amplifiers operating in the third class with 50% duty ratio were assigned to Class-B power amplifiers.[6]

To analytically determine the operation classes of the power amplifier, consider a simple resistive stage shown in Fig. 1.4, where L_{ch} is the ideal choke inductor with zero series resistance and infinite reactance at the operating frequency, C_{b} is the DC-blocking capacitor with infinite value having zero reactance at the operating frequency, and R_{L} is the load resistor. The DC supply voltage V_{cc} is applied to both plates of the DC-blocking capacitor, being constant during entire signal period. The active device behaves as an ideal voltage- or current-controlled current source having zero saturation resistance.

For an input cosine voltage given by Eq. (1.4), the operating point must be fixed at the middle point of the linear part of the device transfer characteristic with $V_{\mathrm{in}} \le V_{\mathrm{bias}} - V_{\mathrm{p}}$, where V_{p} is the device pinch-off voltage. Usually, to simplify an analysis of the power amplifier operation, the device transfer characteristic is represented by a piecewise linear approximation. As a result, the output current is cosinusoidal,

$$i = I_{\mathrm{q}} + I\cos\omega t \tag{1.21}$$

with the quiescent current I_{q} greater or equal to the collector current amplitude I. In this case, the output collector current contains only two components—DC and cosine—and the averaged current magnitude is equal to a quiescent current I_{q}.

The output voltage v across the device collector represents a sum of the DC supply voltage V_{cc} and cosine voltage v_{R} across the load resistor R_{L}; consequently, the greater output current i, the greater voltage v_{R} across the load resistor R_{L}, and the smaller output voltage v. Thus for a purely real load impedance when $Z_{\mathrm{L}} = R_{\mathrm{L}}$, the collector voltage v is shifted by 180 degrees relatively the input voltage v_{in} and can be written as

$$v = V_{\mathrm{cc}} + V\cos(\omega t + 180^\circ) = V_{\mathrm{cc}} - V\cos\omega t, \tag{1.22}$$

where V is the output voltage amplitude.

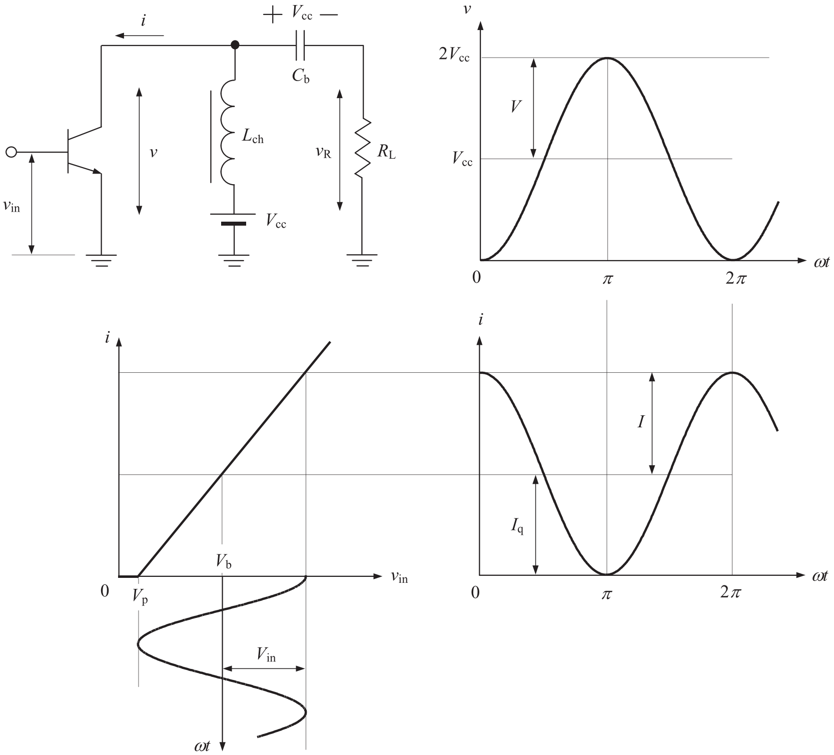


FIG. 1.4

Voltage and current waveforms in Class-A operation.

Substituting Eq. (1.21) into Eq. (1.22) yields

$$v = V_{cc} - \left(i - I_q\right)R_L, \tag{1.23}$$

where $R_L = V/I$, and Eq. (1.23) can be rewritten as

$$i = \left(I_q + \frac{V_{cc}}{R_L}\right) - \frac{v}{R_L}, \tag{1.24}$$

which determines a linear dependence of the collector current versus collector voltage. Such a combination of the cosine collector voltage and current waveforms is known as a Class-A operation mode. In practice, because of the device nonlinearities, it is necessary to connect a parallel *LC* circuit with resonant frequency equal to the operating frequency to suppress any possible harmonic components.

Circuit theory prescribes that the collector efficiency η can be written as

$$\eta = \frac{P}{P_0} = \frac{1}{2}\frac{I}{I_q}\frac{V}{V_{cc}} = \frac{1}{2}\frac{I}{I_q}\xi, \tag{1.25}$$

where

$$P_0 = I_q V_{cc} \tag{1.26}$$

is the DC output power,

$$P = \frac{IV}{2} \tag{1.27}$$

is the power delivered to the load resistance R_L at the fundamental frequency f_0, and

$$\xi = \frac{V}{V_{cc}} \tag{1.28}$$

is the collector voltage peak factor.

Then, by assuming the ideal conditions of zero saturation voltage when $\xi = 1$ and maximum output current amplitude when $I/I_q = 1$, from Eq. (1.25), it follows that the maximum collector efficiency in a Class-A operation mode is equal to

$$\eta = 50\%. \tag{1.29}$$

However, as it also follows from Eq. (1.25), increasing the value of I/I_q can further increase the collector efficiency. This leads to a step-by-step nonlinear transformation of the current cosine waveform to its pulsed waveform when the amplitude of the collector current exceeds zero value during only a part of the entire signal period. In this case, an active device is operated in the active region followed by the operation in the pinch-off region when the collector current is zero, as shown in Fig. 1.5. As a result, the frequency spectrum at the device output will generally contain the second-, third-, and higher-order harmonics of the fundamental frequency. However, because of the high quality factor of the parallel resonant *LC* circuit, only the fundamental-frequency signal is flowing into the load, while the short-circuit conditions are fulfilled for higher-order harmonic components. Therefore ideally, the collector voltage represents a purely sinusoidal waveform with the voltage amplitude $V \leq V_{cc}$.

Eq. (1.8) for the output current can be rewritten through the ratio between the quiescent current I_q and the current amplitude I as

$$\cos\theta = -\frac{I_q}{I}. \tag{1.30}$$

As a result, the basic definitions for nonlinear operation modes of a power amplifier through half the conduction angle θ can be introduced as

- When $\theta > 90$ degrees, then $\cos\theta < 0$ and $I_q > 0$, corresponding to Class-AB operation.
- When $\theta = 90$ degrees, then $\cos\theta = 0$ and $I_q = 0$, corresponding to Class-B operation.
- When $\theta < 90$ degrees, then $\cos\theta > 0$ and $I_q < 0$, corresponding to Class-C operation.

The periodic pulsed output current $i(\omega t)$ can be represented as a Fourier-series expansion

$$i(\omega t) = I_0 + I_1 \cos\omega t + I_2 \cos 2\omega t + I_3 \cos 3\omega t + \cdots, \tag{1.31}$$

where the DC and fundamental-frequency components can be obtained by

$$I_0 = \frac{1}{2\pi} \int_{-\theta}^{\theta} I(\cos\omega t - \cos\theta) d\omega t = I\gamma_0, \tag{1.32}$$

$$I_1 = \frac{1}{\pi} \int_{-\theta}^{\theta} I(\cos\omega t - \cos\theta) \cos\omega t d\omega t = I\gamma_1, \tag{1.33}$$

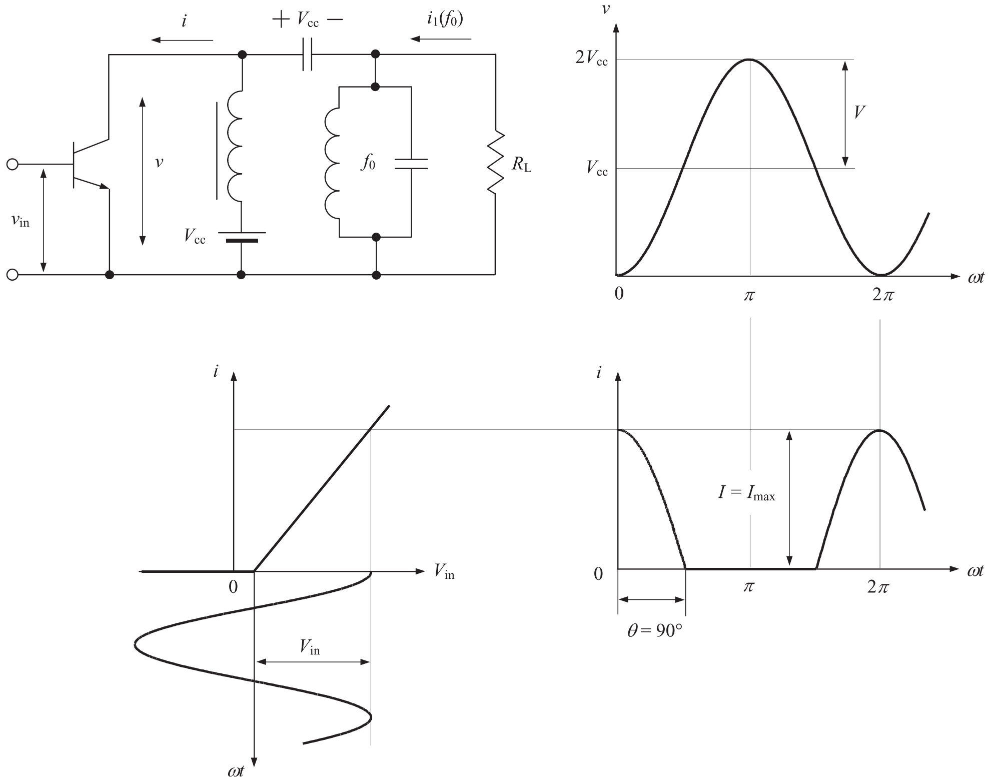

i
$+\,V_{cc}\,-$
$i_1(f_0)$
v
v_{in}
V_{cc}
f_0
R_L
v
$2V_{cc}$
V
V_{cc}
0
π
2π
ωt
i
V_{in}
0
V_{in}
ωt
i
$I = I_{max}$
0
π
2π
ωt
$\theta = 90°$

FIG. 1.5

Voltage and current waveforms in Class-B operation.

respectively, where

$$\gamma_0 = \frac{1}{\pi}(\sin\theta - \theta\cos\theta), \tag{1.34}$$

$$\gamma_1 = \frac{1}{\pi}(\theta - \sin\theta\cos\theta). \tag{1.35}$$

From Eq. (1.32), it follows that the DC current component is a function of θ in the operation modes with $\theta < 180$ degrees, in contrast to a Class-A operation mode where $\theta = 180$ degrees, and the DC current is equal to the quiescent current during the entire period.

The collector efficiency of a power amplifier with resonant circuit, biased to operate in the nonlinear modes, can be obtained by

$$\eta = \frac{P_1}{P_0} = \frac{1}{2}\frac{I_1}{I_0}\xi = \frac{1}{2}\frac{\gamma_1}{\gamma_0}\xi, \tag{1.36}$$

which is a function of θ only, where

$$\frac{\gamma_1}{\gamma_0} = \frac{\theta - \sin\theta\cos\theta}{\sin\theta - \theta\cos\theta}. \tag{1.37}$$

The Class-B power amplifiers were defined as those that operate with a negative grid bias such that the anode current is practically zero with no excitation grid voltage and in which the output power is proportional to the square of the excitation voltage.[7] If $\xi = 1$ and $\theta = 90$ degrees, then from Eqs. (1.36), (1.37), it follows that the maximum collector efficiency in a Class-B operation mode is equal to

$$\eta = \frac{\pi}{4} \cong 78.5\%. \tag{1.38}$$

The fundamental-frequency power delivered to the load $P_L = P_1$ is defined as

$$P_1 = \frac{VI_1}{2} = \frac{VI\gamma_1(\theta)}{2}, \tag{1.39}$$

showing its direct dependence on the conduction angle 2θ. This means that reduction in θ results in lower γ_1, and, to increase the fundamental-frequency power P_1, it is necessary to increase the current amplitude I. Because the current amplitude I is determined by the input voltage amplitude V_{in}, the input power P_{in} must be increased. The collector efficiency also increases with the reduced value of θ and becomes maximum when $\theta = 0$ degrees, where a ratio γ_1/γ_0 is maximal, as follows from Fig. 1.3A. For example, the collector efficiency η increases from 78.5% to 92% when θ reduces from 90 to 60 degrees. However, it requires increasing the input voltage amplitude V_{in} by 2.5 times, resulting in a lower value of the power-added efficiency (PAE), which is defined as

$$PAE = \frac{P_1 - P_{in}}{P_0} = \frac{P_1}{P_0}\left(1 - \frac{1}{G_p}\right), \tag{1.40}$$

where $G_p = P_1/P_{in}$ is the operating power gain.

The Class-C power amplifiers were defined as those that operate with a negative grid bias sufficient to reduce the anode current to zero with no excitation grid voltage and in which the output power varies as the square of the anode voltage between limits.[7] The main distinction between Classes-B and C is in the duration of the output current pulses, which are shorter for Class-C when the active device is biased beyond the cutoff point. It should be noted that, for the device transfer characteristic with an ideal square-law approximation, the odd-harmonic current coefficients $\gamma_n(\theta)$ are not equal to zero in this case, although there is no significant difference between the square-law and linear cases.[8] To achieve the maximum anode efficiency in Class-C, the active device should be biased (negative) considerably past the cutoff (pinch-off) point to provide sufficiently low conduction angles.[9]

In order to obtain an acceptable trade-off between a high-power gain and a high PAE in different situations, the conduction angle should be chosen within the range of 120 degrees $\leq 2\theta \leq$ 190 degrees. If it is necessary to provide high collector efficiency of the active device having a high gain capability, it is necessary to choose a Class-C operation mode with θ close to 60 degrees. However, when the input power is limited and power gain is not sufficient, it is recommended a Class-AB operation mode with small quiescent current when θ is slightly greater than 90 degrees. In the latter case, the linearity of the power amplifier can be significantly improved. From Eq. (1.37), it follows that that the ratio of the fundamental-frequency component of the anode current to the DC current is a function of θ only, which means that, if the operating angle is maintained constant, the fundamental component of the anode current will replicate linearly to the variation of the DC current, thus providing the linear operation of the Class-C power amplifier when the DC current is directly proportional to the grid voltage.[10]

1.3 Load line and output impedance

The graphical method of laying down a load line on the family of the static curves representing anode current against anode voltage for various grid potentials was already known at the end of 1920s.[11] If an active device is connected in a circuit in which the anode load is a pure resistance, the performance may be analyzed by drawing the load line where the lower end of the line represents the anode supply voltage and the slope of the line is established by the load resistance, that is, the load resistance is equal to the value of the intercept on the voltage axis divided by the value of the intercept on the current axis.

In Class-A, the output voltage v across the device anode (collector or drain) represents a sum of the DC supply voltage V_{cc} and cosine voltage across the load resistance R_{L} and can be defined by Eq. (1.22). In this case, the power dissipated in the load and the power dissipated in the device is equal when $V_{\mathrm{cc}} = V$, and the load resistance $R_{\mathrm{L}} = V/I$ is equal to the device output resistance R_{out}.[7] In a pulsed operation mode (Class-AB,B, or C), because the parallel LC circuit is tuned to the fundamental frequency, ideally, the voltage across the load resistor R_{L} represents a cosine waveform. By using Eqs. (1.7), (1.22), (1.33), the relationship between the collector current i and voltage v during a time period of $-\theta \leq \omega t < \theta$ can be expressed by

$$i = \left(I_{\mathrm{q}} + \frac{V_{\mathrm{cc}}}{\gamma_1 R_{\mathrm{L}}} \right) - \frac{v}{\gamma_1 R_{\mathrm{L}}}, \tag{1.41}$$

where the fundamental current coefficient γ_1 as a function of θ is determined by Eq. (1.35), and the load resistance is defined by $R_{\mathrm{L}} = V/I_1$, where I_1 is the fundamental current amplitude. Eq. (1.41) determining the dependence of the collector current on the collector voltage for any values of conduction angle in the form of a straight-line function is called the *load line* of the active device. For a Class-A operation mode with $\theta = 180$ degrees when $\gamma_1 = 1$, the load line defined by Eq. (1.41) is identical to the load line defined by Eq. (1.24).

Fig. 1.6 shows the idealized active device output I–V curves and load lines for different conduction angles, according to Eq. (1.41), with the corresponding collector and current waveforms. From Fig. 1.6, it follows that the maximum collector current amplitude $I_{\max}$ corresponds to the minimum collector voltage V_{sat} when $\omega t = 0$ and is the same for any conduction angle. The slope of the load line defined by its slope angle β is different for different conduction angles and values of the load resistance and can be obtained by

$$\tan\beta = \frac{I_{\max}}{V(1 - \cos\theta)} = \frac{1}{\gamma_1 R_{\mathrm{L}}}, \tag{1.42}$$

from which it follows that a greater slope angle β of the load line results in a smaller value of the load resistance R_{L} for the same θ.

The load resistance R_{L} for the active device as a function of θ, which is required to terminate the device output to deliver the maximum output power to the load, can be written in a general form as

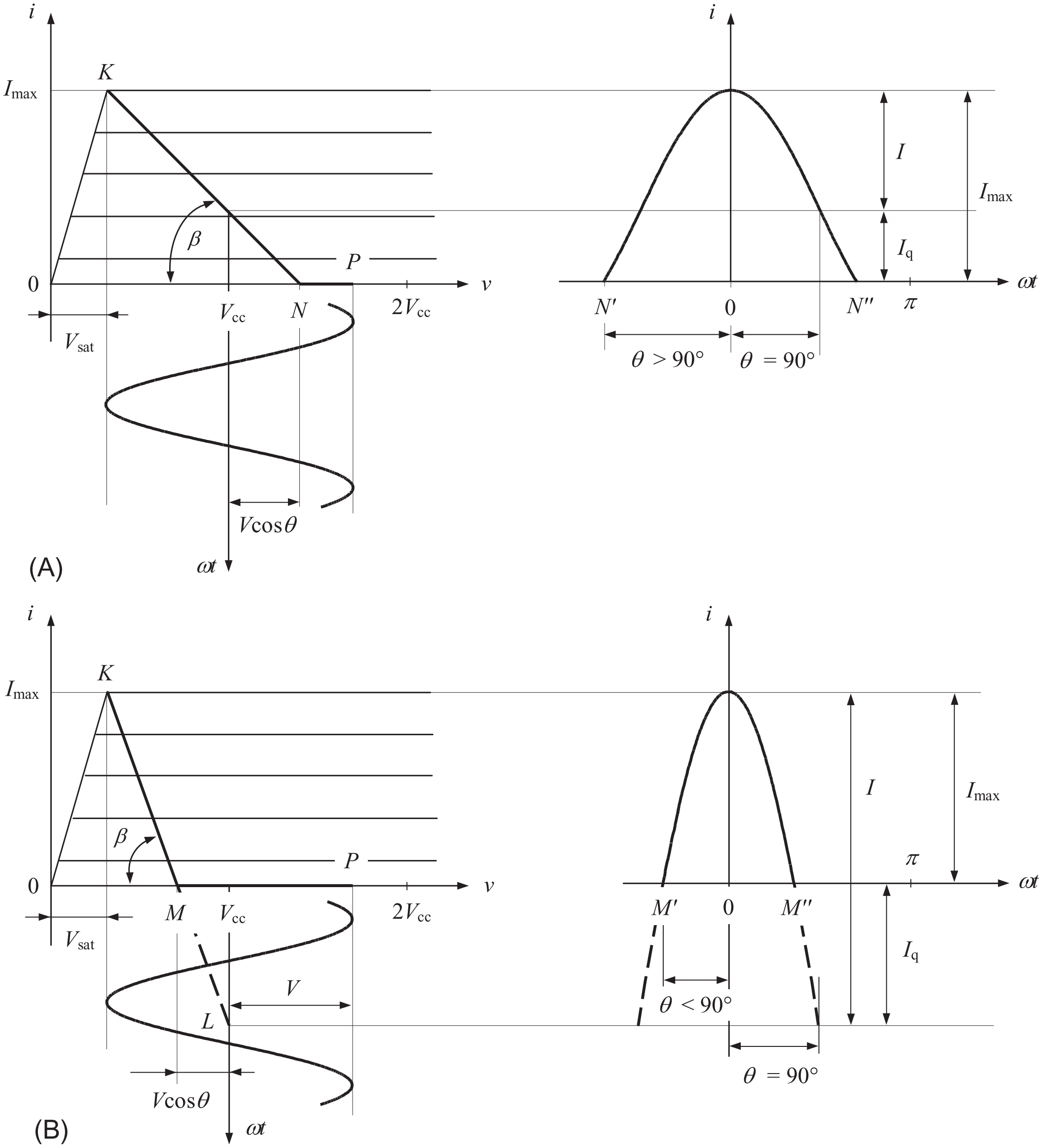

(A)
i
K
I_{max}
β
P
0
v
V_{cc}
N
$2V_{cc}$
V_{sat}
$V\cos\theta$
ωt
i
I
I_{max}
I_q
ωt
N′
0
N″
π
θ > 90°
θ = 90°
(B)
i
K
I_{max}
β
P
0
v
M
V_{cc}
$2V_{cc}$
V_{sat}
V
L
$V\cos\theta$
ωt
i
I
I_{max}
π
ωt
M′
0
M″
I_q
θ < 90°
θ = 90°

FIG. 1.6

Collector current waveforms in Class-AB and Class-C operation modes.

$$R_L(\theta) = \frac{V}{\gamma_1(\theta)I}, \tag{1.43}$$

which is equal to the device equivalent output resistance R_{out} at the fundamental frequency.[7] The term "equivalent" means that this is not a real physical device resistance as in a Class-A mode, but its equivalent output resistance, the value of which determines the optimum load, which should terminate the device output to deliver maximum fundamental-frequency output power. The equivalent output resistance is calculated as a ratio between the amplitudes of the collector cosine voltage and fundamental-frequency collector current component, which depends on the angle θ.

In a Class-B mode, when $\theta = 90°$ and $\gamma_1 = 0.5$, the load resistance R_L^B is defined as $R_L^B = 2V/I_{max}$. Alternatively, considering that $V_{cc} = V$ and $P_{out} = I_1 V$ for the fundamental-frequency output power, the load resistance R_L^B can be rewritten in a simple idealized analytical form with zero saturation voltage V_{sat} as

$$R_L^B = \frac{V_{cc}^2}{2P_{out}}. \tag{1.44}$$

In general, the entire load line represents a broken line PK, including a horizontal part, as shown in Fig. 1.6. Fig. 1.6A represents a load line PNK corresponding to a Class-AB mode with $\theta > 90$ degrees, $I_q > 0$, and $I < I_{max}$. Such a load line moves from point K corresponding to the maximum output current amplitude I_{max} at $\omega t = 0$ and determining the device saturation voltage V_{sat} through the point N located at the horizontal axis v, where $i = 0$ and $\omega t = \theta$. For a Class-AB operation, the conduction angle for the output current pulse between points N' and N'' is greater than 180 degrees. Fig. 1.6B represents a load line PMK corresponding to a Class-C mode with $\theta < 90$ degrees, $I_q < 0$, and $I > I_{max}$. For a Class-C operation, the load line intersects a horizontal axis v in a point M, and the conduction angle for the output current pulse between points M' and M'' is smaller than 180 degrees. Hence generally, the load line represents a broken line with the first section having a slope angle β and the other horizontal section with zero current i. In a Class-B mode, the collector current represents half-cosine pulses with the conduction angle of $2\theta = 180$ degrees and $I_q = 0$.

Now let us consider a Class-B operation with increased amplitude of the cosine collector voltage. In this case, as shown in Fig. 1.7, an active device is operated in the saturation, active, and pinch-off regions, and the load line represents a broken line $LKMP$ with three linear sections (LK, KM, and MP). The new section KL corresponds to the saturation region, resulting in the half-cosine output current waveform with a depression in the top part. With further increase of the output voltage amplitude, the output current pulse can be split into two symmetrical pulses containing a significant level of the higher-order harmonic components. The same result can be achieved by increasing the value of the load resistance R_L when the load line is characterized by a smaller slope angle β.

The collector current waveform becomes asymmetrical for the complex load, the impedance of which represents the load resistance and capacitive or inductive reactance. In this case, the Fourier-series expansion of the output current, given by Eq. (1.31), includes a certain phase for each harmonic component. Then, the output voltage at the device collector is written as

$$v = V_{cc} - \sum_{n=1}^{\infty} I_n |Z_n| \cos(n\omega t + \phi_n), \tag{1.45}$$

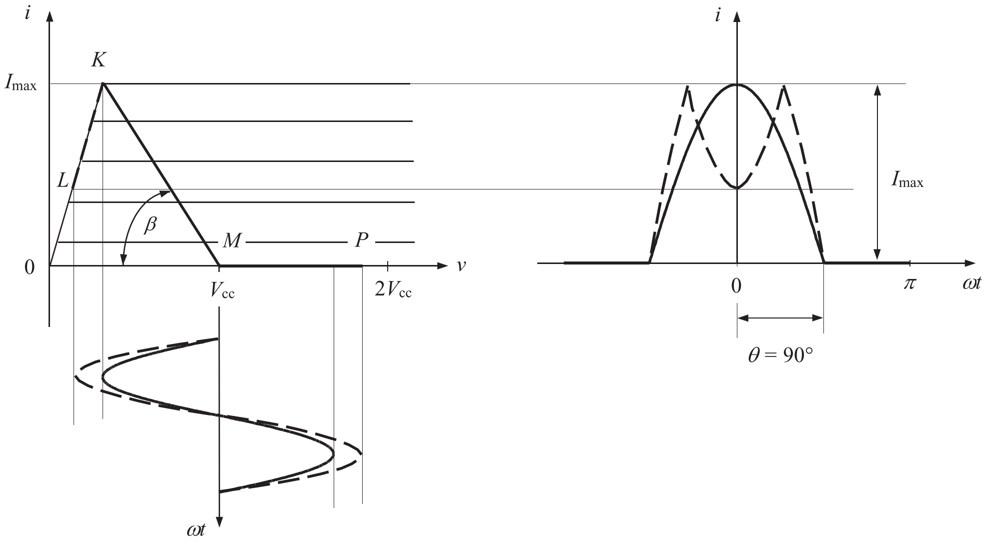


FIG. 1.7

Collector current waveforms for the device operating in saturation, active, and pinch-off regions.

where I_n is the amplitude of nth output current harmonic component, $|Z_n|$ is the magnitude of the load-network impedance at nth output current harmonic component, and ϕ_n is the phase of nth output current harmonic component. Assuming that Z_n is zero for $n=2, 3, \ldots$, which is possible for a resonant load network having negligible impedance at any harmonic component except the fundamental, Eq. (1.45) can be rewritten as

$$v = V_{cc} - I_1|Z_1|\cos(\omega t + \phi_1). \tag{1.46}$$

As a result, for the inductive load impedance, the depression in the collector current waveform reduces and moves to the left side of the waveform, whereas the capacitive load impedance causes the depression to deepen and shift to the right side of the collector current waveform.[12] This effect can simply be explained by different phase conditions for the fundamental and higher-order harmonic components composing the collector current waveform and is illustrated by the different load lines for (*a*) inductive and (*b*) capacitive load impedances shown in Fig. 1.8. Note that now the load line represents a two-dimensional curve with a complicated behavior.

1.4 Classes of operation based upon finite number of harmonics

Fig. 1.9A shows the block diagram of a generic power amplifier, where the active device (which is shown as a MOSFET device but can be a bipolar transistor or any other suitable device) is controlled by its drive and bias to operate as a multiharmonic current source or switch, V_{dd} is the supply voltage, and I_0 is the DC current flowing through the RF choke.[13] The load-network bandpass filter is assumed linear and lossless and provides the drain load impedance $R_1 + jX_1$ at the fundamental frequency and

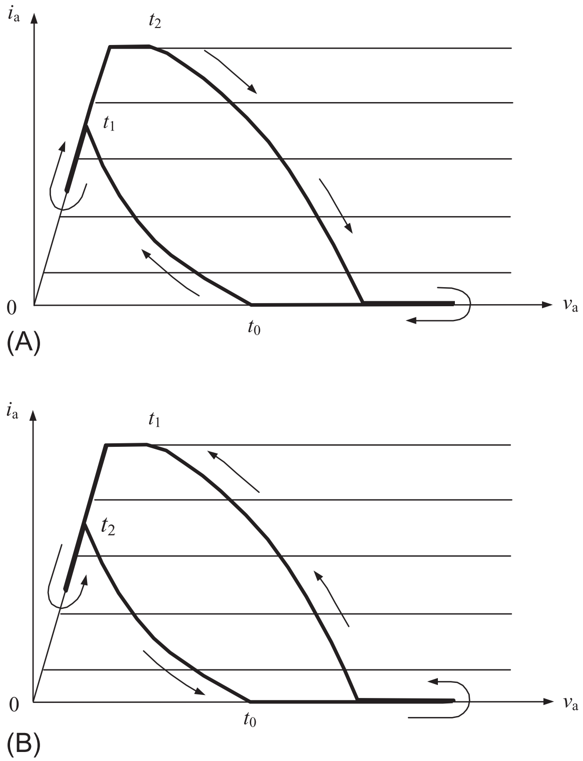


FIG. 1.8

Load lines for (A) inductive and (B) capacitive load impedances.

pure reactances X_k at each kth-harmonic component. For analysis simplicity, the load-network filter can incorporate the reactances of the RF choke and device drain-source capacitance, which is considered voltage independent. Because such a basic power amplifier is assumed to generate power at only the fundamental frequency, harmonic components can be present generally in the voltage and current waveforms, depending upon the class of operation. In a Class-AB,B, or C operation, harmonics are present only in the drain current. However, in a Class-F mode, a given harmonic component is present in either the drain voltage or drain current, but not both, and all or most harmonics are present in both the drain voltage and current waveforms in a Class-E mode. The required harmonics with optimum or near-optimum amplitudes can be produced by driving the power amplifier to saturation. The analysis based on a Fourier-series expansion of the drain voltage and current waveforms shows that maximum achievable efficiency depends not upon the class of operation but upon the number of harmonics employed.[13, 14] For any set of harmonic reactances, the same maximum efficiency can be achieved by proper adjustment of the waveforms and the fundamental-frequency load reactance.

A mechanism for differentiating the various classes of power amplifier operation implemented with small numbers of harmonic components is shown in Fig. 1.9B.[13] It is based on the relative magnitudes of the even (X_e) and odd (X_o) harmonic impedances relative to the fundamental-frequency load

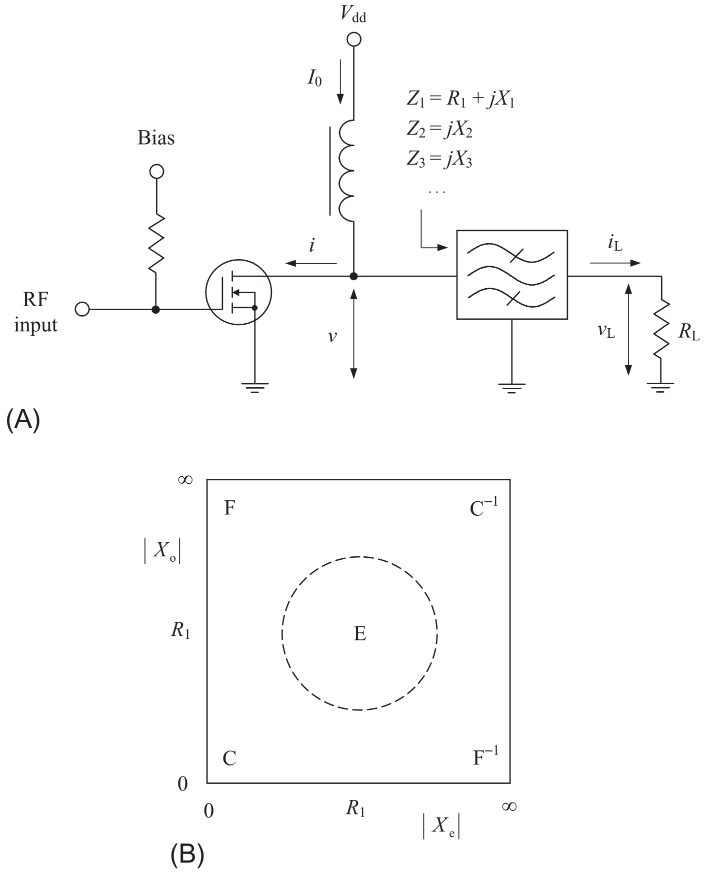


FIG. 1.9

Basic power-amplifier structure and classes of amplification.

resistance R_1. In this case, the classes of operation can be characterized in terms of a small number of harmonics as follows:

- Class-F: Even-harmonic reactances are low and odd-harmonic reactances are high so that the drain voltage is shaped toward a square wave and drain current is shaped toward a half-sine wave.
- Inverse Class-F (Class-F^{-1}): Even-harmonic reactances are high and odd-harmonic reactances are low so that the drain voltage is shaped toward a half-sine wave and drain current is shaped toward a square wave.
- Class-C: All harmonic reactances are low so that the drain current is shaped toward a narrow pulse.
- Inverse Class-C (Class-C^{-1}): All harmonic reactances are high so that the drain voltage is shaped toward a narrow pulse.
- Class-E: All harmonic reactances are negative and comparable in magnitude to the fundamental-frequency load resistance.

The transition from “low” to “comparable” occurs in the range from $R_1/3$ to $R_1/2$, whereas the transition from “comparable” to “high” similarly occurs in the range from $2R_1$ to $3R_1$. In this case, the circular boundary is for illustration only, and the point at which an amplifier transitions from one class to another is somewhat judgmental and arbitrary because there is not an abrupt change in the mode of operation. All power amplifiers degenerate to a Class-A operation when there is only a single (fundamental) frequency component. Class-B is the special case of a pulsed operation with a conduction angle of 180 degrees, which is represented by a half-sine current waveform based upon even harmonics. Class-D power amplifier can be considered as a push-pull Class-F power amplifier, in which two active devices provide each other with paths for even harmonics.

The transition from Class-F to Class-E and then to Class-F^{-1} moves diagonally in Fig. 1.9B by progressively increasing X_2 from zero to ∞ while decreasing X_3 from ∞ to zero so that $X_3 = 1/X_2$. In a Class-F with $X_2 = 0$ and $X_3 = \infty$, the voltage is a third-harmonic maximum-power waveform, while the current is a second-harmonic maximum-power waveform. For $X_2 = X_3 = -1$, the voltage waveform leans leftward and the current waveform leans rightward, thus approximating the all-harmonic Class-E waveforms. Finally, when $X_2 = \infty$ and $X_3 = 0$, the power amplifier operates in an inverse Class-F (Class-F^{-1}). The transition from Class-F to Class-C moves down to the left-hand side of Fig. 1.9B by setting X_2 at zero and progressively decreasing X_3 from ∞ to zero, and the waveforms remain almost unchanged for $X_3 \le -3$. The explicit analytical expression for maximum achievable efficiency of a finite-harmonic Class-C with conduction angle $2\theta \to 0$ can be written as

$$\eta = \cos\left(\frac{\pi}{n+2}\right), \tag{1.47}$$

where n is the number of harmonics.[15]

1.5 Active device models

Generally, for an accurate power amplifier simulation and circuit design for different operating frequencies and output power levels, it is necessary to represent an active device in the form of a nonlinear equivalent circuit, which can adequately describe the small- and large-signal electrical behavior of the power amplifier up to the device transition frequency f_T and higher to its maximum frequency f_{max} that allows a sufficient number of harmonic components to be taken into account. Better approximations of the final design can only be achieved if the nonlinear device behavior is described accurately.

1.5.1 MOSFET device modeling

Accurate MOSFET device modeling is an extremely important procedure to develop low-cost silicon integrated circuits using CMOS technology for higher speed and higher frequency integrated circuits and subsystems within shorter design time. The accuracy of MOSFET models to describe their nonlinear behavior is crucial to predict the entire circuit performance. The lumped-parameter equation-based equivalent circuit model provides a clearer physical description and more design flexibility. The cross-section of the MOSFET and substrate coupling networks are shown in Fig. 1.10A.[16] Here, the considerable ohmic loss caused by the semiconductive silicon substrate is characterized by the resistances R_{b1}, R_{b2}, and R_{sub}. The junction capacitance corresponding to source-drain region is

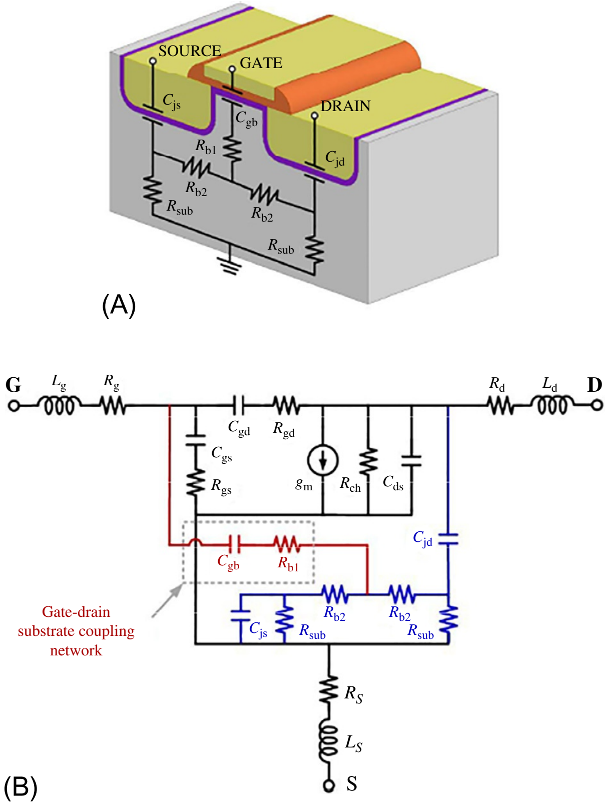


FIG. 1.10

Cross-section (A) and equivalent small-signal circuit (B) of MOSFET device.[16]

represented by the capacitances C_{js} and C_{jd}. The capacitance C_{gb} represents the gate-to-substrate coupling capacitance consisting of the gate oxide capacitance and the depletion layer capacitance.

The complete small-signal MOSFET equivalent circuit with intrinsic nonlinear model and extrinsic parasitic elements, including the gate-drain substrate coupling network and substrate parameters, is shown in Fig. 1.10B.[16] Here, C_{gs} and R_{gs} are the gate-source capacitance and gate channel resistor, respectively, C_{gd} and R_{gd} are the gate-drain capacitance and drain ohmic resistor, respectively, g_m is the device transconductance, R_{ch} is the differential channel resistance as a result of the channel length modulation by the drain voltage, C_{ds} is the drain-source capacitance, L_g is the gate lead inductance, R_s and L_s are the source bulk and ohmic resistance and lead inductance, respectively, and R_d and L_d are the drain bulk and ohmic resistance and lead inductance, respectively. A coupling path between the gate and the drain through the substrate may significantly affect the transfer performance of the transistor. Under an active bias condition, the conductive channel isolates the gate-bulk coupling, and the capacitances C_{gb} and C_{gs} can be merged when the substrate coupling path between the gate and drain terminals can be ignored. However, under pinch-off bias conditions, the conductive channel does not exist, and the signal at the gate terminal is directly coupled to the substrate. Such a device equivalent small-signal model can accurately characterize the performance of the transistors in nanometer CMOS technology up to 60 GHz and above.

Several degradation mechanisms can significantly affect the performance of CMOS power amplifiers, such as gate-oxide breakdown, hot-carrier degradation, punchthrough, drain-bulk breakdown, or negative bias temperature instability. The gate-oxide breakdown and hot-carrier effect are the two most critical issues of deep-submicron CMOS device reliability. The gate-oxide breakdown is the sudden formation of a conductive path in the gate oxide of a MOSFET device as a result of high-voltage application. The allowable gate-oxide voltage becomes smaller as the gate-oxide thickness is reduced. For example, for 0.18- and 0.25-μm CMOS technologies, the breakdown voltages are of about 5.7 and 6 V, respectively.[17, 18] As can be seen in Fig. 1.11A, the channel voltage varies from the source to drain. As a result, the oxide stress (the voltage difference between the top of the oxide and the bottom of the oxide) is a function of position. The highest stress areas occur at the source and drain oxide edges, and therefore, from a design standpoint, the gate-source and the gate-drain voltages (V_{GS} and V_{GD}) should never exceed the prespecified values.[19] There are two basic types of the oxide breakdown: hard

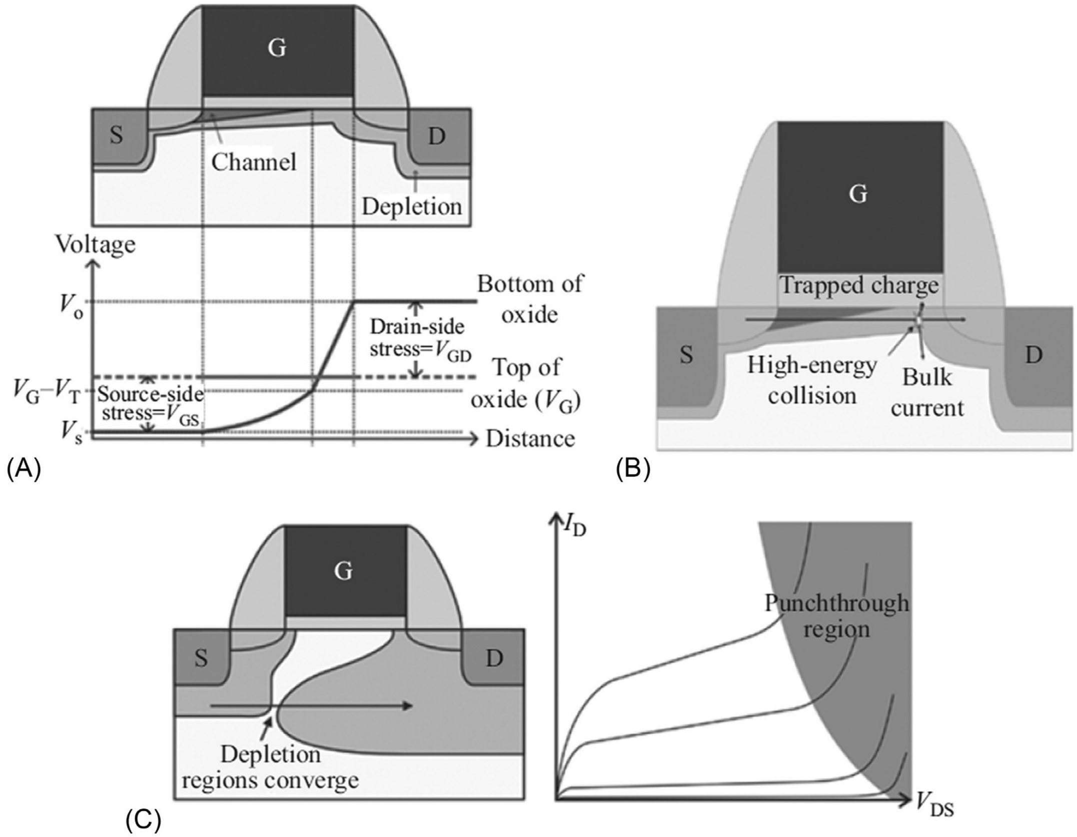

G
S
D
Channel
Depletion
Voltage
V_o
$V_G - V_T$
V_s
Source-side stress=V_{GS}
Drain-side stress=V_{GD}
Bottom of oxide
Top of oxide (V_G)
Distance
(A)
G
Trapped charge
S
D
High-energy collision
Bulk current
(B)
G
S
D
Depletion regions converge
I_D
Punchthrough region
V_{DS}
(C)

FIG. 1.11

Gate-oxide breakdown (A), hot-carrier degradation (B), and punchthrough (C) in a MOSFET transistor.[19]

breakdown and soft breakdown. In hard breakdown, a large gate current increase can be observed, and it has the most disastrous effect on the device performance. This type of breakdown is typically found in thick-oxide devices because of a high-voltage stress. In soft breakdown, a small sudden gate current increase and a sudden gate current noise increase are observed.[20]

The electrical field near the corner of silicon-silicon dioxide (Si-SiO_2) interface, where the drain junction is directly under the gate, is the largest in the device and results in the following hot-carrier effects: electron injection into the SiO_2 layer producing a gate current; an avalanche hole-electron pair production process, increasing the substrate potential and resulting in the built-in bipolar transistor and current source between the drain and substrate; or punchthrough for shortened channel lengths of less than 1 μm contributing to a drain-source leakage current.[21, 22] Consequently, for high-efficiency operation modes with a large drain voltage peak factor, the device is liable to a hot-carrier effect when it is turned off.

In short-channel devices, the lateral field can be extremely high, and consequently, carriers can achieve a very high energy before losing momentum to a collision with the crystal lattice. Some of the hot energy carriers collide with the lattice before arriving at the drain with sufficient energy to result in impact ionization, as shown in Fig. 1.11B.[19] This, in addition to potential avalanche multiplication, can result in surface defects, thus resulting in reduced carrier mobility in the channel. This can also result in trapped charge in the gate oxide or oxide/silicon interface, shifting the local threshold voltage. Usually this damage occurs in the drain region where the electric field is very high causing the damage, resulting in an increase of the device on-resistance and knee voltage.

In a normal operating condition, the drain-source current of a MOSFET device flows close to the surface when a large enough gate bias is applied to create an inversion channel. In the absence of a gate bias, a very little current flows because the drain-bulk and the source-bulk diodes are effectively connected back-to-back with opposite polarities. As larger voltages are applied to the drain, the drain-bulk depletion region extends farther to accommodate the electric potential drop. This depletion region will eventually extend all the way to meet the depletion region of the source-bulk junction, thereby diminishing the potential barrier that stops the direct flow of current between the drain and the source, as shown in Fig. 1.11C.[19] This punchthrough process results in a large current flow that can occur even in the absence of any significant gate bias.

If the gate breakdown is a catastrophic phenomenon, the hot-carrier effect contributes to a long-term power amplifier performance. Because of this hot-carrier effect, an output power of the CMOS power amplifier decreases exponentially, and the slope of this decrease becomes sufficiently small after about 70–80 h of its operation, suggesting that most of the created trap sites at the Si-SiO_2 interface have been filled by electrons. The recovery of the overall degradation in the output power of about 0.7 dB from its nominal value of 23.1 dBm can be achieved by increasing the gate bias voltage by 0.2 V.[18] This indicates that the performance degradation is mainly because of the increase in threshold voltage.

1.5.2 LDMOSFETs

Fig. 1.12A shows the cross-section of the physical structure of an LDMOSFET device, where a heavily doped p^+-sinker is inserted between the top source and p^+-substrate (source grounding) for low resistivity to provide high current flow between the drain and source terminals.[23] The lightly doped *p*-epilayer and *n*-drift layer are required to provide sufficient distance between regions to prevent latchup

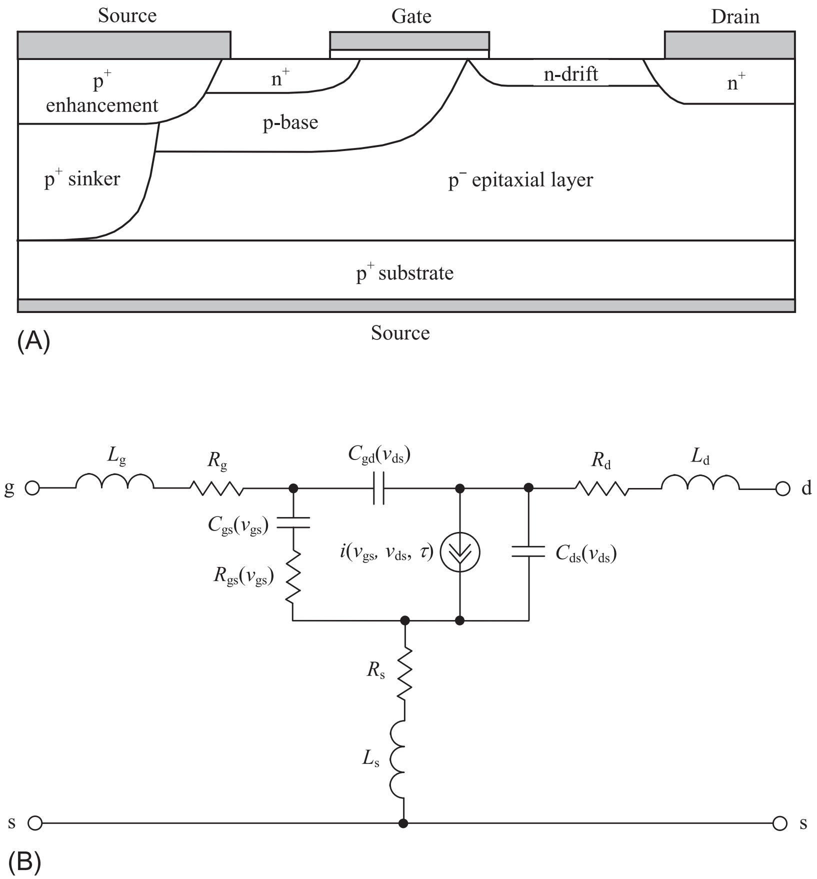

Source
Gate
Drain
p+
enhancement
n+
n-drift
n+
p-base
p+ sinker
p− epitaxial layer
p+ substrate
Source
(A)
L_g
R_g
$C_{gd}(v_{ds})$
R_d
L_d
g
d
$C_{gs}(v_{gs})$
$R_{gs}(v_{gs})$
$i(v_{gs}, v_{ds}, \tau)$
$C_{ds}(v_{ds})$
R_s
L_s
s
s
(B)

FIG. 1.12

A nonlinear LDMOSFET model and its physical structure.

(forward-biased *p-n* diodes) and for the drain-source breakdown protection. The parasitic gate-drain capacitance is directly related to the overlap of the gate oxide onto the heavily doped n^+-source region. To describe accurately the nonlinear properties of the large-size MOSFET device, it is necessary to consider its two-dimensional gate-distributed nature along both the channel length and channel width, resulting in lower values of the intrinsic series gate and shunt gate-source resistances. Fig. 1.12B shows the nonlinear MOSFET equivalent circuit with extrinsic parasitic elements, which can properly describe the nonlinear behavior of both VDMOSFET and LDMOSFET devices.[24, 25]

The nonlinear current source $i(v_{gs}, v_{ds}, \tau)$ as a function of the input gate-source and output drain-source voltages incorporating self-heating effect can be described sufficiently simple and accurate using hyperbolic functions.[25, 26] A careful analytical description of the transition from quadratic to linear regions of the device transfer characteristic enables the more accurate prediction of the intermodulation distortion (IMD).[27] The overall channel carrier transit time τ includes also an effect of the transcapacitance required for charge conservation. The drain-source capacitance C_{ds} and gate-drain capacitance C_{gd} are considered as the junction capacitances that strongly depend on the drain-source voltage. The extrinsic parasitic elements are represented by the gate and drain bondwire inductances L_g and L_d, respectively, source inductance L_s, source and drain bulk and ohmic resistances R_s and R_d, respectively, and gate contact and ohmic resistance R_g. The effect of the gate-source channel resistance R_{gs} becomes significant at higher frequencies close to transition frequency $f_T = g_m/(2\pi C_{gs})$, where g_m is the device transconductance. To account for self-heating effect and substrate loss, a special four-port thermal circuit and a series combination of the resistance and capacitance between the external drain and source terminals can be included.[28]

An empirical nonlinear model developed for silicon LDMOS transistors, which is single-piece and continuously differentiable, can be written as

$$I_{ds} = \beta V_{gst}^{\mathrm{VGexp}} (1 + \lambda V_{ds}) \tanh\left(\frac{\alpha V_{ds}}{V_{gst}}\right)\left[1 + K_1 \exp\left(V_{\mathrm{BR}_{\mathrm{eff}_1}}\right)\right] + I_{ss} \exp\left(\frac{V_{ds} - V_{BR}}{V_T}\right), \tag{1.48}$$

where

$$V_{gst} = V_{st} \ln\left[1 + \exp\left(\frac{V_{gst_2}}{V_{st}}\right)\right],$$

$$V_{gst2} = V_{gst1} - \frac{1}{2}\left(V_{gst1} + \sqrt{\left(V_{gst1} - V_K\right)^2 + \Delta^2} - \sqrt{V_K^2 + \Delta^2}\right),$$

$$V_{gst_1} = V_{gs} - V_{th_0} - \gamma V_{ds},$$

$$V_{\mathrm{BR}_{\mathrm{eff}_1}} = \frac{V_{ds} - V_{\mathrm{BR}_{\mathrm{eff}}}}{K_2} + M_3 \frac{V_{ds}}{V_{\mathrm{BR}_{\mathrm{eff}}}},$$

$$V_{\mathrm{BR}_{\mathrm{eff}}} = \frac{V_{BR}}{2}\left[1 + \tanh\left(M_1 - V_{gst} M_2\right)\right],$$

where λ is the drain current slope parameter, β is the transconductance parameter, V_{th0} is the forward threshold voltage, V_{st} is the subthreshold slope coefficient, V_T is the temperature voltage, I_{ss} is the forward diode leakage current, V_{BR} is the breakdown voltage, K_1, K_2, M_1, M_2, and M_3 are the breakdown parameters, V_K, V_{Gexp}, Δ, and γ are the gate-source voltage parameters.[26]

The gate-source capacitance C_{gs} can be analytically described as a function of the gate-source voltage because it is practically independent on the drain-source voltage. It is equal to the oxide capacitance C_{ox} in the accumulation region, slightly decreases in the weak-inversion region, significantly reduces in the moderate-inversion region, and then becomes practically constant in the strong-inversion or saturation region, as shown in Fig. 1.13.[29] The approximation function for the gate-source capacitance C_{gs} as the dependence of V_{gs} can be derived by using two components containing the hyperbolic functions as.

$$C_{gs} = C_{gs_1} + C_{gs_2}\left\{1 + \tanh\left[C_{gs_6}\left(V_{gs} + C_{gs_3}\right)\right]\right\} + C_{gs4}\left[1 - \tanh\left(C_{gs5} V_{gs}\right)\right], \tag{1.49}$$

where C_{gs_1}, C_{gs_2}, C_{gs_3}, C_{gs_4}, C_{gs_5}, and C_{gs_6} are the approximation parameters.[26]

The gate-source resistance R_{gs} is determined by the effect of the channel inertia in responding to rapid changes of the time varying gate-source voltage and varies in such a manner that the charging time $\tau_g = R_{gs} C_{gs}$ remains approximately constant. Thus the increase of R_{gs} in the velocity saturation

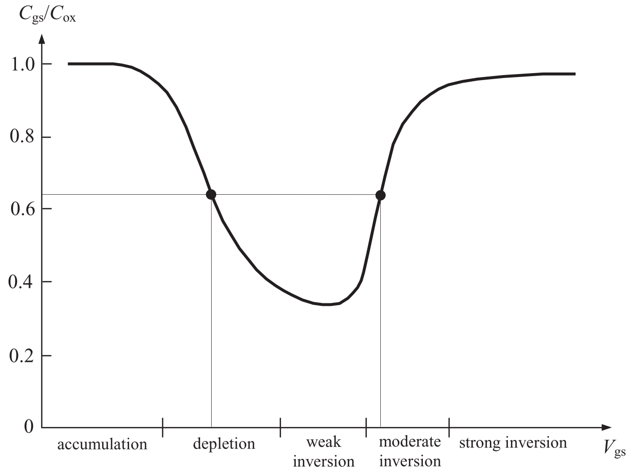


FIG. 1.13

Gate-source capacitance versus gate-source voltage.

region, when the channel conductivity decreases, is partially compensated by the decrease of C_{gs} owing to nonuniform channel charge distribution.[30] The effect of R_{gs} becomes significant at higher frequencies close to the transition frequency f_T of the MOSFET and cannot be taken into consideration when designing RF circuits that operate below 2 GHz, as used for commercial wireless applications.[31, 32]

Fig. 1.14A shows the equivalent representation of a loaded MOSFET input circuit derived from Fig. 1.12B, where $\tau_g = C_{gs}R_{gs}$, $g_m(\theta)$ is the large-signal transconductance as a function of half the conduction angle θ and R_L is the load resistance connected to the drain-source terminal. It is assumed that the series source resistance R_s and inductance L_s and transit time τ are sufficiently small for high-power MOSFETs in a frequency range up to $f \leq 0.3f_T$, and the device drain-source capacitance C_{ds} is inductively compensated. As a result, the equivalent input circuit shown in Fig. 1.14A can be significantly simplified to an equivalent input circuit shown in Fig. 1.14B, where the input inductance L_{in}, resistance R_{in}, and capacitance C_{in} are connected in series and defined as

$$L_{in} = L_g, \tag{1.50}$$

$$R_{in} \cong R_g + R_{gs}, \tag{1.51}$$

$$C_{in} \cong C_{gs} + C_{gd}(1 + g_m R_L). \tag{1.52}$$

Taking into account that usually $C_{gd} \ll C_{gs}$, the device equivalent output circuit can be represented by the series inductance $L_{out} = L_d$ and a parallel connection of the equivalent output resistance R_{out} estimated by Eq. (1.44) at the fundamental frequency and output capacitance $C_{out} = C_{ds} + C_{gd}$.

1.5.3 GaAs MESFETs and GaN HEMTs

Adequate representation for MESFETs and HEMTs in a frequency range up to at least 25 GHz can be provided using a nonlinear model shown in Fig. 1.15A, which is very similar to a nonlinear MOSFET model.[33, 34] The intrinsic model is described by the channel charging resistance R_{gs}, which represents

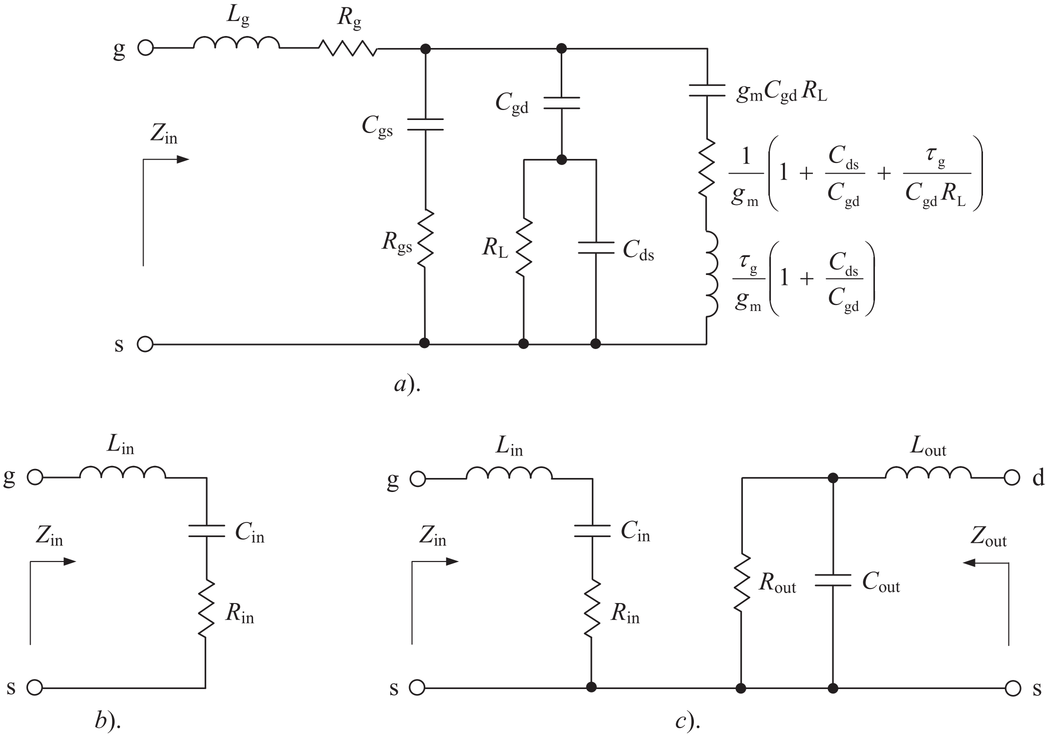


FIG. 1.14

Equivalent circuits characterizing device input and output.

the resistive path for the charging of the gate-source capacitance C_{gs}, the feedback gate-drain capacitance C_{gd}, the drain-source capacitance C_{ds}, the gate-source diode to model the forward conduction current $i_{gs}(v_{gs})$, and the gate-drain diode to account for the gate-drain avalanche current $i_{gd}(v_{gs}, v_{ds})$, which can occur at large-signal operation conditions. The gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} represent the charge depletion region and can be treated as the voltage-dependent Schottky-barrier diode capacitances, being the nonlinear functions of the gate-source voltage v_{gs} and drain-source voltage v_{ds}. For negative gate-source voltage and small drain-source voltage, these capacitances are practically equal. However, when the drain-source voltage is increased beyond the current saturation point, the gate-drain capacitance C_{gd} is much more heavily back-biased than the gate-source capacitance C_{gs}. Therefore the gate-source capacitance C_{gs} is significantly more important and usually dominates the input impedance of the MESFET or HEMT device. The influence of the drain-source capacitance C_{ds} on the device behavior is insignificant, and its value is bias independent. The capacitance C_{dsd} and resistance R_{dsd} model the dispersion of the MESFET or HEMT current-voltage characteristics because of trapping effect in the device channel, which leads to discrepancy between DC measurement and *S*-parameter measurements at higher frequencies.[35, 36] A large-signal model for monolithic power amplifier design should be accurate for all operating conditions. In

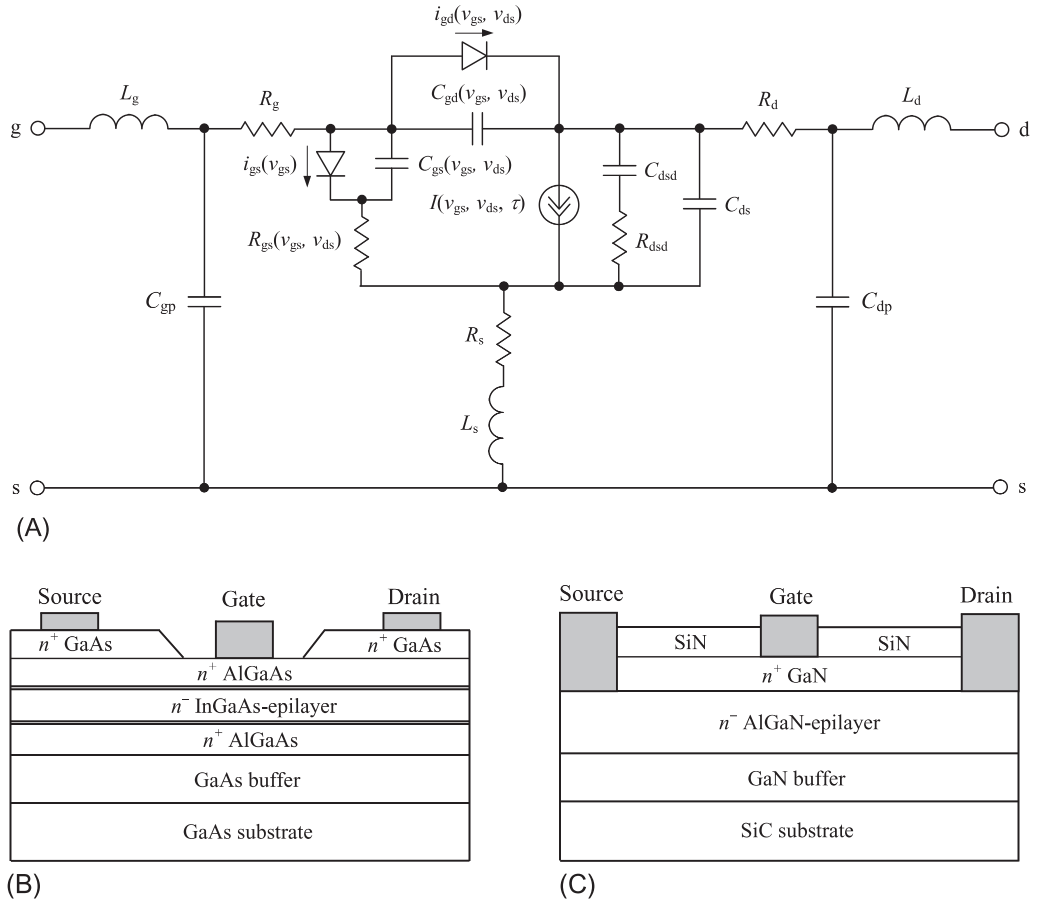

$i_{gd}(v_{gs}, v_{ds})$
L_g
R_g
$C_{gd}(v_{gs}, v_{ds})$
R_d
L_d
g
d
$i_{gs}(v_{gs})$
$C_{gs}(v_{gs}, v_{ds})$
C_{dsd}
$I(v_{gs}, v_{ds}, \tau)$
C_{ds}
$R_{gs}(v_{gs}, v_{ds})$
R_{dsd}
C_{gp}
C_{dp}
R_s
L_s
s
s
(A)
Source
Gate
Drain
n^+ GaAs
n^+ GaAs
n^+ AlGaAs
n^- InGaAs-epilayer
n^+ AlGaAs
GaAs buffer
GaAs substrate
(B)
Source
Gate
Drain
SiN
SiN
n^+ GaN
n^- AlGaN-epilayer
GaN buffer
SiC substrate
(C)

FIG. 1.15

Nonlinear MESFET and HEMT model with HEMT physical structures.

addition, the model parameters should be easily extractable, and the model must be as simple as possible. Various nonlinear MESFET and HEMT models with different complexity are available, and each one can be considered sufficiently accurate for a certain application. For example, although the Materka model does not fulfill charge conservation, it seems to be an acceptable compromise between accuracy and model simplicity for MESFETs, but not for HEMTs, where it is preferable to use the Angelov model.[37, 38] For example, it can be used to predict the large-signal behavior of the pHEMT devices using high-power, high-efficiency 60-GHz MMICs.[39] By using three additional terms of the gate power series function in Angelov model, a better accuracy can be achieved in a large-signal modeling of AlGaN/GaN HEMT devices on SiC substrate.[40] This model can also be improved by incorporating two additional analytical expressions to model the device behavior in saturation region, which is important to design high-efficiency switchmode power amplifiers, for example, in inverse Class-F mode.[41]

Fig. 1.15B shows the cross-section of a physical structure of an InGaAs/AlGaAs HEMT device, where an undoped InGaAs *n*-epilayer is used as a channel and two heavily *n*-doped AlGaAs layers with a high energetic barrier for holes are necessary to maximize high electron mobility in the channel. In this case, spacing between the AlGaAs layer and InGaAs channel is optimized to achieve a high breakdown voltage. An example of the physical structure of an AlGaN/GaN HEMT device is shown in Fig. 1.15C, where an undoped AlGaN *n*-epilayer is used as a channel, *n*-type doped GaN layer can suppress dispersion in the device current-voltage characteristics, and SiN passivation layer with optimized parameters contributes to lower-trap device structure.[42] Thermal conductivity of a GaN HEMT device is improved by using a SiC substrate. Note that the GaN-based technology can provide wider bandwidth and higher efficiency of the power amplifier due to high charge density and the ability to operate at higher voltages for GaN HEMT devices that are characterized by lower output capacitance and on-resistance.[43, 44]

The basic electrical properties of the MESFET or HEMT device can be characterized by the admittance Y-parameters expressed through the device intrinsic small-signal equivalent circuit as

$$Y_{11} = \frac{j\omega C_{\mathrm{gs}}}{1 + j\omega C_{\mathrm{gs}} R_{\mathrm{gs}}} + j\omega C_{\mathrm{gd}}, \tag{1.53}$$

$$Y_{12} = -j\omega C_{\mathrm{gd}}, \tag{1.54}$$

$$Y_{21} = \frac{g_{\mathrm{m}} \exp(-j\omega\tau)}{1 + j\omega C_{\mathrm{gs}} R_{\mathrm{gs}}} - j\omega C_{\mathrm{gd}}, \tag{1.55}$$

$$Y_{22} = \frac{1}{R_{\mathrm{ds}}} + j\omega\left(C_{\mathrm{ds}} + C_{\mathrm{gd}}\right), \tag{1.56}$$

where g_{m} is the device transconductance, and R_{ds} is the differential drain resistance.[25] In this case, the dispersion effect, which is important at higher frequencies and modeled by C_{dsd} and R_{dsd}, cannot be considered.

By separating Eqs. (1.53)–(1.56) into their real and imaginary parts, the elements of the small-signal equivalent circuit can be analytically determined as

$$C_{\mathrm{gd}} = -\frac{\mathrm{Im}Y_{12}}{\omega}, \tag{1.57}$$

$$C_{\mathrm{gs}} = -\frac{\mathrm{Im}Y_{11} - \omega C_{\mathrm{gd}}}{\omega}\left[1 + \left(\frac{\mathrm{Re}Y_{11}}{\mathrm{Im}Y_{11} - \omega C_{\mathrm{gd}}}\right)^2\right], \tag{1.58}$$

$$R_{\mathrm{gs}} = \frac{\mathrm{Re}Y_{11}}{\left(\mathrm{Im}Y_{11} - \omega C_{\mathrm{gd}}\right)^2 + \left(\mathrm{Re}Y_{11}\right)^2}, \tag{1.59}$$

$$g_{\mathrm{m}} = \sqrt{\left(\mathrm{Re}Y_{21}\right)^2 + \left(\mathrm{Im}Y_{21} + \omega C_{\mathrm{gd}}\right)^2}\sqrt{1 + \left(\omega C_{\mathrm{gs}} R_{\mathrm{gs}}\right)^2}, \tag{1.60}$$

$$\tau = \frac{1}{\omega}\sin^{-1}\left(\frac{-\omega C_{\mathrm{gd}} - \mathrm{Im}Y_{21} - \omega C_{\mathrm{gs}} R_{\mathrm{gs}}\,\mathrm{Re}Y_{21}}{g_{\mathrm{m}}}\right), \tag{1.61}$$

$$C_{\mathrm{ds}} = \frac{\mathrm{Im}Y_{22} - \omega C_{\mathrm{gd}}}{\omega}, \tag{1.62}$$

$$R_{ds} = \frac{1}{\mathrm{Re}Y_{22}}, \tag{1.63}$$

which are valid for a wide frequency range up to the transition frequency f_T.[45] If all extrinsic parasitic elements are known, the only problem is to determine the admittance Y-parameters of the intrinsic two-port network from on-bias experimental data.[46] Consecutive steps shown in Fig. 1.16 can represent such a determination procedure[47]:

- Measurement of the S-parameters of the extrinsic device.
- Transformation of the S-parameters to the impedance Z-parameters with subtraction of the series inductances L_g and L_d.
- Transformation of the impedance Z-parameters to the admittance Y-parameters with subtraction of the parallel capacitances C_{gp} and C_{dp}.
- Transformation of the admittance Y-parameters to the impedance Z-parameters with subtraction of series resistances R_g, R_s, and R_d, and inductance L_s.
- Transformation of the impedance Z-parameters to the admittance Y-parameters of the intrinsic device two-port network.

A simple and accurate nonlinear Angelov model can model the drain current-voltage characteristics and its derivatives, as well as the gate-source and gate-drain capacitances, for different submicron gate-length HEMT devices and commercially available MESFETs. The drain current source is described by using the hyperbolic functions as

$$I_{ds} = I_{pk}(1 + \tanh\psi)(1 + \lambda V_{ds})\tanh\alpha V_{ds}, \tag{1.64}$$

where I_{pk} is the drain current at maximum transconductance with the contribution from the output conductance subtracted, λ is the channel-length modulation parameter, and $\alpha = \alpha_0 + \alpha_1 \tanh\psi$ is the saturation voltage parameter, where α_0 is the saturation voltage parameter at pinch-off, and α_1 is the saturation voltage parameter at $V_{gs} > 0$. The parameter ψ is a power-series function centered at V_{pk} with bias voltage V_{gs} as a variable:

$$\psi = P_1\left(V_{gs} - V_{pk}\right) + P_2\left(V_{gs} - V_{pk}\right)^2 + P_3\left(V_{gs} - V_{pk}\right)^3 + \cdots, \tag{1.65}$$

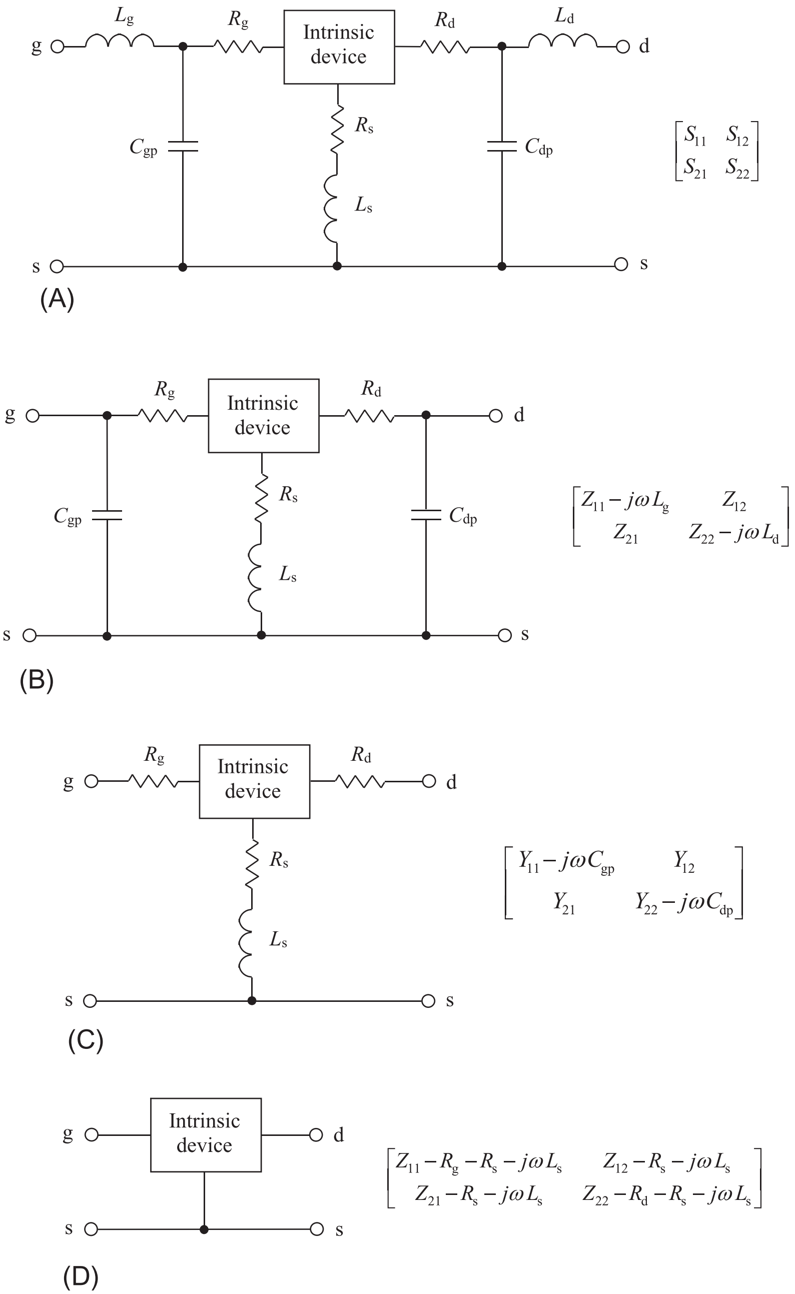
where V_{pk} is the gate voltage for maximum transconductance g_{mpk}. The model parameters as a first approximation can be easily obtained from the experimental $I_{ds}(V_{gs}, V_{ds})$ dependences at a saturated channel condition when all higher terms in ψ are assumed to be zero, and λ is the slope of the I_{ds}–V_{ds} characteristic.

The same hyperbolic functions can be used to model the intrinsic device capacitances C_{gs} and C_{ds}. When an accuracy of 5%–10% is enough, the gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} can be described by

$$C_{gs} = C_{gs0}\left[1 + \tanh\left(P_{1gsg}V_{gs}\right)\right]\left[1 + \tanh\left(P_{1gsd}V_{ds}\right)\right], \tag{1.66}$$

$$C_{gd} = C_{gd0}\left[1 + \tanh\left(P_{1gdg}V_{gs}\right)\right]\left[1 - \tanh\left(P_{1gdd}V_{ds} + P_{1cc}V_{gs}V_{ds}\right)\right], \tag{1.67}$$

where the product $P_{1cc}V_{gs}V_{ds}$ reflects the cross-coupling of V_{gs} and V_{ds} on C_{gd}, and the coefficients P_{1gsg}, P_{1gsd}, P_{1gdg}, and P_{1gdd} are the fitting parameters.


g
L_g
R_g
Intrinsic device
R_d
L_d
d
C_{gp}
R_s
L_s
C_{dp}
s
s
(A)
g
R_g
Intrinsic device
R_d
d
C_{gp}
R_s
L_s
C_{dp}
s
s
(B)
g
R_g
Intrinsic device
R_d
d
R_s
L_s
s
s
(C)
g
Intrinsic device
d
s
s
(D)

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

$$\begin{bmatrix} Z_{11} - j\omega L_g & Z_{12} \\ Z_{21} & Z_{22} - j\omega L_d \end{bmatrix}$$

$$\begin{bmatrix} Y_{11} - j\omega C_{gp} & Y_{12} \\ Y_{21} & Y_{22} - j\omega C_{dp} \end{bmatrix}$$

$$\begin{bmatrix} Z_{11} - R_g - R_s - j\omega L_s & Z_{12} - R_s - j\omega L_s \\ Z_{21} - R_s - j\omega L_s & Z_{22} - R_d - R_s - j\omega L_s \end{bmatrix}$$

FIG. 1.16

Method for extracting device intrinsic *Z*-parameters.

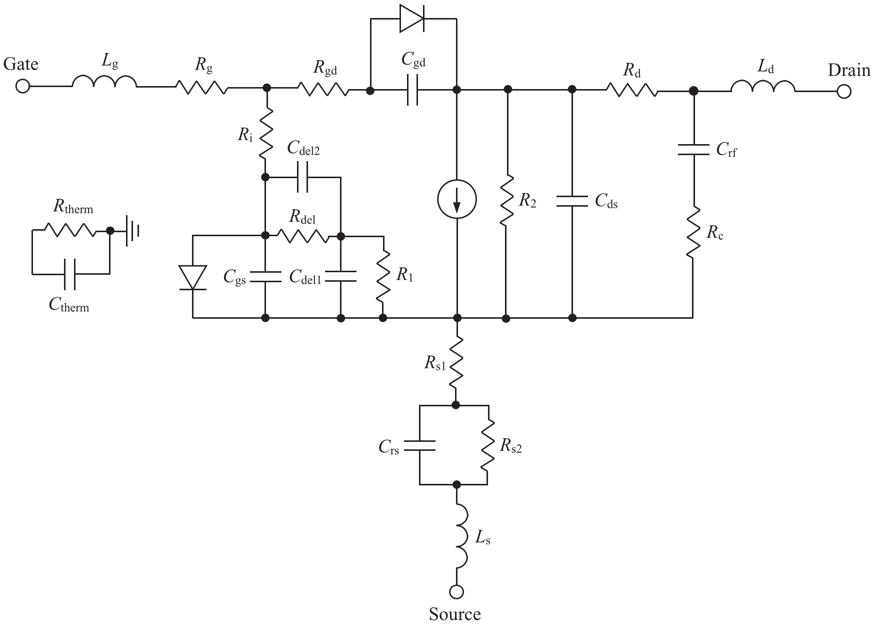


FIG. 1.17

Generalized nonlinear equivalent circuit of GaN HEMT and SiC MESFET devices.

Fig. 1.17 shows the generalized nonlinear equivalent circuit which can describe the nonlinear behavior of the GaN HEMT and SiC MESFET devices.[40, 48] Here, the delay network consisting of the resistance R_c and capacitance C_{rf} is introduced to address the dispersion phenomena, while the resistance R_{del} and capacitances C_{del1} and C_{del2} are included to better describe the transistor response at high frequencies. The values of C_{del1} and C_{del2} are so small that they do not significantly affect the input impedance, but they directly shunt the input capacitance C_{gs} and effectively change the device response at higher frequencies. The thermal subcircuit R_{therm} and C_{therm} describes the dynamic self-heating effect. The presence of the source *RC* network (R_{s1}, R_{s2}, C_{rs}) is very important for the SiC MESFET devices to describe an increase of magnitude of S_{21} versus frequency.

1.5.4 Low- and high-voltage HBTs

Fig. 1.18A shows the modified Gummel-Poon nonlinear model of the bipolar transistor with extrinsic parasitic elements.[49, 50] Such a hybrid-Π equivalent circuit can model the nonlinear electrical behavior of bipolar transistors, in particular HBT devices, with sufficient accuracy up to about 20 GHz. The intrinsic model is described by the dynamic diode resistance r_π, the total base-emitter junction capacitance and base charging diffusion capacitance C_π, the base-collector diode required to account for the nonlinear effects at the saturation, the internal collector-base junction capacitance C_{ci}, the external distributed collector-base capacitance C_{co}, the collector-emitter capacitance C_{ce}, and the nonlinear current source $i(v_{be}, v_{ce})$. The lateral and base semiconductor resistances underneath the base contact and the base semiconductor resistance underneath the emitter are combined into a base-spreading resistance r_b.

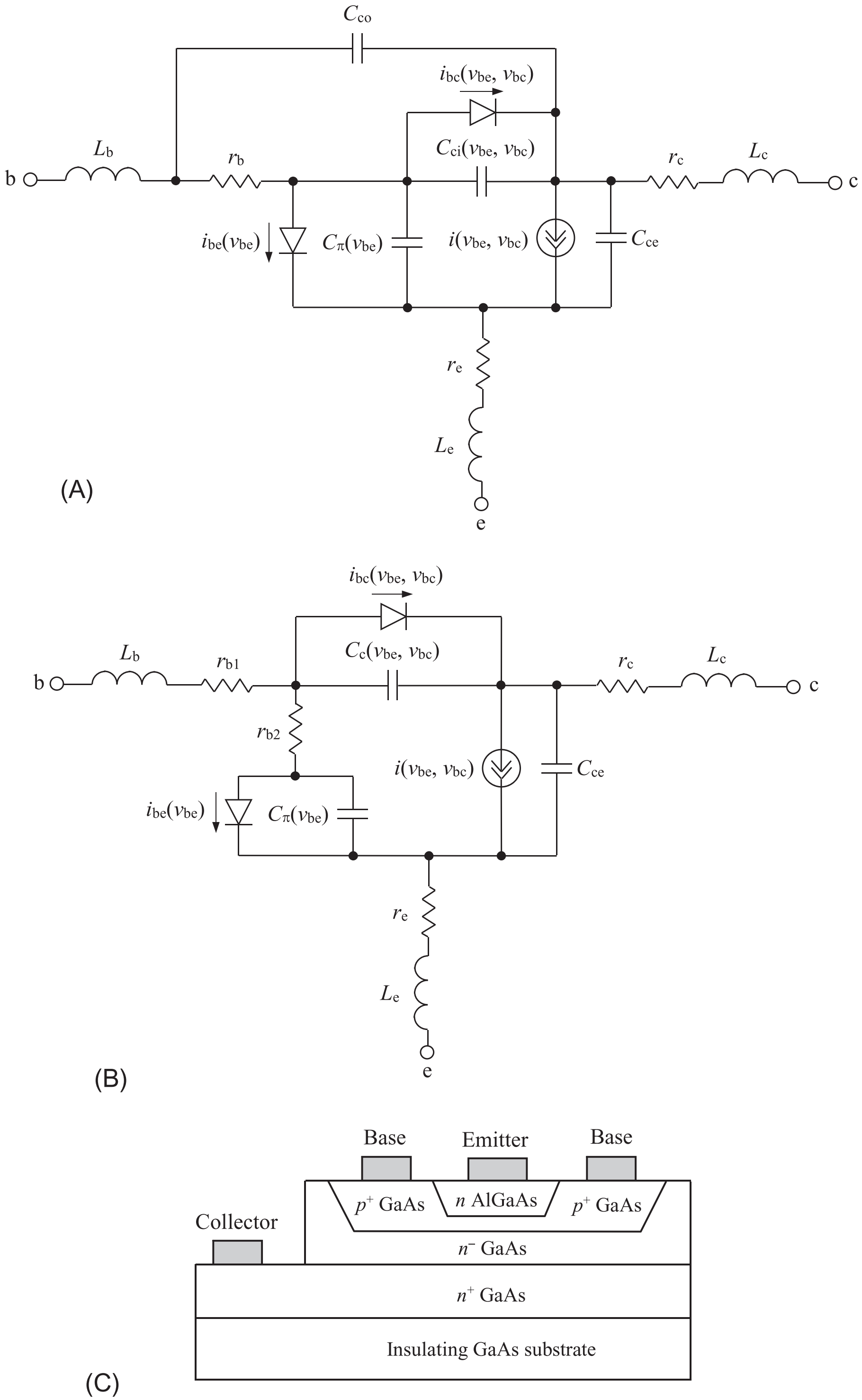

C_{co}
$i_{bc}(v_{be}, v_{bc})$
L_b
r_b
$C_{ci}(v_{be}, v_{bc})$
r_c
L_c
b
c
$i_{be}(v_{be})$
$C_\pi(v_{be})$
$i(v_{be}, v_{bc})$
C_{ce}
r_e
L_e
e
(A)
$i_{bc}(v_{be}, v_{bc})$
L_b
r_{b1}
$C_c(v_{be}, v_{bc})$
r_c
L_c
b
c
r_{b2}
$i(v_{be}, v_{bc})$
C_{ce}
$i_{be}(v_{be})$
$C_\pi(v_{be})$
r_e
L_e
e
(B)
Base
Emitter
Base
p^+ GaAs
n AlGaAs
p^+ GaAs
Collector
n^- GaAs
n^+ GaAs
Insulating GaAs substrate
(C)

FIG. 1.18

Nonlinear BJT and HBT models and HBT physical structure.

The extrinsic parasitic elements are represented by the base bondwire inductance L_b, the emitter ohmic resistance r_e, the emitter inductance L_e, the collector ohmic resistance r_c, and the collector bondwire inductance L_c. To increase the usable operating frequency range of the device up to 50 GHz, it is necessary to include the collector current delay time τ in the collector current source as $g_m \exp(-j\omega\tau)$. The more complicated models such as VBIC, HICUM, or MEXTRAM include the effects of self-heating of a bipolar transistor, take into account the parasitic *p-n-p* transistor formed by the base, collector, and substrate regions, provide an improved description of depletion capacitances at large forward bias, and take into account avalanche and tunneling currents and other nonlinear effects corresponding to the distributed high-frequency effects.[51]

Fig. 1.18B shows the modified version of a bipolar transistor equivalent circuit, where $C_c = C_{co} + C_{ci}$, $r_{b1} = r_b C_{ci}/C_c$, and $r_{b2} = r_b C_{co}/C_c$.[52] Such an equivalent circuit becomes possible because of an equivalent Π- to T-transformation of the elements r_b, C_{co}, and C_{ci} and a condition $r_b << (C_{ci} + C_{co})/\omega C_{ci} C_{co}$, which is usually fulfilled over a frequency range close to the device maximum frequency f_{max}. Then, from a comparison of the transistor nonlinear models, for a bipolar transistor in Fig. 1.18B, for a MOSFET device in Fig. 1.12B, and for a MESFET device in Fig. 1.15A, it is easy to detect the circuit similarity of all these equivalent circuits, which means that the basic circuit design procedure is very similar for any type of bipolar or field-effect transistors. The difference is in the device physics and values of the model parameters. However, techniques for the representation of the input and output impedances, stability analysis based on feedback effect, derivation of power gain, and efficiency are very similar.

The cross-section of the physical structure of an AlGaAs/GaAs HBT device is shown in Fig. 1.18C, with heavily *p*-doped base to reduce base resistance and lightly *n*-doped emitter to minimize emitter capacitance.[53] The lightly *n*-doped collector region allows the collector-base junction to sustain relatively high voltages without breaking down. The forward-bias emitter-injection efficiency is very high because the wider bandgap AlGaAs emitter injects electrons into the GaAs *p*-base at lower energy level, but the holes are prevented from flowing into the emitter by a high-energy barrier, thus resulting in the ability to decrease base length and base-width modulation, and increase frequency response. By using a wide bandgap InGaP layer instead of an AlGaAs layer, the device performance over temperature can be improved.[54] The high linearity power performance in Class-AB condition at the backoff power level, the ruggedness under mismatch and overdrive condition, and the long lifetime of the InGaP/GaAs HBT technology makes it very attractive for the 28-V power amplifier applications.[55] The growth process used for a high-voltage HBT device is identical to the process used for the conventional low-voltage HBT device, which is widely used in handset power amplifiers, except for changes to the collector because of the higher voltage operating requirements. The epitaxial growth process starts with a highly doped *n*-type collector layer and lightly *n*-doped collector drift region, then followed by a heavily doped *p*-type base layer and an InGaP emitter layer, and finishes with an InGaAs cap layer.[56] As a result, the high-voltage HBT devices exhibit collector-base breakdown voltages higher than 70 V.

The bipolar transistor intrinsic small-signal *Y*-parameters can be written as

$$Y_{11} = \frac{1}{r_\pi} + j\omega(C_\pi + C_{ci}), \tag{1.68}$$

$$Y_{12} = -j\omega C_{ci}, \tag{1.69}$$

$$Y_{21} = g_{\mathrm{m}} \exp(-j\omega\tau) - j\omega C_{\mathrm{ci}}, \tag{1.70}$$

$$Y_{22} = \frac{1}{r_{\mathrm{ce}}} + j\omega C_{\mathrm{ci}}, \tag{1.71}$$

where r_{ce} is the output Early resistance that model the effect of the base-width modulation on the transistor characteristics due to variations in the collector-base depletion region.

After separating Eqs. (1.68)–(1.71) into their real and imaginary parts, the elements of the intrinsic small-signal equivalent circuit can be analytically determined as[57]

$$C_\pi = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega}, \tag{1.72}$$

$$r_\pi = \frac{1}{\mathrm{Re}Y_{11}}, \tag{1.73}$$

$$C_{\mathrm{ci}} = -\frac{\mathrm{Im}Y_{12}}{\omega}, \tag{1.74}$$

$$g_{\mathrm{m}} = \sqrt{(\mathrm{Re}Y_{21})^2 + (\mathrm{Im}Y_{21} + \mathrm{Im}Y_{12})^2}, \tag{1.75}$$

$$\tau_\pi = \frac{1}{\omega}\cos^{-1}\frac{\mathrm{Re}Y_{21} + \mathrm{Re}Y_{12}}{\sqrt{(\mathrm{Re}Y_{21})^2 + (\mathrm{Im}Y_{21} + \mathrm{Im}Y_{12})^2}}, \tag{1.76}$$

$$r_{\mathrm{ce}} = \frac{1}{\mathrm{Re}Y_{22}}. \tag{1.77}$$

A simple nonlinear HBT model for computer-aided simulations can be based on the representation of the collector current source through the power series and diffusion capacitances through the hyperbolic functions.[58] To equivalently represent the input impedance of a bipolar transistor, it needs to take into account that C_{ce} is usually much smaller than C_{c}. As a result, the equivalent output capacitance can be defined as $C_{\mathrm{out}} \cong C_{\mathrm{c}}$. The input equivalent R_{in} can approximately be represented by the base resistance r_{b}, while the input equivalent capacitance can be defined as $C_{\mathrm{in}} \cong C_\pi + C_{\mathrm{c}}$. The feedback effect of the collector capacitance C_{c} through C_{c0} and C_{ci} is sufficiently high when load variations are directly transferred to the device input with a significant extent.

1.6 High-frequency conduction angle

An idealized analysis of the physical processes in the nonlinear power amplifier based on the cosinusoidal input signal can be considered sufficiently accurate only at low frequencies when all phase delays due to the effect of the elements of the device equivalent circuit is neglected, and it is represented as an ideal voltage- or current-control current source. However, the electrical behavior of any type of transistor over its entire operating frequency range is described by the sufficiently complicated equivalent circuit, including linear and nonlinear internal and external parasitic elements. The bipolar transistor linear operation at low and medium frequencies up to approximately $(0.1–0.2)f_{\mathrm{T}}$, where f_{T} is the transition frequency, can be adequately characterized by a Giacoletto equivalent circuit shown in Fig. 1.19A.[59] In a linear small-signal mode, all elements of the device equivalent circuit are considered

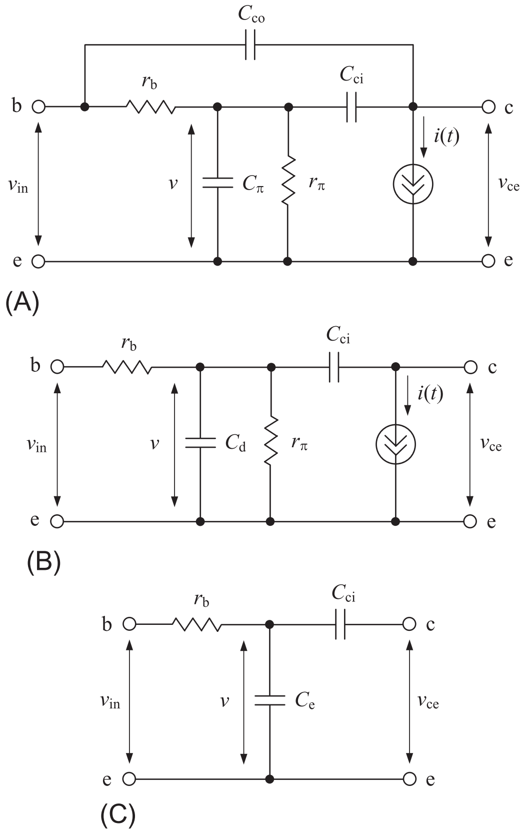


FIG. 1.19

Giacoletto model for bipolar transistor.

constant, including the base-emitter diffusion capacitance C_d and differential resistance r_π. To analyze device behavior in a large-signal mode when the transistor is operated in the pinch-off and active regions, it is necessary to compose two equivalent circuits: the first should correspond to a linear-active region, as shown in Fig. 1.19B, and the other corresponding to a pinch-off region, as shown in Fig. 1.19C. In this case, it is necessary to take into account that the capacitance C_d and resistance r_π, whose values depend significantly on the driving signal amplitude, are set by their averaged values in an active mode. The external feedback capacitance C_{co} can be included to external circuitry.

By applying a piecewise linear approximation of the transistor transfer current-voltage characteristic, the current i as a function of the driving junction voltage v can be written as

$$i(v) = \begin{cases} g_m(v - V_p) & v \geq V_p \\ 0 & v < V_p \end{cases}, \tag{1.78}$$

while the input driving voltage applied to the device input port is defined as

$$v_{\mathrm{in}}(\omega t) = V_{\mathrm{p}} + V_{\mathrm{in}}(\cos\omega t - \cos\theta), \tag{1.79}$$

with the base DC-bias voltage $V_{\mathrm{bias}} = V_{\mathrm{p}}$, where V_{p} is the pinch-off voltage.

Consider that the current flowing through the internal feedback capacitance C_{ci} is sufficiently small when its effect can be neglected. Then, to compose the differential equation describing the device behavior in an active mode, we can write

$$\frac{\mathrm{v}_{\mathrm{in}} - v}{r_{\mathrm{b}}} = \frac{v}{r_{\pi}} + \omega C_{\mathrm{d}} \frac{dv}{d\omega t}. \tag{1.80}$$

As a result, the transistor behavior for $v \geq V_{\mathrm{p}}$ can be described by the first-order linear differential equation written as

$$\omega\tau_1 \frac{dv}{d\omega t} + v = kV_{\mathrm{p}} - kV_{\mathrm{in}}(\cos\omega t - \cos\theta), \tag{1.81}$$

where $\tau_1 = r_{\mathrm{b}} k C_{\mathrm{d}}$ and $k = r_{\pi}/(r_{\mathrm{b}} + r_{\pi})$.

Similarly, for $v < V_{\mathrm{p}}$,

$$\omega\tau_2 \frac{dv}{d\omega t} + v = V_{\mathrm{p}} - V_{\mathrm{in}}(\cos\omega t - \cos\theta), \tag{1.82}$$

where $\tau_2 = r_{\mathrm{b}} C_{\mathrm{e}}$ and C_{e} is the base-emitter junction capacitance.

Depending on the bipolar transistor type, the ratio between the diffusion capacitance C_{d} and junction capacitance C_{e} can be different. In most cases, when C_{d} is greater than C_{e} by an order, the effect of the junction capacitance C_{e} can be neglected for analysis simplicity. Then, by assuming that $\tau_2 = 0$, Eq. (1.82) can be rewritten as

$$v = V_{\mathrm{p}} - V_{\mathrm{in}}(\cos\omega t - \cos\theta), \tag{1.83}$$

which means that the input driving signal is applied to the device junction without any changes in its voltage shape during a pinch-off mode.

Thus the solution of Eq. (1.81) in the time domain for an initial condition $v(-\theta) = V_{\mathrm{p}}$ can be obtained as.

$$v = V_{\mathrm{p}} + V_{\mathrm{in}}\cos\phi_1 \left\{ \cos(\omega t + \phi_1) - \frac{\cos\theta}{\cos\phi_1} - \left[\cos(\theta - \phi_1) - \frac{\cos\theta}{\cos\phi_1} \right] \exp\left(-\frac{\omega t + \theta}{\omega\tau_1} \right) \right\} \tag{1.84}$$

where $\cos\phi_1 = 1/\sqrt{1 + (\omega\tau_1)^2}$ and $\phi_1 = -\tan^{-1}\omega\tau_1$.[52]

Fig. 1.20 shows the time domain dependences of the periodical base input voltage v_{in}, base junction voltage v, and collector current i for the base DC-bias voltage $V_{\mathrm{bias}} = 0$. In this case, if the input driving voltage v_{in} is cosinusoidal, the junction voltage v contains an exponential component demonstrating a transient response that occurs when the transistor is turned on. At the time moment θ_1, when the voltage v becomes equal to V_{p}, the transistor is turned off, and the voltage v provides an instant step change to a certain negative value because it was assumed that $C_{\mathrm{e}} = 0$, and any transient response during the pinch-off mode is not possible. Owing to the effect of the diffusion capacitance C_{d} during an active device mode, the transistor is turned off when the input driving voltage v_{in} is negative at that time. In this case, the shape of the junction voltage v is no longer cosinusoidal. Now it is characterized by a much smaller amplitude and is stretched to the right-hand side, thus making the conduction angle longer compared to a low-frequency case. According to Eq. (1.78), the time-domain behavior of the collector current i

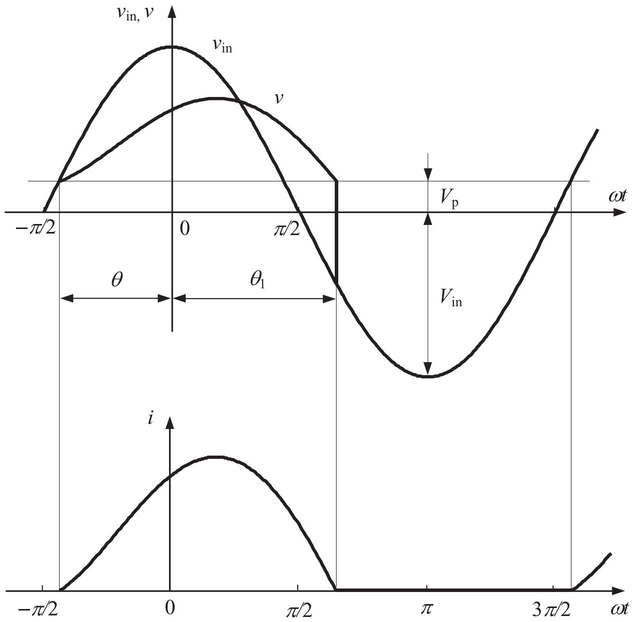


FIG. 1.20

Device voltage and current waveforms when $C_e = 0$.

represents the waveform similar to that of the junction voltage waveform during an active mode and equal to zero during a pinch-off mode.

The time moment θ_1 can be defined from Eq. (1.84) by setting $\omega t = \theta_1$ and $v = V_p$ that results in a transcendental equation

$$\cos(\theta_1 + \phi_1) - \frac{\cos\theta}{\cos\phi_1} - \tan\phi_1 \sin(\theta - \phi_1) \exp\left(\frac{\theta_1 + \theta}{\tan\phi_1}\right) = 0 \tag{1.85}$$

from which the dependences $\theta_1(\theta)$ for different values of the input time constant $\omega\tau_1$ can be numerically calculated.[52, 60] As seen from Fig. 1.21, $\theta_1 = \theta$ when $\omega\tau_1 = 0$, corresponding to a low-frequency case. However, at higher operating frequencies, the collector current pulses corresponding to the conduction state become longer with increased values of $\theta_1 > \theta$. Beginning from a boundary value of $\theta = 180$ degrees + ϕ_1, the transistor is operated in an active region only because the pinch-off operation region does not occur anymore. As a result, the sum $(\theta_1 + \theta)$, which is called the *high-frequency conduction angle*, is always greater than the low-frequency conduction angle 2θ for any certain value of $\omega\tau_1$.

In a common case, when it is impossible to neglect the effect of the junction capacitance C_e, Eq. (1.83) is rewritten by using Eq. (1.82) as

$$\begin{aligned} v = V_p + V_{in}\cos\phi_2 \Bigg\{ & \cos(\omega t + \phi_2) - \frac{\cos\theta}{\cos\phi_2} \\ & - \left[\cos(\theta_1 + \phi_2) - \frac{\cos\theta}{\cos\phi_2}\right] \exp\left(-\frac{\omega t - \theta_1}{\omega\tau_2}\right) \Bigg\}, \end{aligned} \tag{1.86}$$

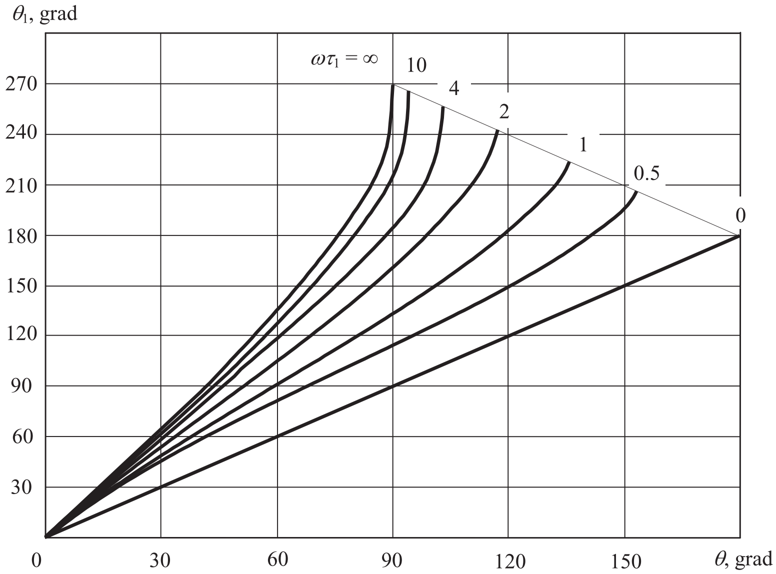


FIG. 1.21

High-frequency conduction angle as a function of $\omega\tau_1$.

where $\cos\phi_2 = 1/\sqrt{1+(\omega\tau_2)^2}$ and $\phi_2 = -\tan^{-1}\omega\tau_2$.

Eq. (1.86) describes the transient response when $v < V_p$ ($V_p > V_{bias} = 0$), which occurs when the transistor is turned off. This transient response arises when the transistor turns off for the first time, as shown in Fig. 1.22. Then, when the junction voltage v becomes equal to a pinch-off voltage V_p again, the transistor turns on. The more the active-mode time constant τ_1 exceeds the pinch-off-mode time constant τ_2, the shorter is the transient response, resulting in a steady-state periodical pulsed current i with fixed amplitude and conduction angle. The time constant τ_2 directly affects the duration of the transient response. When $\tau_2 = 0$, the instant damping of the transient response will occur and voltage v steps down to the value of the input voltage v_{in}. However, when $\tau_2 \neq 0$, the voltage dependence becomes smooth and more symmetrical.

For a boundary case of equal capacitances in active and pinch-off modes when $\tau_1 = \tau_2$, both the junction voltage and collector current pulses become fully symmetrical, representing the truncated cosine waveform with a high-frequency conduction angle $(\theta_1 + \theta)$ different from a low-frequency conduction angle 2θ. The high-frequency conduction angle can be greater, equal, or smaller than its low-frequency counterpart depending upon the device base DC-bias conditions. For a Class-C mode with $V_{bias} < V_p$, the junction voltage pulse when $v > V_p$ is shorter because $\theta_1 + \theta < 2\theta$, as shown in Fig. 1.23A for $V_p = 0$. For a Class-B mode when $V_{bias} = V_p$, both high-frequency and low-frequency conduction angles are equal and $\theta_1 = \theta$, as shown in Fig. 1.23B for $V_p = 0$. Finally, in a Class-AB mode when $V_{bias} > V_p$, the junction voltage pulse becomes longer when $v > V_p$ because $\theta_1 + \theta > 2\theta$, as shown in Fig. 1.23C for $V_p = 0$.

Analytically, the high-frequency angle can be easily calculated when $C_\pi = C_d = C_e$ and $\phi = \phi_1 = \phi_2$ from

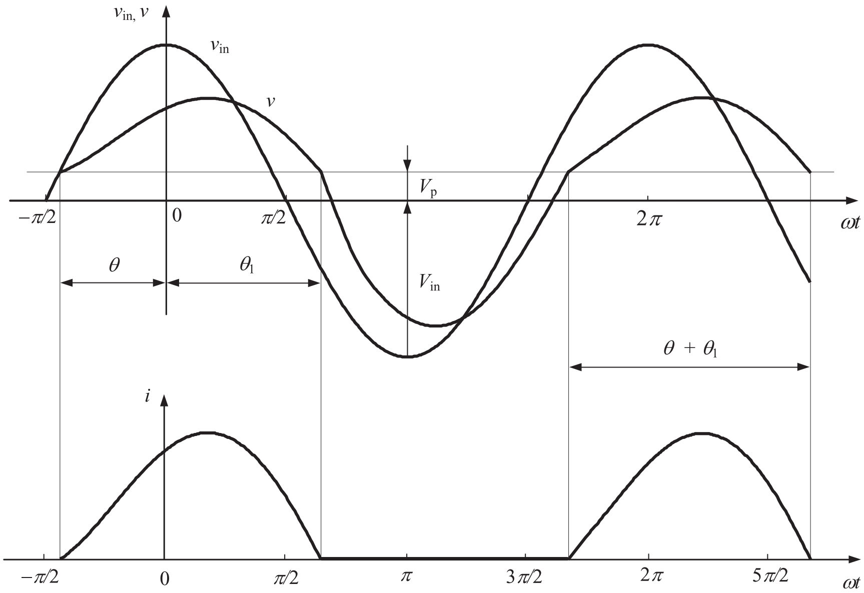


FIG. 1.22

Device voltage and current waveforms when $C_e \neq 0$.

$$\cos\theta_1 = -\frac{V_{bias} - V_p}{V_{in}} \frac{1}{\cos\phi}, \tag{1.87}$$

where $\cos\phi = 1/\sqrt{1 + (\omega\tau_0)^2}$ and $\tau_0 = r_b C_\pi$.

To consider the effect of the feedback collector capacitance C_{ci}, the equivalent input driving voltage $v'_{in}(\omega t)$ can be represented through the input base-emitter voltage v_{in} and collector-emitter voltage v_{ce} as

$$v'_{in}(\omega t) = v_{in}(\omega t) + j\omega\tau_c v_{ce}(\omega t), \tag{1.88}$$

where $\tau_c = r_b C_{ci}$.

1.7 Mixed-mode Class-B and nonlinear effect of collector capacitance

In contrast to the conventional Class-C power amplifiers with a parallel resonant circuit resulting in a sinusoidal collector voltage waveform, the so-called mixed-mode Class-C configuration with a series resonant circuit was widely although somewhat accidentally adopted for most VHF and UHF transistor power amplifiers that could provide better efficiency performance and where it is easier to provide the drive and bias.[61, 62] Such mixed-mode Class-C power amplifiers are the practical implementations of an inverse Class-C (Class-C^{-1}) mode, or Class-B^{-1} mode for a 50% duty ratio, when all harmonic reactances are high.[13] For low saturation resistance and significant nonlinear collector capacitance, it is difficult to maintain a sinusoidal collector voltage waveform. Instead, a nonlinear collector

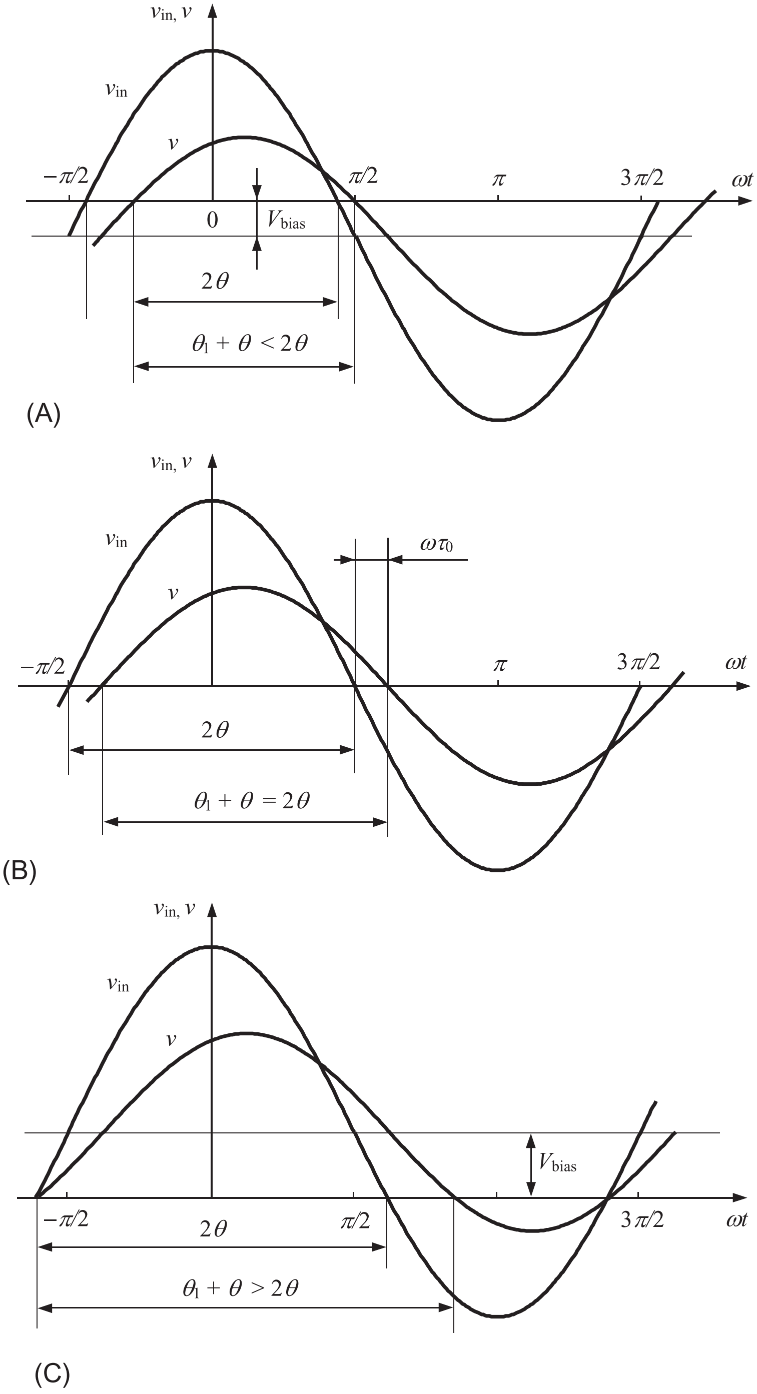


FIG. 1.23

Device voltage and current waveforms when $C_d = C_e$.

capacitance produces a voltage waveform containing harmonics in response to a sinusoidal current. As a result, the saturated bipolar transistor usually dominates the parallel-tuned circuit, flattening the collector voltage waveform.[63] Besides, it is enough difficult in practice to implement the parallel-resonant circuit required for true Class-C operation in power amplifiers using either FET or BJT devices, especially with a high-quality factor. There are several additional difficulties in implementing true Class-C operation in solid-state power amplifiers, especially at VHF and UHF in view of the device lead lengths and stray reactances, causing a significant effect at these frequencies.

Fig. 1.24 shows the simplified schematic of a mixed-mode Class-C power amplifier with a series resonant circuit in the load network, which provides the near-sinusoidal collector current and pulsed collector voltage with pulse duration less than one half of the period, depending upon the value of the collector capacitance. The level of a Class-C operation with corresponding conduction angle is defined by the value of the resistor in a base bias circuit, where the inductor value is chosen to maximize the operating power gain.

As an example, by using a 28-V MRF373A LDMOSFET device in a series-tuned Class-C power amplifier, whose simplified circuit schematic is shown in Fig. 1.25A, an output power of 50 W and a drain efficiency of 58% (by 10% lower than obtained with the idealized simulations) were achieved at 435 MHz.[64] Here, for the theoretical analysis, it was assumed that the transistor is driven so hard that its operation can be described by a switch, and the switch is turned on (closed) when the gate-source voltage is above the threshold voltage and turned off (open) when it is below. When the transistor is turned off, the total drain current i_d, which is a sum of the sinusoidal load current and DC supply current, charges or discharges the transistor drain-source capacitance C_{ds}. In this case, there are two basic power loss mechanisms: the transistor series loss due to finite value of its saturation voltage and the switching loss that accompanies the switch turning on. The switching loss is determined by the value of the capacitor voltage V_{csw} obtained prior to the start of switching on. Fig. 1.25B shows the drain voltage and current waveforms, where the switch starts turning off at zero time instant and the drain voltage $v_d(\omega t)$ achieves maximum value V_{dmax} when the drain current $i_d(\omega t)$ turns negative through zero-crossing

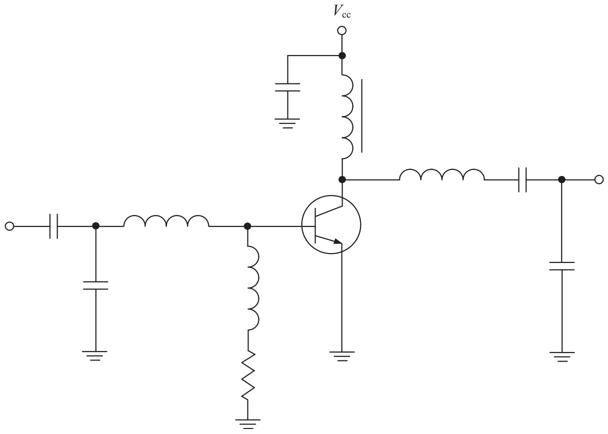


FIG. 1.24

High-efficiency bipolar mixed-mode Class-C power amplifier.

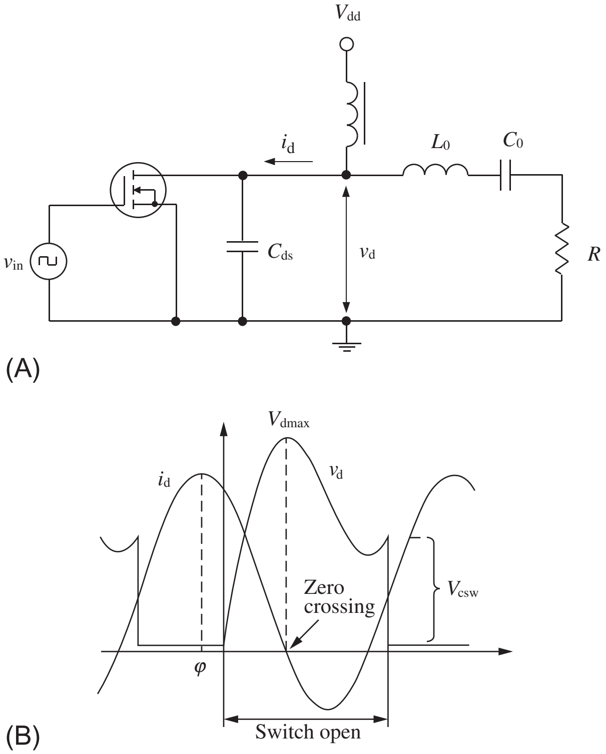


FIG. 1.25

High-efficiency LDMOSFET mixed-mode Class-C power amplifier.

point. Significantly higher efficiency was achieved using the Cree CGH40120F transistor when the output power of 115 W was achieved under pulsed conditions with the drain efficiency between 78.4% and 82.7% at the same operating frequency for the duty ratio varying from 36% to 25%.[65] By using a load-pull tuning to provide high impedance load-network conditions at the second and third harmonics, a drain efficiency of 87% at an output power of 39.8 dBm with a power gain of 10 dB at an operating frequency of 1.0 GHz was achieved for a 1.95-mm GaN HEMT power amplifier using a three-harmonic Class-B^{-1} operation mode.[66]

Generally, the dependence of the collector capacitance on the output voltage represents a nonlinear function. To evaluate the influence of the nonlinear collector capacitance on electrical behavior of the power amplifier, let us consider the load network including a series resonant L_0C_0 circuit tuned to the fundamental frequency that provides open-circuit conditions for the second- and higher-order harmonic components of the output current and a low-pass L-type matching circuit with the series inductor L and shunt capacitor C, as shown in Fig. 1.26A. The matching circuit is needed to match the equivalent output resistance R, corresponding to the required output power at the fundamental frequency, with the standard load resistance R_L. Fig. 1.26B shows the simplified output equivalent circuit of the bipolar power amplifier.

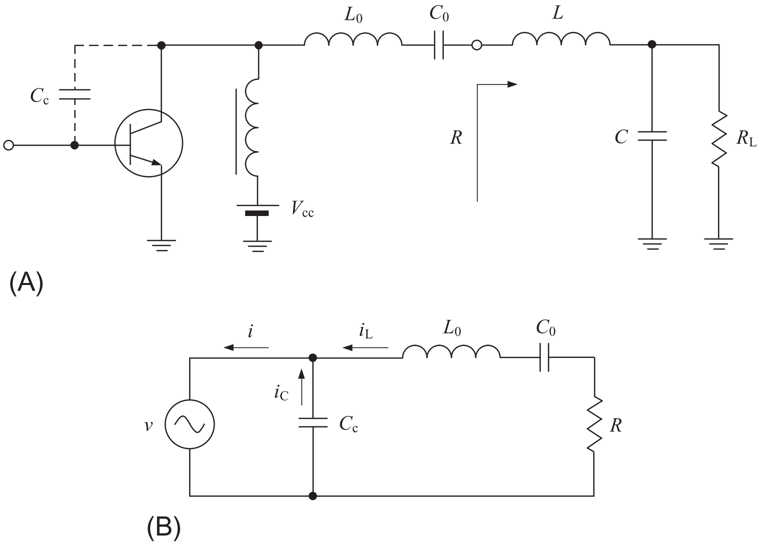


FIG. 1.26

Circuit schematics of a bipolar tuned power amplifier.

The total output current flowing through the device collector can be written as

$$i = I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega t + \phi_n), \tag{1.89}$$

where I_n and ϕ_n are the amplitude and phase of the nth-harmonic component, respectively.

An assumption of a high-quality factor of the series resonant circuit allows the only fundamental-frequency current component to flow into the load. The current flowing through the nonlinear collector capacitance consists of the fundamental-frequency and higher-order harmonic components, which is written as

$$i_C = I_C \cos(\omega t + \phi_1) + \sum_{n=2}^{\infty} I_n \cos(n\omega t + \phi_n), \tag{1.90}$$

where I_C is the fundamental-frequency capacitor current amplitude.

The nonlinear behavior of the collector junction capacitance is described by

$$C_c = C_0 \left(\frac{\varphi + V_{cc}}{\varphi + v} \right)^{\gamma}, \tag{1.91}$$

where C_0 is the collector capacitance at $v = V_{cc}$, V_{cc} is the supply voltage, φ is the contact potential, and γ is the junction sensitivity (grading coefficient) equal to 0.5 for abrupt junction.

As a result, the expression for charge flowing through the collector capacitance can be obtained by

$$q=\int_0^v C(v)dv=\int_0^v \frac{C_0(\varphi+V_{cc})^\gamma}{(\varphi+v)^\gamma}dv. \tag{1.92}$$

When $v=V_{cc}$, then

$$q_0=\frac{C_{0(}(\varphi+V_{cc})}{1-\gamma}\left[1-\left(\frac{\varphi}{\varphi+V_{cc}}\right)^{1-\gamma}\right]. \tag{1.93}$$

Although the DC charge component q_0 is a function of the voltage amplitude, its variations at maximum voltage amplitude normally do not exceed 20% for $\gamma=0.5$. Then, assuming q_0 is determined by Eq. (1.93) as a DC component, the total charge q of the nonlinear capacitance can be represented by the DC component q_0 and ac component Δq written as

$$q=q_0+\Delta q=q_0\left(1+\frac{\Delta q}{q_0}\right)=q_0\frac{(\varphi+v)^{1-\gamma}-\varphi^{1-\gamma}}{(\varphi+V_{cc})^{1-\gamma}-\varphi^{1-\gamma}}. \tag{1.94}$$

Because $V_{cc}>>\varphi$ in the normal case, from Eq. (1.94), it follows that

$$\frac{v}{V_{cc}}=\left(1+\frac{\Delta q}{q_0}\right)^{\frac{1}{1-\gamma}}, \tag{1.95}$$

where $q_0\cong C_0V_{cc}/(1-\gamma)$.

On the other hand, the charge component Δq can be written using Eq. (1.90) as

$$\Delta q=\int i_C(t)dt=\frac{I_C}{\omega}\sin(\omega t+\phi_1)+\sum_{n=2}^{\infty}\frac{I_n}{n\omega}\sin(n\omega t+\phi_n). \tag{1.96}$$

As a result, substituting Eq. (1.96) into Eq. (1.95) yields

$$\frac{v}{V_{cc}}=\left[1+\frac{I_C(1-\gamma)}{\omega C_0V_{cc}}\sin(\omega t+\phi_1)+\sum_{n=2}^{\infty}\frac{I_n(1-\gamma)}{n\omega C_0V_{cc}}\sin(n\omega t+\phi_n)\right]^{\frac{1}{1-\gamma}}. \tag{1.97}$$

After applying a Taylor-series expansion to Eq. (1.97), it is sufficient to be limited to its first three terms to reveal the parametric effect. Then, equating the fundamental-frequency collector voltage components gives

$$\begin{aligned}\frac{v_1}{V_{cc}}=&\frac{I_C}{\omega C_0V_{cc}}\sin(\omega t+\phi_1)+\frac{I_CI_2\gamma}{(2\omega C_0V_{cc})^2}\cos(\omega t+\phi_2-\phi_1)\\&+\frac{I_2I_3\gamma}{12(\omega C_0V_{cc})^2}\cos(\omega t+\phi_3-\phi_2).\end{aligned} \tag{1.98}$$

Consequently, by taking into account that $v_1=V_1\sin(\omega t+\phi_1)$, the fundamental voltage amplitude V_1 can be obtained from Eq. (1.98) as.

$$\frac{V_1}{V_{cc}}=\frac{I_C}{\omega C_0V_{cc}}\left[1+\frac{I_2\gamma}{4\omega C_0V_{cc}}\cos(90^\circ+\phi_2-2\phi_1)+\frac{I_2I_3\gamma}{12\omega C_0V_{cc}I_C}\cos(90^\circ+\phi_3-\phi_2-\phi_1)\right]. \tag{1.99}$$

Because a large-signal value of the abrupt-junction collector capacitance usually does not exceed 20%, the fundamental-frequency capacitor current amplitude I_C as a first-order approximation can be written as

$$I_C \cong \omega C_0 V_1. \tag{1.100}$$

As a result, from Eq. (1.99) it follows that, because of the parametric transformation due to the collector capacitance nonlinearity, the fundamental-frequency collector voltage amplitude increases by σ_p times according to.

$$\sigma_p = 1 + \frac{I_2 \gamma}{4\omega C_0 V_{cc}} \cos\left(90^\circ + \phi_2 - 2\phi_1\right) + \frac{I_2 I_3 \gamma}{12(\omega C_0)^2 V_1 V_{cc}} \cos\left(90^\circ + \phi_3 - \phi_2 - \phi_1\right), \tag{1.101}$$

where $\sigma_p = \xi_p/\xi$, and ξ_p is the collector voltage peak factor with parametric effect.[12]

From Eq. (1.101), it follows that, to maximize the collector voltage peak factor and consequently, the collector efficiency for a given value of the supply voltage V_{cc}, it is necessary to provide the following phase conditions:

$$\phi_2 = 2\phi_1 - 90^\circ, \tag{1.102}$$

$$\phi_3 = 3\phi_1 - 180^\circ. \tag{1.103}$$

Then, for $\gamma = 0.5$,

$$\sigma_p = 1 + \frac{I_2}{8\omega C_0 V_{cc}} + \frac{I_2 I_3}{24(\omega C_0)^2 V_1 V_{cc}}. \tag{1.104}$$

Eq. (1.104) shows the theoretical possibility to increase the collector voltage peak factor by 1.1–1.2 times, thus achieving collector efficiency of 85%–90%. Physically, the improved efficiency can be explained by the transformation of powers corresponding to the second- and higher-order harmonic components into the fundamental-frequency output power because of the nonlinearity of the collector capacitance. However, this becomes effective only in the case of the load network with a series resonant circuit, because it ideally provides an infinite impedance at the second- and higher-order harmonics, unlike the load network with a parallel resonant circuit having ideally zero impedance at these harmonics.

1.8 Push-pull power amplifiers

Generally, if it is necessary to increase an overall output power of the power amplifier, several active devices can be used in parallel or push-pull configurations. In a parallel configuration, the active devices are not isolated from each other, which requires a very good circuit symmetry, and output impedance becomes too small in the case of high output power. The latter drawback can be eliminated in a push-pull configuration, which provides increased values of the input and output impedances. For the same output power level, the input impedance Z_{in} and output impedance Z_{out} under a push-pull operation mode are approximately four times as high as for a parallel connection of the active devices. At the same time, the loaded quality factors of the input and output matching circuits remain unchanged because both the real and reactive parts of these impedances are increased by the factor of four. Very good circuit symmetry can be provided using balanced active devices with common emitters in a single package. The basic concept of a push-pull operation can be analyzed by using the corresponding circuit schematic shown in Fig. 1.27.[62]

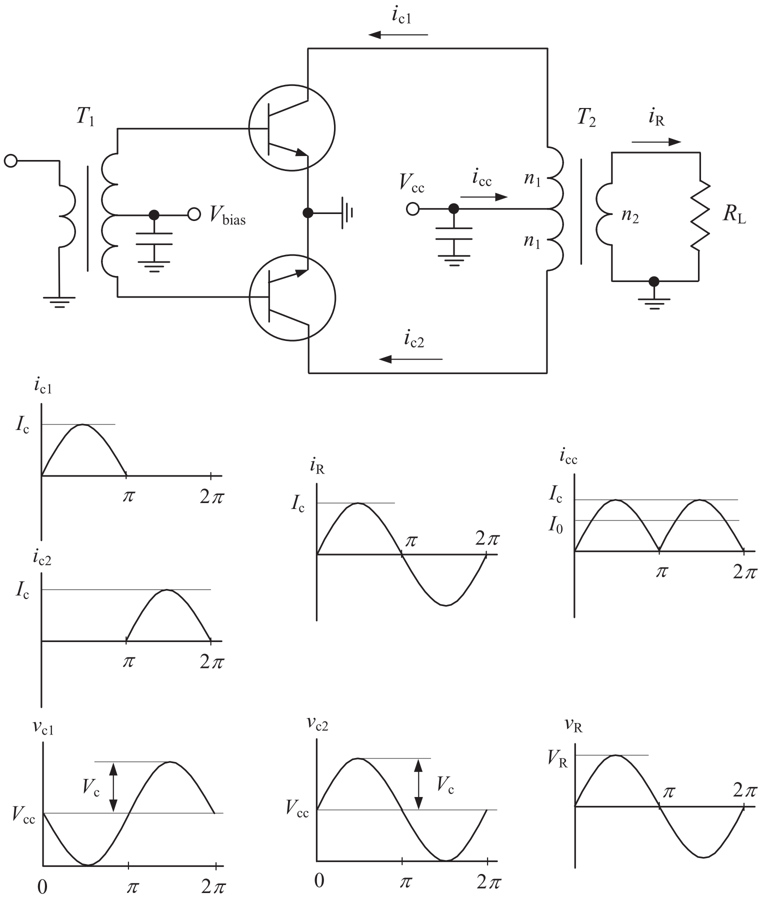

i_{c1}
T_1
T_2
i_R
V_{bias}
V_{cc}
i_{cc}
n_1
n_2
n_1
R_L
i_{c2}
i_{c1}
I_c
π
2π
i_R
I_c
π
2π
i_{cc}
I_c
I_0
π
2π
i_{c2}
I_c
π
2π
v_{c1}
V_c
V_{cc}
0
π
2π
v_{c2}
V_c
V_{cc}
0
π
2π
v_R
V_R
π
2π

FIG. 1.27

Basic concept of push-pull operation.

It is most convenient to consider an ideal Class-B operation, which means that each transistor conducts exactly half a cycle (180 degrees) with zero quiescent current. Let us also assume that the number of turns of both primary and secondary windings of the output transformer T_2 is equal ($n_1 = n_2$), and the collector current of each transistor can be presented in the following half-sinusoidal form:

for the first transistor

$$i_{c1} = \begin{cases} +I_c \sin\omega t & 0 \le \omega t < \pi \\ 0 & \pi \le \omega t < 2\pi \end{cases} \tag{1.105}$$

for the second transistor

$$i_{c2} = \begin{cases} 0 & 0 \le \omega t < \pi \\ -I_c \sin\omega t & \pi \le \omega t < 2\pi' \end{cases} \tag{1.106}$$

where I_c is the output current amplitude.

Being transformed through the output transformer T_2 with the appropriate phase conditions, the total current flowing through the load R_L is obtained as

$$i_R(\omega t) = i_{c1}(\omega t) - i_{c2}(\omega t) = I_c \sin \omega t. \tag{1.107}$$

The current flowing into the center tap of the primary windings of the output transformer T_2 is the sum of the collector currents, resulting in

$$i_{cc}(\omega t) = i_{c1}(\omega t) + i_{c2}(\omega t) = I_c |\sin \omega t|. \tag{1.108}$$

Ideally, even-order harmonics being in phase are canceled out and should not appear at the load. In practice, a level of the second-harmonic component of 30–40 dB below the fundamental is allowable. However, it is necessary to connect a bypass capacitor to the center tap of the primary winding to exclude power losses due to even-order harmonics. The current $i_R(\omega t)$ produces the load voltage $v_R(\omega t)$ onto the load R_L as

$$v_R(\omega t) = I_c R_L \sin(\omega t) = V_R \sin(\omega t), \tag{1.109}$$

where V_R is the load voltage amplitude.

The total DC collector current is defined as the average value of $i_{cc}(\omega t)$, which yields

$$I_0 = \frac{1}{2\pi} \int_0^{2\pi} i_{cc}(\omega t) d\omega t = \frac{2}{\pi} I_c. \tag{1.110}$$

For the ideal case of zero saturation voltage of both transistors when $V_c = V_{cc}$ and considering that $V_R = V_c$ for equal turns of windings when $n_1 = n_2$, the total DC power P_0 and fundamental-frequency output power P_{out} are obtained by

$$P_0 = \frac{2}{\pi} I_c V_{cc}, \tag{1.111}$$

$$P_{out} = \frac{I_c V_{cc}}{2}. \tag{1.112}$$

Consequently, the maximum theoretical collector efficiency that can be achieved in a push-pull Class-B operation is equal to

$$\eta = \frac{P_{out}}{P_0} = \frac{\pi}{4} \cong 78.5\%. \tag{1.113}$$

In a balanced circuit, identical sides carry 180 degrees out-of-phase signals of equal amplitude. If perfect balance is maintained on both sides of the circuit, the difference between signal amplitudes becomes equal to zero in each midpoint of the circuit, as shown in Fig. 1.28. This effect is called the *virtual grounding*, and this midpoint line is referred to as the *virtual ground*. The virtual ground, being actually inside the device package, reduces a common mode inductance and results in better stability and usually higher power gain.

When using a balanced transistor, new possibilities for both internal and external impedance matching procedure emerge. For instance, for a push-pull operation mode of two single-ended transistors, it is necessary to provide reliable grounding for input and output matching circuits for each device, as shown in Fig. 1.29A. Using the balanced transistors simplifies significantly the matching circuit

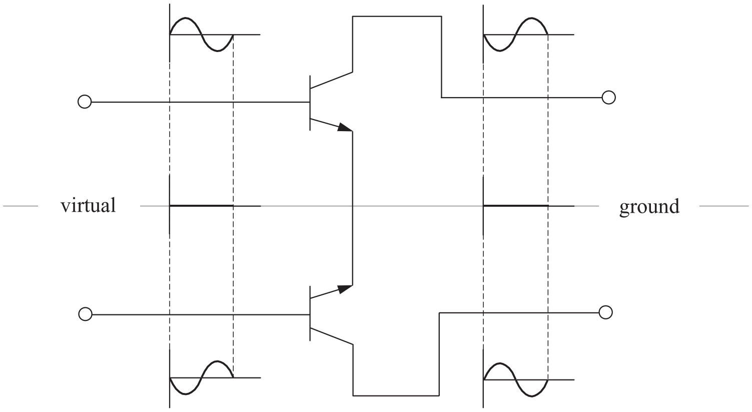


FIG. 1.28

Basic concept of a balanced transistor.

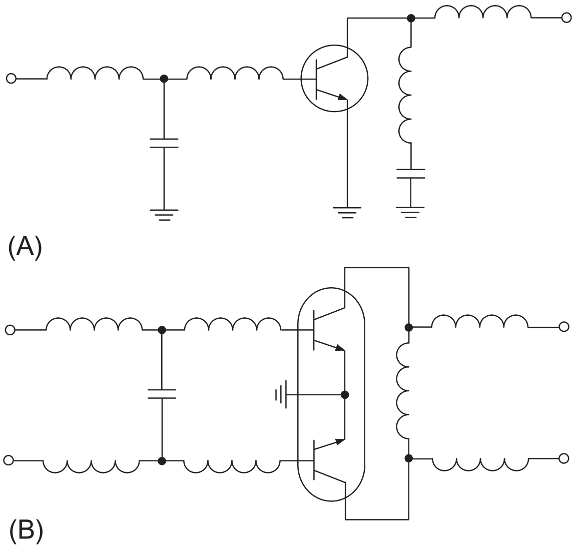


FIG. 1.29

Matching technique for single-ended and balanced transistors.

topologies with the series inductors and parallel capacitors connected between amplifying paths, as shown in Fig. 1.29B, and DC-blocking capacitors are not needed.

For a push-pull operation of the power amplifier with a balanced transistor, it is also necessary to provide the unbalanced-to-balanced transformation referenced to the ground both at the input and at the output of the power amplifier. The most suitable approach to solve this problem in the best possible manner at high frequencies and microwaves is to use the transmission-line transformers, as shown in

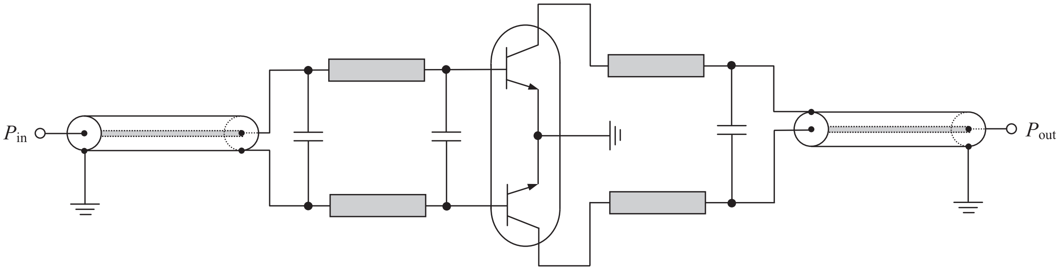


FIG. 1.30

Push-pull power amplifier with balanced-to-unbalanced transformers.

Fig. 1.30. If the characteristic impedance Z_0 of the coaxial transmission line is equal to the input impedance at the unbalanced end of the transformer, the total impedance from both devices seen at the balanced end of the transformer will be equal to the input impedance. Hence such a transmission-line transformer can be used as a 1:1 balanced-to-unbalanced (balun) transformer. For the standard input impedance of $50\,\Omega$, if $Z_0 = 50\,\Omega$, the impedance seen at each balanced part is equal to $25\,\Omega$, which then is necessary to match with the appropriate input impedance of each part of a balanced transistor. The input and output matching circuits can easily be realized by using the series microstrip lines with parallel capacitors.

The miniaturized compact input unbalanced-to-balanced transformer shown in Fig. 1.31 covers the frequency bandwidth up to an octave with well-defined rejection-mode impedances.[25, 67] To avoid the parasitic capacitance between the outer conductor and the ground, the coaxial semirigid transformer T_1 is mounted atop microstrip shorted stub l_1 and soldered continuously along its length. The electrical

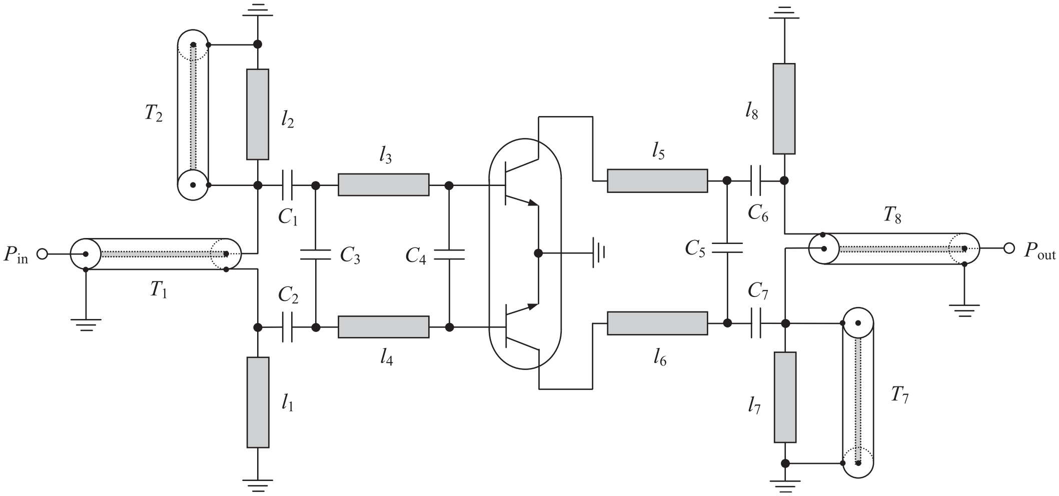


FIG. 1.31

Push-pull power amplifier with compact balanced-to-unbalanced transformers.

length of this stub is usually chosen from the condition of $\theta \leq 90$ degrees on the high bandwidth frequency depending upon the matching requirements. To maintain circuit symmetry on the balanced side of the transformer network, another semirigid coaxial section T_2 with unconnected center conductor is soldered continuously along microstrip shorted stub l_2. The lengths of T_2 and l_2 are equal to the lengths of T_1 and l_1, respectively. Because the input short-circuited microstrip stubs provide inductive impedances, the two series capacitors C_1 and C_2 of the same value are used for matching purposes, thereby forming the first high-pass matching section and providing DC blocking at the same time. The practical circuit realization of the output matching circuit and balun transformer can be the same as for the input matching circuit.

1.9 Power gain and impedance matching

Power amplifier design aims for maximum power gain and efficiency for a given value of output power with a predictable degree of stability. In order to extract the maximum power from a generator, it is a well-known fact that the external load should have a vector value that is conjugate of the internal impedance of the source.[68] The power delivered from a generator to a load, when matched on this basis, will be called the available power of the generator.[69] In this case, the power gain of the four-terminal network is defined as the ratio of the power delivered to the load impedance connected at the output terminals to the power available from the generator connected to the input terminals, usually measured in decibels, and this ratio is called the *power gain* irrespective of whether it is greater or less than one.[70, 71]

Fig. 1.32 shows the basic block schematic of a single-stage power-amplifier circuit, which includes an active device, an input matching circuit to match with the source impedance, and an output matching circuit to match with the load impedance. Generally, the two-port active device is characterized by a system of the immittance W-parameters, that is, any system of impedance Z-parameters, hybrid H-parameters, or admittance Y-parameters.[72, 73] The input and output matching circuits transform the source and load immittances W_S and W_L into specified values between points 1–2 and 3–4, respectively, by means of which the optimal design operation mode of the power amplifier is realized.

The operating power gain G_P, which represents the ratio of power dissipated in the active load ReW_L to the power delivered to the input port of the active device, can be expressed in terms of the immittance W-parameters as

$$G_P = \frac{|W_{21}|^2 \mathrm{Re}W_L}{|W_{22} + W_L|^2 \mathrm{Re}W_{in}}, \tag{1.114}$$

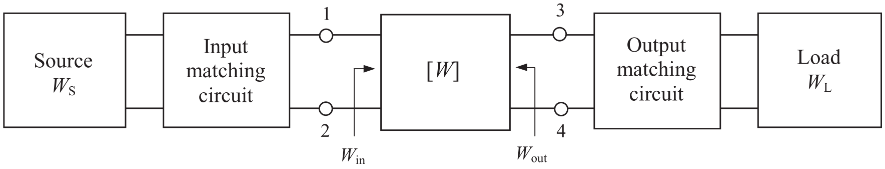


FIG. 1.32

Block schematic of single-stage power amplifier.

where

$$W_{\text{in}} = W_{11} - \frac{W_{12}W_{21}}{W_{22} + W_{\text{L}}} \tag{1.115}$$

is the input immittance, and W_{ij} $(i, j = 1, 2)$ are the immittance two-port parameters of the active device equivalent circuit.

The transducer power gain G_{T}, which represents the ratio of power dissipated in the active load $\text{Re}W_{\text{L}}$ to the power available from the source, can be expressed in terms of the immittance W-parameters as

$$G_{\text{T}} = \frac{4\,|W_{21}|^2\,\text{Re}W_{\text{S}}\,\text{Re}W_{\text{L}}}{|\,(W_{11} + W_{\text{S}})(W_{22} + W_{\text{L}}) - W_{12}W_{21}|^2}. \tag{1.116}$$

The operating power gain G_{P} does not depend on the source parameters and characterizes only the effectiveness of the power delivery from the input port of the active device to the load. This power gain helps to evaluate the gain property of a multistage amplifier when the overall operating power gain $G_{\text{P (total)}}$ is equal to the product of each stage G_{P}. The transducer power gain G_{T} includes an assumption of conjugate matching of the load and the source.

The bipolar transistor simplified small-signal Π-hybrid equivalent circuit shown in Fig. 1.33 provides an example for a conjugate-matched bipolar power amplifier. The impedance Z-parameters of the equivalent circuit of the bipolar transistor in a common-emitter configuration can be written as

$$\begin{aligned} Z_{11} &= r_{\text{b}} + \frac{1}{g_{\text{m}} + j\omega C_\pi} & \quad Z_{12} &= \frac{1}{g_{\text{m}} + j\omega C_\pi} \\ Z_{21} &= -\frac{1}{j\omega C_{\text{c}}}\frac{g_{\text{m}} - j\omega C_{\text{c}}}{g_{\text{m}} + j\omega C_\pi} & \quad Z_{22} &= \left(1 + \frac{C_\pi}{C_{\text{c}}}\right)\frac{1}{g_{\text{m}} + j\omega C_\pi}, \end{aligned} \tag{1.117}$$

where g_{m} is the transconductance, r_{b} is the series base resistance, C_π is the base-emitter capacitance, including both diffusion and junction components, and C_{c} is the feedback collector capacitance.

By setting the device feedback impedance Z_{12} to zero and complex conjugate-matching conditions at the input of $R_{\text{S}} = \text{Re}Z_{\text{in}}$ and $L_{\text{in}} = -\text{Im}Z_{\text{in}}/\omega$ and at the output of $R_{\text{L}} = \text{Re}Z_{\text{out}}$ and $L_{\text{out}} = -\text{Im}Z_{\text{out}}/\omega$, the small-signal transducer power gain G_{T} can be calculated from

$$G_{\text{T}} = \left(\frac{f_{\text{T}}}{f}\right)^2 \frac{1}{8\pi f_{\text{T}} r_{\text{b}} C_{\text{c}}}, \tag{1.118}$$

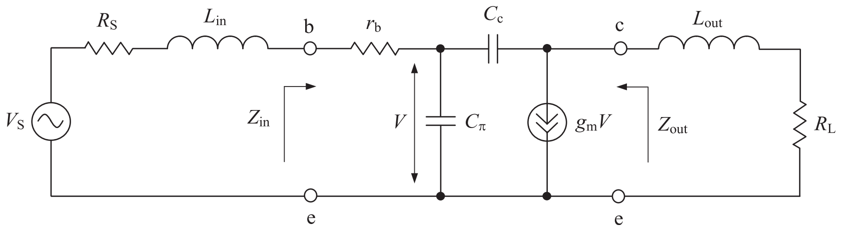


FIG. 1.33

Simplified equivalent circuit of a matched bipolar power amplifier.

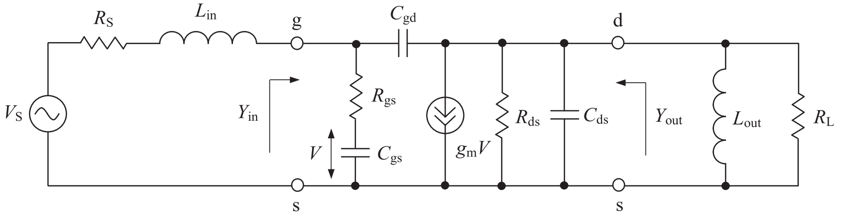


FIG. 1.34

Simplified equivalent circuit of a matched FET power amplifier.

where $f_T = g_m/2\pi C_\pi$ is the device transition frequency.

Fig. 1.34 shows the simplified circuit schematic for a conjugate-matched FET (field-effect transistor) power amplifier. The admittance Y-parameters of the small-signal equivalent circuit of any FET device in a common-source configuration can be written as

$$\begin{aligned} Y_{11} &= \frac{j\omega C_{gs}}{1 + j\omega C_{gs}R_{gs}} + j\omega C_{gd} \qquad & Y_{12} &= -j\omega C_{gd} \\ Y_{21} &= \frac{g_m}{1 + j\omega C_{gs}R_{gs}} - j\omega C_{gd} \qquad & Y_{22} &= \frac{1}{R_{ds}} + j\omega\left(C_{ds} + C_{gd}\right) \end{aligned}, \tag{1.119}$$

where g_m is the transconductance, R_{gs} is the gate-source resistance, C_{gs} is the gate-source capacitance, C_{gd} is the feedback gate-drain capacitance, C_{ds} is the drain-source capacitance, and R_{ds} is the differential drain-source resistance.

Because the value of the gate-drain capacitance C_{gd} is normally relatively small, the effect of the feedback admittance Y_{12} can be neglected in a simplified case. Then, it is necessary to set $R_S = R_{gs}$ and $L_{in} = 1/\omega^2 C_{gs}$ for input matching, while $R_L = R_{ds}$ and $L_{out} = 1/\omega^2 C_{ds}$ for output matching. Hence the small-signal transducer power gain G_T can approximately be calculated from the expression

$$G_T\left(C_{gd} = 0\right) = MAG = \left(\frac{f_T}{f}\right)^2 \frac{R_{ds}}{4R_{gs}}, \tag{1.120}$$

where $f_T = g_m/2\pi C_{gs}$ is the device transition frequency, and MAG is the maximum available gain representing a theoretical limit on the power gain that can be achieved under complex conjugate-matching conditions.

From Eqs. (1.118), (1.120), it follows that the small-signal power gain of a conjugate-matched power amplifier for any type of the active device drops off as $1/f^2$ or 6 dB per octave. Therefore $G_T(f)$ can readily be predicted at a certain frequency f, if a power gain is known at the transition frequency f_T, by

$$G_T(f) = G_T(f_T)\left(\frac{f_T}{f}\right)^2. \tag{1.121}$$

It should be noted that previous analysis is based upon the linear small-signal consideration when generally nonlinear device current source as a function of both input and output voltages can be characterized by the linear transconductance g_m as a function of the input voltage and the output differential resistance R_{ds} as a function of the output voltage. This is a result of a Taylor-series expansion of the output current as a function of the input and output voltages with maintaining only the DC and linear components. Such an approach helps to understand and derive the maximum achievable power amplifier parameters in a linear approximation. In this case, an active device is operated in a Class-A mode when one half of DC power is dissipated in the device, while the other half is transformed to the fundamental-frequency output power flowing into the load, resulting in a maximum ideal collector efficiency of 50%. The device output resistance R_{out} remains constant and can be calculated as a ratio of the DC supply voltage to the DC current flowing through the active device. In a common case, for a complex conjugate-matching procedure, the device output immittance under large-signal consideration should be calculated using a Fourier-series analysis of the output current and voltage fundamental components. This means that, unlike in a linear Class-A mode, an active device is operated in a device linear region only part of the entire period, and its output resistance is defined as a ratio of the fundamental-frequency output voltage to the fundamental-frequency output current. This is not a physical resistance resulting in a power loss inside the device but an equivalent resistance required to use for a conjugate matching procedure. In this case, the complex conjugate matching is valid and necessary, firstly, to compensate for the reactive part of the device output impedance and, second, to provide a proper load resistance, resulting in a maximum power gain for a given supply voltage and required output power delivered to the load. Note that this is not a maximum available small-signal power gain that can be achieved in a linear operation mode but a maximum achievable large-signal power gain that can be achieved for a particular operation mode with a certain conduction angle. Of course, the maximum large-signal power gain is smaller than the small-signal power gain for the same input power because the output power in a nonlinear operation mode also includes the powers at the harmonic components of the fundamental frequency.

Therefore it makes more practical sense not to separately introduce the concepts of the gain match with respect to the linear power amplifiers and the power match in nonlinear power amplifier circuits because the maximum large-signal power gain being a function of half the conduction angle θ corresponds to the maximum fundamental-frequency output power delivered to the load due to large-signal conjugate output matching. It is very important to provide a conjugate matching at both input and output device ports to achieve maximum power gain in a large-signal mode. In a Class-A mode, the maximum small-signal power gain ideally remains constant regardless of the output power level.

The transistor characterization in a large-signal mode can be done based on equivalent quasi-harmonic nonlinear approximation under the condition of sinusoidal port voltages.[74] In this case, the large-signal impedances are generally determined in the following manner. The designer tunes the load network (often by trial and errors) to maximize the output power to the required level using a particular transistor at a specified frequency and supply voltage. Then, the transistor is removed from the circuit, and the impedance seen by the collector is measured at the carrier frequency. The complex-conjugate of the measured impedance then represents the equivalent large-signal output impedance of the transistor at that frequency, supply voltage, and output power. A similar design process is used to measure the input impedance of the transistor and to maximize PAE of the power amplifier.

To deliver maximum power to the load, it is necessary to use some impedance matching network that can modify the load as viewed from the generator.[68] The design of reactance networks to connect a resistive load efficiently to a source of power can be carried out most conveniently by the theory of image impedances. In this case, if the image impedances of such a network are pure resistances and it is connected between a generator and a load whose impedances are equal to these image impedances, the impedances will match at both junctions. Under these conditions, with an assumption of pure reactances of the arms of the connecting network, no power will dissipate during transmission, and so this maximum power will be delivered to the load. If the terminating impedances are not pure resistances, they can be made so at any single frequency by additional reactance in series with them. Such reactance networks can provide not only for high efficiency but can also attenuate undesired harmonics. A variety of configurations can be designed to accomplish the desired result.[25] Generally, L-type, T-type, and Π-type configurations of reactances are used for matching networks depending on convenience of the circuit implementation and particular application technology. They can be implemented in both low-pass and high-pass topologies.

1.10 Load-pull characterization

In designing power amplifiers, it is important to know the transistor input impedance and load characteristics at a high input-driving power level and to optimize the output matching circuit based on the large-signal characteristics. A computer-controlled technique for large-signal characterization of microwave power transistors used to map contours of constant power and efficiency on a Smith chart for dynamic matching of both input and output circuits was originally developed for the interstage matching between a varactor multiplier and a transistor power stage and then successfully applied to the broadband optimization of Class-A and Class-C transistor power amplifiers.[75, 76] The power-load contours consist of a series of curves on a Smith chart representing constant-output power, approaching the point of maximum output power, as shown in Fig. 1.35A. When drawn at several frequencies over the band of interest, they represent loci of required output impedance for various output power levels. If constant-efficiency contours are overlaid on the constant-power contours, the efficiency is also known at each of the load impedances. Generally, the points for maximum output power and maximum efficiency can be located at different positions, each corresponding to its optimum impedance, as shown in Fig. 1.35B, because the maximum power is achieved at the fundamental frequency, whereas the maximum efficiency significantly depends on the effect of the second- and higher-order harmonic components.

A power transistor operated in a Class-C mode has an output equivalent circuit, which is represented by a nonlinear multiharmonic current source and a nonlinear reactance. To obtain maximum output power, the load impedance must produce the maximum current and voltage swing. The relationship between the required load impedance and nonlinear output impedance determines the shape of the power-load contour, which can vary with input drive level from elliptical to circle contours.[77] With the conventional passive load-pull technique, external tuners are adjusted, demounted, and measured. In this case, the DC bias-dependent transistor small-signal impedances can be used as references [78]. To get a variable load, in addition to the traditional passive-network technique with variable elements, an active load-pull characterization can be used where the reflection coefficient is obtained using an auxiliary signal derived from the same test generator to inject into the output port.[79, 80] One of the advantages of this technique lies in the inherent simplicity of the calibration procedure necessary to correct the transmission-line losses in the measurement system. However, its accuracy critically depends on the effective directivities of the directional couplers in the system.[81] The accuracy of the load-pull measurements can be improved by using ultralow-loss broadband tuners based on nonuniform, nonsymmetrical rectangular coaxial-to-microstrip directional couplers.[82] Independent tuning of the

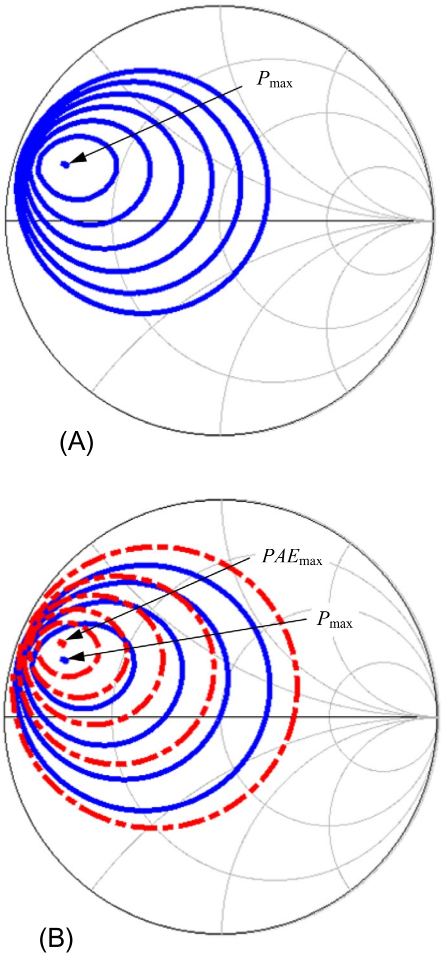


FIG. 1.35

Constant-power and constant-efficiency load-pull contours.

fundamental frequency and its second harmonic component had become possible by using a scheme with frequency-selective tuners.[83]

The load impedance Z_L, incident and reflected traveling waves a_2 and b_2, respectively, and reflection coefficient Γ_L at the output port of the transistor are related as

$$\Gamma_L = \frac{a_2}{b_2} = \frac{Z_L - Z_0}{Z_L + Z_0}, \tag{1.122}$$

where Z_0 is the characteristic impedance of the system, in which the device under test (DUT) is used. The function of the tuners is to vary the magnitude and phase of the reflected signal so as to synthesize an appropriate Γ_L. This functionality can be obtained by altering the tuner setting by way of moving the slug or stub up and down and back and forth in a passive tuner or by actively injecting a magnitude- and phase-controlled signal in active load-pull system.[84] In this case, as the stub (probe or slug) is inserted into the tuner transmission line, it introduces mismatch by adding parallel susceptance, and the parallel susceptance increases as the stub approaches the line and aids in the synthesis of the desired reflection coefficient. As a result, the magnitude of the impedance mismatch is determined by the stub position (depth), and the phase of the impedance mismatch is determined by the carriage position (length).

However, most of the load-pull tuners developed with broadband capability and intended for creating controlled impedances at the fundamental frequency f_0 have also created uncontrolled impedances at harmonic frequencies of the fundamental, such as $2f_0$ and $3f_0$. Efforts to control this test environment had led to the development of harmonic load-pull solutions, using a fundamental-frequency test tone and one or more harmonic frequencies of that fundamental frequency. The use of harmonic load-pull testing has often helped to increase the efficiency of a power amplifier or to reduce the error vector magnitude (EVM) of a power amplifier being operated in backed-off bias conditions. Early attempts to develop harmonic load-pull tuners typically inserted narrowband frequency discriminators, such as diplexers or triplexers, between a DUT and a wideband impedance tuner, as shown in Fig. 1.36A.[85, 86] The triplexer method gives full magnitude and phase control of all three harmonics f_0, $2f_0$, and $3f_0$. This results in a complete Smith chart coverage, as shown in Fig. 1.36B, limited by the losses inherent to the triplexer, but the optimal impedance may fall outside the covered area because of the restricted coverage.[86] While such an approach can provide some control over the harmonic frequencies, it is typically limited in its power range and bandwidth and susceptible to spurious signal products.

Fig. 1.37A shows the load-pull system with programmable harmonic rejection tuner (PHT) included between the load fundamental-frequency tuner and the DUT, which use a set of remote-controlled open-stub quarter-wavelength resonators at $2f_0$, and $3f_0$ having little effect on the fundamental-frequency impedance.[85, 86] This approach offers the phase control at harmonic frequencies $2f_0$ and $3f_0$ setting the magnitude at the highest attainable level, while the fundamental tuner gives full magnitude and phase control at f_0, with harmoning tuning coverage shown in Fig. 1.37B.[86] The load-pull system with a multipurpose tuner (MPT) shown in Fig. 1.38A provides full magnitude and phase control of all three harmonic frequencies f_0, $2f_0$, and $3f_0$ when nearly the entire Smith chart is covered because of multiplicity of tunable probe combinations, as shown in Fig. 1.38B, resulting in impedance matching at all the three frequencies with a high tuning accuracy and harmonic tuning isolation.[85, 86] The MPT is essentially a cascade of three wideband, single-probe tuners, all covering the same bandwidth and contained within a single instrument housing.

Generally, the number of probes determines the possible tuner setting, as shown in Fig. 1.39, and a three-probe load-pull tuner system allows an almost infinite number of different probe position combinations.[85] However, a load-pull system with three integrated probes must be calibrated within a limited period of time, and developing such a system requires the development of efficient tuning algorithms using the calibration data. Hence a three-probe MPT system with its greater complexity can present a significant number of issues to overcome, especially tuning time.

Generally, tuning with a load-pull system (mechanical or fully automatic) is a very complicated procedure, especially if it is necessary to consider several harmonics of the fundamental frequency. Besides, it can only give the optimum input and output impedances, which are usually incorporated in datasheet for power transistors for specified output power, supply voltage, and frequency range.

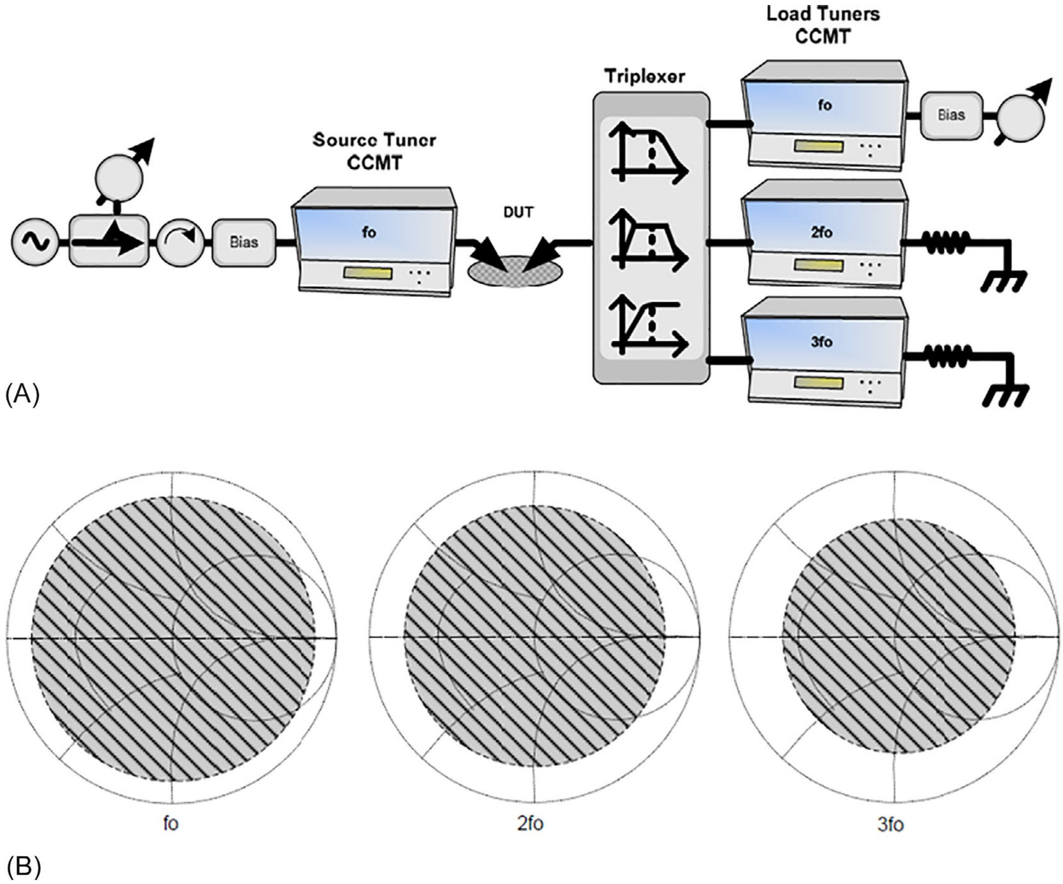


FIG. 1.36

Harmonic load-pull system with triplexer and tuning coverage at f_0, $2f_0$, and $3f_0$.

Courtesy of Focus Microwaves.

In a monolithic implementation, however, this is difficult to physically realize, and this can be done based on the load-pull setup incorporated into the simulation tool. But, in all cases, this measurement should be followed by the subsequent load-network design with real elements. Therefore in most cases, where the device nonlinear model is available, the device equivalent output circuit can be represented by the output admittance where the equivalent output resistance R_{out} can be estimated from Eq. (1.44) for certain half the conduction angle θ and supply voltage V_{cc}, which is equal in an ideal case to the cosine voltage amplitude (the corresponding device saturation voltage can be subtracted). For example, in a Class-B mode with $\theta = 90$ degrees, it is written as $R_{\text{L}} = R_{\text{out}} = V/I_1 = V_{\text{cc}}^2/2P_{\text{out}}$, where P_{out} is the maximum fundamental-frequency power delivered to the load, and the output shunt reactance is represented by the sum of the output and feedback capacitances.

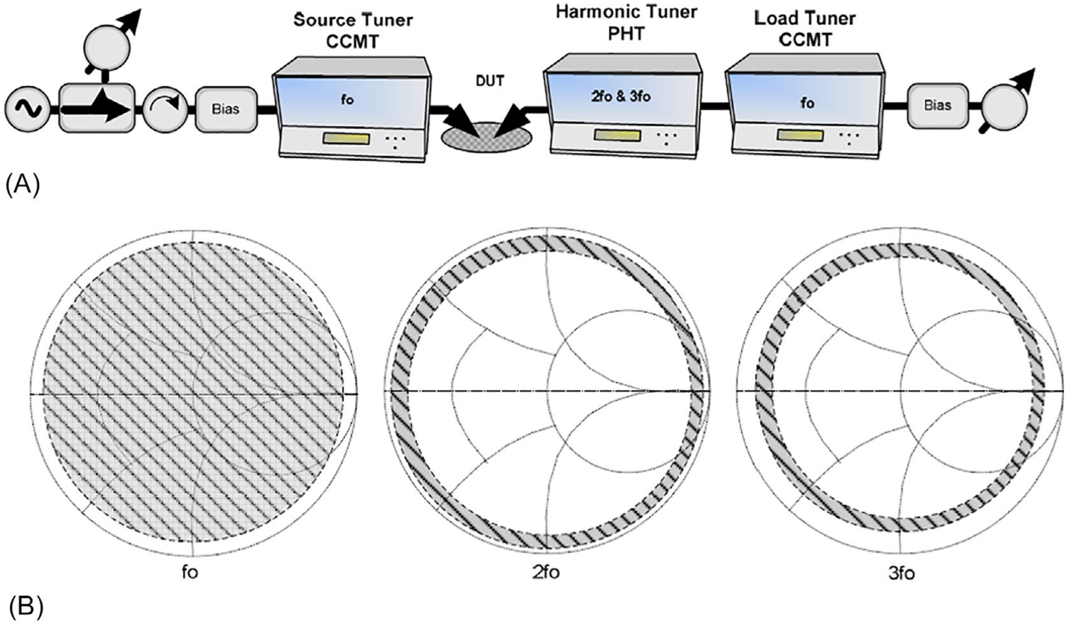


FIG. 1.37

Harmonic load-pull system with harmonic rejection tuners and tuning coverage at f_0, $2f_0$, and $3f_0$.

Courtesy of Focus Microwaves.

1.11 Amplifier stability

In early radio frequency vacuum-tube transmitters, it was observed that the tubes and associated circuits may have damped or undamped oscillations depending upon the circuit losses, the feedback coupling, the grid and anode potentials, and the reactance or tuning of the parasitic circuits.[87, 88] Various parasitic oscillator circuits such as the tuned-grid-tuned-anode circuit with capacitive feedback, Hartley, Colpitts, or Meissner oscillators can be realized at high frequencies, which potentially can be eliminated by adding a small resistor close to the grid or anode connections of the tubes for damping the circuits. Inductively coupled rather than capacitively coupled input and output circuits should be used wherever possible.

According to the immittance approach to the stability analysis of the active nonreciprocal two-port network, it is necessary and sufficient for its unconditional stability if the following system of equations can be satisfied for the given active device:

$$\mathrm{Re}[W_S(\omega) + W_{in}(\omega)] > 0, \tag{1.123}$$

$$\mathrm{Im}[W_S(\omega) + W_{in}(\omega)] = 0, \tag{1.124}$$

or

$$\mathrm{Re}[W_L(\omega) + W_{out}(\omega)] > 0, \tag{1.125}$$

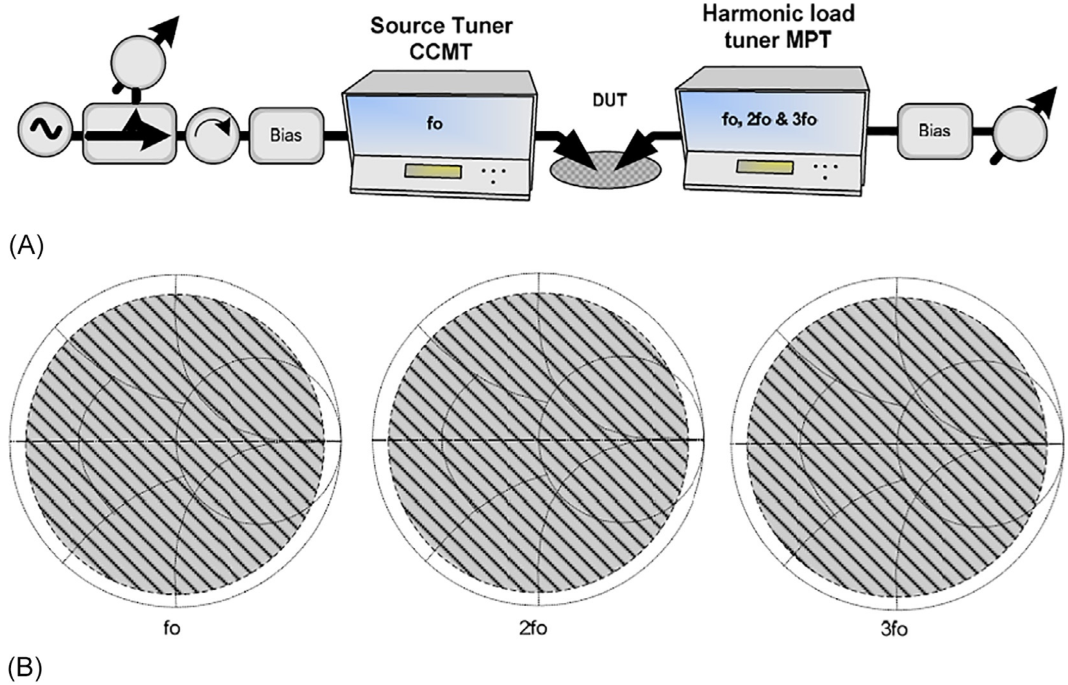


FIG. 1.38

Harmonic load-pull system with multipurpose tuner and tuning coverage at f_0, $2f_0$, and $3f_0$.

Courtesy of Focus Microwaves.

$$\mathrm{Im}[W_\mathrm{L}(\omega)+W_\mathrm{out}(\omega)]=0, \tag{1.126}$$

where $\mathrm{Re}W_\mathrm{S}$ and $\mathrm{Re}W_\mathrm{L}$ are considered to be greater than zero.[89, 90] The active two-port network can be treated as unstable or potentially unstable in the case of the opposite signs in Eqs. (1.123), (1.125).

Analysis of Eq. (1.123) or (1.125) on extremum results in a special relationship between the device immittance parameters is called the device stability factor

$$K=\frac{2\,\mathrm{Re}W_{11}\,\mathrm{Re}W_{22}-\mathrm{Re}(W_{12}W_{21})}{|W_{12}W_{21}|}, \tag{1.127}$$

which shows a stability margin, indicating how far from zero value are the real parts in Eqs. (1.123), (1.125) if they are positive.[90] An active device is unconditionally stable if $K\geq 1$ and potentially unstable if $K<1$.

When the active device is potentially unstable, an improvement of the power amplifier stability can be provided with the appropriate choice of the source and load immittances W_S and W_L, respectively. In this case, the circuit stability factor K_T is defined in the same way as the device stability factor K (with the addition of $\mathrm{Re}W_\mathrm{S}$ and $\mathrm{Re}W_\mathrm{L}$ to the device W-parameters) and written as

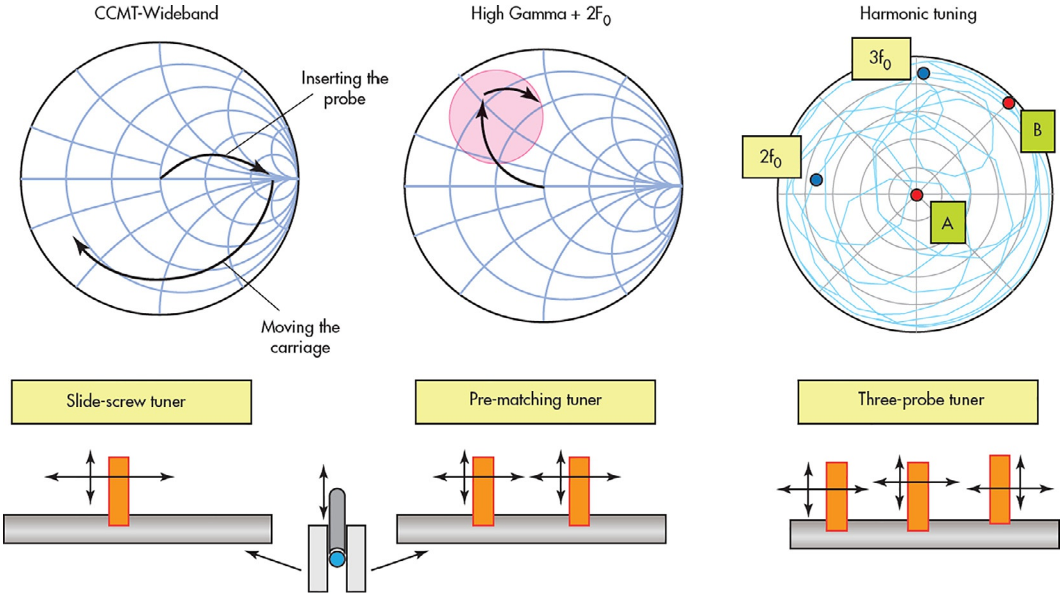


FIG. 1.39

Three-probe load-pull tuner with different probe position combinations.

Courtesy of Focus Microwaves.

$$K_T = \frac{2\mathrm{Re}(W_{11} + W_S)\mathrm{Re}(W_{22} + W_L) - \mathrm{Re}(W_{12}W_{21})}{|W_{12}W_{21}|}. \tag{1.128}$$

If the circuit stability factor $K_T \geq 1$, the power amplifier is unconditionally stable. However, the power amplifier becomes potentially unstable if $K_T < 1$. The value of $K_T = 1$ corresponds to the border of the circuit's unconditional stability. The values of the circuit stability factor K_T and device stability factor K become equal if $\mathrm{Re}W_S = \mathrm{Re}W_L = 0$.

For active device stability factor $K > 1$, the operating power gain G_P has to be maximized. By analyzing Eq. (1.114) in extremum, it is possible to find optimum values $\mathrm{Re}W_L^o$ and $\mathrm{Im}W_L^o$ when the operating power gain G_P is maximal.[91, 92] As a result,

$$G_{\mathrm{Pmax}} = \left|\frac{W_{21}}{W_{12}}\right| / \left(K + \sqrt{K^2 - 1}\right). \tag{1.129}$$

The power amplifier with an unconditionally stable active device provides a maximum power gain operation only if the input and output of the active device are conjugate matched with the source and load impedances, respectively. For the lossless input matching circuit when the power available at the source is equal to the power delivered to the input port of the active device, that is, $P_S = P_{\mathrm{in}}$, the maximum operating power gain is equal to the maximum transducer power gain, that is, $G_{P_{\max}} = G_{T_{\max}}$.

Domains of the device's potential instability include the operating frequency ranges with $K < 1$. Within the bandwidth of such a frequency domain, the parasitic oscillations can occur, defined by internal positive feedback and operating conditions of the active device. The instabilities may not be self-sustaining, induced by the RF drive power but remaining on its removal. One of the most serious cases of the power amplifier instability can occur when there is a variation of the load impedance. Under these conditions, the transistor may be destroyed almost instantaneously. However, even if it is not destroyed, the instability can result in an increased level of the spurious emissions in the output spectrum of the power amplifier tremendously. Generally, the following classification for linear instabilities can be made[93]:

- Low-frequency oscillations produced by thermal feedback effects.
- Oscillations due to internal feedback.
- Negative resistance or conductance-induced instabilities due to transit-time effects, avalanche multiplication, etc.
- Oscillations due to external feedback as a result of insufficient decoupling of the DC supply, etc.

Therefore it is very important to determine the effect of the device feedback parameters on the origin of the parasitic self-oscillations and to establish possible circuit configurations of the parasitic oscillators. Based on the simplified bipolar equivalent circuit shown in Fig. 1.33, the device stability factor can be expressed through the parameters of the transistor equivalent circuit as

$$K = 2r_b g_m \frac{1 + \dfrac{g_m}{\omega_T C_c}}{\sqrt{1 + \left(\dfrac{g_m}{\omega C_c}\right)^2}}, \tag{1.130}$$

where $\omega_T = 2\pi f_T$.[25, 52]

At very low frequencies, the bipolar transistors are potentially stable, and the fact that $K \to 0$ when $f \to 0$ can be explained by simplifying the bipolar equivalent circuit. In practice, at low frequencies, it is necessary to consider the dynamic base-emitter resistance r_π and Early collector-emitter resistance r_{ce}, the presence of which substantially increases the value of the device stability factor. This gives only one unstable frequency domain with $K < 1$ and low-boundary frequency f_{p1}. However, an additional region of possible low-frequency oscillations can occur due to thermal feedback, where the collector junction temperature becomes frequently dependent, and the common-base configuration is especially affected by this.[94]

Equating the device stability factor K with unity allows us to determine the high-boundary frequency of a frequency domain of the bipolar transistor potential instability as

$$f_{p_2} = \frac{g_m}{2\pi C_c} \bigg/ \sqrt{(2r_b g_m)^2 \left(1 + \frac{g_m}{\omega_T C_c}\right)^2 - 1}. \tag{1.131}$$

When $r_b g_m > 1$ and $g_m \gg \omega_T C_c$, Eq. (1.131) is simplified to

$$f_{p_2} \approx \frac{1}{4\pi r_b C_\pi}. \tag{1.132}$$

At higher frequencies, the presence of the parasitic reactive intrinsic transistor parameters and package parasitics can be of great importance in view of power amplifier stability. The parasitic series emitter lead inductance L_e shown in Fig. 1.40 has a major effect on the device stability factor. The presence of L_e leads to the appearance of the second frequency domain of potential instability at higher frequencies.

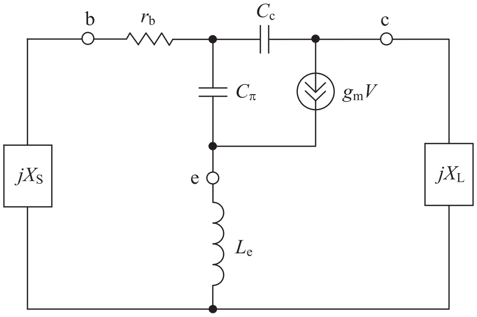


FIG. 1.40

Simplified bipolar equivalent circuit with emitter lead inductance.

The circuit analysis shows that the second frequency domain of potential instability can be realized only under certain ratios between the normalized parameters $\omega_T L_e / r_b$ and $\omega_T r_b C_c$.[25, 52] For example, the second domain does not occur for any values of L_e when $\omega_T r_b C_c \geq 0.25$.

An appearance of the second frequency domain of the device potential instability is the result of the corresponding changes in the device feedback phase conditions and takes place only under a simultaneous effect of the collector capacitance C_c and emitter lead inductance L_e. If the effect of one of these factors is lacking, the active device is characterized by only the first domain of its potential instability. Fig. 1.41 shows the potentially realizable equivalent circuits of the parasitic oscillators. If the value of a series-emitter inductance L_e is negligible, the parasitic oscillations can occur only when the values of

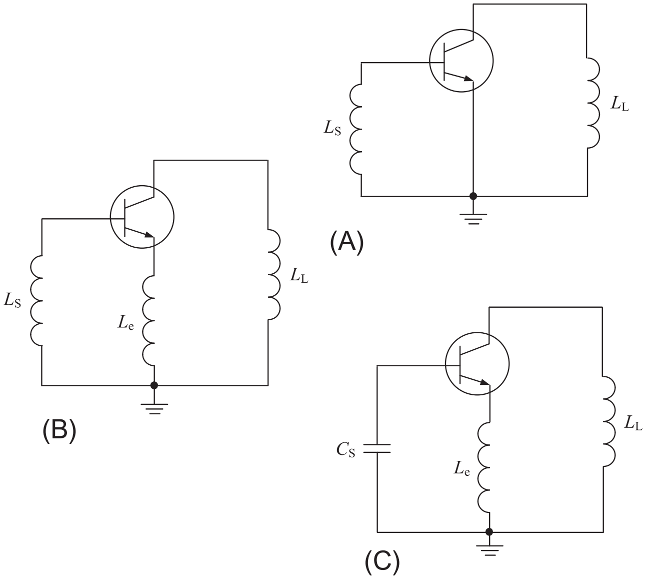


FIG. 1.41

Equivalent circuits of parasitic bipolar oscillators.

the source and load reactances are positive, that is, $X_S > 0$ and $X_L > 0$. In this case, the parasitic oscillator shown in Fig. 1.41A represents the inductive three-point circuit, where the inductive elements L_S and L_L in combination with the collector capacitance C_c form a Hartley oscillator. From a practical point of view, the more the value of the collector DC-feed inductance exceeds the value of the base-bias inductance, the more likely low-frequency parasitic oscillators can be created. It was observed that a very low inductance, even a short between the emitter and the base, can produce very strong and dangerous oscillations that may easily destroy a transistor.[93] Therefore it is recommended to increase a value of the base choke inductance and to decrease a value of the collector choke inductance.

The presence of L_e leads to narrowing of the first frequency domain of the potential instability, which is limited to the high-boundary frequency f_{p2} and can contribute to appearance of the second frequency domain of the potential instability at higher frequencies. The parasitic oscillator that corresponds to the first frequency domain of the device potential instability can be realized only if the source and load reactances are inductive, that is, $X_S > 0$ and $X_L > 0$, with the equivalent circuit of such a parasitic oscillator shown in Fig. 1.41B. The parasitic oscillator corresponding to the second frequency domain of the device potential instability can be realized only if the source reactance is capacitive and the load reactance is inductive, that is, $X_S < 0$ and $X_L > 0$, with the equivalent circuit shown in Fig. 1.41C. The series emitter inductance L_e is an element of fundamental importance for the parasitic oscillator that corresponds to the second frequency domain of the device potential instability. It changes the circuit phase conditions, so it becomes possible to establish the oscillation phase-balance condition at high frequencies. Increasing of L_e will result to narrowing of a low-frequency domain of potential instability, thus making the power amplifier potentially more stable, although at the expense of reduced power gain.

A similar analysis of the MOSFET power amplifier also shows two frequency domains of MOSFET potential instability due to the internal feedback gate-drain capacitance C_{gd} and series source inductance $L_{s.}$[25] Because of the very high gate-leakage resistance, the value of the low-boundary frequency f_{p1} is sufficiently small. For usually available conditions for power MOSFET devices when $g_m R_{ds} = 10$–30 and $C_{gd}/C_{gs} = 0.1$–0.2, the high boundary frequency f_{p2} can approximately be calculated from

$$f_{p2} \approx \frac{1}{4\pi R_{gs} C_{gs}}. \tag{1.133}$$

It should be noted that power MOSFET devices have a substantially higher value of $g_m R_{ds}$ at small values of the drain current than at its high values. Consequently, for small drain current, the MOSFET device is characterized by a wider domain of potential instability. This domain is significantly wider than the same first domain of the potential instability of the bipolar transistor. The series source inductance L_s contributes to the appearance of the second frequency domain of the device potential instability. The potentially realizable equivalent circuits of the MOSFET parasitic oscillators are the same as for the bipolar transistor shown in Fig. 1.41.[25]

Thus to prevent the parasitic oscillations and to provide a stable operation mode of any power amplifier, it is necessary to take into consideration the following common requirements:

- Use an active device with stability factor $K > 1$.
- If it is impossible to choose an active device with $K > 1$, it is necessary to provide the circuit stability factor $K_T > 1$ by the appropriate choice of the real parts of the source and load immittances.

- Disrupt the equivalent circuits of the possible parasitic oscillators.
- Choose proper reactive parameters of the matching circuit elements adjacent to the input and output ports of the active device, which are necessary to avoid the self-oscillation conditions.

Generally, the parasitic oscillations can arise at any frequency within the potential instability domains for certain values of the source and load immittances W_S and W_L, respectively. The frequency dependences of W_S and W_L are very complicated and very often cannot be predicted exactly, especially in multistage power amplifiers. Therefore it is very difficult to propose a unified approach to provide a stable operation mode of the power amplifiers with different circuit configurations and operation frequencies. In practice, the parasitic oscillations can arise close to the operating frequencies because of the internal positive feedback inside the transistor and at the frequencies sufficiently far from the operating frequencies because of the external positive feedback created by the surface mounted elements. As a result, the stability analysis of the power amplifier must include the methods to prevent the parasitic oscillations in different frequency ranges.

It should be noted that expressions in Eqs. (1.123)–(1.129) are given using the device immittance Z- or Y-parameters that allow the power gain and stability to be calculated using the parameters of the device equivalent circuit and to physically understand the corresponding effect of each circuit parameter but not through the scattering S-parameters, which are very convenient during the measurement procedure required for device modeling. Moreover, using modern simulation tools, there is no need to even draw the stability circles on a Smith chart or analyze the stability K-factor across the wide frequency range because K-factor is just an analytical derivation from the basic stability conditions and usually is a function of linear parameters, which can only reveal linear instabilities. Besides, it is difficult to predict unconditional stability for a multistage power amplifier because parasitic oscillations can be caused by the interstage circuits. In this case, the easiest and most effective way to provide stable operation of the multistage power amplifier (or single-stage power amplifier) is to simulate the real part of the device input impedance $Z_{in} = V_{in}/I_{in}$ at the input terminal of each transistor as a ratio between the input voltage and current by placing a voltage node and a current meter, as shown in Fig. 1.42A. If $\mathrm{Re}Z_{in} < 0$, then either a small series resistor must be added to the device base terminal as a part of the input matching circuit or a load-network configuration can be properly chosen to provide the resulting positive value of $\mathrm{Re}Z_{in}$. In this case, not only linear instabilities with small-signal soft startup oscillation conditions but also nonlinear instabilities with large-signal hard startup oscillation conditions or parametric oscillations can be identified around the operating region. Fig. 1.42B shows the parallel RC stabilizing circuit with a bypass capacitor C_{bypass} connected in series to the input port of a GaN HEMT device.[95] In this case, using a stabilizing resistor R_{gate} and a low-value gate-bias resistor R_{bias} improves the stability factor considerably at low frequencies without affecting the device performance at higher frequencies.

Fig. 1.43 shows the example of a stabilized bipolar VHF power amplifier configured to operate in a zero-bias Class-C mode. Conductive input and output loading due to resistances R_1 and R_2 eliminate a low-frequency instability domain. The series inductors L_3 and L_4 contribute to higher power gain if the resistance values are too small and can compensate for the capacitive input and output device impedances. To provide a negative-bias Class-C mode, the shunt inductor L_2 can be removed. The equivalent circuit of the potential parasitic oscillator at higher frequencies is realized by means of the parasitic reactive parameters of the transistor and external circuitry. The only possible equivalent circuit of such a parasitic oscillator at these frequencies is shown in Fig. 1.41C. It can only be realized if the series-

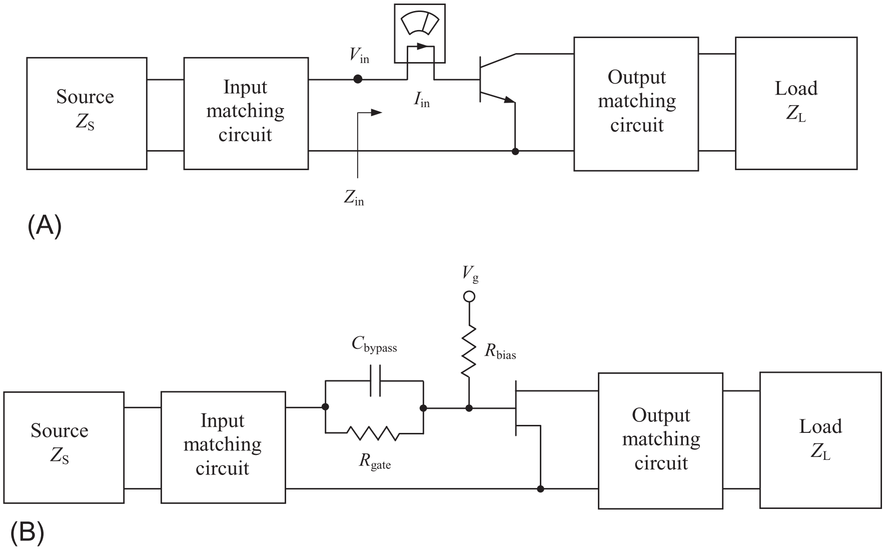

Source
Z_S
Input matching circuit
V_{in}
I_{in}
Z_{in}
Output matching circuit
Load
Z_L
(A)
V_g
C_{bypass}
R_{bias}
R_{gate}
Source
Z_S
Input matching circuit
Output matching circuit
Load
Z_L
(B)

FIG. 1.42

Single-stage power amplifiers with measured device input impedance.

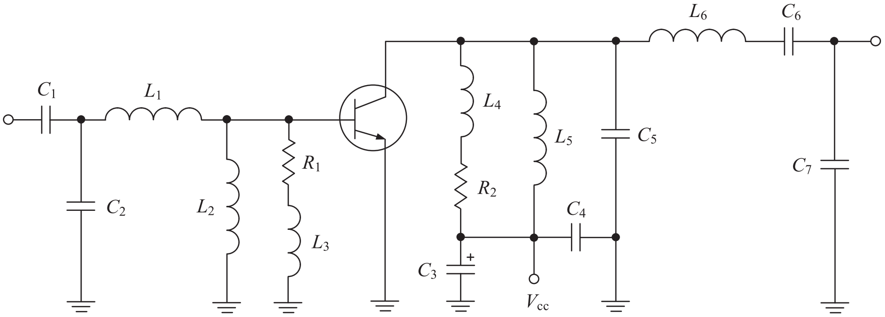

C_1
L_1
C_2
L_2
R_1
L_3
L_4
R_2
C_3
L_5
V_{cc}
C_4
C_5
L_6
C_6
C_7

FIG. 1.43

Stabilized bipolar Class-C VHF power amplifier.

emitter lead inductance is present. Consequently, the electrical length of the emitter lead should be reduced as much as possible, or, alternatively, the appropriate reactive immittances at the input and output transistor ports are provided. For example, it is possible to avoid the parasitic oscillations at these frequencies if the inductive immittance is provided at the input of the transistor and capacitive reactance is provided at the output of the transistor. This is realized by an input series inductance L_1 and an output shunt capacitance C_5.

The collector efficiency of the power amplifier can be increased by removing the shunt capacitor and series *RL*-circuit in the load network. The remaining series *LC* circuit provides high impedances at the second- and higher-order harmonic components of the output current, which flows now through the device collector capacitance unlike being grounded by the shunt capacitance. As a result, the bipolar Class-C power amplifier, whose circuit schematic is shown in Fig. 1.44, achieved a collector efficiency of 73% and a power gain of 9 dB with an output power of 13.8 W at an operating frequency of 160 MHz.[96] However, special care must be taken to eliminate parasitic spurious oscillations. In this case, the most important element in preventing the potential instability is the base bias resistor R_b. For example, for a relatively large base choke inductance L_b and $R_b = 1\,k\Omega$, spurious oscillations exist at any tuning. Tuning becomes possible with no parasitic oscillations when the output voltage standing wave ratio ($VSWR$) is less than 1.3 or supply voltage more than 22 V for reduced R_b to 470 Ω. However, a very small reduction in input driving power causes spurious oscillations. Further reduction of R_b to 47 Ω provides a stable operation for output $VSWR \leq 7$ and supply voltages down to 7 V. Finally, no spurious oscillations occur at any load, supply voltage, and driving power level for $R_b = 26\,\Omega$.

1.12 Parametric oscillations

Because the transistor using as an active device in power amplifiers is characterized by a substantially nonlinear behavior, this can result in nonlinear instabilities, which provide generally the parametric generation of both harmonic and subharmonic components. The presence of subharmonics can be explained by parametric varactor-junction action of the collector-base voltage-dependent capacitance when the large-signal driving acts like pumping a varactor diode, as in a parametric amplifier.[97, 98] Such an amplifier exhibits negative resistance under certain conditions when a circuit starts oscillating at subharmonics or rational fractions of the operating frequency.[99, 100] Generally, the parametric oscillations are the result of the external force impact on the element of the oscillation system by varying its parameter. Understanding of the physical origin of this parametric effect is very important in order to disrupt any potentially realizable parametric oscillator circuits. It is an especially serious concern for a high-efficiency power amplifier with very high voltage peak factor and voltage swing across

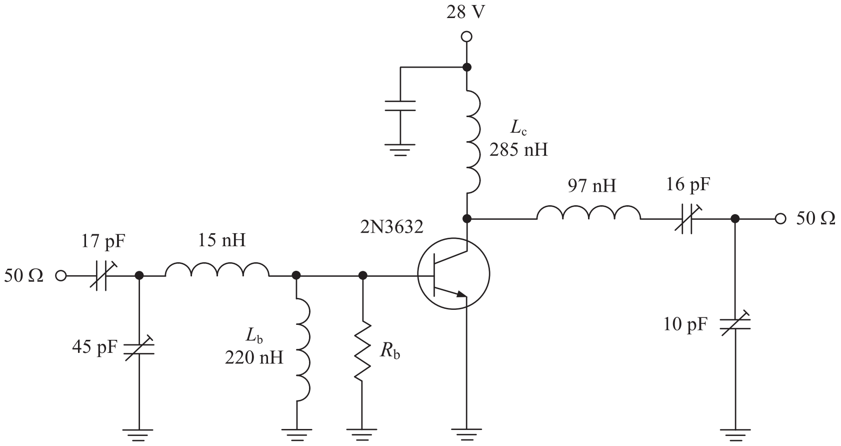


FIG. 1.44

High-efficiency VHF bipolar Class-C power amplifier.

the device nonlinear output capacitance because the transistor is operated in pinch-off, active, and saturation regions.

Fig. 1.45 shows the simplified large-signal equivalent circuit of the (A) MOSFET device and (B) bipolar device with a nonlinear current source $i(t)$, respectively. The most nonlinear capacitances are the bipolar collector capacitance C_c and the MOSFET gate-drain capacitance C_{gd} and drain-source capacitance C_{ds}, which can be modeled as junction capacitances with different grading coefficients (or sensitivities) γ. However, because the drain-source capacitance C_{ds} is normally greater by about the order than the gate-drain capacitance C_{gd}, the parametric effect because of C_{ds} causes a major effect on potential parametric oscillations in a MOSFET power amplifier. The value of the collector capacitance C_c is by the order smaller than the value of the base-emitter capacitance C_π in active mode. In this case, the circuit of a potential parametric oscillator represents a system with one degree of freedom, as shown in Fig. 1.45C, where V_{cc} is the supply voltage applied to the varying output capacitance C_{out} ($C_{out} \approx C_c$ for a bipolar device and $C_{out} \approx C_{ds}$ for a MOSFET device), while the capacitor C_0 and inductor L_0 represent the series high-Q resonant circuit tuned to the fundamental frequency having high impedances at the second- and higher-order harmonics.

The theoretical analysis can be simplified by representing the output power amplifier circuit in the form of a basic series RLC circuit, as shown in Fig. 1.46A.[101] Let us assume that the nonlinear

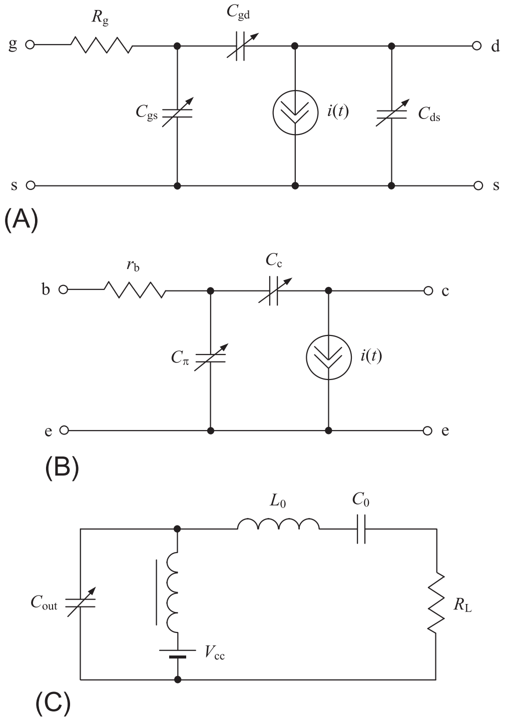


FIG. 1.45

Simplified nonlinear transistor models and output amplifier circuit.

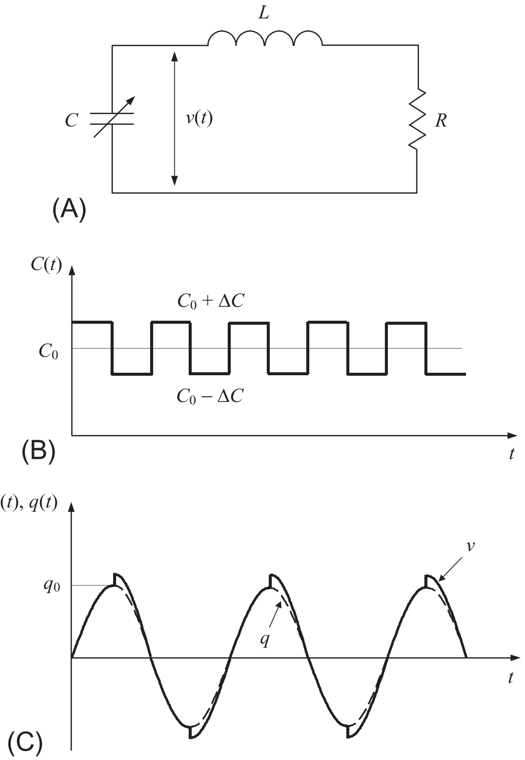


FIG. 1.46

Nonlinear resonant circuit with parametric pumping.

capacitance C varies in time relatively its average value C_0 because of external large-signal voltage drive representing a pulsed function, as shown in Fig. 1.46B, while the charge $q(t)$ generally represents a sinusoidal function of time shown in Fig. 1.46C. When the capacitance C decreases by $2\Delta C$, the voltage amplitude $V_0 = q_0 C_0$ across the capacitor and the energy $W_0 = q_0^2/2C_0$ stored by the capacitor just prior to its stepped change increases. The charge $q(t)$ during these rapid capacitance variations in time does not change its behavior being a slowly time-varying parameter. In this case, if $\Delta C \ll C_0$, the increment of the energy obtained by the capacitor at the single-step moment is defined as $\Delta W = W_0 2\Delta C/C_0 = 4mq_0^2/2C_0$, where $m = \Delta C/C_0$ is the parameter modulation factor.

The maximum energy contribution into the oscillation system will be at the times of maximum charge amplitude q_0, and no energy contribution will be at zero-crossing. This means that the capacitance as a parameter changes two times faster than the oscillation frequency. The entire energy increment into the system for a period will be $2\Delta W$. At the same time, the energy lost during the period $T = 2\pi/\omega$ for the sinusoidal charge variation with amplitude q_0 is defined as $0.5R\omega^2 q_0^2 T = \pi\omega q_0^2 R$. If the losses in the oscillation system are smaller than the energy input into the system when $4mq_0^2/2C_0 > \pi\omega q_0^2 R$ or $m > 0.5\pi\omega R C_0$, the build-up of the self-oscillations can occur. Such a process of the excitation of self-oscillations due to periodic changes of the energy-storing parameter of an oscillation system is called the *parametric excitation of self-oscillations* or *parametric resonance*. If the capacitance C varies with the same periodicity but having a different behavior, quantitatively the result will be the same.

Now assume that the nonlinear capacitance C in the oscillation system is time varying according to

$$C(t) = \frac{C_0}{1 + m\cos pt}, \tag{1.134}$$

where $p = 2\omega/n$ is the frequency of the parameter variation, ω is the frequency of the self-oscillations, and $n = 1, 2, 3, \ldots$

The voltage across the nonlinear capacitance C with abrupt junction grading coefficient $\gamma = 0.5$ can be written as

$$v(t) = \frac{1}{C_0}\left(q - \beta q^2\right), \tag{1.135}$$

where C_0 is the small-signal capacitance corresponding to the DC-bias condition, and β is the coefficient responsible for the capacitance nonlinear behavior. The mathematical description of parametric oscillations in a single-resonant oscillation system with a time-varying junction capacitance $C(t)$ can be done based on the second-order differential equation characterizing this circuit, which can generally be written in the form

$$\frac{d^2q}{dt^2} + 2\delta\frac{dq}{dt} + \omega_0^2(1 + m\cos pt)\left(q - \beta q^2\right) = 0, \tag{1.136}$$

where $\omega_0 = 1/\sqrt{LC_0}$ is the small-signal resonant frequency, $2\delta = \omega_0/Q$ is the dissipation factor, and $Q = \omega_0 L/R$ is the quality factor of the resonant circuit.[101] In a linear case when $\beta = 0$, Eq. (1.136) simplifies to a well-known Mathieu equation, the stable and unstable solutions and important properties of which are thoroughly developed and analyzed.

The basic results in a graphical form presenting the domains of the potential parametric instability as a function of the parameter $n = 2\omega_0/p$ are plotted in Fig. 1.47. The shaded areas corresponding to a

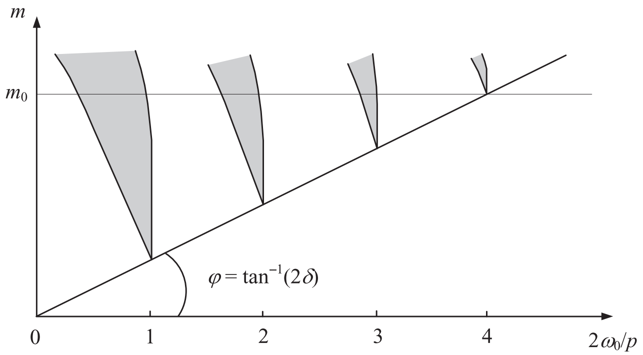


FIG. 1.47

Domains of parametric instability for damping systems.

growing self-oscillating process with a frequency $\omega = np/2 \approx \omega_0$ rise, and their ends are located on the line having an angle φ with a horizontal axis. This means that the greater the dissipation factor 2δ of the oscillation system, the greater modulation factor m is necessary to realize the parametric oscillations. For a fixed modulation factor m_0, the width of the instability domain for different n is different, being smaller for higher n. As this number grows due to more seldom energy input into the system ($p = 2\omega/n$), it is necessary to increase the modulation factor. The effect of nonzero β in the nonlinear voltage-charge dependence given in Eq. (1.135) leads to a deviation of the oscillation frequency in a steady-state mode from its start-up value because the averaged junction capacitance differs from its small-signal value for a large-signal mode. The difference becomes greater with the growth of the oscillation amplitude reaching the border of the instability domain. This decreases the energy input into the oscillation, thus limiting the increase in amplitude.

Consequently, the most probable parametric oscillations in the nonlinear power amplifier can occur at a subharmonic frequency $\omega_{1/2} = \omega_p/2$, where ω_p is the operating frequency varying the device capacitance. In this case, the subharmonic frequency $\omega_{1/2}$ corresponds to the resonant frequency ω_0 of the circuit shown in Fig. 1.46A, being equal to half the operating frequency ω_p, that is, $n = 1$ and $p = \omega_p = 2\omega_0$. Hence to eliminate such a parasitic subharmonic parametric oscillation, it is necessary to provide the circuit design solution when the device output can see very high impedance at a subharmonic frequency $\omega_{1/2}$. Alternatively, an additional lossy element in the subharmonic circuit with its proper isolation from the fundamental circuit can be incorporated. In other words, it is necessary to break out any possible resonant conditions at the subharmonic frequency component, which can cause the parametric oscillations.

Thus while the power amplifier may appear perfectly stable under small-signal conditions, oscillations can occur as the power amplifier is driven harder. These oscillations tend to be very sensitive to input drive, bias conditions, and operating frequency. Fig. 1.48A shows the subharmonic $f/2$ ($f_{1/2}$) and $3f/2$ ($f_{3/2}$) oscillations, where f is the operating frequency of 12 GHz, while Fig. 1.48B shows the 200-MHz spurious oscillations that appeared because of the modulation effect around the fundamental and subharmonic frequencies as the power amplifier was driven about 0.5 dB into compression.[102, 103] In this case, to eliminate the parametric oscillations, the parallel *RC* network at the device input, as shown in Fig. 1.42B, is used when the capacitance is chosen so that the capacitive reactance was equal to the resistance at the low end of the frequency bandwidth. In a three-stage monolithic InGaP/GaAs HBT power amplifier operating in *Ku*-band, the stabilizing *RC* circuit was connected in series at the transistor inputs in the second and third stages.[104]

Although the parametric oscillation often takes place at the subharmonic frequency $f_0/2$, it also may happen at a frequency f_a, which is nonharmonically related with the operating frequency f_0, thus resulting in either a frequency division or a mixer-like behavior with two fundamental frequencies f_0 and f_a. In the latter case, the circuit behaves like a self-oscillating mixer with a quasiperiodic solution, where the operating frequency f_0 mixes with an oscillation at about 4-MHz offset, as shown in Fig. 1.49A.[105, 106] Other phenomena can also occur in highly nonlinear circuits, like the one shown in Fig. 1.49B, which is associated with chaotic oscillations. A chaotic solution is a particular type of steady-state solution, which is neither periodic nor quasi-static and thus exhibits a continuous spectrum, at least in some frequency intervals. Chaotic oscillations are usually obtained from instabilities of the quasi-periodic or subharmonic regimes when varying the input power (or other circuit parameter). As the parameter is continuously modified and several qualitatively different solutions are generated, the process ends in a chaotic regime.[107]

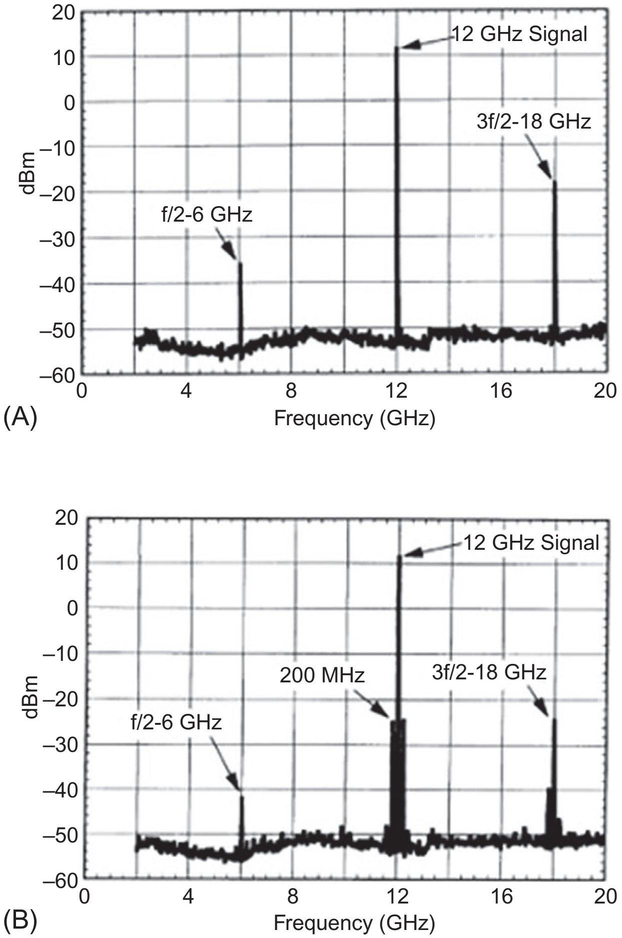


FIG. 1.48

Plots of (A) subharmonic and (B) spurious parasitic oscillations.

Unlike in a single-device power amplifier, several oscillation mechanisms can affect multidevice power amplifiers. In this case, in addition to the parametric frequency divisions, the symmetry in the topology of the multidevice power amplifiers and the presence of power combining blocks in the final stage of the multidevice power amplifier introduce the possibility of odd modes of oscillation.[108, 109] In the odd mode, signals in both branches of the basic cell of the final stage of the multistage power amplifier composed of two devices with a simplified parallel power splitter at the input and at the output are 180 degrees out-of-phase at the oscillation frequency, assuming a virtual ground at the symmetry line of the power splitter and power combiner. In this case, the most suitable approach to eliminate odd-mode oscillations relies on the connection of optimum resistances between the gates (or bases) of the basic cells.[109, 110] In monolithic power amplifiers, to eliminate parametric even- and odd-mode instabilities simultaneously, it is necessary to include both parallel resistances between the gates of each

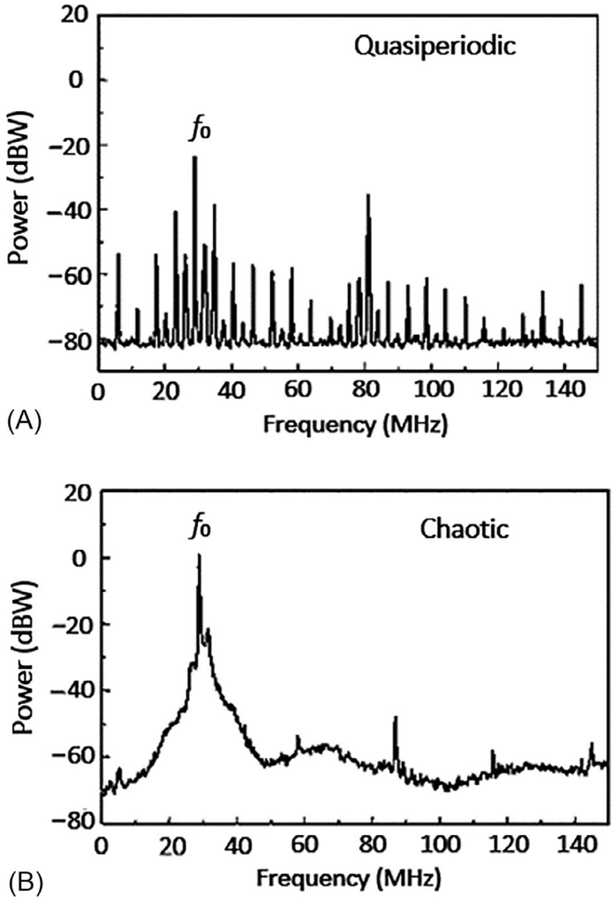


FIG. 1.49

Examples of anomalous behavior in a power amplifier: (A) self-oscillating mixer and (B) chaotic spectrum.

basic cell and a parallel *RC* network in series to each device gate.[111] For a hybrid 1.8-GHz microstrip MESFET power amplifier based on four CLY5 transistors connected in two basic cells, as shown in Fig. 1.50, the two stabilization resistors $R_s = 75\,\Omega$ are connected between two gates of the MESFET devices in each pair to eliminate any instabilities.[112] Here, a 180 degrees shorted stub (at the second harmonic) was introduced in parallel with the final 50-Ω load, which should help to reduce the impact of mismatch instability effects at higher frequencies.

1.13 Bias circuits

The simplest way to provide a Class-AB DC-bias condition for a power MOSFET device is to use the potentiometer-type voltage divider for the gate bias, with a choke inductor in the drain circuit, as shown in Fig. 1.51A. In this case, any variation of the ambient temperature or supply voltage leads

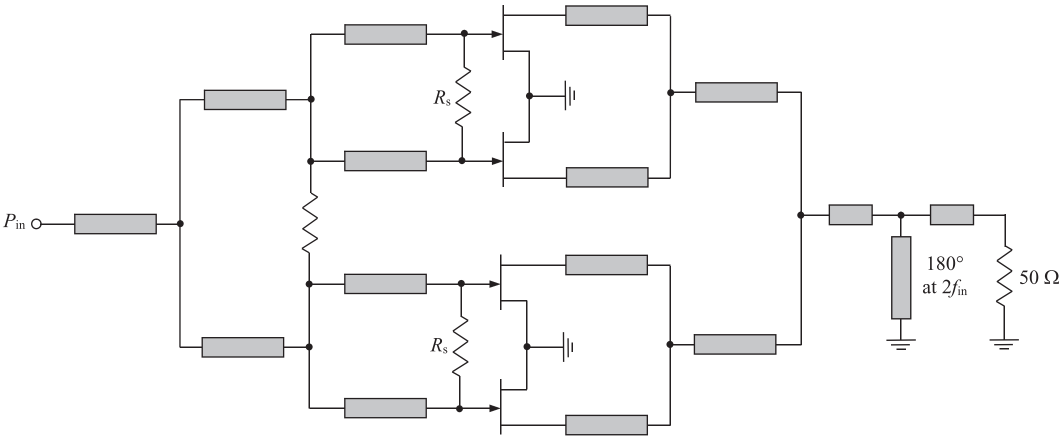


FIG. 1.50

Simplified circuit schematic of a stabilized microstrip power amplifier with four devices.

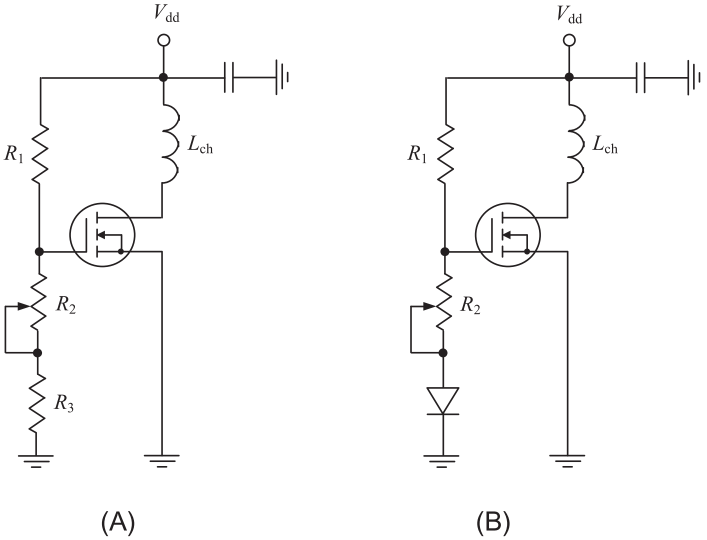


FIG. 1.51

MOSFETs with simple bias circuits.

to the variations of quiescent current and, as a result, to appropriate variations of the output power, linearity, drain efficiency, and power gain of the power amplifier. The threshold voltage of the MOSFET transistor V_{th} varies versus temperature T linearly with approximate velocity of $\Delta V_{th}/\Delta T \cong 2\,\text{mV/°C}$. The simple addition of a diode in series to the variable resistor allows the quiescent current variation to be reduced substantially over temperature. A bias circuit corresponding to this stabilizing condition is shown in Fig. 1.51B. For a high value of V_{th}, several diodes can be connected in series. Such a simple bias circuit configuration for power MOSFET transistors is possible when an extremely small value of the DC gate current, which is restricted to a value of the gate leakage current, is present.

In contrast to the MOSFET devices, where it can be possible to choose the optimum operating point with practically zero temperature coefficient or to be limited to connection of an additional diode only, the bipolar transistors require the more complicated approach of DC biasing depending on the class of operation. In a Class-AB bias mode, the bias circuit has to deliver a constant voltage, slightly adjustable approximately within limits of 0.7–0.8 V, with a wide range of the current values to stabilize the base current of the bipolar transistor. Besides, it is necessary to provide an operation mode of the power amplifier with temperature compensation (collector current stabilization over temperature) and minimum possible reference current (DC current from the reference DC voltage supply). One of the simplest versions of such a bias circuit with diode temperature compensation is shown in Fig. 1.52A. In this bias circuit, each diode can be replaced by the *n-p-n* diode-connected transistor, the collector and the base of which are directly connected between each other. A better temperature-compensating result can be achieved using the same transistors as for the RF power transistor for each bias circuit transistor, but with reduced area size. Such an approach is usually used in monolithic integrated circuit design when transistor cells with different area sizes are used for both an RF power device and bias circuit transistors.

Fig. 1.52B shows the more complicated bias circuit that is commonly used for biasing the high-power bipolar transistors to provide their temperature-stable and reliable operation mode.[113] The temperature stabilization is provided by the parallel connection of the base-emitter diode junction of the

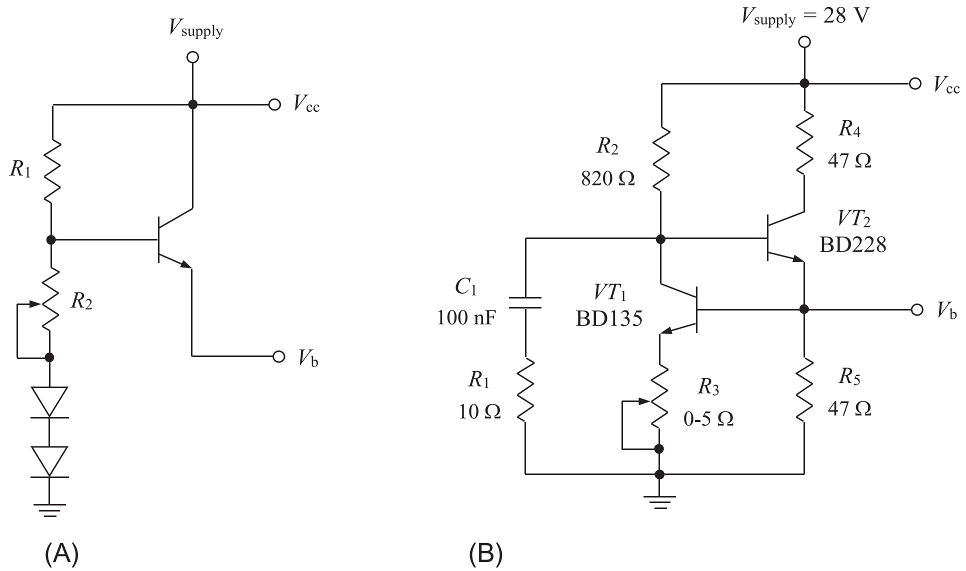


FIG. 1.52

Typical bipolar Class-AB bias circuits.

transistor VT_1, whereas high value of the bias drive current for the RF power transistor is delivered by the transistor VT_2. If the DC collector current of an RF power transistor is 5 A and the value of its forward current gain β_F is approximately equal to 10, then the maximum base current of the RF power transistor can be 0.5 A. In this bias circuit, the resistor R_5 is used to reduce the base current variations. At $V_b = 0.7\,\text{V}$, for a current of 15 mA, the value of R_5 should be equal to $0.7\,\text{V}/15\,\text{mA} = 47\,\Omega$. Suppose that a value of the collector current of VT_1 is 30 mA, then, if the base-emitter junction voltage of VT_2 is equal to 0.8 V with a voltage across the resistor R_2 of $28\,\text{V} - 1.5\,\text{V} = 26.5\,\text{V}$, its value is $26.5\,\text{V}/30\,\text{mA} \cong 820\,\Omega$. The variable resistor R_3 serves to adjust the output voltage in limits of 0.1 V. To limit the maximum collector current of VT_2 by a value of 0.5 A, the resistor R_4 is used. Because VT_2 has a value of the saturation voltage of 0.8 V, it follows that the maximum value of R_4 is $26.5\,\text{V}/0.5\,\text{A} = 53\,\Omega$. It is enough to use its value of $47\,\Omega$ with a power dissipation of $(0.5\,\text{A})^2 \times 47\,\Omega = 11.75\,\text{W}$. Such a bias circuit can develop the parasitic oscillations near 1 MHz with highly capacitive loads. Therefore to prevent these oscillations, it is necessary to connect the RC circuit between the collector of VT_1 and ground.

In most wireless communication systems, it is preferable that the power amplifier operates with high efficiency, maintaining an acceptable linearity over the desired supply voltage and output power ranges. However, there is a tradeoff between efficiency and linearity, with improvement in one coming at the expense of another. This means that it is necessary to provide an optimum fixed or adaptive bias point over a wide temperature range and process variations. As a current-controlled device, the bipolar transistor in RF operation requires a DC base driving current, the value of which depends on the output power and device parameters. Because technologically the bipolar device represents a parallel connection of the basic cells, it is important to use the ballast series resistors to avoid current imbalance and possible device collapse at higher current-density levels. Another important aspect is to keep the DC base-emitter bias point constant (or properly variable) over any RF input power variations to prevent the linearity degradation at the maximum output power for power amplifiers with a variable envelope signal (such as GSM/EDGE, WCDMA/LTE, or CDMA2000).

The typical temperature-compensation current-mirror bias circuit with one reference transistor Q_1 and one driving transistor Q_2 is shown in Fig. 1.53A.[25] This circuit keeps the quiescent current for the RF device Q_0 practically constant over temperature variations, and the current flowing through the resistor R_2 is sufficiently small. It is very important to provide the proper ratio between the ballast resistors R_1 and R_0 equal to the ratio of the device areas Q_0/Q_1. This can minimize the overall performance variation with temperature, as well as stabilize the DC bias point. The latter case is very important for the variable envelope signals because the DC bias voltage V_{be_0} establishes the conduction angle and operation class for the RF device. If the DC base-emitter bias voltage reduces with the increase of RF input power, the Class-AB bias mode required for linear operation changes to a Class-C bias point corresponding to nonlinear operation with zero quiescent current.

Fig. 1.53B shows the dependence of the DC base-emitter bias voltage V_{be0} versus input power P_{in} for the second stage of a WCDMA InGaP/GaAs HBT power amplifier for three cases, including two of them with ballast resistor $R_1 = 0$ (curve 1) and optimum ballast resistor R_1 (curve 2). From Fig. 1.53B, it follows that including the ballast resistor with an optimum value results in a more constant base-emitter DC bias voltage over a wider range of input powers, thus improving the linearity performance of the power amplifier at high power levels. In addition, it is advisable to use a shunt capacitance C_1 connected to the base terminal of the device Q_1 to form a low-pass RC filter, which provides better isolation

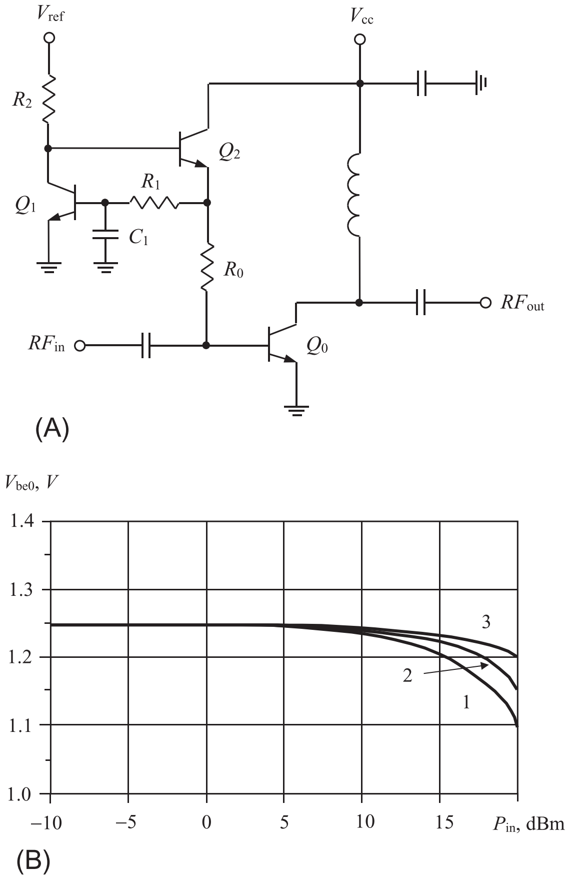


FIG. 1.53

Bipolar power amplifier stage with current-mirror bias circuit and its performance.

of the bias circuit from the RF signal, with a much more constant base-emitter DC bias voltage (curve 3).

Fig. 1.54 shows the emitter-follower bias circuit that provides temperature compensation and minimizes reference current requirements.[114] The emitter-follower bias circuit requires only several tens of microamperes of reference current, whereas the current-mirror bias circuit requires a few milliamperes of reference current. Both the current-mirror and emitter-follower bias circuits have the same current-voltage behavior, but for the same circuit parameters (R_0, R_1, and R_2) and device areas for Q_0, Q_1, and Q_2, the emitter-follower bias circuit is less sensitive to the reference voltage variations. Variations of the collector supply voltage V_{cc} in limits of 3.0–5.0 V have no effect on the quiescent current set by the reference voltage V_{ref}.

GaN HEMTs are depletion mode devices that require a negative voltage to be applied to its gate terminal. Therefore it is very important to keep the bias sequence when the negative gate bias voltage

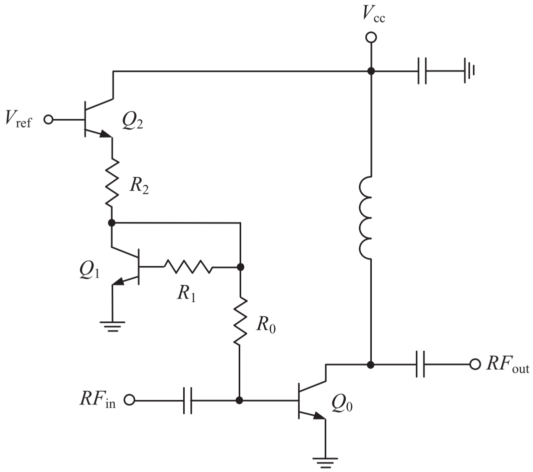


FIG. 1.54

Bipolar power amplifier stage with emitter-follower bias circuit.

corresponding to the required quiescent current is applied earlier than the nominal positive drain supply voltage before turning on the RF power. In addition, attention needs to be paid to how to deal with a positive gate current, which will arise when the device is driven into saturation. Fig. 1.55 shows the gate bias circuit that provides simultaneously the bias sequencing and temperature compensation to maintain a constant quiescent current over temperature, where the gate resistor R_{gate} along the gate bias line is required to suppress parasitic oscillations.[115] The bias sequence and negative gate voltage is generated by the MAX881R bias supply IC that contains an integrated charge pump to supply the necessary negative voltage rail to the operational amplifier MIC7300 and generates a power-OK signal ($\overline{\text{POK}}$) used to turn on the drain switch after the negative supply is stable. The operational amplifier must be capable of supplying the maximum negative and positive gate current for the GaN HEMT being biased, and the charge pump must be capable of supplying the maximum negative current needed for that circuit. The quiescent current that is maintaining constant over temperature is set by the 20-kΩ potentiometer. The operational amplifier is configured as an inverting amplifier with the positive terminal grounded, while the negative terminal is fed from +5 V voltage reference, and a feedback circuit where the 100-kΩ thermistor provides a temperature-dependent resistance and mounted near the active GaN HEMT device.

1.14 Distortion fundamentals

1.14.1 Linearity

The relationship between the output signal $y(t)$ and the input signal $x(t)$ of a system can be written as

$$y(t) = T[x(t)], \tag{1.137}$$

where $T[x(t)]$ is the transfer function that characterizes the system, and t is the time.

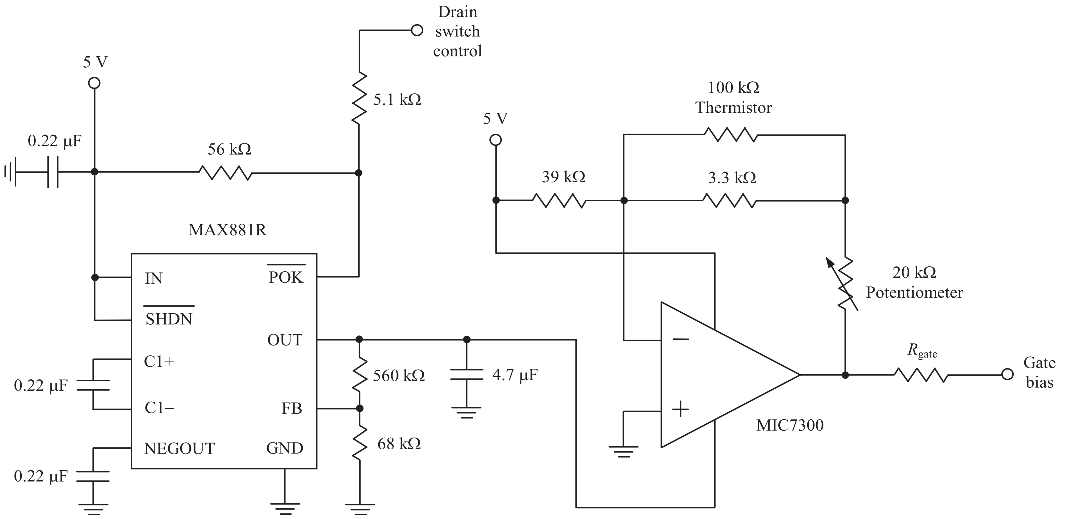

Drain
switch
control
5 V
5.1 kΩ
0.22 µF
56 kΩ
5 V
100 kΩ
Thermistor
39 kΩ
3.3 kΩ
MAX881R
IN
POK
SHDN
OUT
C1+
C1−
FB
NEGOUT
GND
0.22 µF
0.22 µF
560 kΩ
68 kΩ
4.7 µF
20 kΩ
Potentiometer
R_{gate}
Gate
bias
MIC7300

FIG. 1.55

Gate bias circuit for GaN HEMT with temperature compensation.

A system is considered linear if it satisfies the following two conditions:

$$T\left[\sum_i x_i(t)\right] = \sum_i T[x_i(t)], \tag{1.138}$$

$$T[kx(t)] = kT[x(t)]. \tag{1.139}$$

The first condition requires that the response of the system to the sum of many input signals must be the same as the sum of the responses of the system to the individual signals. This concept is also known as superposition. For example, if a multitone signal is applied to a linear amplifier, the effect of the amplifier on each tone must be the same as if each tone was applied individually, that is, there would be no interaction between the tones, which will result in no additional frequencies appearing at the output with respect to the input.

The second condition requires that any scaling of the input signal by a constant factor k must result in the scaling of the output signal by the same scale factor. If the amplitude of a single tone applied to the input of a linear amplifier is doubled, the amplitude of the output tone must also double. If the gain of the system is defined as the ratio between the output and the input signal amplitude, it can be concluded that the gain of a linear system must be independent of the input signal amplitude.

Both Eqs. (1.138) and Eq. (1.139) can be combined into a single expression for n input signals as

$$T[k_1x_1(t) + k_2x_2(t) + \cdots + k_nx_n(t)] = k_1T[x_1(t)] + k_2T[x_2(t)] + \cdots + k_nT[x_n(t)]. \tag{1.140}$$

1.14.2 Time variance

The input/output relationship of the system described by Eq. (1.137) is given by the operator T. If the system is observed at any given time and T remains unchanged, the system is said to be *time invariant*. As a consequence, if the input signal is delayed by a constant time τ, then the only consequence will be that the output will also be delayed by the same amount of time. Analytically,

$$y(t-\tau) = T[x(t-\tau)]. \tag{1.141}$$

1.14.3 Memory

Memory is the dependence of a system transfer function on the input signal past values. The transfer function T of a system can be approximated by a polynomial of degree n and coefficients a_i, which is written as

$$y(t) = \sum_{i=0}^{n} a_i \left[x^i(t)\right]. \tag{1.142}$$

If the system is linear, the polynomial must be of the first degree. This polynomial approximation can only describe the system at an instant, without the possibility of specifying any initial conditions. If the system under consideration contains a capacitor, the system response at a given instant will depend on the charge stored in the capacitor, which will itself depend on the past value of the input signal. For that reason, systems with memory cannot be described with simple algebra but with integro-differential equations of time.

1.14.4 Distortion of electrical signals

Distortion of an electrical signal is any change in its waveform, with the exception of scaling and a constant time delay. Scaling is a fixed amplitude change regardless of time and frequency, and it can be produced by a linear attenuator or amplifier. A constant delay assures a linear change in phase as a function of frequency, like when a signal travels through an ideal transmission line.

A system with a transfer function $T[x(t)]$ is considered to have distortion if, for any given input signal $x(t)$, its output signal $y(t)$ differs from the input by other than a multiplying constant k and a positive finite time delay τ.

The system shown in Fig. 1.56 will be distortionless if, for all time t, the distortion $d(t)$ equals to zero:

$$d(t) = T[x(t)] - kx(t-\tau) = 0. \tag{1.143}$$

1.14.5 Types of distortion

If the distortion signal $d(t)$ from Eq. (1.143) does not equal 0, the system generates distortion, which can be appropriately classified for linear and nonlinear systems.

For linear systems, the transfer function of the system of Fig. 1.45 can be written as a function of the angular frequency ω as

$$T(\omega) = |T(\omega)|e^{j\theta(\omega)}. \tag{1.144}$$

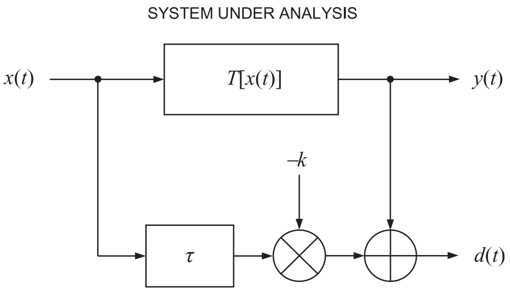


FIG. 1.56

Block diagram used for the definition of distortion in a system.

Amplitude distortion occurs when

$$|T(\omega)| \neq \text{constant} \quad \text{for all}\,\omega. \tag{1.145}$$

Phase or *delay distortion* occurs when

$$\theta(\omega) \neq \omega\tau \quad \text{for all}\,\omega, \tag{1.146}$$

which means that the system does not have a constant delay as a function of frequency. Amplitude and phase distortions are often called *linear distortions* because they are linear processes and can be corrected by using a linear filter.

Nonlinear distortion occurs when the system includes nonlinear elements. If the system of Fig. 1.57 is memoryless, its transfer function $y(t) = T\,[x(t)]$ can be approximated by the power series given by Eq. (1.142). All powers of $x(t)$, which are greater than 1, as in Eq. (1.142), give rise to nonlinear distortion.

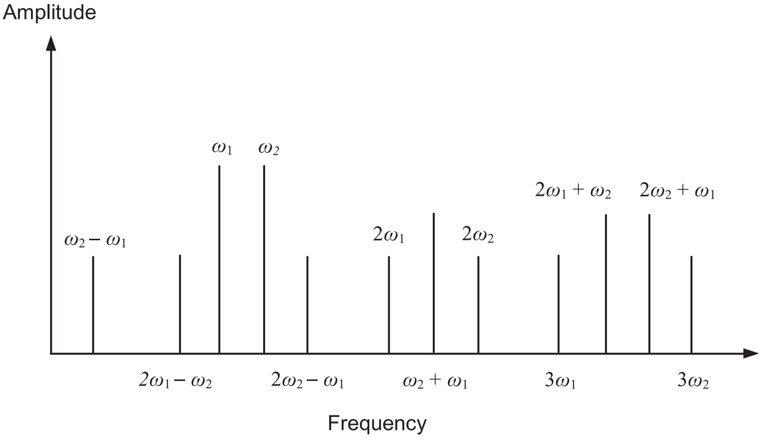


FIG. 1.57

Frequency spectrum of third-order nonlinearity with two-tone sinusoidal excitation.

1.14.6 Nonlinear distortion analysis for sinusoidal signals—Measures of nonlinear distortion

Given a single-tone sinusoidal signal applied to a system, its nonlinear distortion can be measured as the *total harmonic distortion* (THD) defined as the ratio of (1) the sum of the powers of all harmonic frequencies above the fundamental frequency of the input signal to (2) the power of the fundamental frequency, all measured at the output of the system. If P_1 is the fundamental signal power and P_2-P_n are the powers of the n harmonics of the input signal, the THD can be written as

$$\mathrm{THD} = \frac{\sum_{i=2}^{n} P_i}{P_1}. \tag{1.147}$$

Another type of nonlinear distortion occurs when two or more sinusoidal signals of different frequencies are applied to the input of a nonlinear system. In this case, the output will contain additional signals not existent at the input, whose frequencies are not only harmonically related to the fundamental tones. If a power series such as Eq. (1.142) is used to approximate the transfer function of a memoryless system, the output of the system $y(t)$ can be found by replacing $x(t)$ with a two-tone test signal of amplitude $A = 1$,

$$x(t) = A[\cos\alpha + \cos\beta], \tag{1.148}$$

where $\alpha = \omega_1 t$, $\beta = \omega_2 t$, ω_1 and ω_2 are the frequencies of each tone, and t is the time. The output $y(t)$ will contain the two tones plus additional signals of different frequencies (some very close to the input tones). Those frequencies are given by $2\omega_2 - \omega_1$, $2\omega_1 - \omega_2$, $3\omega_2 - 2\omega_1$, $3\omega_1 - 2\omega_2$, etc., and they are called IMD products. Based on the sum of the coefficients of each term, the coefficient $2\omega_2 - \omega_1$ is defined as a third-order intermodulation coefficient IM_3, the coefficient $3\omega_2 - 2\omega_1$ is defined as a fifth-order intermodulation coefficient IM_5, etc.

IMD products are a major problem in communication systems because their frequencies fall very close to the fundamental signal, and it is not feasible to implement linear filters that are capable to suppress them. It is customary to measure IMD as a dB ratio between the power of one of the IMD products and the power of the fundamental tones.

As an example, the distortion $d(t)$ in Eq. (1.143) of the system shown in Fig. 1.56 with $\tau = 0$, for a third-degree nonlinearity represented by the power series of Eq. (1.142) and the two-tone input signal of Eq. (1.148), will be written as.

$$d(t) = \left[a_1(\cos\alpha + \cos\beta) + a_2(\cos\alpha + \cos\beta)^2 + a_3(\cos\alpha + \cos\beta)^3\right] - k\cos\alpha - k\cos\beta, \tag{1.149}$$

$$\begin{aligned} d(t) = \{&a_1\cos\alpha + a_1\cos\beta + a_2\left[\cos^2\alpha + 2\cos\alpha\cos\beta + \cos^2\beta\right] + a_3\left[\cos^3\alpha + 3\cos^2\alpha\cos\beta + 3\cos\alpha\cos^2\beta + \cos^3\beta\right]\} \\ &- k\cos\alpha - k\cos\beta, \end{aligned} \tag{1.150}$$

$$\begin{aligned} d(t) = \{&a_1\cos\alpha + a_1\cos\beta \\ &+a_2\left[\left(\frac{1}{2} + \frac{1}{2}\cos 2\alpha\right) + \cos(\beta - \alpha) + \cos(\beta + \alpha) + \left(\frac{1}{2} + \frac{1}{2}\cos 2\beta\right)\right] \\ &+a_3\left[\frac{3}{4}\cos\alpha + \frac{1}{4}\cos 3\alpha + 3\left(\frac{1}{2} + \frac{1}{2}\cos 2\alpha\right)\cos\beta + 3\cos\alpha\left(\frac{1}{2} + \frac{1}{2}\cos 2\beta\right)\right. \\ &\left.+\frac{3}{4}\cos\beta + \frac{1}{4}\cos 3\beta\right]\Bigg\} - k\cos\alpha - k\cos\beta, \end{aligned} \tag{1.151}$$

$$\begin{aligned} d(t) = \Bigg\{ & a_1 \cos\alpha + a_1 \cos\beta + a_2 \left[1 + \frac{1}{2}\cos 2\alpha + \frac{1}{2}\cos 2\beta + \cos(\beta-\alpha) + \cos(\beta+\alpha)\right] \\ & + a_3 \left[\frac{3}{4}\cos\alpha + \frac{1}{4}\cos 3\alpha + \frac{3}{2}\cos\beta + \frac{3}{4}\cos(2\alpha-\beta) + \frac{3}{4}\cos(2\alpha+\beta) \right. \\ & \left. + \frac{3}{2}\cos\alpha + \frac{3}{4}\cos(2\beta-\alpha) + \frac{3}{4}\cos(2\beta+\alpha) + \frac{3}{4}\cos\beta + \frac{1}{4}\cos 3\beta\right]\Bigg\} \\ & - k\cos\alpha - k\cos\beta, \end{aligned} \tag{1.152}$$

$$\begin{aligned} d(t) = & \left(a_1 + \frac{9a_3}{4} - k\right)\cos\alpha + \left(a_1 + \frac{9a_3}{4} - k\right)\cos\beta + a_2 + \frac{a_2}{2}\cos 2\alpha + \frac{a_2}{2}\cos 2\beta \\ & + a_2\cos(\beta-\alpha) + a_2\cos(\beta+\alpha) + \frac{a_3}{4}\cos 3\alpha + \frac{3a_3}{4}\cos(2\alpha-\beta) \\ & + \frac{3a_3}{4}\cos(2\alpha+\beta) + \frac{3a_3}{4}\cos(2\beta-\alpha) + \frac{3a_3}{4}\cos(2\beta+\alpha) + \frac{a_3}{4}\cos 3\beta. \end{aligned} \tag{1.153}$$

If the input tones are removed by making k equal $a_1 + 9a_3/4$, the resultant distortion $d(t)$ is written as.

$$\begin{aligned} d(t) = & a_2 + \frac{a_2}{2}\cos 2\alpha + \frac{a_2}{2}\cos 2\beta + a_2\cos(\alpha-\beta) + a_2\cos(\alpha+\beta) + \frac{a_3}{4}\cos 3\alpha \\ & + \frac{3a_3}{4}\cos(2\alpha-\beta) + \frac{3a_3}{4}\cos(2\alpha+\beta) + \frac{3a_3}{4}\cos(2\beta-\alpha) \\ & + \frac{3a_3}{4}\cos(2\beta+\alpha) + \frac{a_3}{4}\cos 3\beta. \end{aligned} \tag{1.154}$$

Replacing α by $\omega_1 t$ and β by $\omega_2 t$ in Eq. (1.148), the IMD products are written as

the second-order components:

$$a_2\cos(\omega_2-\omega_1)t \quad \text{(envelope)}, \tag{1.155}$$

$$a_2\cos(\omega_2+\omega_1)t \quad \text{(sum)}, \tag{1.156}$$

the third-order components:

$$\frac{3a_3}{4}\cos(2\omega_2-\omega_1)t, \tag{1.157}$$

$$\frac{3a_3}{4}\cos(2\omega_1-\omega_2)t, \tag{1.158}$$

$$\frac{3a_3}{4}\cos(2\omega_1+\omega_2)t, \tag{1.159}$$

$$\frac{3a_3}{4}\cos(2\omega_2+\omega_1)t. \tag{1.160}$$

Fig. 1.57 represents the frequency spectrum of the third-order nonlinearity with the two-tone excitation generated by Eq. (1.154).

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CHAPTER

Class-D power amplifiers

2

In this chapter, different configurations of Class-D power amplifiers are presented, the increased efficiency of which is a result of employing the active device as switches. First, the switchmode power amplifiers with resistive load of different configurations, which can be considered driver power amplifiers, are discussed. Then, the current-switching and voltage-switching configurations based on complementary and transformer-coupled topologies are analyzed. The effects of the saturation resistance, rectangular and sinusoidal driving signals, finite transition time, and parasitic shunt capacitance and series inductance are studied and discussed in detail in this chapter. The practical design examples of the voltage-switching and current-switching Class-D power amplifiers intended to operate at high frequencies and microwaves are described. Finally, a high-frequency Class-S amplification architecture employing a switching mode Class-D power amplifier to efficiently amplify digitally modulated transmitting signal is shown and discussed.

2.1 Switchmode power amplifiers with resistive load

The efficiency of a power amplifier can be maximized if the active device is operated as a switch. When the transistor is turned on, the voltage is nearly zero and a high current flows through the device, and the transistor acts as a low resistance (closed switch) during this part of the period, whereas when the transistor is turned off, the current is zero and there is a high voltage across the device, and the transistor acts as an open switch during the other part of the period.

Let us consider the three types of a switchmode power amplifier with resistive load: a single-ended amplifier, a complementary voltage-switching push-pull amplifier, and a transformer-coupled current-switching push-pull amplifier.[1] Fig. 2.1A shows the simplified circuit schematic of a switchmode single-ended bipolar power amplifier, where L_{ch} is the RF choke required to isolate a DC power supply from RF circuit, C_b is the bypass capacitor, and C_0 is the blocking capacitor with the supply voltage V_{cc} applied to its plates.

The theoretical analysis of the operation conditions of a single-ended switchmode power amplifier can be carried out based on an equivalent circuit shown in Fig. 2.1B, where the active device is considered a switch with a saturation resistance r_{sat} driven in such a way as to provide the device an instantaneous switching between its on-state and off-state operation conditions under an assumption of a 50% duty ratio.

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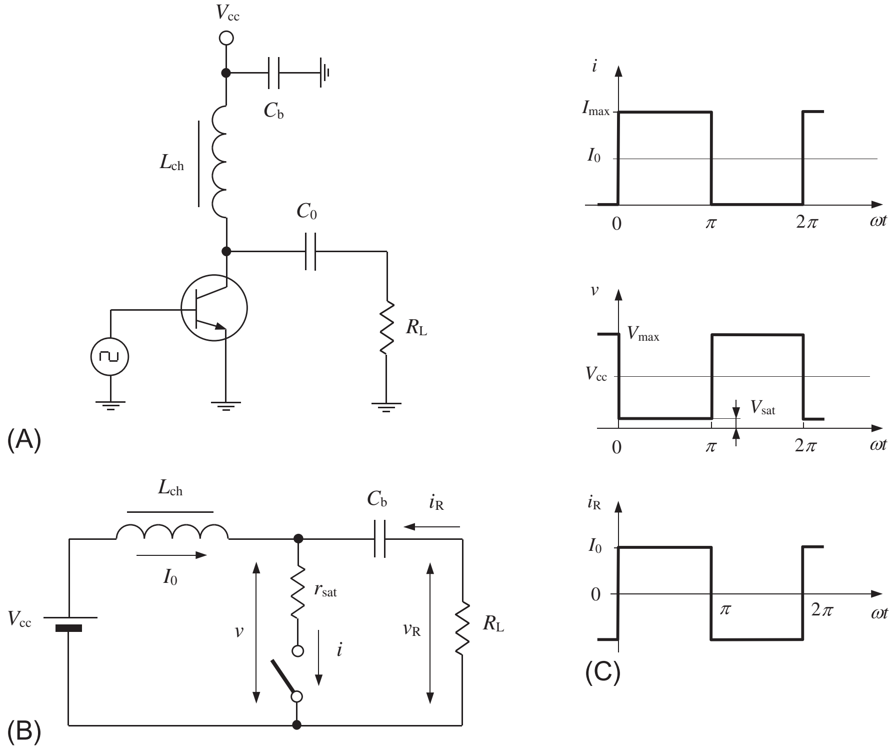
V_{cc}
C_b
L_{ch}
C_0
R_L
(A)
L_{ch}
C_b
i_R
I_0
r_{sat}
V_{cc}
v
v_R
R_L
i
(B)
i
I_{max}
I_0
0
π
2π
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v
V_{max}
V_{cc}
V_{sat}
0
π
2π
ωt
i_R
I_0
0
π
2π
ωt
(C)

FIG. 2.1

Switchmode single-ended pulsed power amplifier.

When the switch is turned on for $0 \le \omega t \le \pi$,

$$i(\omega t) = I_{max} = \frac{V_{cc} + R_L I_0}{R_L + r_{sat}}, \tag{2.1}$$

$$v(\omega t) = V_{sat} = r_{sat} I_{max}, \tag{2.2}$$

$$i_R(\omega t) = I_0, \tag{2.3}$$

$$v_R(\omega t) = R_L I_0, \tag{2.4}$$

where I_0 is the DC current, I_{max} is the peak collector current, V_{sat} is the saturation voltage, and R_L is the load resistance.

When the switch is turned off for $\pi \le \omega t \le 2\pi$,

$$i(\omega t) = 0, \tag{2.5}$$

$$v(\omega t) = V_{max} = V_{cc} + R_L I_0, \tag{2.6}$$

$$i_R(\omega t) = -I_0, \tag{2.7}$$

$$v_R(\omega t) = -R_L I_0, \tag{2.8}$$

where $V_{\max}$ is the peak collector voltage.

The rectangular collector voltage, collector current, and load current waveforms are shown in Fig. 2.1C, demonstrating that zero collector current corresponds to maximum collector voltage and minimum collector voltage corresponds to maximum collector current. However, because the current flowing to the load is not sinusoidal, its harmonic components are also present in the output spectrum.

The DC current I_0 can be calculated by applying a Fourier transform to Eq. (2.1) as

$$I_0 = \frac{1}{2\pi}\int_0^{\pi} i(\omega t)d\omega t = \frac{V_{\mathrm{cc}}}{R_{\mathrm{L}} + r_{\mathrm{sat}}}\left(1 + \frac{r_{\mathrm{sat}}}{R_{\mathrm{L}} + r_{\mathrm{sat}}}\right)^{-1}. \tag{2.9}$$

Similarly, the fundamental frequency current amplitude I can be calculated as

$$I = \frac{1}{\pi}\int_0^{\pi} i(\omega t)\sin\omega t\; d\omega t = \frac{4}{\pi}I_0. \tag{2.10}$$

Considering that $I_{\max} = 2I_0$ for a duty ratio of 50% or a conduction angle of 180 degrees, the fundamental frequency output power P can be obtained by

$$P = \frac{1}{2}I^2 R_{\mathrm{L}} = \frac{8}{\pi^2}\frac{R_{\mathrm{L}}}{(R_{\mathrm{L}} + r_{\mathrm{sat}})^2}\frac{V_{\mathrm{cc}}^2}{\left(1 + \frac{r_{\mathrm{sat}}}{R_{\mathrm{L}} + r_{\mathrm{sat}}}\right)^2}. \tag{2.11}$$

Fig. 2.2A shows the simplified circuit schematic of a quasi-complementary voltage-switching push-pull bipolar power amplifier, where C_{b} is the bypass capacitor, C_0 is the blocking capacitor, and R_{L} is the load resistance. The input transformer causes both active devices to be driven with currents that are 180 degrees out of phase by reversing one secondary winding on the transformer. However, there is no need of phase reversing if the transistors are true complementary with different base or channel majority carrier type that simplifies the circuit schematic. Note that any type of the vacuum tubes, bipolar, or MOSFET transistors can be used in this circuit if a suitable drive is applied. Because of the grounding effect of a bypass capacitor C_{b}, the RF connection of the transistor outputs is parallel, thus resulting in an equivalent load resistance equal to $2R_{\mathrm{L}}$ for each device.

The theoretical analysis of the operation conditions of a quasi-complementary voltage-switching push-pull power amplifier is based on its equivalent circuit shown in Fig. 2.2B, where each active device is considered a switch with a saturation resistance r_{sat} driven in such a way as to provide an alternating switching between the on-state and off-state operation conditions of the transistor under an assumption of a 50% duty ratio. It should be noted that, for a voltage-switching push-pull power amplifier, the operation conditions only with duty ratios equal or less than 50% are acceptable, because when both devices are turned on for duty ratios greater than 50%, both DC power supplies are connected to each other through small saturation resistances of identical transistors equal to $2r_{\mathrm{sat}}$, thus resulting in significant efficiency reduction due to an increased total current flowing through both the transistors.

When the left-hand switch is turned on for $0 \le \omega t \le \pi$,

$$i(\omega t) = I_{\max} = \frac{V_{\mathrm{cc}}}{R_{\mathrm{L}} + r_{\mathrm{sat}}}, \tag{2.12}$$

$$v(\omega t) = V_{\mathrm{sat}} = r_{\mathrm{sat}} I_{\max}, \tag{2.13}$$

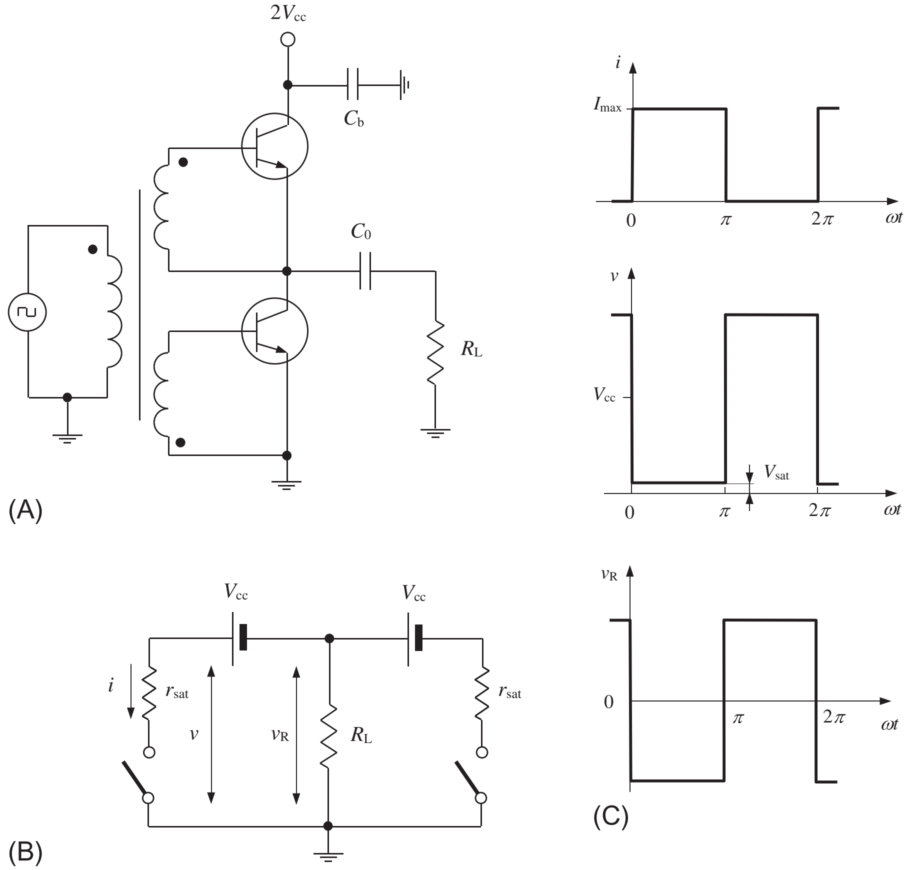
2Vcc
Cb
C0
RL
(A)
i
Imax
0
π
2π
ωt
v
Vcc
Vsat
0
π
2π
ωt
vR
0
π
2π
ωt
(C)
Vcc
Vcc
i
rsat
v
vR
RL
rsat
(B)

FIG. 2.2

Voltage-switching push-pull power amplifier.

$$v_{\mathrm{R}}(\omega t) = -R_{\mathrm{L}} I_{\max}. \tag{2.14}$$

When the left-hand switch is turned off for $\pi \leq \omega t \leq 2\pi$,

$$i(\omega t) = 0, \tag{2.15}$$

$$v(\omega t) = V_{\max} = V_{\mathrm{cc}}\left(2 - \frac{r_{\mathrm{sat}}}{R_{\mathrm{L}} + r_{\mathrm{sat}}}\right), \tag{2.16}$$

$$v_{\mathrm{R}}(\omega t) = V_{\mathrm{R}} = R_{\mathrm{L}} I_{\max}. \tag{2.17}$$

The DC current I_0 can be calculated by applying a Fourier transform to Eq. (2.12) as

$$I_0 = \frac{1}{2}\frac{V_{\mathrm{cc}}}{R_{\mathrm{L}} + r_{\mathrm{sat}}}. \tag{2.18}$$

The fundamental frequency output power P can be obtained using Eqs. (2.12) and (2.17) by

$$P = \frac{8}{\pi^2}\frac{V_R^2}{R_L} = \frac{8}{\pi^2}\frac{R_L}{(R_L + r_{sat})^2}V_{cc}^2. \tag{2.19}$$

The rectangular collector current, collector voltage, and load voltage waveforms are shown in Fig. 2.2C, demonstrating that zero collector current corresponds to maximum collector voltage and minimum collector voltage corresponds to maximum collector current. However, because the voltage on the load is not sinusoidal, its harmonic components are also presented in the output spectrum. The maximum collector voltage peak factor for an idealized case of zero saturation resistance is equal to $v/V_{cc} = 2$.

Fig. 2.3A shows the simplified circuit schematic of a transformer-coupled current-switching push-pull bipolar power amplifier, where C_b is the bypass capacitor, C_0 is the blocking capacitor, L_{ch} is the RF choke, and R_L is the load resistance. As before, the input transformer causes both active devices to be driven with currents that are 180 degrees out of phase. However, the transistors of the same type have the series output RF connection with an equivalent load resistance equal to $R_L/2$ for each device. The RF chokes provide bipolar $\pm I_0$ pulses of the current flowing to the load through the output balanced-to-unbalanced (balun) transformer.

The theoretical analysis of the operation conditions of a transformer-coupled current-switching push-pull power amplifier is based on its equivalent circuit shown in Fig. 2.3B, where each active device is considered a switch with a saturation resistance r_{sat} driven in such a way to provide an alternating switching between the on-state and off-state operation conditions of the transistor under an assumption of a 50% duty ratio. It should be noted that, for a current-switching push-pull power amplifier, the operation conditions only with duty ratios equal or greater than 50% are acceptable, because when both devices are turned off for duty ratios less than 50%, the choke currents will result in a significant voltage increase at the device collectors, which may cause their breakdown.

When the left-hand switch is turned on for $0 \le \omega t \le \pi$,

$$i(\omega t) = I_{max} = 2I_0, \tag{2.20}$$

$$v(\omega t) = V_{sat} = r_{sat}I_{max}, \tag{2.21}$$

$$i_R(\omega t) = I_R = I_0. \tag{2.22}$$

When the left-hand switch is turned off for $\pi \le \omega t \le 2\pi$,

$$i(\omega t) = 0, \tag{2.23}$$

$$v(\omega t) = V_{max} = (R_L + 2r_{sat})I_0, \tag{2.24}$$

$$i_R(\omega t) = -I_0. \tag{2.25}$$

The DC supply voltage V_{cc} can be calculated by applying a Fourier transform to Eqs. (2.21) and (2.24) as

$$V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)d\omega t = \frac{V_{max} + V_{sat}}{2}. \tag{2.26}$$

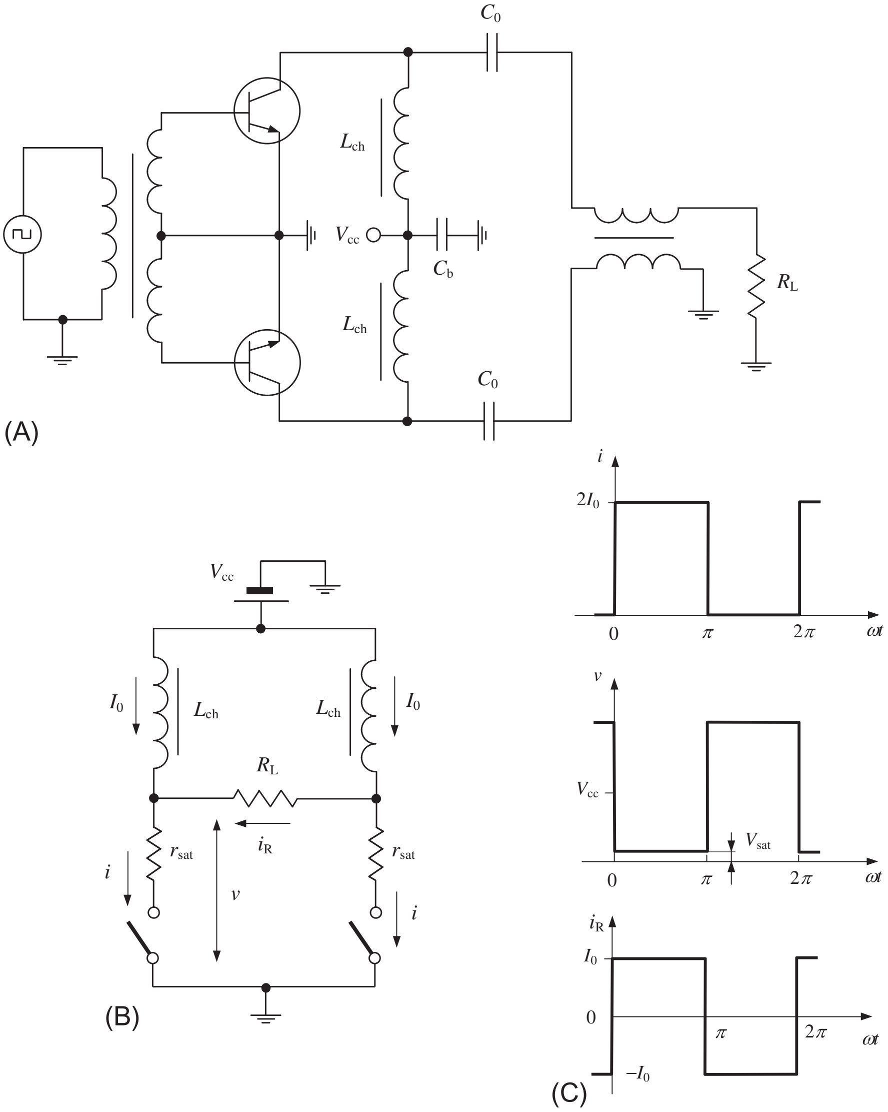
C_0
L_{ch}
V_{cc}
C_b
L_{ch}
C_0
R_L
(A)
V_{cc}
I_0
L_{ch}
L_{ch}
I_0
R_L
i_R
r_{sat}
r_{sat}
i
v
i
(B)
i
$2I_0$
0
π
2π
ωt
v
V_{cc}
V_{sat}
0
π
2π
ωt
i_R
I_0
0
π
2π
ωt
$-I_0$
(C)

FIG. 2.3

Current-switching push-pull power amplifier.

The DC current I_0 can then be obtained by

$$I_0 = \left(\frac{1}{2} + 2\frac{r_{\text{sat}}}{R_{\text{L}}}\right)^{-1} \frac{V_{\text{cc}}}{R_{\text{L}}}. \tag{2.27}$$

Finally, the fundamental frequency output power P can be written using Eqs. (2.22) and (2.27) as

$$P = \frac{8}{\pi^2} I_{\text{R}}^2 R_{\text{L}} = \frac{8}{\pi^2}\left(\frac{1}{2} + 2\frac{r_{\text{sat}}}{R_{\text{L}}}\right)^{-2} \frac{V_{\text{cc}}^2}{R_{\text{L}}}. \tag{2.28}$$

To provide sufficient isolation between the transistors, it is preferable to use the balanced circuit schematic of a switchmode push-pull power amplifier with an additional broadband transformer T_1 and a ballast resistor R_{bal} connected to its midpoint through the blocking capacitor C_0, as shown in Fig. 2.4. In this case, when $R_{\text{bal}} \to 0$, the balanced push-pull schematic transforms to a transformer-coupled voltage-switching push-pull circuit, while when $R_{\text{bal}} \to \infty$, this schematic represents a transformer-coupled current-switching push-pull power amplifier. If both transistors are identical, they operate independently from each other being fully isolated, and such a switchmode balanced power amplifier can be considered as two switchmode single-ended power amplifiers operating independently, with opposite phases on the same load through the balanced power combiner, including a balanced to unbalanced transformer T_2. Because the output currents from both transistors are combined at the load resistor R_{L} and subtracted at the ballast resistor R_{bal}, the load output power spectrum contains the power corresponding to the fundamental frequency and odd harmonic components, while the even harmonic components are combined at the ballast resistor.

Generally, the choice of a conduction angle of 180 degrees is optimal because, in this case, it provides the collector efficiency close to maximum, the maximum voltage peak factor of <2, the maximum fundamental frequency power delivered to the load, and zero power at even harmonics for all types of the switchmode power amplifiers with resistive load. The maximum collector efficiency when the saturation r_{sat} is equal to zero can be obtained using Eqs. (2.9), (2.11), (2.18), (2.19), (2.27), and (2.28) by

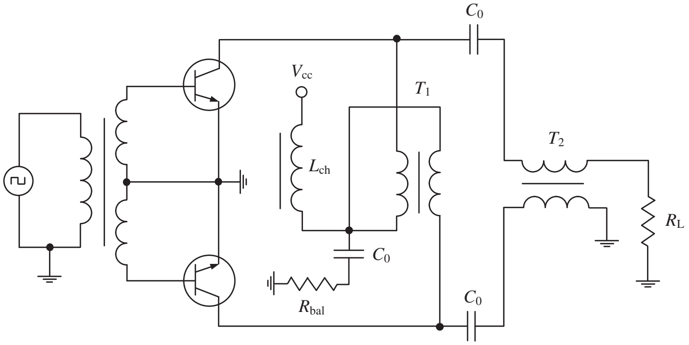

FIG. 2.4

Transformer-coupled current-switching push-pull power amplifier.

$$\eta = \frac{P}{P_0} = \frac{8}{\pi^2} \cong 81\%. \tag{2.29}$$

Consequently, with a rectangular voltage waveform on the load, the relative harmonic power is about 19% of the total output power. As a result, these switchmode single-ended and push-pull power amplifiers can be directly used as the driver power amplifiers when the harmonic level and power loss at the harmonics are not so significant. To compensate for the transformer magnetizing (leakage) and device stray input inductances, the external shunt capacitors can be used in addition to the device input capacitances, thus extending an operating high-bandwidth frequency.[2] If it is intended to be used as a final power amplifier stage, the special filter sections must be included between the device output and the load to suppress the harmonic components down to the required level.

For example, a filter-diplexer can be used to separate the signals with fundamental frequency and other harmonic components, as shown in Fig. 2.5A. Fig. 2.5B shows the simplest representation of a filter-diplexer is a parallel connection of a single low-pass filter section and a single high-pass filter section. To further improve the isolation between these two branches, the number of low-pass and high-pass filter sections can be increased. A better passband and stopband performance with higher cutoff rate can be obtained by using the elliptic function or Chebyshev polynomial filters. Fig. 2.5C shows an example of a filter-diplexer using a single passband filter section for a fundamental frequency signal having very high impedance at the second- and higher-order harmonic components and a single stop-band filter section for a fundamental frequency signal with minimum attenuation at the second- and higher-order harmonic components. In addition, it is possible to improve the efficiency of the power amplifier by using a power recycling technique when the harmonic power can be transformed to the DC power by means of the RF-to-DC diode converter and returned back to the DC power supply.

2.2 Complementary voltage-switching configuration

The switchmode RF power amplifiers with output filter tuned to the fundamental frequency, which were called Class-D power amplifiers, transform ideally the total DC power into a fundamental frequency power delivered to the load without power losses at the harmonics, unlike the switchmode power amplifiers with resistive load.[3, 4] Conceptually, a Class-D power amplifier employs a pair of active devices operating in a push-pull mode and a tuned output circuit. The transistors are driven to act as a two-pole switch that defines either a rectangular voltage or rectangular current collector (or drain) waveforms. The output circuit is tuned to the switching frequency and removes ideally its higher-order harmonic components, resulting in a purely sinusoidal signal delivered to the load. Consequently, the theoretical efficiency of an idealized Class-D power amplifier achieves 100%. Let us consider the basic principles, circuit schematics, and voltage/current waveforms corresponding to the different types of a Class-D power amplifier with output filter.[1, 5–7]

Fig. 2.6A shows the simplified circuit schematic of a quasi-complementary voltage-switching Class-D bipolar power amplifier consisting of the same type of the active devices, fundamentally tuned series L_0C_0 filter, and load resistance R_L. The large-value bypass capacitor C_b is necessary to isolate the DC power supply by bypassing the RF current to ground. The input transformer causes both the active devices to be driven with currents that are 180 degrees out of phase by reversing one secondary winding on the transformer. However, there is no need of phase reversing if the transistors are true

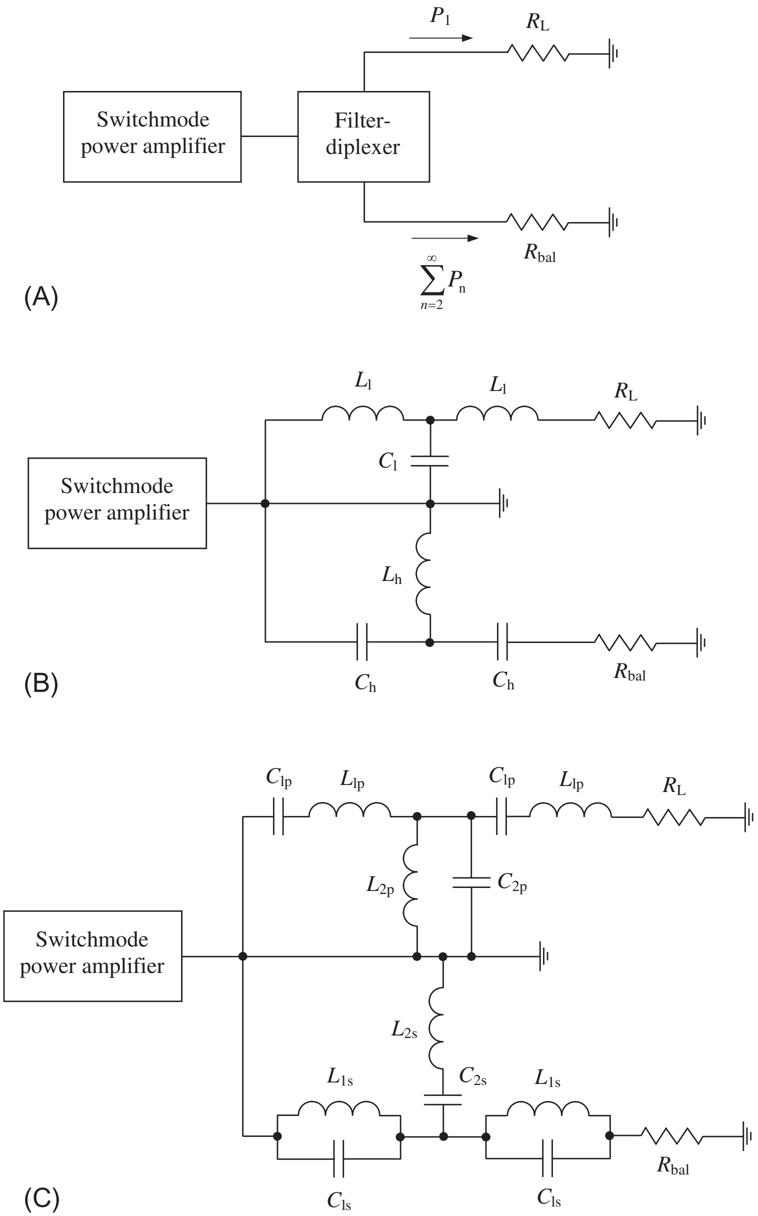
P_1
R_L
Switchmode power amplifier
Filter-diplexer
R_{bal}
$\sum_{n=2}^{\infty} P_n$
(A)
L_l
L_l
R_L
C_l
Switchmode power amplifier
L_h
C_h
C_h
R_{bal}
(B)
C_{lp}
L_{lp}
C_{lp}
L_{lp}
R_L
L_{2p}
C_{2p}
Switchmode power amplifier
L_{2s}
L_{1s}
C_{2s}
L_{1s}
C_{ls}
C_{ls}
R_{bal}
(C)

FIG. 2.5

Switchmode power amplifiers with filter-diplexer.

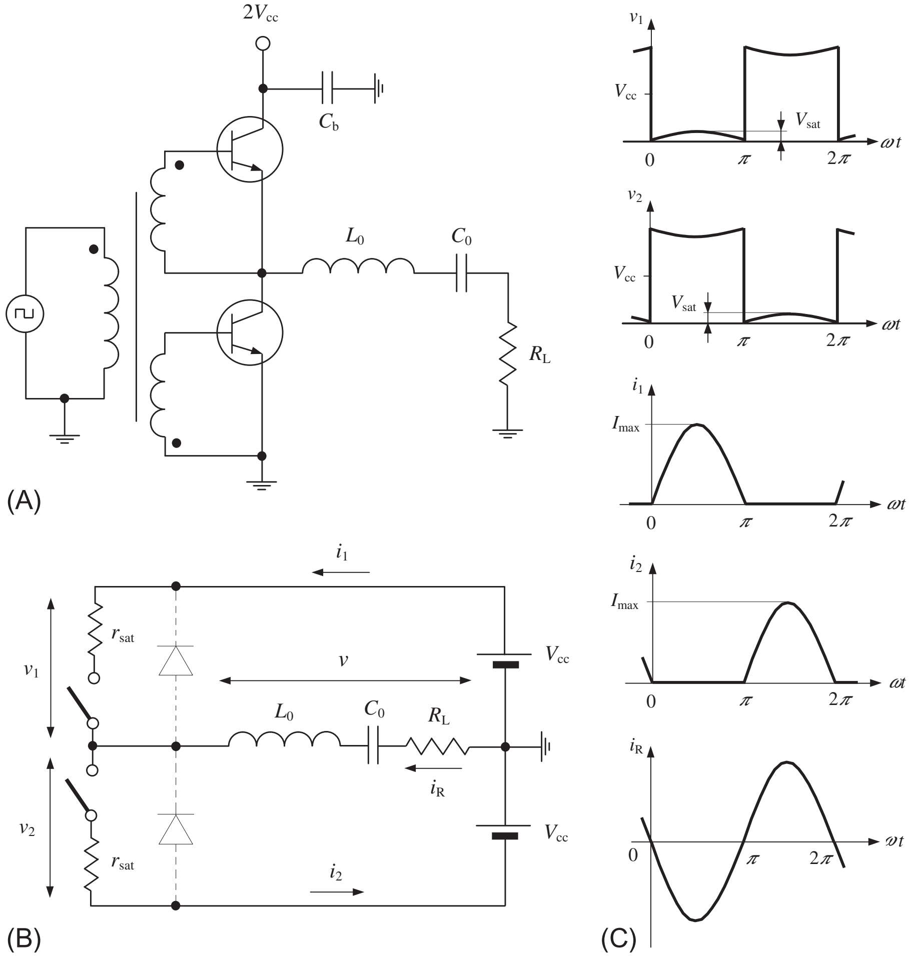
2V_cc
C_b
L_0
C_0
R_L
(A)
i_1
r_sat
v_1
v
V_cc
L_0
C_0
R_L
i_R
v_2
r_sat
V_cc
i_2
(B)
v_1
V_cc
V_sat
0
π
2π
ωt
v_2
V_cc
V_sat
0
π
2π
ωt
i_1
I_max
0
π
2π
ωt
i_2
I_max
0
π
2π
ωt
i_R
0
π
2π
ωt
(C)

FIG. 2.6

Quasi-complementary voltage-switching configuration with series filter.

complementary with different base or channel majority carrier type that simplifies the circuit schematic. Note that any type of the vacuum tubes, bipolar, or MOSFET transistors can be used in this circuit if a suitable drive is applied. Owing to the grounding effect of a bypass capacitor C_b, the RF connection of the transistor outputs is parallel, thus resulting in an equivalent load resistance equal to $2R_L$ for each device.

To determine the collector voltage and current waveforms and to calculate the output power and collector efficiency, the following assumptions should be taken into account:

- Power loss due to flow of leakage current during transistor pinch-off is negligible.
- Power loss due to nonideal tuning is negligible.
- Power loss during switching transitions is negligible.

In this case, each active device is considered a switch with a saturation resistance r_{sat} shown in Fig. 2.6B that is driven in such a way as to provide an alternating switching between the on-state and off-state operation conditions of the transistor under an assumption of a 50% duty ratio. The alternating half-period switching of the two transistors between their pinch-off mode and voltage saturation mode results in rectangular collector voltage pulses with a maximum amplitude of $2V_{\text{cc}}$, as shown in Fig. 2.6C. The collector voltage pulses, which contain the odd harmonic components only, are applied to the series L_0C_0 filter with a high loaded quality factor $Q_{\text{L}} = \omega L_0/R_{\text{L}} \gg 1$ tuned to the fundamental frequency $f_0 = \omega_0/2\pi = 1/2\pi\sqrt{L_0C_0}$, resulting in the fundamental frequency sinusoidal current $i_{\text{R}} = -I_{\text{R}} \sin\omega t$, which flows to the load R_{L}. The half-waves of this current flow through the transistors representing the half-sinusoidal collector current pulses that contain the fundamental frequency and second-, and higher-order even harmonic components only. The shape of the saturation voltage with a maximum amplitude V_{sat} is fully determined by the collector current waveform when $i(\omega t) > 0$ according to $v_{\text{sat}}(\omega t) = r_{\text{sat}}\, i(\omega t)$, where $i(\omega t) = i_1(\omega t) = i_2(\omega t)$ for a symmetrical circuit with identical transistors. The collector voltage peak factor is equal to $v/V_{\text{cc}} = 2$.

It should be noted that, for an operation with conduction angles less than 180 degrees, when both the transistors are turned on for duty ratios less than 50%, there is a time period when both the transistors are turned off simultaneously. Therefore in order that the load current $i_{\text{R}}(\omega t)$ could flow continuously, it is necessary to include a diode in parallel to each device, as shown in Fig. 2.6B. The operation conditions with conduction angles greater than 180 degrees are unacceptable because both DC power supplies are connected to each other through the small saturation resistances of the identical transistors equal to $2r_{\text{sat}}$, thus resulting in the significant efficiency reduction owing to an increased total current flowing through both transistors when they are turned on simultaneously.

Now let us determine the voltage $v(\omega t) = v_1(\omega t) - V_{\text{cc}}$ at the input of a series L_0C_0 circuit and collector current $i_1(\omega t)$ for the first transistor operating as a switch with a saturation resistance r_{sat}. When the switch is turned on for $0 \le \omega t \le \pi$,

$$v(\omega t) = -V_{\text{cc}} + r_{\text{sat}} I_{\text{R}} \sin\omega t, \tag{2.30}$$

$$i_1(\omega t) = I_{\text{R}} \sin\omega t, \tag{2.31}$$

where I_{R} is the load current amplitude.

When the switch is turned off for $\pi \le \omega t \le 2\pi$,

$$v(\omega t) = V_{\text{cc}} + r_{\text{sat}} I_{\text{R}} \sin\omega t, \tag{2.32}$$

$$i_1(\omega t) = 0. \tag{2.33}$$

The fundamental frequency voltage amplitude V of the voltage $v(\omega t)$ can be calculated by applying a Fourier transform to Eqs. (2.30) and (2.32) as

$$V = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin\omega t\, d\omega t = \frac{4}{\pi}V_{\text{cc}} - r_{\text{sat}} I_{\text{R}}. \tag{2.34}$$

Similarly, the DC current I_0 can be obtained from Eq. (2.31) by

$$I_0 = \frac{1}{2\pi}\int_0^{\pi} i_1(\omega t) d\omega t = \frac{I_{\text{R}}}{\pi}. \tag{2.35}$$

Considering that $I_{\mathrm{R}} = V/R_{\mathrm{L}}$ and the fact that the sinusoidal output current flows through either one or another transistor depending on which device is turned on and having a half-sinusoidal waveform, using Eq. (2.34) will result in

$$I_{\mathrm{R}} = I_{\max} = \frac{4}{\pi}\frac{V_{\mathrm{cc}}}{R_{\mathrm{L}}}\frac{1}{1+\dfrac{r_{\mathrm{sat}}}{R_{\mathrm{L}}}}. \tag{2.36}$$

The DC power P_0 and fundamental frequency output power P can be obtained using Eqs. (2.35) and (2.36) by

$$P_0 = 2V_{\mathrm{cc}}I_0 = \frac{8}{\pi^2}\frac{V_{\mathrm{cc}}^2}{R_{\mathrm{L}}}\frac{1}{1+\dfrac{r_{\mathrm{sat}}}{R_{\mathrm{L}}}}, \tag{2.37}$$

$$P = \frac{1}{2}I_{\mathrm{R}}^2 R_{\mathrm{L}} = \frac{8}{\pi^2}\frac{V_{\mathrm{cc}}^2}{R_{\mathrm{L}}}\frac{1}{\left(1+\dfrac{r_{\mathrm{sat}}}{R_{\mathrm{L}}}\right)^2}. \tag{2.38}$$

As a result, the collector efficiency η of a quasi-complementary voltage-switching push-pull power amplifier with a series filter can be expressed as

$$\eta = \frac{P}{P_0} = \frac{1}{1+\dfrac{r_{\mathrm{sat}}}{R_{\mathrm{L}}}}. \tag{2.39}$$

From Eq. (2.39), it follows that the collector efficiency is equal to 100% for an idealized case of the lossless active devices with zero saturation resistance. It should be mentioned that the DC current drawn from the power supply represents the form of a half-sinusoidal pulse train. Therefore it is very important to provide a proper RF bypassing circuit representing either a single large-value capacitor or an additional filter with a low cutoff frequency in the power supply line, including the series RF choke and shunt capacitors. In addition, the loaded quality factor for a simple series-tuned L_0C_0 circuit >5 must be chosen to provide a good compromise between the prevention of harmonic current and coil losses. An additional harmonic suppression can be obtained by inserting standard filters between the series-tuned L_0C_0 circuit and the load. Note that the collector efficiency degrades with increasing operating frequency where the switching transitions become an appreciable fraction of the signal period. In practice, it was found that high efficiency of a Class-D power amplifier can be maintained to frequencies of the order of $0.1f_{\mathrm{T}}$ for low-power transistors and of $0.01f_{\mathrm{T}}$ for high-power transistors rated at $>10\,\mathrm{W}$, where f_{T} is the device transition frequency.[8]

The circuit schematic of a voltage-switching Class-D power amplifier shown in Fig. 2.6A is called a quasi-complementary circuit because it is based on the same type of the two identical transistors, n-p-n bipolar or *n*-channel MOSFET devices, each in a common-emitter or a common-source configuration.[9] A true complementary power-amplifier circuit configuration requires two transistors of different types, n-p-n and p-n-p bipolar or n- and p-channel MOSFET devices. Fig. 2.7 shows two examples of such a true complementary voltage-switching Class-D push-pull power amplifier, a configuration with input transformer shown in Fig. 2.7A and a transformerless configuration shown in Fig. 2.7B. In the latter case, there is no need for a driving transformer because both transistors can be mounted on a single heatsink without electrical insulation.[10] The coupling capacitor C_1 must have a very low reactance

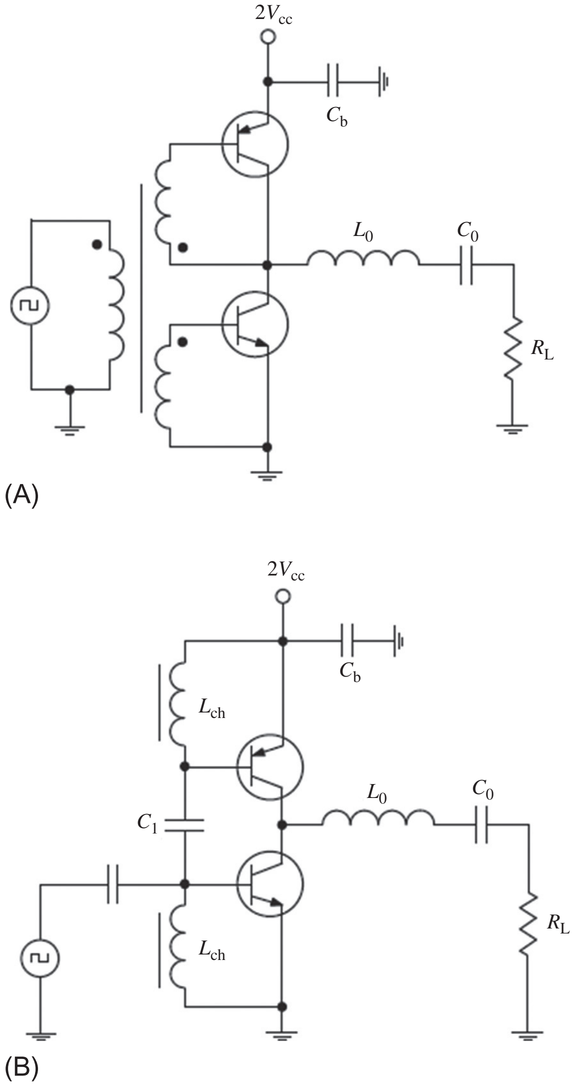
$2V_{cc}$
C_b
L_0
C_0
R_L
(A)
$2V_{cc}$
C_b
L_{ch}
C_1
L_0
C_0
R_L
L_{ch}
(B)

FIG. 2.7

True complementary voltage-switching Class-D power amplifier circuits.

to make a voltage drop at carrier frequency across it negligible compared with the input signal amplitude. Its value can be chosen as

$$C_1 \gg \frac{1}{2\pi f_0 r_b}, \tag{2.40}$$

where f_0 is the fundamental frequency of the input voltage, and r_b is the series base resistance of the bipolar transistor.

However, in practice, such circuits can be used at sufficiently low frequencies because of the much higher transition losses, resulting from performance mismatch between the complementary transistors. Consequently, further development in technology to provide similar electrical characteristics of truly complementary transistors would offer a new possibility for these Class-D power amplifiers, especially for a transformerless configuration, which can easily be integrated in a monolithic structure.

2.3 Transformer-coupled voltage-switching configuration

The broadband center-tapped and balanced-to-unbalanced (balun) transformers can also be used in voltage-switching Class-D power amplifiers in much the same manner as they are used in the switch-mode power amplifiers with resistive load or conventional Class-B push-pull power amplifiers. In this case, such a configuration is called the transformer-coupled voltage-switching Class-D power amplifier. Fig. 2.8A shows the simplified circuit schematic of a transformer-coupled voltage-switching bipolar Class-D power amplifier, including an output series-tuned L_0C_0 circuit and a load resistance R_L. The output transformer T_2 is considered as ideal, having m turns in each half of the primary winding and n turns in the secondary winding. As in the complementary voltage-switching configuration, the input transformer T_1 causes both active devices Q_1 and Q_2 to be driven with currents that are 180 degrees out of phase to switch on and off alternately. During the first half-cycle, when the transistor Q_1 is turned on, its collector voltage $v_1(\omega t)$ is equal to zero, assuming zero saturation resistance. As a result, the DC supply voltage V_{cc} is placed across one half of the primary winding of the transformer T_2, being then transformed to the voltage $(-n/m)V_{cc}$ on its secondary winding. When the transistor Q_2 is turned on, the DC supply voltage V_{cc} is applied to the other half of the primary winding causing voltage $(n/m)V_{cc}$ to appear on the secondary winding, as shown in Fig. 2.8B.

Consequently, when the switch Q_1 is turned on for $0 \leq \omega t \leq \pi$,

$$v_1(\omega t) = 0, \tag{2.41}$$

$$v_2(\omega t) = 2V_{cc}, \tag{2.42}$$

$$v(\omega t) = -\frac{n}{m}V_{cc}. \tag{2.43}$$

When the switch Q_1 is turned off for $\pi \leq \omega t \leq 2\pi$,

$$v_1(\omega t) = 2V_{cc}, \tag{2.44}$$

$$v_2(\omega t) = 0, \tag{2.45}$$

$$v(\omega t) = \frac{n}{m}V_{cc}. \tag{2.46}$$

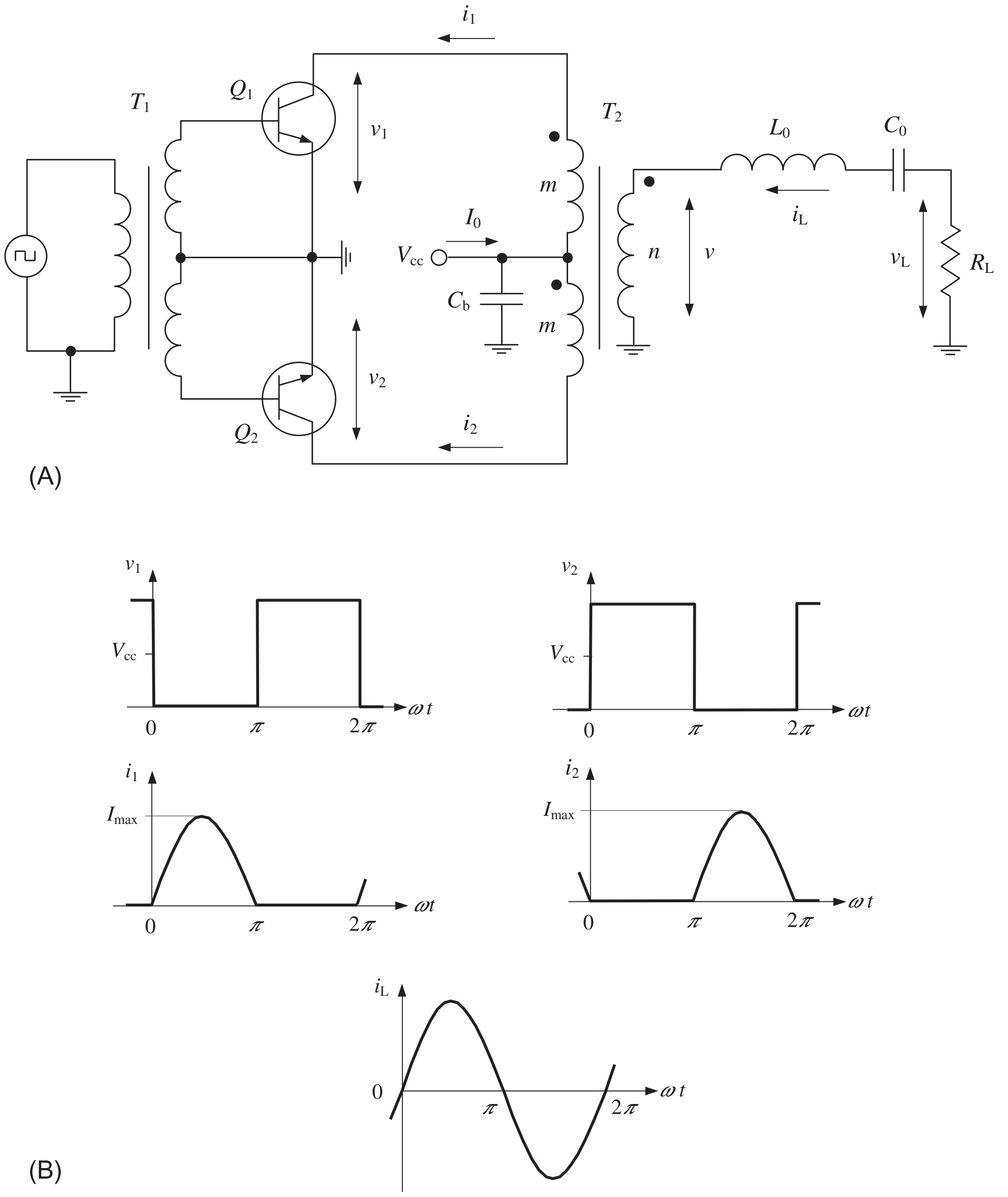
i_1
T_1
Q_1
v_1
T_2
L_0
C_0
m
I_0
i_L
V_{cc}
n
v
v_L
R_L
C_b
m
v_2
Q_2
i_2
(A)
v_1
V_{cc}
0
π
2π
ωt
v_2
V_{cc}
0
π
2π
ωt
i_1
I_{max}
0
π
2π
ωt
i_2
I_{max}
0
π
2π
ωt
i_L
0
π
2π
ωt
(B)

FIG. 2.8

Transformer-coupled voltage-switching push-pull configuration with series filter.

Thus the resulting secondary voltage $v(\omega t)$ represents a square wave with levels of $\pm(n/m)V_{\mathrm{cc}}$, while the collector voltages are square waves with levels of 0 and $+2V_{\mathrm{cc}}$. The fundamental frequency voltage amplitude V of the voltage $v(\omega t)$ can be calculated as

$$V_{\mathrm{L}} = V = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin\omega t \, d\omega t = \frac{4}{\pi}\frac{n}{m}V_{\mathrm{cc}}, \tag{2.47}$$

where V_{L} is the fundamental-frequency voltage amplitude on the load R_{L}.

Then, the fundamental-frequency output power P can be obtained by

$$P = \frac{1}{2}\frac{V_{\mathrm{L}}^2}{R_{\mathrm{L}}} = \frac{8}{\pi^2}\left(\frac{n}{m}\right)^2\frac{V_{\mathrm{cc}}^2}{R_{\mathrm{L}}} = \frac{8}{\pi^2}\frac{V_{\mathrm{cc}}^2}{R}, \tag{2.48}$$

where

$$R = \left(\frac{m}{n}\right)^2 R_{\mathrm{L}}, \tag{2.49}$$

is the equivalent fundamental-frequency resistance across one half of the primary winding of the output transformer T_2 seen by each device output, with the other one half of the primary winding open.

The amplitude I_{L} of a sinusoidal current $i_{\mathrm{L}}(\omega t)$ flowing to the load is given by

$$I_{\mathrm{L}} = \frac{V_{\mathrm{L}}}{R_{\mathrm{L}}} = \frac{4}{\pi}\frac{V_{\mathrm{cc}}}{R}. \tag{2.50}$$

Consequently, the collector currents of each transistor represent the half-sinusoidal waveforms with opposite phase of 180 degrees between each other, whose peak amplitudes are $(4/\pi)(V_{\mathrm{cc}}/R)$. The DC supply current I_0 represents a sum of two collector currents drawn into the center tap; hence

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi}[i_1(\omega t) + i_2(\omega t)]d\omega t = \frac{8}{\pi^2}\left(\frac{n}{m}\right)^2\frac{V_{\mathrm{cc}}}{R_{\mathrm{L}}}, \tag{2.51}$$

resulting in the collector efficiency of 100%, because the fundamental frequency power and dc power are equal. Note that a high efficiency can only be accomplished at lower frequencies because the presence of a parasitic device output capacitance during the transition from the off-state to on-state in addition to the requirement of a wideband balun rapidly reduces the efficiency with frequency. However, this performance degradation is less severe in current-mode Class-D power amplifiers.

2.4 Transformer-coupled current-switching configuration

Fig. 2.9A shows the circuit schematic of a current-switching Class-D power amplifier where the output balanced-to-unbalanced (balun) transformer is used to connect to a standard load by providing a push-pull operation. In this case, such a configuration is called the transformer-coupled current-switching Class-D power amplifier, which is the dual of the transformer-coupled voltage-switching Class-D power amplifier because the collector voltage and current waveforms are interchanged. As in the transformer-coupled voltage-switching configuration, the input transformer T_1 is necessary to drive both the active devices with currents having opposite phases for the on-to-off alternate device switching. The output transformer T_2 is considered ideal, having m turns in each half of the primary winding and n turns in the secondary winding. However, the DC current supply is connected to the center tap of

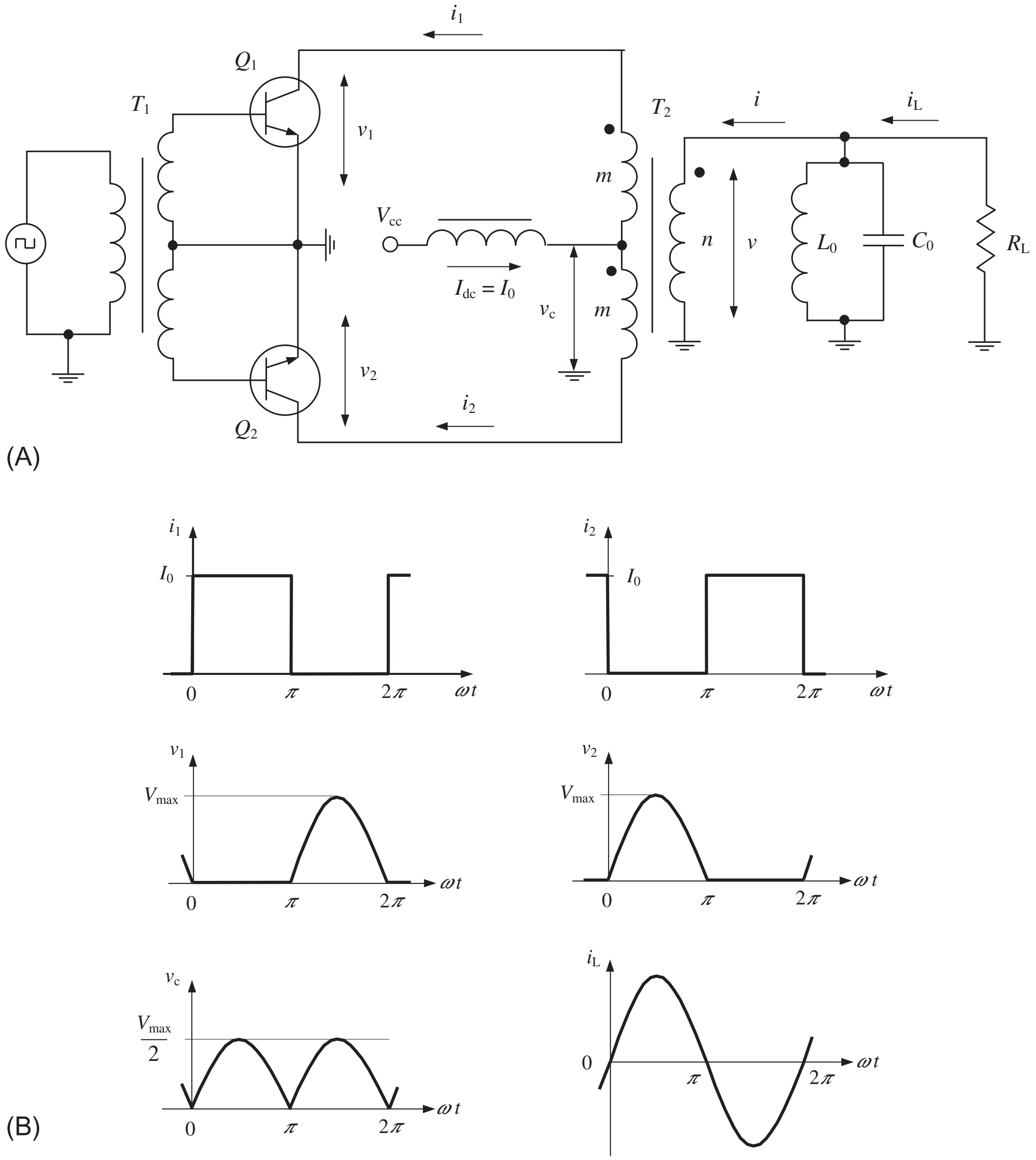
i_1
Q_1
T_1
v_1
T_2
i
i_L
m
V_{cc}
n
v
L_0
C_0
R_L
$I_{dc} = I_0$
v_c
m
v_2
i_2
Q_2
(A)
i_1
I_0
0
π
2π
ωt
i_2
I_0
0
π
2π
ωt
v_1
V_{max}
0
π
2π
ωt
v_2
V_{max}
0
π
2π
ωt
v_c
$\frac{V_{max}}{2}$
0
π
2π
ωt
i_L
0
π
2π
ωt
(B)

FIG. 2.9

Transformer-coupled current-switching configuration with parallel filter.

the transformer primary winding through the RF choke. The wideband balun at the output provides an open-circuit condition at even harmonics.

The load network of the transformer-coupled current-switching configuration requires a parallel fundamentally tuned resonant L_0C_0 circuit connected in parallel to the load R_L that provides low impedance to the two active devices at odd harmonics, instead of a series fundamentally tuned resonant L_0C_0 circuit required for the transformer-coupled voltage-switching configuration. Whichever device is turned on during the first half-cycle, it takes the entire DC current I_0, resulting in a rectangular collector current waveform with levels of 0 and I_0, as shown in Fig. 2.9B. Its collector voltage is equal to zero when it is turned on, assuming zero saturation resistance. Transformation of the rectangular collector current from half of the primary winding to the secondary winding produces a rectangular current $i(\omega t)$ with levels of $\pm(m/n)I_0$.

Consequently, when the switch Q_1 is turned on for $0 \le \omega t \le \pi$,

$$i_1(\omega t) = I_0, \tag{2.52}$$

$$i_2(\omega t) = 0, \tag{2.53}$$

$$i(\omega t) = \frac{m}{n} I_0. \tag{2.54}$$

When the switch Q_1 is turned off for $\pi \le \omega t \le 2\pi$,

$$i_1(\omega t) = 0, \tag{2.55}$$

$$i_2(\omega t) = I_0, \tag{2.56}$$

$$i(\omega t) = -\frac{m}{n} I_0. \tag{2.57}$$

Because the output parallel-tuned resonant circuit suppresses the harmonic components of the secondary current $i(\omega t)$, allowing only the fundamental frequency component $i_L(\omega t)$ to flow to the load R_L, its amplitude I_L can be expressed as

$$I_L = \frac{1}{\pi} \int_0^{2\pi} i(\omega t) \sin \omega t \, d\omega t = \frac{4}{\pi} \frac{m}{n} I_0. \tag{2.58}$$

The fundamental-frequency sinusoidal current $i_L(\omega t)$ produces the sinusoidal voltage $v(\omega t) = v_L(\omega t) = i_L(\omega t) R_L$ on the load resistance R_L with amplitude

$$V_L = V = \frac{4}{\pi} \frac{m}{n} I_0 R_L, \tag{2.59}$$

where V is the sinusoidal secondary voltage amplitude.

The sinusoidal voltage $v(\omega t)$ across the secondary winding is transformed to the primary winding, where it produces the sinusoidal voltage across each half of the primary winding with amplitude of $(m/n)V$. Because during half a period, one of the two transistors is turned on and the corresponding end of the primary winding is grounded, the peak amplitude of the voltage at the collector of the other transistor can be obtained by

$$V_{\max} = 2\left(\frac{m}{n}\right) V_L = \frac{8}{\pi} I_0 R, \tag{2.60}$$

where

$$R = \left(\frac{m}{n}\right)^2 R_\mathrm{L}, \tag{2.61}$$

is the equivalent fundamental-frequency resistance across one half of the primary winding of the output transformer T_2 seen by each device output, with the other one half of the primary winding open. Thus the sinusoidal voltage $v(\omega t)$ being transformed to the primary winding produces two half-sinusoidal collector voltages with opposite phases.

Because the center-tap voltage $v_\mathrm{c}(\omega t)$ represents half of the sum of two collector voltages, its average value can be calculated using Eq. (2.60) as

$$V_\mathrm{cc} = \frac{1}{2\pi}\int_0^{2\pi}\left[\frac{v_1(\omega t)}{2} + \frac{v_2(\omega t)}{2}\right] d\omega t = \frac{8}{\pi^2}\left(\frac{m}{n}\right)^2 I_0 R_\mathrm{L}, \tag{2.62}$$

where $v_1(\omega t) = -V_\mathrm{max}\sin\omega t$ for $\pi \le \omega t \le 2\pi$ and $v_2(\omega t) = V_\mathrm{max}\sin\omega t$ for $0 \le \omega t \le \pi$.

As a result, we have

$$I_0 = \frac{\pi^2}{8}\left(\frac{n}{m}\right)^2 \frac{V_\mathrm{cc}}{R_\mathrm{L}} = \frac{\pi^2}{8}\frac{V_\mathrm{cc}}{R}. \tag{2.63}$$

Then, the peak collector voltage V_max given by Eq. (2.60) can be rewritten as a function of the DC supply voltage V_cc only as

$$V_\mathrm{max} = \pi V_\mathrm{cc}. \tag{2.64}$$

Because there is no voltage drop across RF choke, the peak value of the voltage $v_\mathrm{c}(\omega t)$ having a full-wave rectified shape is equal to $(\pi/2)V_\mathrm{cc}$. By using Eqs. (2.59) and (2.63), the fundamental-frequency output power P and DC supply power P_0 can be obtained by

$$P = \frac{1}{2}\frac{V_\mathrm{L}^2}{R_\mathrm{L}} = \frac{\pi^2}{8}\left(\frac{n}{m}\right)^2 \frac{V_\mathrm{cc}^2}{R_\mathrm{L}}, \tag{2.65}$$

$$P_0 = V_\mathrm{cc} I_0 = \frac{\pi^2}{8}\left(\frac{n}{m}\right)^2 \frac{V_\mathrm{cc}^2}{R_\mathrm{L}}, \tag{2.66}$$

resulting in the collector efficiency of 100%, because the fundamental frequency power and DC power are equal.

The transformer-coupled current-switching Class-D power amplifier shown in Fig. 2.9A requires a wideband balun, which should have 180 degrees phase shift between its two ports at least up to the third harmonic. Therefore this topology is mainly used at low frequencies where wideband transformer can easily be designed. To avoid this problem of designing a wideband balun at higher frequencies, a symmetrical current-switching structure can be used where the output parallel-tuned tank is moved from the unbalanced load side to the balanced side that reduces the bandwidth requirement for the balun to one octave instead of multiple octaves.

2.5 Symmetrical current-switching configuration

Fig. 2.10A shows the simplified circuit schematic of a symmetrical current-switching Class-D bipolar power amplifier consisting of the same type of the active devices, fundamentally tuned parallel L_0C_0 filter, and balanced load resistance R_L. The RF choke L_{ch} connected to the center point of the inductor L_0 is necessary to isolate the DC power supply and make the circuit symmetrical. Each active device is considered a switch with the saturation resistance r_{sat}, as shown in Fig. 2.10B, which is driven in such a way as to provide an alternating switching between the on-state and off-state operation conditions of the transistor under an assumption of a 50% duty ratio. Because the only DC current I_0 is flowing through the RF choke L_{ch}, the alternating half-period device switching between their pinch-off mode and saturation mode results in rectangular collector current pulses with a maximum amplitude of $2I_0$, as shown in Fig. 2.10C.

The collector current pulses, which contain the odd harmonic components only, are applied to the parallel L_0C_0 filter with a high loaded quality factor $Q_L = \omega C_0 R_L \gg 1$ tuned to the fundamental frequency $f_0 = \omega_0/2\pi = 1/2\pi\sqrt{L_0C_0}$, resulting in the fundamental frequency sinusoidal voltage $v_R = V_R \sin\omega t$ across the load R_L. During half a period, when one transistor is turned on, the half-wave of this voltage is applied to the other transistor representing the half-sinusoidal collector voltage pulses, which contain the fundamental frequency, second-, and higher-order even harmonic components only. The flat shape of the saturation voltage with maximum amplitude V_{sat} is fully determined by the collector current waveform when $i_1(\omega t)$, $i_2(\omega t) > 0$ according to $v_{sat}(\omega t) = r_{sat}\, i_1(\omega t) = r_{sat}\, i_2(\omega t)$ for a symmetrical circuit with identical transistors. Unlike a complementary voltage-switching configuration, the transistor outputs are connected in series, thus resulting in an equivalent load resistance equal to $R_L/2$ for each device.

It should be noted that the symmetrical current-switching Class-D power amplifier, the collector voltage and current waveforms of which are shown in Fig. 2.10C, is the dual of the complementary voltage-switching Class-D power amplifier, the collector voltage and current waveforms of which are shown in Fig. 2.6C, because the voltage and current waveforms are interchanged. However, if, in the case of a voltage-switching configuration, the collector peak voltage is defined by the DC supply voltage V_{cc} only, then, in the latter case of a current-switching configuration, the transistors represent current switches with the current amplitude defined by the DC voltage supply V_{cc}, saturation resistance r_{sat}, and load resistance R_L. For an operation mode with conduction angles greater than 180 degrees, there is a time period when both active devices are turned on simultaneously, and parallel-tuned circuit is shunted by a small resistance $2r_{sat}$. Therefore to eliminate this shunting effect accompanied by power losses in both transistors, it is necessary to include a diode in series to each device collector, as shown in Fig. 2.10B. However, the operation conditions with conduction angles less than 180 degrees are unacceptable, because there are time intervals when both transistors are turned off simultaneously causing significant increase in the collector voltage amplitude owing to the growth of the current flowing through RF choke.

Now let us determine the current $i(\omega t) = i_1(\omega t) - I_0$ in a parallel L_0C_0 circuit and collector voltage $v_1(\omega t)$ for the first transistor operating as a current switch with a saturation resistance r_{sat}. When the first switch is turned on for $0 \le \omega t \le \pi$, then $i_1(\omega t) = 2I_0$, resulting in

$$i(\omega t) = I_0, \tag{2.67}$$

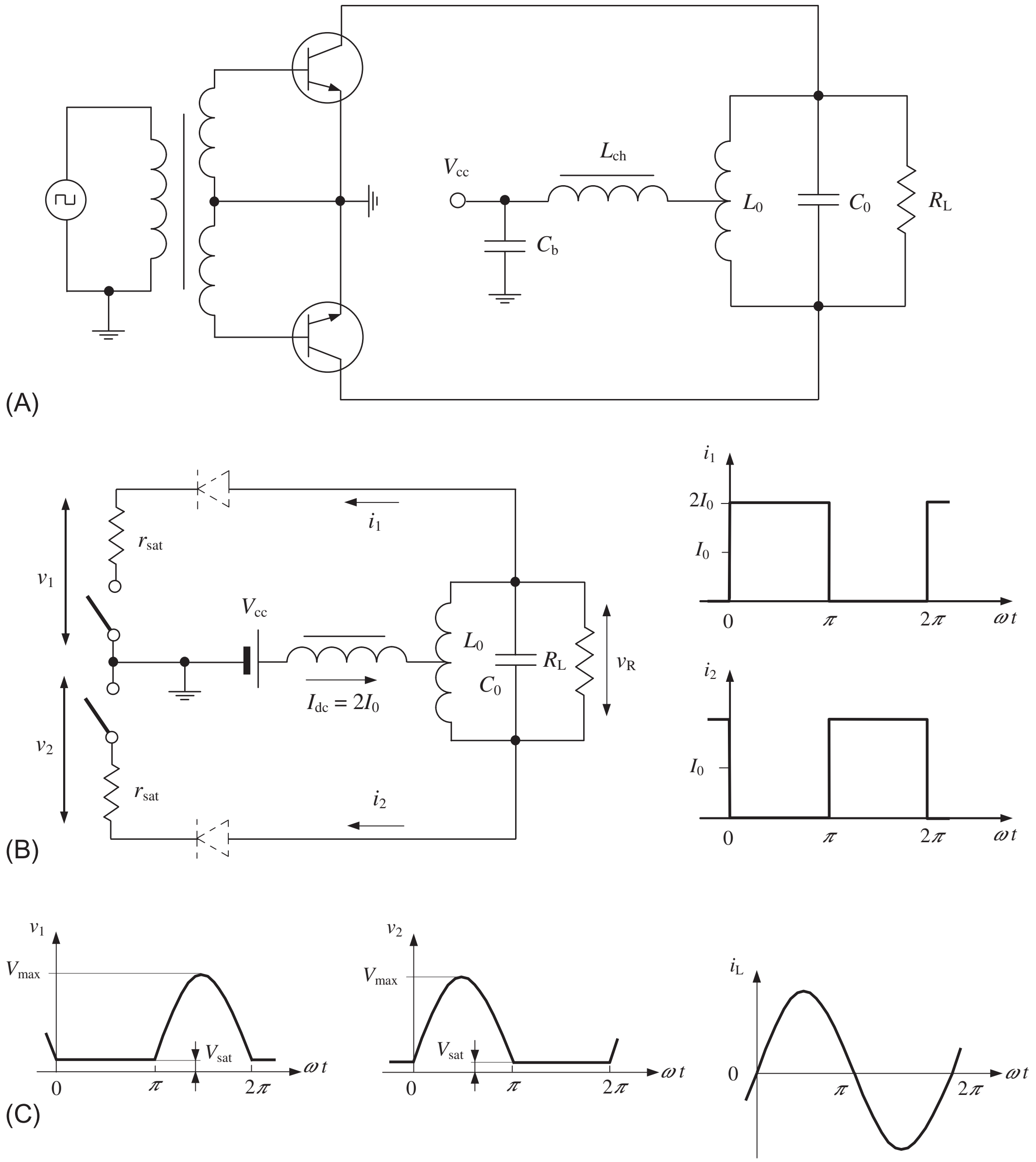
(A)
V_{cc}
L_{ch}
L_0
C_0
R_L
C_b
(B)
v_1
v_2
r_{sat}
r_{sat}
i_1
i_2
V_{cc}
$I_{dc} = 2I_0$
L_0
C_0
R_L
v_R
i_1
$2I_0$
I_0
i_2
I_0
0
π
2π
ωt
(C)
v_1
v_2
V_{max}
V_{sat}
i_L
0
π
2π
ωt

FIG. 2.10

Symmetrical current-switching configuration with parallel filter.

$$v_1(\omega t) = V_{\text{sat}} = 2r_{\text{sat}}I_0, \tag{2.68}$$

where I_0 is the DC supply current of each device.

When the first switch is turned off for $\pi \le \omega t \le 2\pi$, then $i_1(\omega t) = 0$, resulting in

$$i(\omega t) = -I_0, \tag{2.69}$$

$$v_1(\omega t) = -(V_{\max} - 2r_{\text{sat}}I_0)\sin\omega t + 2r_{\text{sat}}I_0, \tag{2.70}$$

where $V_{\max}$ is the collector peak voltage.

The fundamental frequency current amplitude I of the current $i(\omega t)$ can be calculated by applying a Fourier transform to Eqs. (2.67) and (2.69) as

$$I = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)\sin\omega t\, d\omega t = \frac{4}{\pi}I_0. \tag{2.71}$$

Similarly, the DC supply voltage V_{cc} can be written from Eqs. (2.68) and (2.70) as

$$V_{\text{cc}} = \frac{1}{2\pi}\int_0^{\pi} v_1(\omega t)d\omega t = \frac{1}{\pi}(V_{\max} - 2r_{\text{sat}}I_0). \tag{2.72}$$

Considering that $V_1 = V_{\max} - 2r_{\text{sat}}\ I_0 = IR_{\text{L}}$, the DC current I_0 and fundamental-frequency collector voltage V_1 can be obtained, respectively, by

$$I_0 = \left(\frac{\pi}{2}\right)^2 \left(1 + \frac{\pi^2}{2}\frac{r_{\text{sat}}}{R_{\text{L}}}\right)^{-1} \frac{V_{\text{cc}}}{R_{\text{L}}}, \tag{2.73}$$

$$V_1 = \pi\left(1 + \frac{\pi^2}{2}\frac{r_{\text{sat}}}{R_{\text{L}}}\right)^{-1} V_{\text{cc}}. \tag{2.74}$$

The DC power P_0 and fundamental-frequency output power P can be obtained, using Eqs. (2.73) and (2.74) and considering that $V_1 = V_{\text{R}}$, by

$$P_0 = 2V_{\text{cc}}I_0 = \frac{\pi^2}{2}\frac{V_{\text{cc}}^2}{R_{\text{L}}}\frac{1}{1 + \frac{\pi^2}{2}\frac{r_{\text{sat}}}{R_{\text{L}}}}, \tag{2.75}$$

$$P = \frac{1}{2}\frac{V_{\text{R}}^2}{R_{\text{L}}} = \frac{\pi^2}{2}\frac{V_{\text{cc}}^2}{R_{\text{L}}}\frac{1}{\left(1 + \frac{\pi^2}{2}\frac{r_{\text{sat}}}{R_{\text{L}}}\right)^2}. \tag{2.76}$$

As a result, the collector efficiency η of a symmetrical current-switching push-pull power amplifier with parallel filter can be written as

$$\eta = \frac{P}{P_0} = \frac{1}{1 + \frac{\pi^2}{2}\frac{r_{\text{sat}}}{R_{\text{L}}}}. \tag{2.77}$$

Microwave current-switching Class-D power amplifiers can be designed around 1 GHz by relying on the basic structure shown in Fig. 2.11, where the parallel L_0C_0 filter can be realized either by an air-wound inductor, a chip inductor, or by using high-impedance transmission lines together with a chip

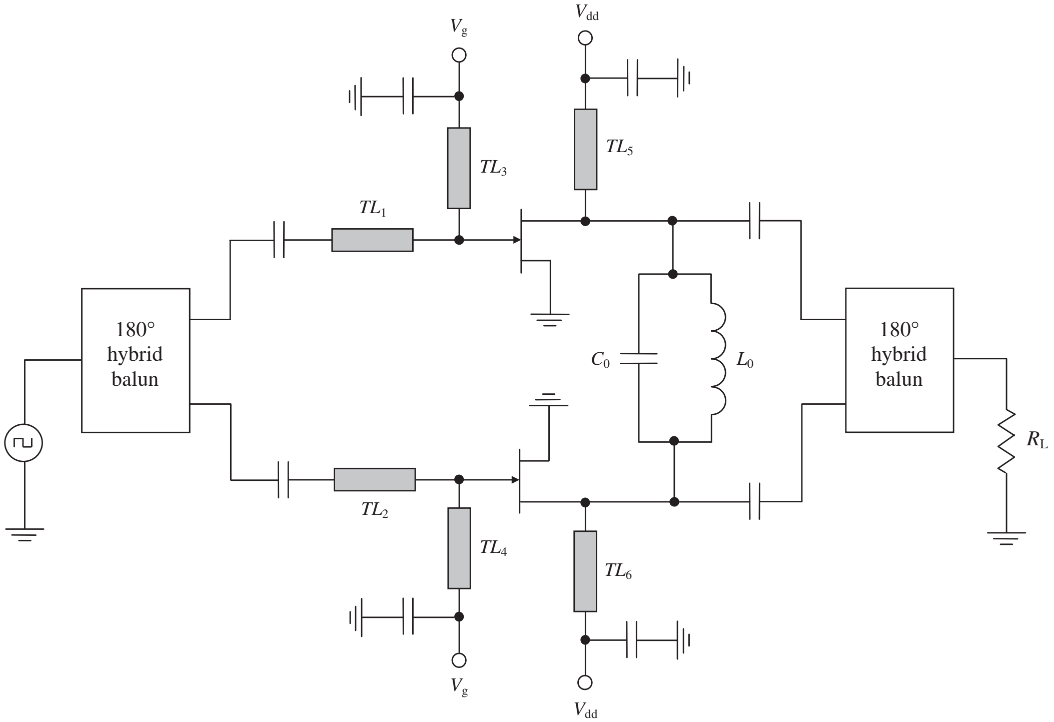

FIG. 2.11

Microwave symmetrical current-switching configuration with parallel filter.

capacitor.[11] An advantage of this approach at microwaves is that the parasitic output capacitances of the devices can be partially absorbed into external tank capacitance C_0. This reduces the frequency-dependent capacitive losses typical for voltage-switching Class-D power amplifiers and makes the design less sensitive to component tolerance. For such a 900-MHz current-switching Class-D power-amplifier, the required higher-order harmonic impedance termination can be provided by a second-order lattice lumped balun and a lumped-element parallel-tuned tank (air-coil inductor and ceramic capacitor) connected between the drain terminals of two devices, resulting in a peak drain efficiency of 75% at a saturated output power of 20 W using packaged GaN high-electron-mobility transfer (HEMT) devices.[12] A drain efficiency of 71% can be achieved with an output power of 20.3 W at an operating frequency of 1 GHz using a narrow transmission line as a tank inductor between two LDMOSFET devices.[13] However, the amplifier performance degrades as the operating frequency increases because of the bandwidth requirement of the balun, which should have absolute bandwidth of a few gigahertz, in this case, to cover at least the second-harmonic component. The other important problem is the implementation of a tank with lumped elements, whose self-resonance frequency lies beyond the third harmonic of the operating frequency. Otherwise, uncontrolled impedance termination at the most relevant harmonic frequencies degrades the performance of a current-switching Class-D power amplifier, resulting in a considerably lower efficiency than expected.

2.6 Voltage-switching configuration with reactive load

In practice, the load network of a switchmode Class-D power amplifier can have a nonzero reactance at the operating frequency caused by its mistuning or influence of the device parasitic reactive elements. Fig. 2.12A shows the circuit schematic of a quasi-complementary voltage-switching configuration with

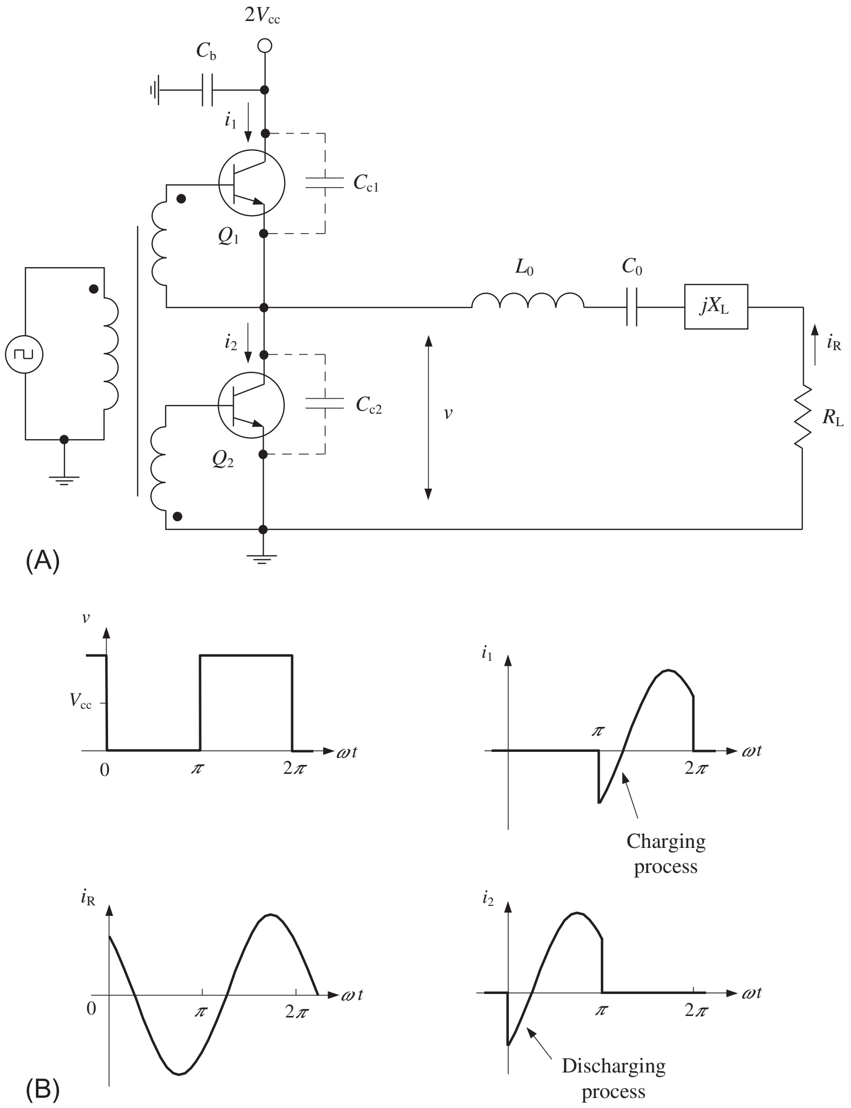
2V_cc
C_b
i_1
C_c1
Q_1
L_0
C_0
jX_L
i_R
i_2
C_c2
v
R_L
Q_2
(A)
v
V_cc
0
π
2π
ωt
i_1
π
2π
ωt
Charging process
i_R
0
π
2π
ωt
i_2
π
2π
ωt
Discharging process
(B)

FIG. 2.12

Voltage-switching Class-D power amplifier with reactive load.

reactive load, where C_{c1} and C_{c2} are the equivalent collector capacitances of each transistor, and X_L is the series load network reactance. The series fundamentally tuned L_0C_0 circuit reduces output currents at the harmonic frequencies flowing to the load to negligible level. The collector voltage waveforms of each transistor are unchanged by the load reactance. However, because of the effect of the series reactance X_L, the output current $i_R(\omega t)$ is shifted in phase relative to the collector voltage waveform, as shown in Fig. 2.12B. Because of this phase shift, both collector currents $i_1(\omega t)$ and $i_2(\omega t)$ tend to be negative during a portion of each period. In this case, the series resonant circuit represents an inductive load. If both transistors Q_1 and Q_2 are MOSFET devices, the negative currents can be passed without any potential damage, since the MOSFET intrinsic body-drain p-n junction diode may be used as an antiparallel diode. However, bipolar devices in general do not conduct in reverse direction. As a result, the negative currents will charge their equivalent collector capacitances C_{c1} and C_{c2}, producing large voltage spikes that can damage the transistors.

The series reactance reduces the amplitude of the output current and output power. If $Z_L = R_L + jX_L$, the load current $i_R(\omega t)$ of a complementary voltage-switching configuration with zero saturation resistance can be written using Eq. (2.36) as

$$i_R(\omega t) = \frac{4}{\pi} \frac{V_{cc}}{|Z_L|} \sin(\omega t + \varphi), \tag{2.78}$$

where the phase shift φ is defined by

$$\varphi = \tan^{-1} \frac{X_L}{R_L}. \tag{2.79}$$

Consequently, the fundamental frequency power P delivered to the load R_L will be reduced to

$$P = \frac{8}{\pi^2} \frac{V_{cc}^2}{R_L} \rho^2, \tag{2.80}$$

where

$$\rho = \frac{R_L}{|Z_L|} < 1. \tag{2.81}$$

A suitable reverse-direction current path is provided by diodes D_1 and D_2, as shown in Fig. 2.13A. In this case, the sinusoidal phase-shifted load current always passes through one of the four devices (Q_1, Q_2, D_1, or D_2), preventing the collector voltage spikes, as shown in Fig. 2.13B. Here, the shunt capacitance C_c represents a sum of both collector capacitances C_{c1} and C_{c2} and may include any parasitic stray circuit capacitance associated with the method of practical implementation. The same protection approach can be used in a transformer-coupled voltage-switching configuration. Active devices used in the symmetrical and transformer-coupled current-switching Class-D power amplifiers may be protected from the negative collector voltages by placing diodes in series with the collectors. Note that the collector efficiency of a Class-D power amplifier is essentially unchanged by the load network reactance.

The operation with a capacitive load is not recommended because the antiparallel diodes generate high reverse-recovery current spikes.[14] These spikes occur in the switch current waveforms at both the switch turn-on and switch turn-off and may destroy the transistors. The transistors are turned on at a high voltage equal to $2V_{cc}$, and the transistor output capacitance is short-circuited by a low transistor

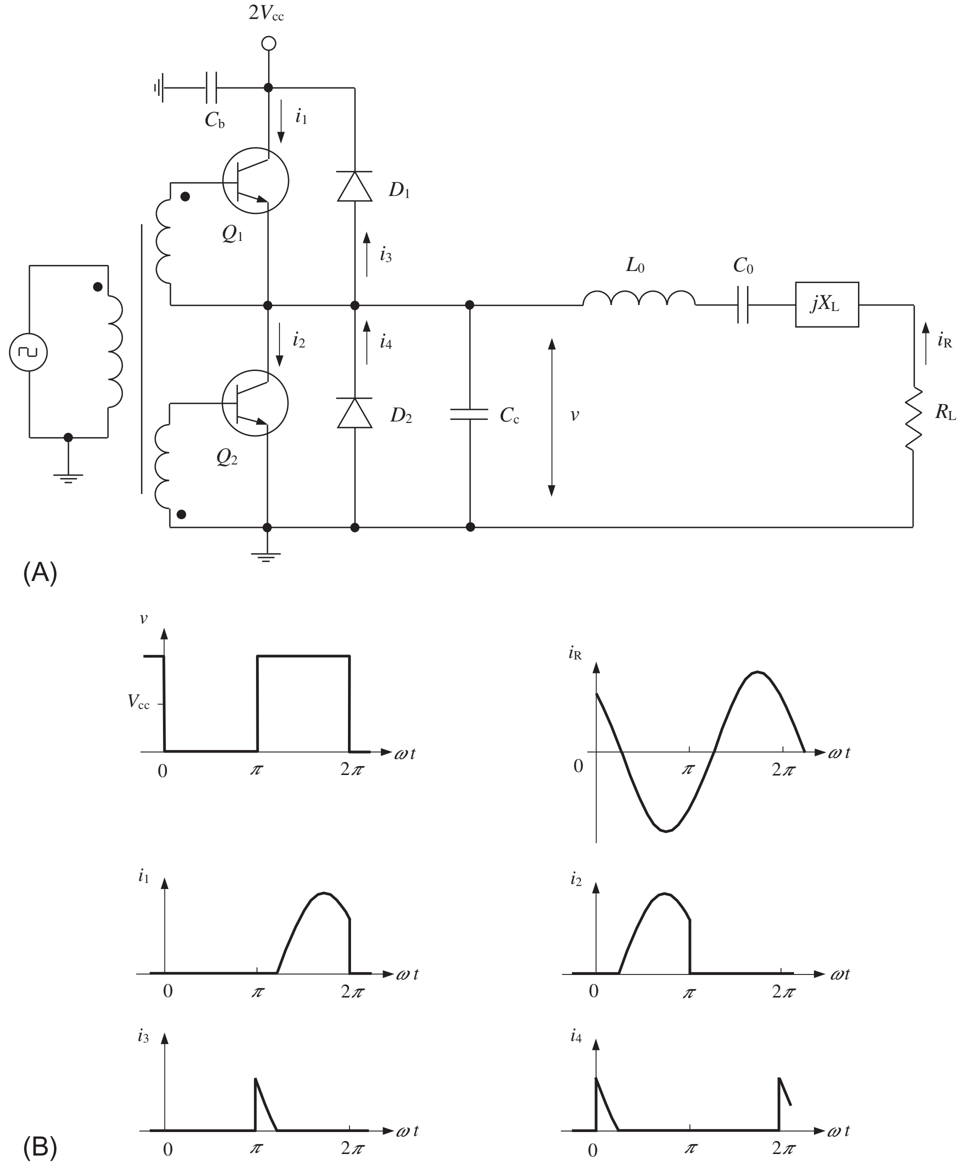
2V_{cc}
C_b
i_1
D_1
Q_1
i_3
L_0
C_0
jX_L
i_R
i_2
i_4
D_2
C_c
v
R_L
Q_2
(A)
v
V_{cc}
0
π
2π
ωt
i_R
i_1
i_2
i_3
i_4
(B)

FIG. 2.13

Voltage-switching Class-D power amplifier with reactive load and protection diodes.

saturation resistance, dissipating the energy stored in that capacitance. Therefore the turn-on switching loss is high, the effect of a feedback capacitance is significant, increasing the transistor input capacitance and the gate drive requirements, and the turn-on transition speed is reduced. Generally, the power amplifier can operate safely with an open circuit at the output. However, it is prone to catastrophic failure if the output is short-circuited at the operating frequency close to the resonant frequency of the output series resonant L_0C_0 circuit.

The presence of the parasitic collector capacitances C_{c1} and C_{c2} causes the power losses due to finite charge storage process. When the transistor Q_1 is turned on and the transistor Q_2 is turned off, the capacitor C_{c1} is discharged through the Q_1 and the capacitor C_{c2} is charged instantaneously to $2V_{cc}$. However, when the transistor Q_2 is turned on and the transistor Q_1 is turned off, the capacitor C_{c2} is discharged instantaneously through Q_2 and the capacitor C_{c1} is charged instantaneously to $2V_{cc}$. Because this occurs twice during each period and the power losses due to energy dissipated in both transistors with charging and discharging processes are equal, the total power losses due to finite switching time for a complementary voltage-switching Class-D power amplifier with supply voltage of $2V_{cc}$ and zero saturation resistance can be written as

$$P_s = (C_{c1} + C_{c2})(2V_{cc})^2 f_0 = 4C_c V_{cc}^2 f_0, \tag{2.82}$$

where $C_c = C_{c1} + C_{c2}$, and f_0 is the operating frequency. The total switching power losses described by Eq. (2.82) can also characterize the transformer-coupled voltage-switching Class-D power amplifier with a supply voltage of V_{cc}, in which the parasitic collector capacitances C_{c1} and C_{c2} are charged and discharged between 0 and $2V_{cc}$.

In the current-switching Class-D power amplifier, the parasitic capacitances do not provide charging and discharging losses because the collector currents flowing through the transistor have fixed constant values (either zero or maximum I_{DC}). However, there is another mechanism of power loss associated with parasitic inductances L_{c1} and L_{c2} (owing to finite lead length and leakage inductance in transformer) in series with transistor collectors. In this case, the currents flowing through the active devices jump when switching occurs because they must be changed from zero to I_{DC} instantaneously, twice during each period. Therefore the total power losses due to finite switching time for a current-switching Class-D power amplifier with zero saturation resistance can be written as

$$P_s = L_c I_{dc}^2 f_0, \tag{2.83}$$

where $L_c = L_{c1} + L_{c2}$.

2.7 Drive and transition time

The driving circuitry of a Class-D power amplifier must provide the driving signal sufficient to ensure that the active devices are alternately saturated or pinched off during the proper time period. Generally, if a current-switching Class-D power amplifier requires a rectangular current or voltage driving waveform, a voltage-switching Class-D power amplifier can be driven by either a rectangular or sinusoidal driving signal. Fig. 2.14 shows the input part of a voltage-switching bipolar Class-D power amplifier and the waveforms associated with rectangular voltage and sinusoidal current driving waveforms.

The sinusoidal current driven through the primary winding of the input transformer causes the half-sinusoidal currents to be driven into each base from the transformer secondary winding. The current flowing into the corresponding base results in a rise of the base-emitter voltage to V_{bmax}, which is approximately equal to its threshold voltage of 0.7 V for a bipolar device and corresponds to the maximum value required to saturate the MOSFET device. At the same time, the current flowing into the base of

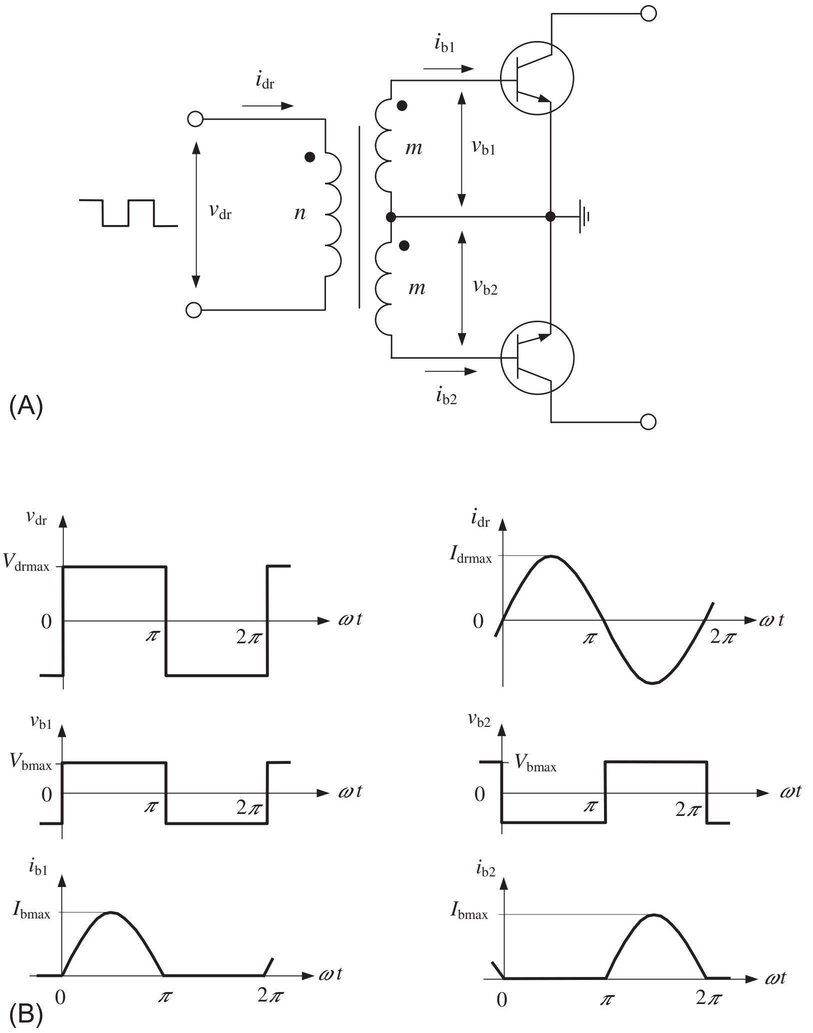
i_{b1}
i_{dr}
v_{dr}
n
m
v_{b1}
m
v_{b2}
i_{b2}
(A)
v_{dr}
V_{drmax}
0
π
2π
ωt
i_{dr}
I_{drmax}
0
π
2π
ωt
v_{b1}
V_{bmax}
0
π
2π
ωt
v_{b2}
V_{bmax}
0
π
2π
ωt
i_{b1}
I_{bmax}
0
π
2π
ωt
i_{b2}
I_{bmax}
0
π
2π
ωt
(B)

FIG. 2.14

Driving voltage and current waveforms.

the other transistor is shifted by 180 degrees, causing the fall of its base-emitter voltage to $-V_{\mathrm{bmax}}$, ensuring that the transistor is pinched off.

Hence the rectangular voltage with levels $\pm(m/n)V_{\mathrm{bmax}}$ appears across the primary winding. The impedance seen by the driver at the switching frequency represents a ratio of the fundamental frequency voltage driving amplitude to the current amplitude, written as

$$R_{\mathrm{dr}} = \frac{4}{\pi}\left(\frac{n}{m}\right)^2 \frac{V_{\mathrm{bmax}}}{I_{\mathrm{bmax}}}, \tag{2.84}$$

where I_{bmax} is the peak base current amplitude, which must be large enough to sustain the collector current.

Then, the required driving power is given by

$$P_{\mathrm{dr}} = \frac{2}{\pi} V_{\mathrm{bmax}} I_{\mathrm{bmax}}. \tag{2.85}$$

From Eq. (2.84), it follows that the driving resistance R_{dr} is a function of the driving current amplitude and is not related to transistor parameters other than the voltage corresponding to a forward-biased base-emitter junction. For this reason, the driver output current must be limited to prevent transistor failure.[5]

In a current-switching Class-D power amplifier, the rectangular collector (or drain) current requires the rectangular voltage and current driving waveforms. In this case, Eqs. (2.84) and (2.85) can be rewritten as

$$R_{\mathrm{dr}} = \left(\frac{n}{m}\right)^2 \frac{V_{\mathrm{bmax}}}{I_{\mathrm{bmax}}}, \tag{2.86}$$

$$P_{\mathrm{dr}} = V_{\mathrm{bmax}} I_{\mathrm{bmax}}, \tag{2.87}$$

where the driver output current also must be limited.

Fig. 2.15 shows the different configurations of the input driving circuits for a current-switching bipolar Class-D power amplifier. In the case of the driver with a rectangular current waveform, the active devices can be connected either in parallel, as shown in Fig. 2.15A, or in series, as shown in Fig. 2.15B, where L_{ch} is the choke inductor. For a parallel connection, the driving current is distributed between bipolar transistors being inversely proportional to their input impedances. The input impedance of the transistor at saturation is significantly less than that in the active and pinch-off regions. Because the transistor cannot change instantly its saturation mode to pinch-off conditions under a negative driving signal, it absorbs the most part of the driving current, thus preventing the other transistor to go into saturation under a positive driving signal. Therefore the series connection of the bipolar transistors is more effective because the driving current flows through both devices. However, the voltage across the reverse-biased base-emitter junction will be increased, the value of which must be controlled to prevent the device failure.

When the driver with a rectangular voltage waveform is used, the driving current flows through the forward-biased base-emitter junction of one transistor and the reverse-biased base-emitter junction of the other transistor when they are connected in series, as shown in Fig. 2.15C. If a shunt resistor R is connected in parallel to the transistor input, the effect of switching losses can be reduced because the device input capacitance is discharged faster through this resistor. A similar correction effect can be achieved by using a parallel RC circuit connected in series to each transistor when both transistors are connected in parallel, as shown in Fig. 2.15D. However, an increased current is required from the driver to saturate the transistor.

Generally, the input circuit of the transistor, either bipolar or MOSFET, can be represented as purely capacitive at low frequencies. In switching applications, however, the finite rise and fall times are the result of the effect of the much higher frequency components rather than the fundamental. For example, if the switching time of 4 ns can be tolerated at amplitude of 80% with a 30-MHz carrier, it represents roughly a 100-MHz sine wave.[15] Besides, the input capacitance is usually nonlinear and varies over bias conditions. For example, the MOSFET gate-source and gate-drain capacitances vary

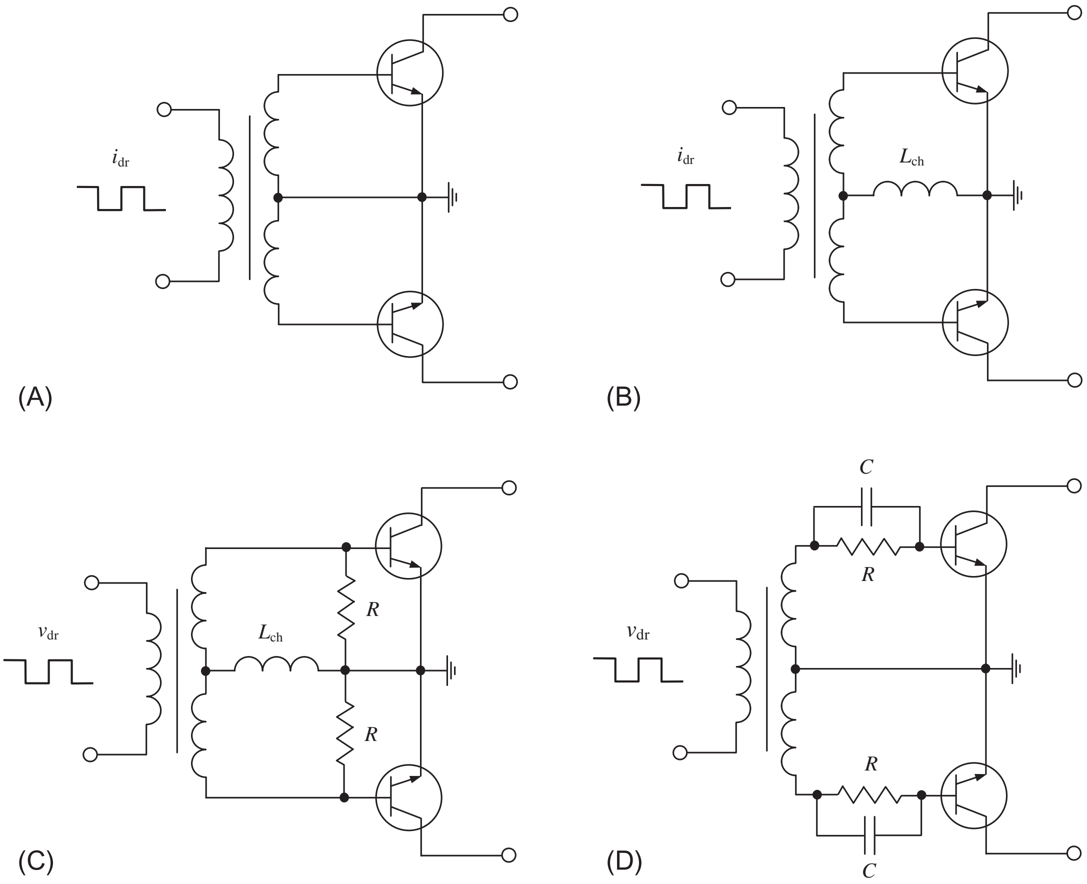

FIG. 2.15

Input driving circuits.

with gate and drain voltages. At increased gate voltage, the gate-source capacitance goes down to its lowest value, just before reaching the threshold voltage, and then goes up to be constant at saturation. At the same time, when the MOSFET device begins to draw drain current, the drain voltage is lowered, resulting in reduction of the depletion area and causing an overlap between the gate and bulk material. This in turn increases the value of the gate-drain capacitance, which takes maximum value at zero drain voltage and positive gate voltage corresponding to the maximum device transconductance. In bipolar transistors, the base-emitter nonlinear capacitance represents the large diffusion capacitance in the active and saturation regions and much lower junction capacitance in the pinch-off region.

However, at higher frequencies, the device equivalent input circuit must also include a series resistance, representing the base ohmic resistance for a bipolar transistor or effective gate resistance consisting of the distributed channel and gate electrode resistances for a MOSFET device. Let us consider the effect of a rectangular voltage drive with a duty ratio of 50% on the device input circuit shown in

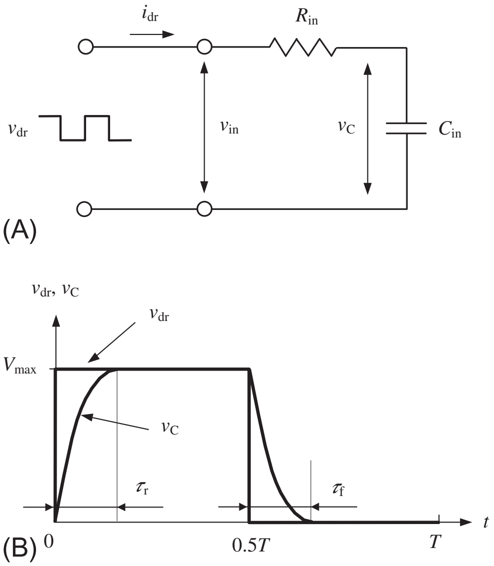

FIG. 2.16

Rectangular driving of equivalent input transistor circuit.

Fig. 2.16A, where R_{in} is the device input series resistance, and C_{in} is the device input capacitance. According to Kirchhoff's voltage law, the algebraic sum of all voltage drops taken around any closed path is zero, which gives

$$v_R + v_C - v_{in} = 0, \tag{2.88}$$

where

$$v_R = i_{dr}R = R_{in}C_{in}\frac{dv_C(t)}{dt}, \tag{2.89}$$

and both the resistance R_{in} and capacitance C_{in} are assumed to be voltage independent.

For a time period when $0 \le t \le 0.5T$,

$$v_{in} = V_{max}, \tag{2.90}$$

where V_{max} is the input peak voltage corresponding to the device saturation conditions.

Substituting Eqs. (2.89) and (2.90) into Eq. (2.88) yields

$$R_{in}C_{in}\frac{dv_C(t)}{dt} + v_C(t) = V_{max}. \tag{2.91}$$

The general solution of the linear nonhomogeneous first-order differential equation under initial condition of $v_C(t) = 0$ at $t = 0$, when there is no energy stored in the input capacitance, can be obtained by

$$\frac{v_C(t)}{V_{max}} = 1 - \exp\left(-\frac{t}{R_{in}C_{in}}\right), \tag{2.92}$$

which determines the length of a voltage angular rise time τ_r through the time constant $\tau_{in} = R_{in}C_{in}$ required for the input capacitance to charge up from 0 to V_{max}.

Similarly, for a time period when $0.5T \le t \le T$,

$$v_{in} = 0, \tag{2.93}$$

resulting in the linear homogeneous first-order differential equation

$$R_{in}C_{in}\frac{dv_C(t)}{dt} + v_C(t) = 0. \tag{2.94}$$

Under the initial condition of $v_C(t) = V_{max}$ when $t = 0.5T$, the solution of Eq. (2.94) can be written as

$$\frac{v_C(t)}{V_{max}} = \exp\left(-\frac{t}{R_{in}C_{in}}\right), \tag{2.95}$$

which determines the length of a voltage angular fall time τ_f through the time constant $\tau_{in} = R_{in}C_{in}$ required for the input capacitance to discharge down from V_{max} to zero.

From Eqs. (2.92) and (2.95), it follows that the switching losses due to charging and discharging effects of the input capacitance are the same with voltage rise time τ_r and fall time τ_f, both equal to $4\tau_{in}$ at the voltage level of 98% of V_{max}, which is shown in Fig. 2.16B. Note that the power requirement for the input drive is independent of the switching speed, and the switching speed is ultimately limited by the input resistance. Hence there is an intrinsic limit to how fast the input capacitance can be charged, which becomes a serious factor as the operating frequency increases.

Now let us consider a response of the same circuit to a sinusoidal voltage driving and its effect on the power losses during the switching time. For the device input circuit shown in Fig. 2.17A with a sinusoidal drive $v_{dr}(\omega t) = V_{dr}\sin\omega t$, we can write

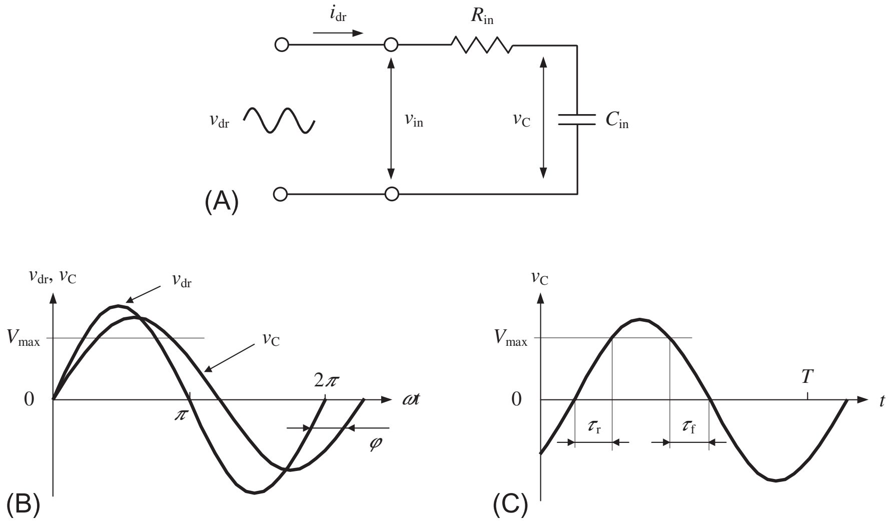

FIG. 2.17

Sinusoidal driving of equivalent input transistor circuit.

$$R_{\text{in}}C_{\text{in}}\frac{dv_C(t)}{dt}+v_C(t)=V_{\text{dr}}\sin\omega t, \tag{2.96}$$

where V_{dr} is the voltage amplitude of the driving signal.

The general solution of the linear nonhomogeneous first-order differential equation can be written as

$$v_C(t)=A\exp\left(-\frac{t}{\tau_{\text{in}}}\right)+\frac{V_{\text{dr}}}{1+(\omega\tau_{\text{in}})^2}(\sin\omega t-\tau_{\text{in}}\cos\omega t). \tag{2.97}$$

Let us assume that the driving voltage $v_{\text{dr}}(t)$ is zero at $t<0$, so that the initial voltage across the input capacitance is zero. Then, under the initial condition of $v_{\text{C}}(t)=0$ at $t=0$ required to determine the unknown coefficient A, Eq. (2.97) can be rewritten in a normalized form as

$$\frac{v_C(t)}{V_{\text{dr}}}=\frac{1}{\sqrt{1+(\omega\tau_{\text{in}})^2}}\left[\sin\varphi\exp\left(-\frac{t}{\tau_{\text{in}}}\right)+\sin(\omega t-\varphi)\right], \tag{2.98}$$

where $\varphi=\tan^{-1}(\omega\tau_{\text{in}})$ is the phase shift. From Eq. (2.98), it follows that, after a few time constants, the natural response corresponding to the capacitance-charging process becomes negligible, and only the sinusoidal response with phase shift of φ remains, as shown in Fig. 2.17B. Then, the circuit is operated in a sinusoidal steady-state mode with reduced amplitude.

The voltage rise time τ_{r} and fall time τ_{f} become longer with increasing input time constant $\tau_{\text{in}}=R_{\text{in}}C_{\text{in}}$ because the voltage amplitude across the capacitance reduces, becoming closer to the maximum amplitude $V_{\max}$ required for the saturation mode of the transistor. Consequently, to minimize power losses, it is just necessary to increase the voltage amplitude of the driving signal. An advantage of the sinusoidal driving signal compared with rectangular drive is that there is no need to use a broadband input transformer, and all lead and leakage inductances in the gate-drive circuit can be absorbed into the input resonant circuit. With a sinusoidal driving technique, a quasi-complementary voltage-switching Class-D power amplifier was capable of providing an output power of 300 W at an operating frequency of 13.56 MHz with a drain efficiency of over 90% using a low-inductance half-bridge MOSFET die package on an alumina substrate.[2]

Generally, an exact analysis that includes transition waveforms and effects of elements of the complete device equivalent circuit is very complicated. This analysis of power losses can be substantially simplified by assuming that the resultant collector (or drain) voltage waveform of a complementary voltage-switching Class-D power amplifier is trapezoidal when the transitions produce ramp voltage waveforms, as shown in Fig. 2.18.[5] From Fig. 2.17C, we can see that, under sinusoidal drive with increased voltage amplitude, the shape of the rise time τ_{r} and fall time τ_{f} is close to ramp. The transition time required by a single transistor to complete the entire switching process is shown in Fig. 2.18, being converted to the angular time τ_{s}. This time can include an effect of the output capacitance and other device parasitics. Both transistors are assumed to have zero saturation resistances, and switching is completed within $2\tau_{\text{s}}$.

The fundamental frequency collector voltage amplitude V is obtained by a Fourier integral of the trapezoidal waveform with the DC supply voltage of $2V_{\text{cc}}$ as

$$V=\frac{4}{\pi}V_{\text{cc}}\frac{\sin\tau_{\text{s}}}{\tau_{\text{s}}}\approx\frac{4}{\pi}V_{\text{cc}}\left(1-\frac{\tau_{\text{s}}^2}{6}\right), \tag{2.99}$$

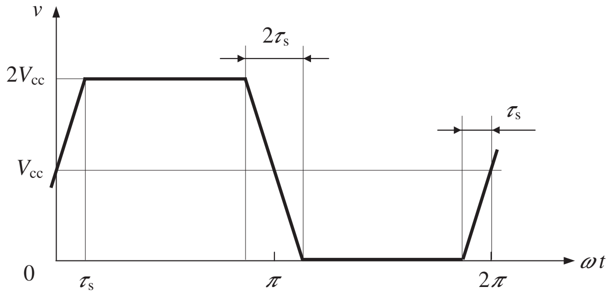

FIG. 2.18

Transition time in Class-D power amplifier.

where the linear approximation is valid only for small values of τ_s.

For the fundamental-frequency output power $P = V^2/(2R_L)$ and DC current $I_0 = V/(\pi R_L)$, where R_L is the load resistance, the collector efficiency can be calculated from

$$\eta = \frac{\pi}{4}\frac{V}{V_{cc}} = \frac{\sin \tau_s}{\tau_s}. \tag{2.100}$$

The same results may also be obtained for the symmetrical current-switching and both voltage-switching and current-switching transformer-coupled Class-D power amplifier configurations.[16]

2.8 Practical Class-D power amplifier implementation

Fig. 2.19 shows the circuit schematic of a quasi-complementary MOSFET voltage-switching Class-D power amplifier, where the DC power supply is connected to the drain of the top device and the source of the other device is connected to the ground.[17] The devices are driven through a three-winding transformer with appropriate polarities on the output so that the same drive is used for both the devices. The midpoint between the two devices is connected to the series resonant L_0C_0 circuit with a reasonable loaded quality factor of about 10, which can provide a small impedance at the fundamental frequency and high impedances at the harmonic components. To design a 300-W Class-D power amplifier operating at 13.56 MHz from a 75-V DC supply voltage, it is necessary to provide the load resistance $R_L = 3.8\,\Omega$ and peak drain current $I_{max} = 12.56$ A in accordance with Eqs. (2.36) and (2.38), assuming zero device saturation resistance. To satisfy these requirements, the MOSFET devices IRF540 were chosen, which can operate under DC voltage and current conditions of 100 V and 25 A, respectively. This MOSFET device has a saturation resistance equal to 0.085 Ω, thus providing the conduction losses per device of 3.35 W. The output capacitance of the device is equal to 500 pF. Consequently, according to Eq. (2.82), the switching losses per device owing to capacitance discharging process are equal to 38.14 W. As a result, the maximum expected drain efficiency can reach a value of 80%. However, it also needs to consider an effect of the device input circuit with a time constant $\tau_{in} = 39$ ns for a gate voltage of 10 V to rectangular drive that makes the overall transition time even longer.

Digitally driven power amplifiers can enable straightforward programmable operation with flexible modulation using input signals provided by digital CMOS circuits, which can directly contribute to a

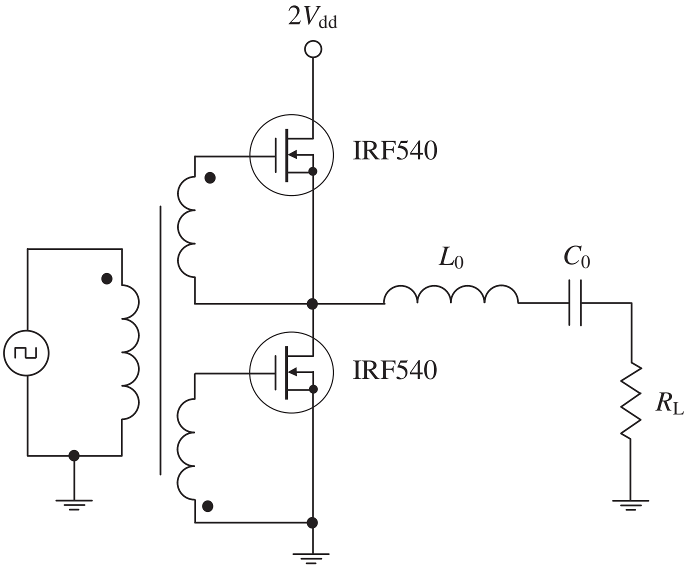

FIG. 2.19

MOSFET voltage-switching Class-D power amplifier.

highly efficient switchmode operation. Fig. 2.20. shows the circuit schematic of a voltage-mode Class-D power amplifier which was implemented in a 0.25-μm GaN HEMT monolithic microwave integrated circuit (MMIC) process, with external series L_0C_0 resonator for harmonic filtering.[18] Here, the driver stages are required to supply the digital input signals to the gates of the corresponding transistors in the output stage, which comprises a series stack of two GaN HEMTs. Owing to the absence of the *p*-channel transistors in GaN technology, the high-side driver design is more complicated than that for the low-side driver because the gate voltage for the top device must have a very large swing, from below ground to approximately the full power supply voltage. This is accomplished with the bootstrap driver without an increase in DC power consumption. In this case, when M_2 is turned on, the blocking capacitor C_b charges to the auxiliary supply voltage V_{ddH}. However, when M_2 is turned off, the output voltage V_{out} rises and, hence, the voltage V_a rises as well. This provides an appropriately high drive voltage for the gate of M_1. The performance of the fabricated voltage-switching Class-D power amplifier was evaluated by using a digital input signal with a 50% duty ratio at the carrier frequency of 465 MHz. As a result, a drain efficiency of 77.2% and a maximum *PAE* of 66.6% were achieved with an output power of 3.3 W at $V_{ddF} = 35$ V.

The circuit schematic of a transformer-coupled voltage-switching GaN HEMT Class-D power amplifier providing wideband operation conditions is shown in Fig. 2.21A.[19] Here, two GaN HEMT devices are operated in a push-pull mode, two parallel *RC* circuits are included to provide stable operation conditions, and a 1:1 balun is used at the output for power combining. Each GaN HEMT device should be driven into saturation to operate as a switch and generate the desired symmetrical rectangular-wave voltage at the drain. Two pairs of twisted-isolated wires are used to feed the DC-supply drain currents to both devices. In this case, the mutual inductive coupling coefficient between twisted-isolated wires is

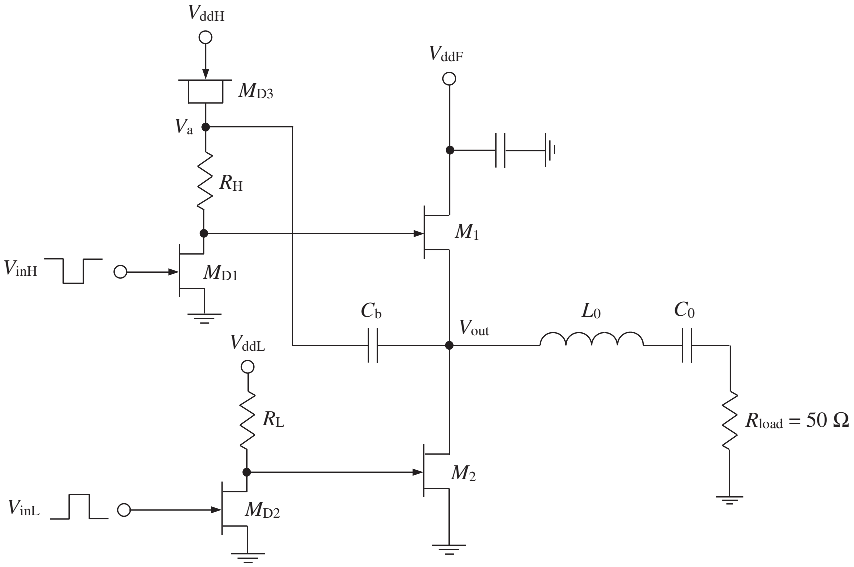

FIG. 2.20

Circuit schematic of a voltage-mode GaN HEMT Class-D power amplifier.

critical to achieve a voltage-mode operation and to sustain high drain efficiency. The optimum load impedance for each device was estimated as 25 Ω for a 25-W output power at a supply voltage of 28 V. When using a push-pull topology, the even-order harmonic signals are cancelled out in the output balun. Therefore a bank of low-pass filters is used on the output side of the 1:1 balun to reject the third harmonic of the rectangular waveform. The simulated transient drain voltage and current waveforms at 200 MHz are shown in Fig. 2.21B, while the drain efficiency and output power over 50–550 MHz are shown in Fig. 2.21C. The transformer-coupled voltage-switching Class-D power amplifier using two Cree CGH40010F devices was fabricated on a FR4 substrate. The measured drain efficiency of 63%–72% was achieved across the wide frequency range of 50–550 MHz with an output power of 43–45 dBm.

Applying a current-switching Class-D configuration enables to eliminate switching losses due to the device output shunt capacitances. In this case, it is necessary to minimize the switching losses due to the parasitic series inductances, which can be represented by the lead inductances of the device package. However, by on-chip integration of the parallel *LC* resonator, it is possible to reduce the circuit complexity and eliminate parasitic reactance losses.

Fig. 2.22 shows the circuit schematic a current-switching InGaP/GaAs HBT Class-D power amplifier where active devices represent 80 emitter fingers with emitter area of 2 μm × 20 μm and peak current density of 0.11 mA/μm^2.[16] A 180 degrees input balun based on a 50-Ω coaxial line generates differential input signals, while a 180 degrees output balun converts the balanced output with 180 degrees out-of-phase output signals to a single-ended output signal. To maximize the power gain, the input and output matching circuits in the form of high-pass L-sections are applied to each transistor. The LC resonator comprises a bondwire inductor and a metal-insulator-metal (MIM) capacitor. Using a

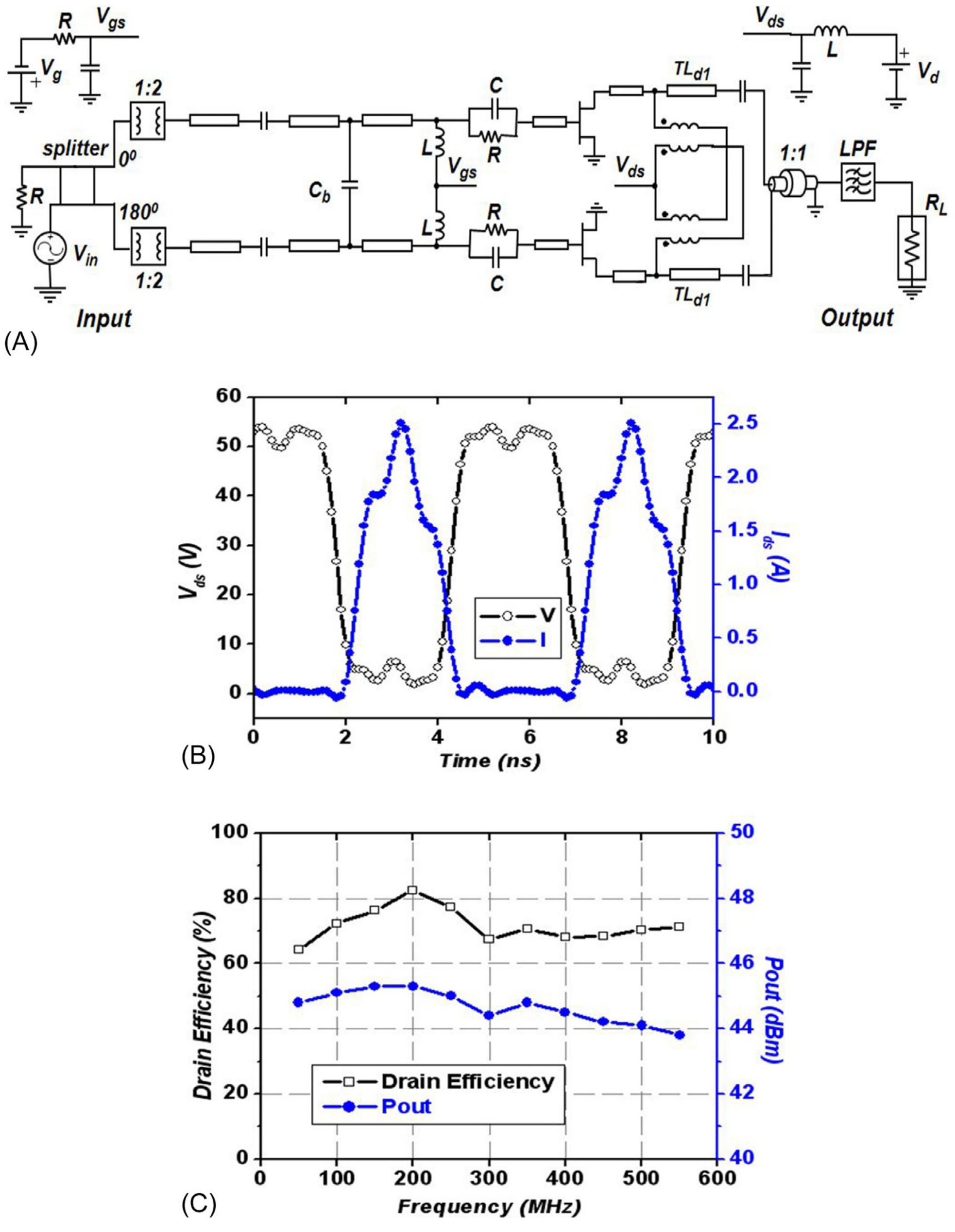
R
Vgs
Vg
1:2
splitter
0°
R
180°
Vin
1:2
Input
(A)
C
R
Cb
L
Vgs
L
R
C
TLd1
Vds
TLd1
Vds
L
Vd
1:1
LPF
RL
Output
60
50
40
30
20
10
0
Vds (V)
0
2
4
6
8
10
Time (ns)
2.5
2.0
1.5
1.0
0.5
0.0
Ids (A)
V
I
(B)
100
80
60
40
20
0
Drain Efficiency (%)
0
100
200
300
400
500
600
Frequency (MHz)
50
48
46
44
42
40
Pout (dBm)
Drain Efficiency
Pout
(C)

FIG. 2.21

Circuit schematic and simulated performance of transformer-coupled voltage-mode GaN HEMT Class-D power amplifier.[19]

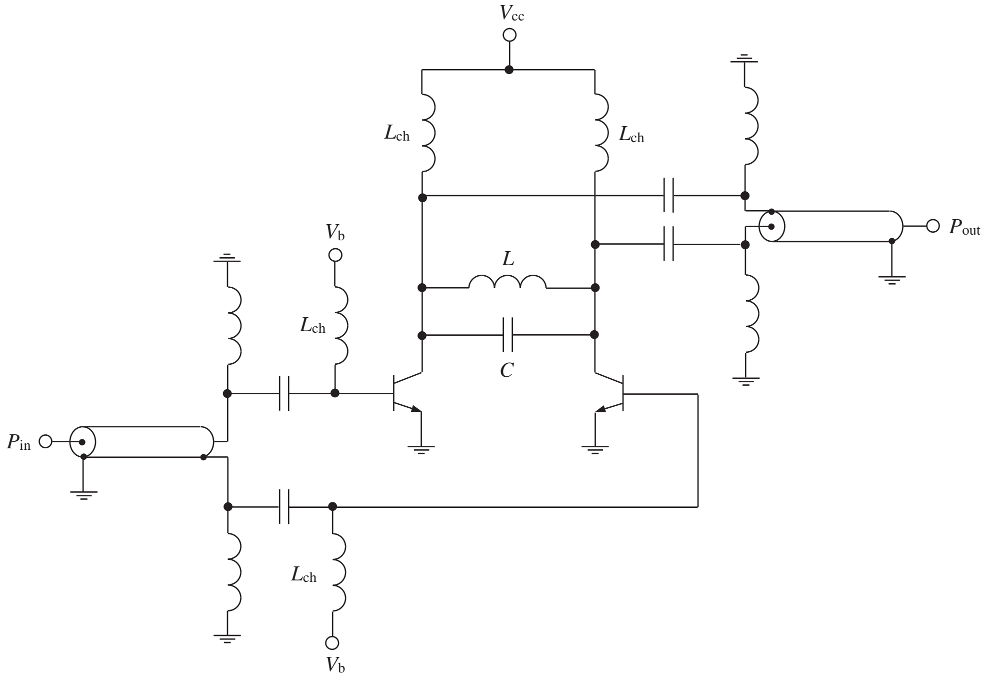

FIG. 2.22

Schematic of bipolar current-switching Class-D power amplifier.

spiral inductor with a lower quality factor reduces collector efficiency by 5%. At a supply voltage of 3.4 V, the transistor saturation resistance r_{sat} and transition time τ_s were equal to $0.58\,\Omega$ and 0.1π, respectively. The bases of both HBTs are biased to a turn-on voltage of 1.2 V for operation as switches. As a result, the current-switching Class-D power amplifier achieved a collector efficiency of 78.5% at an output power of 29.5 dBm with a maximum PAE of 68.5% at an operating frequency of 700 MHz. The best efficiency was achieved at a high drive level, resulting in a power gain of about 9 dB. By using a similar approach with GaAs MESFETs devices, a *PAE* of 75.6% with an output power of 28.6 dBm and a power gain of 13.9 dB was achieved at the operating frequency of 900 MHz and supply voltage of 5 V.[20]

Enhanced current-switching Class-D architecture for a high-frequency operation can provide the required harmonic impedance conditions (open circuit for even-harmonic and short circuit for odd-harmonic components of the fundamental frequency) using a transmission-line multiharmonic load coupling network, which makes the amplifier performance independent of the performance of the balun and the parallel tank at higher harmonics. Practically, it is difficult to control more than the second- and third-harmonic components, which provide the most contribution to the output voltage and current waveforms. Therefore the multiharmonic load transformation network connected to the output terminal of each device performs simultaneously the fundamental load transformation and the correct impedance termination at the second and third harmonics of the fundamental frequency. Basically, this results

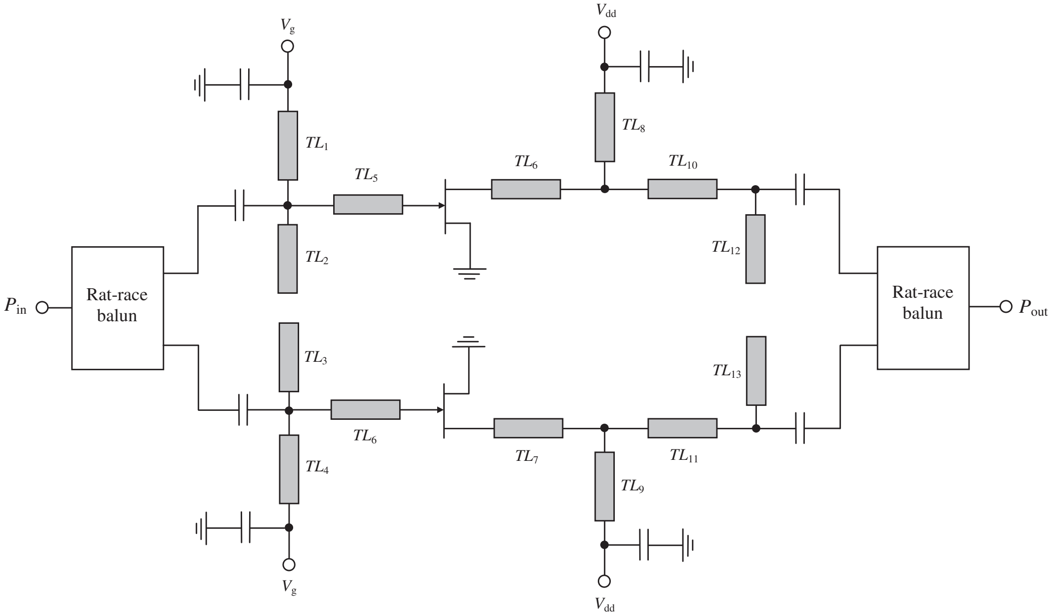

FIG. 2.23

Microwave current-switching configuration with multiharmonic transformation networks.

in an inverse Class-F operation mode for each single amplification branch, which in turn is equivalent to the current-switching Class-D operation mode. In this case, harmonic components in the load are removed by the impedance transformation networks instead of by the combination of balun and parallel-tuned tank as in conventional architecture.

Fig. 2.23 shows the schematic diagram of a high-frequency current-switching Class-D power amplifier with transmission-line multiharmonic transformation networks.[11] In this structure, the lumped-element tank is avoided and replaced by open-circuited quarterwave transmission lines (TL_{12} and TL_{13}) at the third harmonic, which provide the low impedance at the drain of the active devices at this frequency. Should it be necessary to also present low impedance at higher-order odd harmonics, more stubs can be used. Instead of relying on the balun to provide high impedance at even harmonics, a short-circuit stub can be included in the output network. Using this approach, the balun needs to be designed to operate at the fundamental frequency only, thus avoiding the difficulties associated with the implementation of a wideband balun at microwave frequencies. The drain bias for each device is applied through the corresponding quarterwave transmission line (TL_8 or TL_9) shorted to ground by a large capacitor at one side. Each transmission line provides a high impedance at the fundamental frequency, as well as at all odd harmonics, whereas it provides a low input impedance at the second harmonic. This low impedance at the second harmonic is then transformed into a high impedance at the drain of the device by using an appropriate series transmission line (TL_6 or TL_7). As a result, a 39-dBm GaN HEMT current-switching Class-D power amplifier designed at 2.35 GHz achieved a drain efficiency of 68% and a *PAE* of 65% using a narrowband 180 degrees rat-race balun. The baluns can also

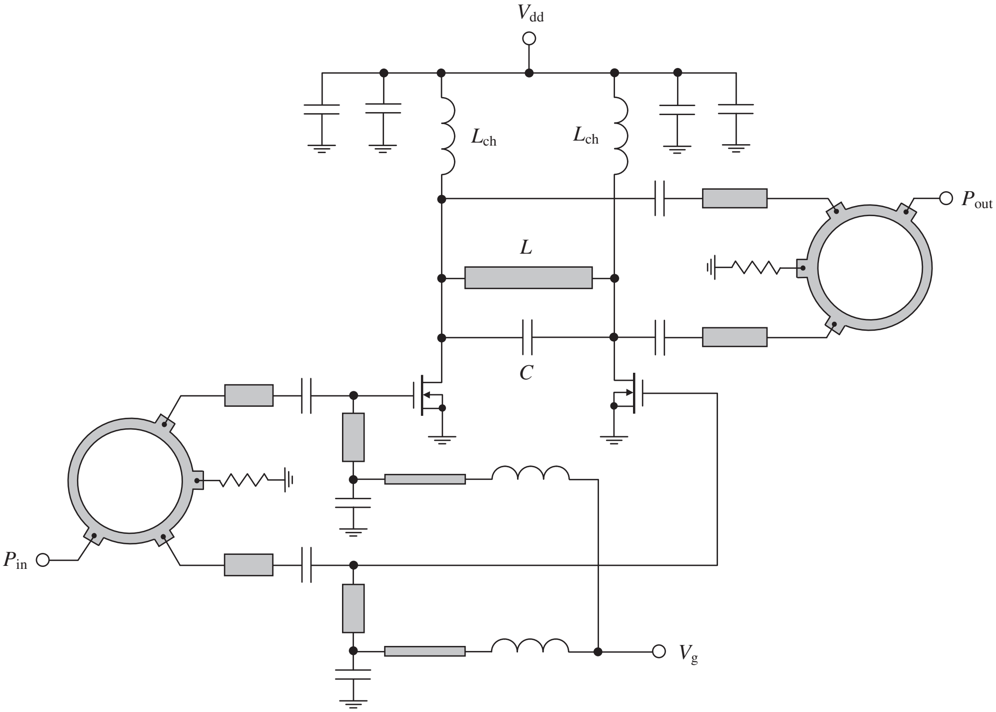

FIG. 2.24

Schematic of LDMOSFET current-switching Class-D power amplifier.

be constructed using low-loss quarterwave microstrip lines together with commercial 90 degrees hybrids or microstrip-based coupled-line 180 degrees hybrid structures.[21, 22]

Fig. 2.24 shows a 1-GHz current-switching Class-D power amplifier using LDMOSFET devices.[23] The input and output baluns are represented by the 180 degrees rat-race hybrids built on a high-dielectric substrate to minimize the physical size. The input matching circuits are added between the input of each transistor and hybrid to reduce the input return loss. The *LC* resonator was designed by converting the ideal inductor *L* and capacitor *C* to a real microstrip line and parallel capacitor. The power amplifier begins operating in a switching mode beyond 25-dBm input power. As a result, a maximum output power of 13 W was observed with a drain efficiency of 60% and power gain of 14 dB.

2.9 Class-D for digital pulse-modulation transmitters

Voltage-switching (or voltage-mode) Class-D power amplifiers with a series filter are attractive candidates for digital RF transmitters based on a delta-sigma modulator (DSM) for linear and efficient amplification. In this case, the output switched voltage waveform is applied to a series fundamentally tuned filter, which exhibits a high impedance at all frequencies except for the resonant fundamental frequency, thus removing the out-of-band signals such as harmonics and quantization noise. Taking into account that no current flows outside of the desired frequency band, no power is dissipated at these frequencies. Because the transistors are switched alternately, a voltage-switching Class-D amplifier can be approximated as a voltage-controlled voltage source, which operates effectively when feeding a series resonator. This high-efficiency level can be maintained even if it is driven by nonperiodic digital signals, as long as the reverse currents appearing in this condition can be provided by the transistors or parallel diodes when they are turned on. A simple series resonator is usually sufficient for periodic driving signals because the spectrum is discrete with widely spaced harmonics. However, for a broadband power spectrum such as bandpass DSM, a higher-order filter is required to properly attenuate the quantization noise.

In CMOS voltage-switching Class-D power amplifiers, during the on-to-off transition of the devices, there is generally a short period of time when both pMOS and nMOS transistors are turned on, resulting in a low resistance between the power supply and the ground. In this case, a large drain current (known as a shoot-through current) may be induced, which can cause significant energy loss. To minimize this loss, the pMOS and nMOS transistors are designed to have different driving circuits, as shown in Fig. 2.25A.[24] By modifying the pull-up and pull-down device size ratio of the drivers, the overlap of the turn-on time between the pMOS device and the nMOS device during the transition can be minimized.

A voltage-switching Class-D power amplifier is suitable for digital transmitters employing two-level DSM signals (levels 1 or 0). In a simplified case for a half-bridge voltage-switching Class-D power amplifier shown in Fig. 2.25B, the driving signal states correspond to the two states of the Class-D amplifier operation. For example, level 1 corresponds to turn-on mode of the switch S_1 and turn-off mode of the switch S_2. At the same time, level 0 corresponds to turn-off mode of the switch S_1 and turn-on mode of the switch S_2. However, a single Class-D power amplifier is unable to differentiate the three driving states associated with three-level DSM signals. Therefore two voltage-switching Class-D power amplifiers can be configured in a full-bridge scheme shown in Fig. 2.25C, with two pairs of switches to produce three different driving conditions. For example, level 1 corresponds to conditions when switches S_{11} and S_{22} are turned on and switches S_{12} and S_{21} are turned off, level -1 corresponds to conditions when switches S_{11} and S_{22} are turned off and switches S_{12} and S_{21} are turned on, and level 0 corresponds to conditions when switches S_{11} and S_{21} are turned off and switches S_{12} and S_{22} are turned on. The output combining circuit is composed of two quarter-wavelength transmission lines connected in series to the outputs of each Class-D amplifier and required for impedance transformation and a quarter-wavelength coaxial-line balun connected to the load. For CDMA IS-95 signals at 800 MHz, the drain efficiency can be increased from 31% to 33% at an output power of 15 dBm for three-level DSM with an adjacent-channel power ratio of -43 dBc.[24] By reducing the capacitance associated with the transistors resulting in a shorter transition time, an amplifier efficiency can be improved significantly, especially in a low-power region. A full-bridge switching power amplifier suited as a driver for a high-power GaN HEMT amplifier in a Class-S transmission scheme, which can be operated with a pseudo-random digital pulse train up to 7.5 Gbit/s, can be implemented using a 0.25-μm SiGe BiCMOS technology.[25]

Although the out-of-band spectral components do not dissipate any power in an ideal Class-D circuit, a high level of out-of-band spectral power is wasteful and reduces the utility of the pulse train to generate the load power. Significant out-of-band power is generated by one-bit quantization, and coding efficiency is introduced as a figure of merit to evaluate an encoder performance. The coding

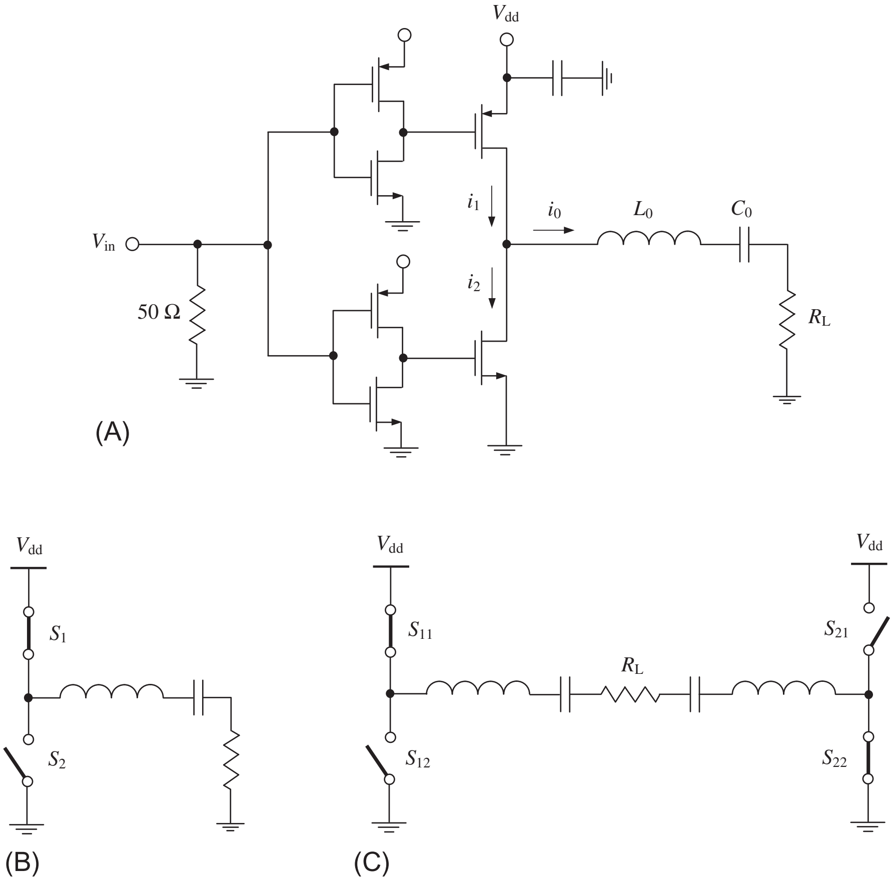

FIG. 2.25

Schematics of CMOS voltage-switching Class-D power amplifiers.

efficiency η_{code} is defined as the ratio of the reconstructed load power relative to the total pulse-train power and can be written as

$$\eta_{\text{code}} = \frac{8}{\pi^2}\sin^2(\pi D), \tag{2.101}$$

where D is the duty ratio.[26] The coding efficiency is maximized with a duty ratio of 50% when equal to $8/\pi^2 \approx 81\%$, as in Eq. (2.29). In this case, the further efficiency degradation owing to the device saturation resistance r_{sat}, which is equivalently connected in series to each ideal switch, can be determined by

$$\eta = \frac{1}{1 + \dfrac{4}{\eta_{\text{code}}}\dfrac{r_{\text{sat}}}{R_L}}, \tag{2.102}$$

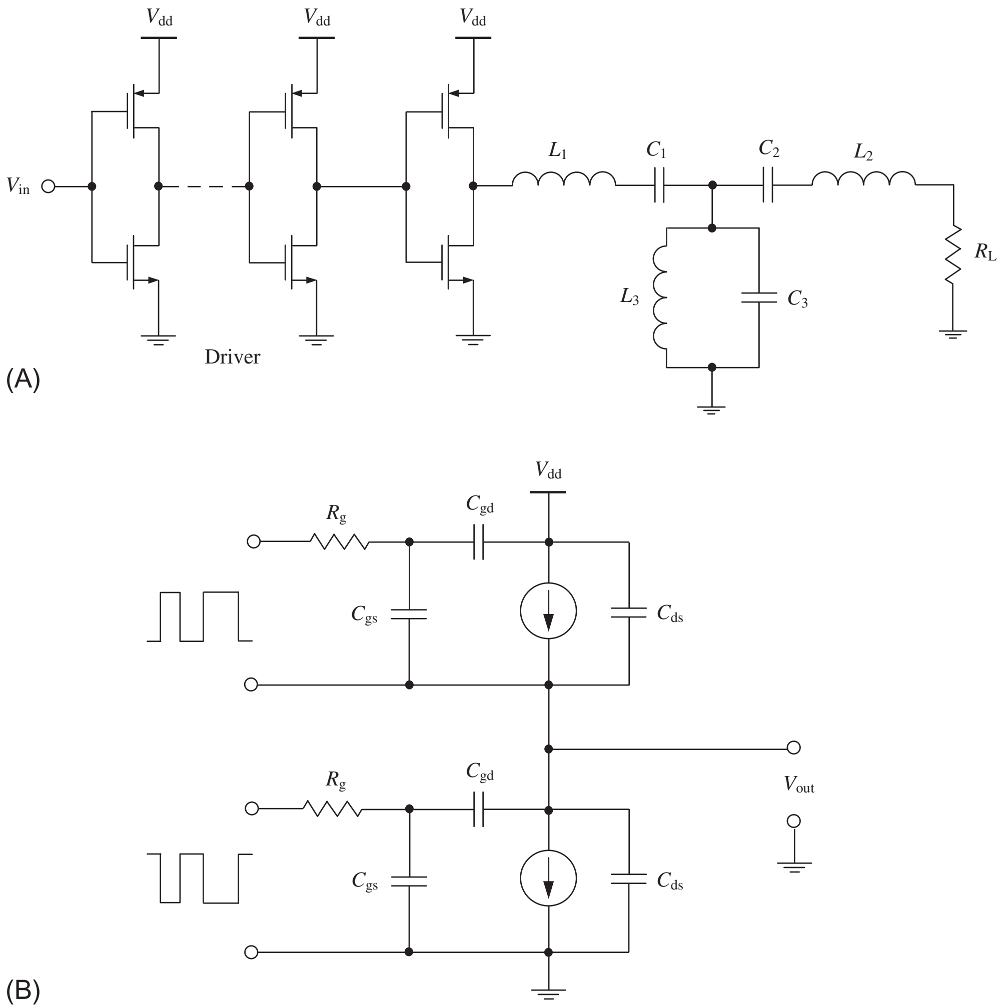

FIG. 2.26

CMOS voltage-switching Class-D power amplifier modeling.

where R_L is the load resistance.[27]

Fig. 2.26A shows a 0.5-μm CMOS amplifying path consisting of a multistage driver and a complementary voltage-switching Class-D power amplifier driven with a bandpass DSM signal.[28] The multistage driver consisting of five inverters of increasing gate width is necessary to provide enough current to drive the gate capacitances of the Class-D power amplifier. The Class-D amplifier stage consisting of two complementary switches could deliver above 50 mW of output power with a drain efficiency of about 32% for a WCDMA signal at 181 MHz with a DC supply voltage of 3.3 V. The switches of the Class-D power amplifier have a large gate width to minimize the channel resistance when the switches are turned on. As a result, the power dissipation in the Class-D switches consists of both capacitive switching power losses and ohmic conductive power losses for the load current. The output pulse train signal is filtered by a sixth-order Butterworth bandpass reconstruction filter with a 3-dB bandwidth of 10 MHz.

Fig. 2.26B shows the complementary voltage-switching Class-D amplifier circuit, where each of two switches is modeled by a current source, a gate resistance R_g, and three intrinsic capacitances C_{gs}, C_{gd}, and $C_{ds.}$[26] Both capacitances C_{gs} and C_{gd} are considered nonlinear capacitances that are highly nonlinear when the switch is turned on and relatively constant when the switch is turned off, while the capacitance C_{ds} is modeled as a linear capacitance. An analysis of energy loss from parasitic capacitances shows that the gate-drain capacitance C_{gd} is the dominant parasitic and has the largest change in stored energy. When the switch is turned on, the voltage across the capacitances is relatively small and the stored energy is small, even though the nonlinear capacitances C_{gs} and C_{gd} are large in the on-state. In the off-state mode, the nonlinear capacitances are small, but the voltage is large, and the stored energy is much larger since the stored energy is proportional to the square of the voltage. As a result, it was shown for the driving pulse train with a modulator sample rate of 1.5 GHz at a carrier frequency of 500 MHz and the load signal flowing through a 15-MHz six-order reconstruction filter that the noise floor of the reconstructed signal with linear models for the capacitances of the 1-mm pHEMT switches is dependent only on the modulator noise floor. At the same time, when the switch has the nonlinear resistance characteristic of a pHEMT in the on-state, significant distortion is introduced by the power amplifier when the signal-noise ratio (*SNR*) is reduced by about 30 dB. The *SNR* is reduced a further 10 dB when the full nonlinear device circuit model with nonlinear capacitances is used. The drain efficiency, including the conductive losses, switching losses, and filter insertion loss of 0.5 dB for a WCDMA signal with a peak-to-average ratio (*PAR*) of 7.1 dB, reduces from approximately 60% at 500 MHz through 50% at 1 GHz to less than 40% at 2 GHz. Generally, improvements in efficiency could be obtained by providing better coding efficiency or using better devices with lower on-resistance, lower gate-drain capacitances, and high breakdown voltages.

The use of external lumped inductors to drive the push-pull final GaN HEMTs can drastically reduce the dissipated DC power so that the overall efficiency of the power amplifier could be significantly improved. Fig. 2.27A shows the circuit schematic of a voltage-mode Class-D power amplifier, including a three-stage 0.25-μm GaN MMIC with connected external DC-fed inductors L_1 and L_2 and a lumped output network.[29] The three-stage circuit includes two common-source transistors (1) at the input, which are fed differentially with a digital bit sequence through input terminals 1 and 2, followed by a differential stage (2), and the final stage (3) consists of two GaN HEMTs with a gate width of 4 × 250 μm each in a push-pull configuration, switching the output voltage on and off between V_{DD} and 0 V. Because no complementary GaN HEMTs are available, different voltage swings need to be generated at the input of the final-stage transistors. In particular, a high voltage swing between −5 V and V_{DD} (max 40 V) is required at the gate of the upper transistor T_1, whereas a comparatively small voltage swing from −5 to 1 V is required at the input of the transistor T_2. The transistors T_{D3} and T_{D4} in the differential stage are biased with a constant voltage without using any resistors, which allows to reduce the DC power consumption. The lumped output network used to filter out the signal frequency of 800 MHz from the amplified bit stream consists of two series *LC* resonant circuits with inductor quality factors of about 70 and self-resonant frequency (*SRF*) of 5.4 GHz. As a result, the final-stage drain efficiency could demonstrate the value around 80% over the whole range of

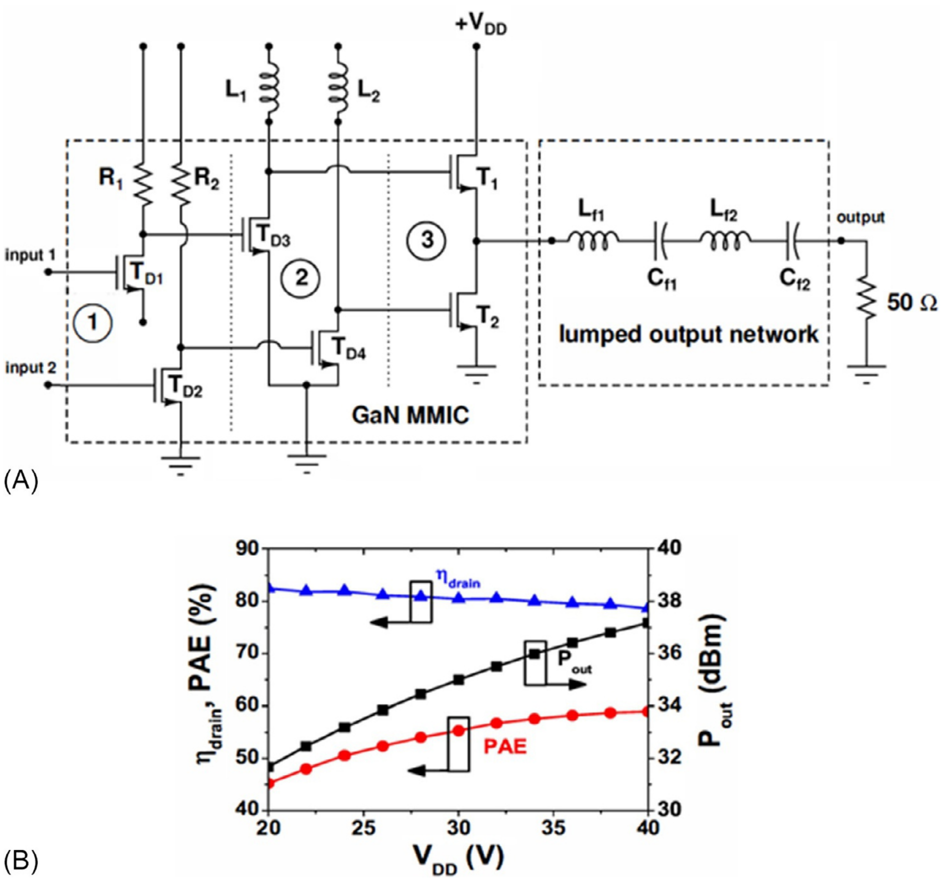
+VDD
L1
L2
R1
R2
T1
TD3
input 1
TD1
1
2
3
Lf1
Lf2
output
Cf1
Cf2
50 Ω
T2
lumped output network
input 2
TD4
TD2
GaN MMIC
(A)
ηdrain, PAE (%)
90
80
70
60
50
40
ηdrain
Pout
PAE
40
38
36
34
32
30
Pout (dBm)
20
25
30
35
40
VDD (V)
(B)

FIG. 2.27

Circuit schematic of voltage-mode Class-D power amplifier with external lumped output network and its measured performance.[29]

DC-supply voltages, with a maximum *PAE* of 59% and an output power of 5.2 W at $V_{DD} = 40$ V, as shown in Fig. 2.27B, with a power gain of 20.2 dB.

Fig. 2.28 shows the circuit schematic of a four-stage voltage-mode 0.25-μm Class-D power amplifier with two digital inputs, where the differential input signal feeds two cascaded common-source pre-driver stages.[30] Here, the bridging capacitor C_1 improves the slew rate of the differential signals, whereas the use of the external inductor L_1, on-chip inductor L_2, and feedback circuit (C_2R_7) improves the overall efficiency. With external lumped output filter having a high loaded quality factor, a drain efficiency of 82% and an output power of 37.9 dBm were achieved at $V_{dd} = 50$ V in the 800-MHz band. The high drain efficiency remains over a wide range of the output powers, reducing to 47% at 10.2-dB power backoff. Two of these GaN MMICs combined in an H-bridge Class-D power amplifier could

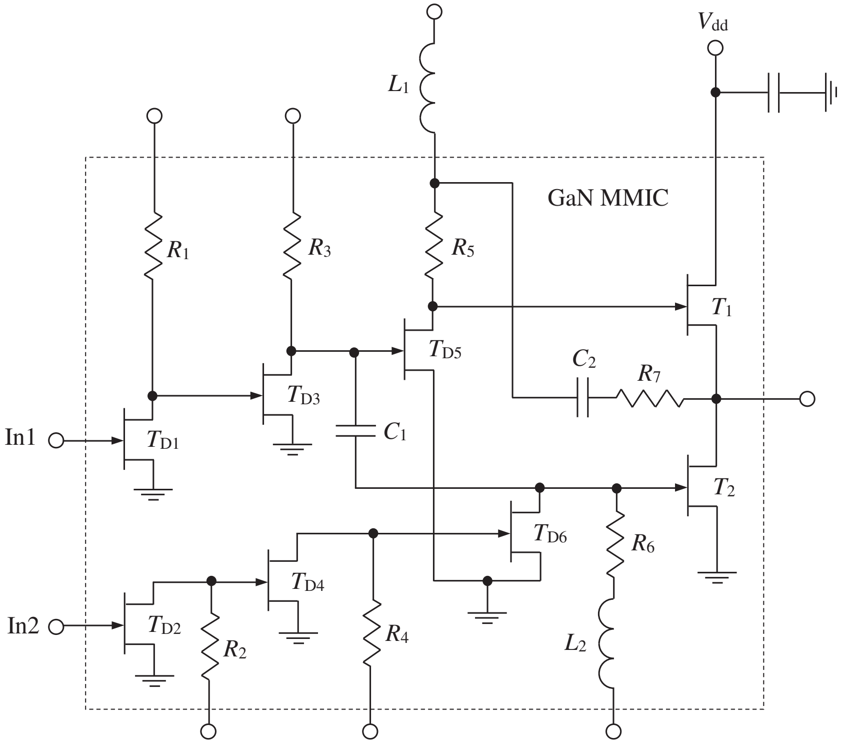

FIG. 2.28

Circuit schematic of digital GaN HEMT voltage-mode Class-D power amplifier.

deliver the maximum output power of 14 W with a final-stage drain efficiency of 69%, while maintaining above 60% to 7.5-dB power backoff with a *PAE* in the 35%–45% range.[30, 31]

To further improve the backoff efficiency of a voltage-mode Class-D power amplifier, a three-level Class-D architecture shown in Fig. 2.29A can be used.[32] Here, an auxiliary switch M_3 is added to the main top switch M_2 in parallel, and the supply voltage V_{DD_L} applied to M_3 is set lower than the supply voltage V_{DD_H} for M_2. Such a configuration of a Class-D power amplifier can provide a three-level output pulse train, or a so-called 1.5-bit operation, as opposed to the conventional 1-bit operation. In this case, when the output power is small, a complimentary pulse signal with a lower switching rate f_{M1-M3} is fed to the transistor M_3, whereas the transistor M_2 is off. However, at the maximum output power, the transistors M_1 and M_2 compose a Class-D power amplifier with a switching rate f_{M1-M2} equal to the carrier frequency. Generally, the output power is controlled by the ratio of f_{M1-M2} and f_{M1-M3}. This allows to reduce the total power loss due to lower effective parasitic capacitance of the switches at the output common node. The measured drain efficiency of a three-level Class-D power amplifier implemented in a 0.25-μm GaN HEMT process versus output power when V_{DD_H} is fixed to

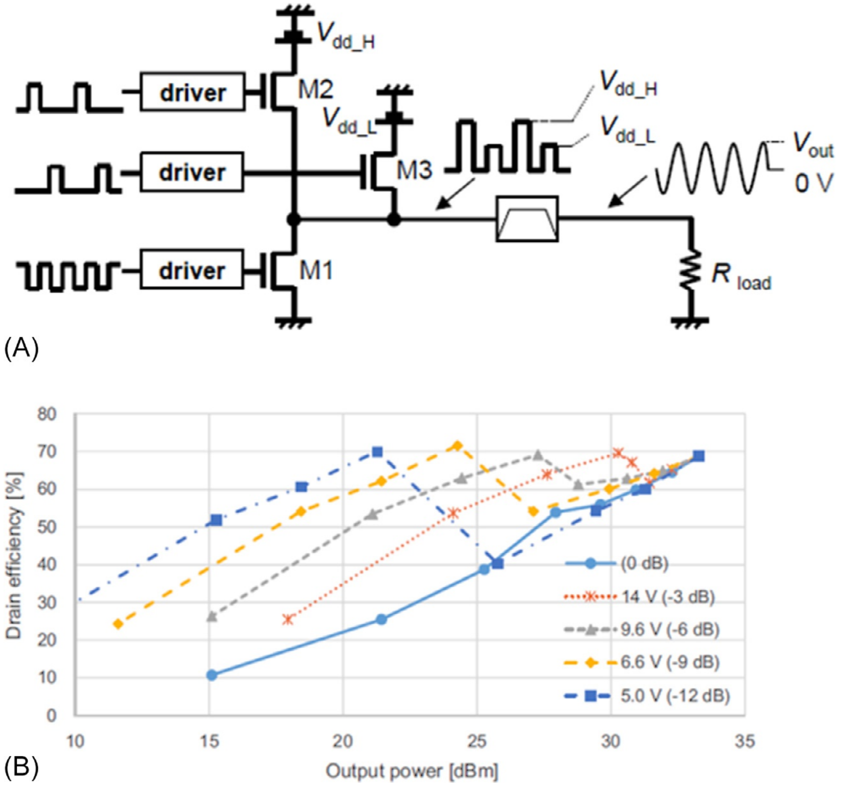

FIG. 2.29

Circuit schematic of three-level voltage-mode Class-D power amplifier and measured drain efficiencies.[32]

22 V is shown in Fig. 2.29B. A maximum drain efficiency of 68.7% at a maximum output power of 2.1 W (33.2 dBm) and a drain efficiency of 71.6% at 9-dB power backoff were measured in the 700-GHz band.

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CHAPTER

Class-F power amplifiers

3

A highly efficient operation of a power amplifier (PA) can be obtained by applying biharmonic or polyharmonic modes when an additional single-resonant or multiresonant circuit tuned to the odd harmonics of the fundamental frequency is added into the load network. An infinite number of odd-harmonic resonators results in an idealized Class-F mode with a square voltage waveform and a half-sinusoidal current waveform at the device output terminal. In Class-F PAs analyzed in the frequency domain, the fundamental and harmonic load impedances are optimized by short-circuit termination and open-circuit peaking to control the voltage and current waveforms at the device output to obtain maximum efficiency. In this chapter, different Class-F techniques using lumped and transmission-line elements, including a quarterwave transmission line, are analyzed. The effect of the saturation resistance and parasitic shunt capacitance is demonstrated. The design examples and practical radio frequency (RF) and microwave Class-F PAs are described and discussed.

3.1 History of biharmonic and polyharmonic operation modes

The possibility of improving efficiency of vacuum-tube PAs by a proper approximation of the anode voltage and current waveforms had been discussed by the early 1920s.[1,2] It was concluded that, theoretically, three-electrode tubes constitute converters of direct current to alternating current having generally unforeseen efficiencies. This means that, for different waveforms, anode efficiency will be different. For example, it may change from 50% for a purely sinusoidal anode current to 100% for rectangular pulses. Under operation with the conduction angle of 180 degrees, corresponding to Class-B operation mode, the maximum theoretical anode efficiency achieves $\pi/4$ or 78.5%, characterized by the sinusoidal anode voltage waveform and half-sinusoidal current waveform.

One of the commercial companies who played a significant role in the development of high-efficiency radio transmitters was Telefunken in Germany, where the first vacuum-tube transmitters of small power up to 15 W were built at the beginning of 1915. To provide high operating efficiency of the transmitter, the special waveform should be produced on the anode of the vacuum tube (proposed by Hans Rukop) or else an auxiliary voltage of triple frequency should be impressed on the grid (proposed by Alexander Meissner).[3] In both cases, the tube losses are greatly reduced because during the operation of the tube, the time during which the highest voltages are applied to the tube is reduced, and, furthermore, because at the time when the highest voltages are applied to the tube, the passage of current through it is prevented.

The possibility to maximize efficiency was first demonstrated by a suitable choice of grid voltage with a corresponding anode arrangement to produce an anode current or a voltage waveform that is

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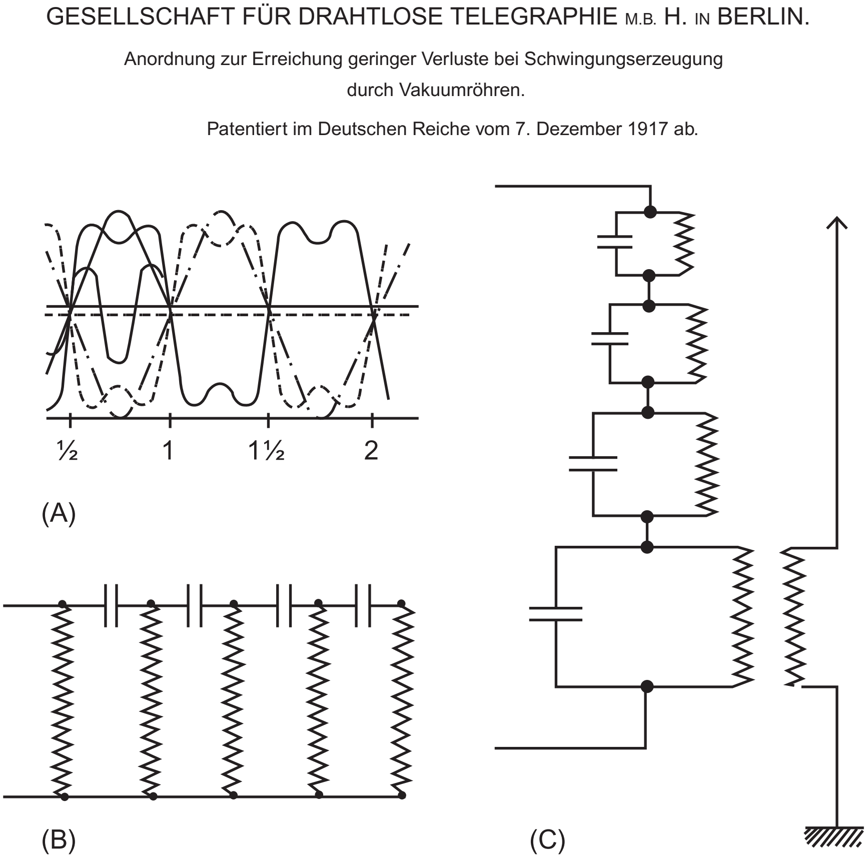

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FIG. 3.1

Waveforms and multiresonant load networks.

composed principally of the fundamental frequency and the third harmonic and has a “Meander”-like form, as shown in Fig. 3.1A.[4, 5] The third harmonic is added to the fundamental-frequency component, and both amplitudes are correctly dimensioned by suitable values of high resistances. As a result, such a combination of the fundamental and third-harmonic components, being 180 degrees out of phase at the center point, results in a flattened voltage or current waveform with depression in its center. This means that the power loss on the device is partly compensated by the reactive power provided by the harmonic resonator. What is shown for the fundamental frequency and the third harmonic is equally valid for the other harmonics. The load network can be designed as a ladder-type high-pass circuit, as shown in Fig. 3.1B, or with multiple resonators, each tuned to the corresponding harmonic, as shown in Fig. 3.1C. As a result, the power loss must be zero and the efficiency equal to 100% if either the tube current or voltage is always zero with meander-type shapes. The means for producing such curves consist of employing resonators in the anode circuit to include not only the fundamental frequency but also a considerable number of higher-order harmonic components. The shapes of the anode voltage and current waveforms can be significantly flattened with increasing fundamental voltage amplitude by adding even one additional harmonic component being properly phased.

Independently, it was suggested by Henry Round based on his experiments with a variety of different aspects of radio transmitter technology at Marconi and RCA to use a square voltage driving waveform and an additional resonator tuned to the fifth harmonic for efficiency improvement of vacuum-tube amplifiers, as shown in Fig. 3.2.[6] Consequently, the basic theoretical background and potential circuit solutions to increase the efficiency of vacuum-tube amplifiers were generally understood about 100 years ago.

In real practical PA design, especially at high frequencies and low supply voltage, the efficiency significantly degrades. Therefore some design solutions contributing to the efficiency improvement were published a long time ago with regard to the vacuum-tube PAs and were based on the harmonic tuning at the anode of the active device. To understand the basic approach, a contribution of each harmonic component to ideal half-sinusoidal current waveform and square voltage waveform is evaluated by using a Fourier-series analysis. In this case, it is useful to calculate the partial Fourier series of current $i(\omega t)$ and voltage $v(\omega t)$ in normalized forms according to.

$$\frac{i(\omega t)}{I_0} = 1 - \frac{\pi}{2}\sin\omega t - 2\sum_{n=2,4,6,\ldots}^{N} \frac{\cos n\omega t}{n^2 - 1}, \tag{3.1}$$

$$\frac{v(\omega t)}{V_0} = 1 + \frac{4}{\pi}\sin\omega t + \frac{4}{\pi}\sum_{n=3,5,7,\ldots}^{N} \frac{\sin n\omega t}{n}, \tag{3.2}$$

where I_0 and V_0 are the DC current and voltage components, respectively.

Fig. 3.3 shows that the shapes of the voltage and current waveforms can be significantly changed with increasing fundamental voltage amplitude by adding even one additional harmonic component with a proper phase. For example, the combination of the fundamental and third-harmonic components, being 180 degrees out of phase at the center point, results in a flattened voltage waveform with

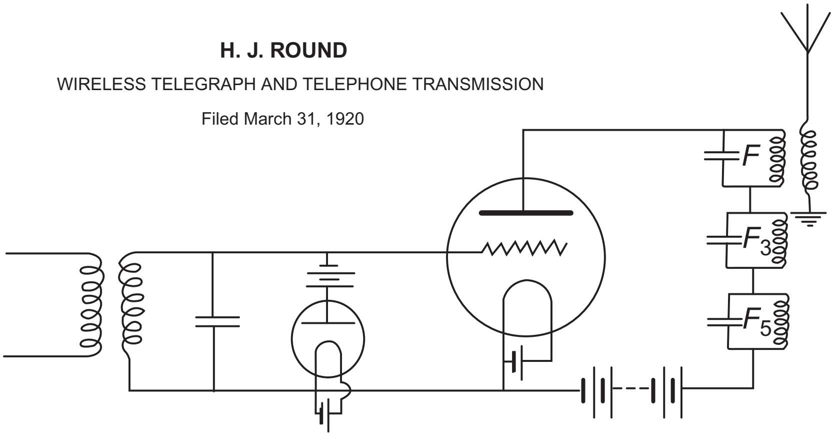


FIG. 3.2

Schematic of a vacuum-tube amplifier with harmonic traps.

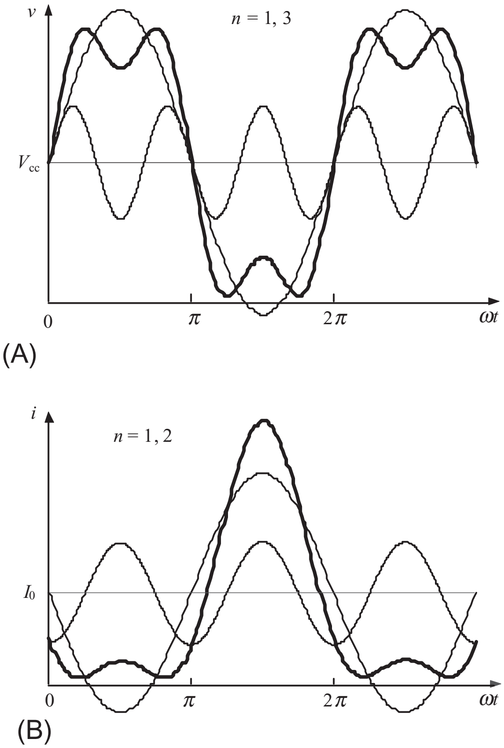


FIG. 3.3

Fourier voltage and current waveforms with the third and second harmonics.

depression in its center. It is clearly seen from Fig. 3.3A that the proper ratio between the amplitudes of the fundamental and third-harmonic components can provide the flattened voltage waveform with minimum depression and maximum difference between its peak amplitude and amplitude of the fundamental harmonic. Similarly, the combination of the fundamental and second-harmonic components, being in phase at the center point, flattens the current waveform corresponding to the maximum values of the voltage waveform and sharpens the current waveform corresponding to the minimum values of the voltage waveform, as shown in Fig. 3.3B. The optimum ratio between the amplitudes of the fundamental and second current harmonic components can maximize a peak value of the current waveform with its minimized value determined by the device saturation resistance in a practical circuit. Thus power loss due to the active device can be minimized because the results of the integration over the period when minimum voltage corresponds to maximum current will give a small value when compared with the power delivered to the load. In a common case, the same result can be achieved by adding the second harmonic into the voltage waveform and the third harmonic into the current waveform, resulting in an inverse operation mode.

Ideally, the half-sinusoidal current waveform does not contain the third-harmonic component, as it follows from Eq. (3.3), because its third-harmonic Fourier current coefficient $\gamma_3(\theta)$ is equal to zero.

However, a load line analysis of a Class-B PA with sinusoidal output voltage waveform—under overdriven condition when device operates in pinch-off, active, and saturation modes during the entire period—shows that operation in the saturation mode is characterized by a depression in the output current waveform. From Fourier analysis, it follows that such a current waveform includes the third harmonic component, which is 180 degrees out of phase with the fundamental component at the point of symmetry of $\omega t = \pi/2$. Therefore when an additional resonant circuit tuned to the third harmonic is included in the anode circuit operating in a saturation mode, the voltage drop with opposite phase will appear across this resonant circuit, resulting in a similar depressed voltage waveform, as shown in Fig. 3.3A by a solid line. Hence for the increased fundamental voltage amplitude, the output power at the fundamental frequency and anode efficiency can be increased for the same input drive. Physically, an efficiency improvement can be explained by the fact that the fundamental voltage or current has negative values during some part of the period, corresponding to the negative power as an integration of a product of the instantaneous fundamental voltage and current. This means that the power loss on the active device is partly compensated by the reactive power provided by the harmonic resonator.

Adding the one or more higher-order harmonic components can further improve the voltage or current waveform. Fig. 3.4A shows the voltage waveform with third- and fifth-harmonic peaking, which is close to an ideal rectangular waveform, while Fig. 3.4B shows the current waveform with second- and fourth-harmonic peaking, which is close to an ideal half-sinusoidal waveform.

Thus based on the results of a Fourier analysis, it was concluded at that time that efficiency and output conditions may be changed substantially if the load network is made to be responsive to certain harmonics, so that all input on this harmonics need not be absorbed as a tube loss. Fig. 3.5A shows the type of a load network with a third-harmonic trap that was discussed and first published in 1923 as a journal paper dedicated to a vacuum-tube oscillator.[7] At the same time, it was experimentally found that applying the biharmonic driving signal containing the fundamental and second-harmonic components produces the signal amplification more efficiently because of the much steeper driving waveform.[8] In this case, the resultant driving waveform consists of the fundamental and second-harmonic components being in phase at their maximum amplitudes, as shown in Fig. 3.3B, with the

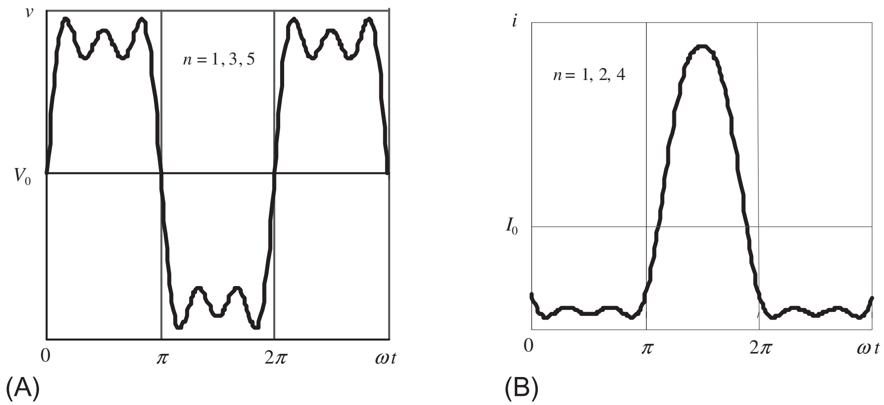


FIG. 3.4

Fourier (A) voltage and (B) current voltage waveforms with three harmonics.

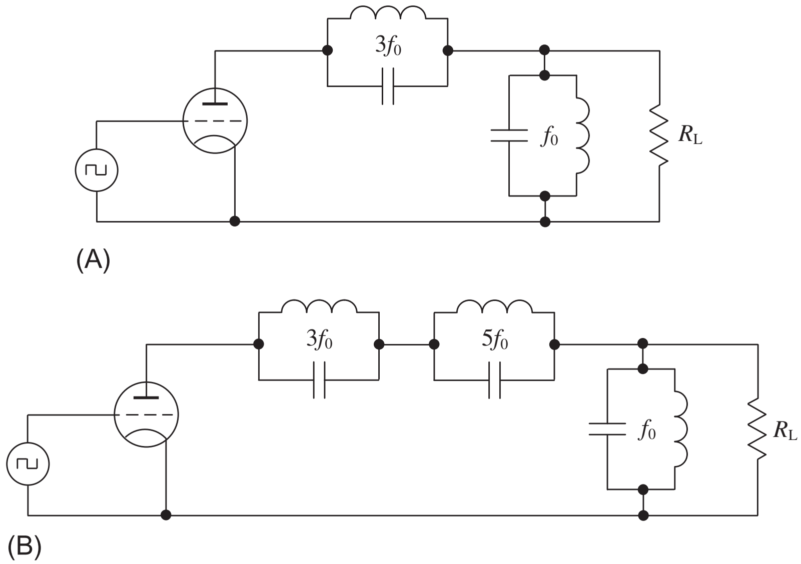


FIG. 3.5

Biharmonic and polyharmonic PAs with even-harmonic resonant tanks.

amplitude of the second harmonic chosen as approximately one-quarter the amplitude of the fundamental. Fig. 3.5B shows the basic circuit schematic of the vacuum-tube amplifier using an additional resonator tuned to the fifth harmonic. The effect of the inclusion of the parallel resonant circuit tuned to the third-harmonic component and located in series to the anode was later described in a textbook.[5] Consequently, the basic theoretical background and potential circuit solutions to increase the efficiency of vacuum-tube PAs and oscillators were generally understood already in the 1920s.

Nevertheless, in the next few decades, the basic operation mode for the vacuum tubes in PAs of the amplitude-modulated broadcasting radio transmitters was Class-B, with a resonant tank tuned to the fundamental. In this case, to improve the efficiency, different transmitter architectures were proposed, based on Chireix and Doherty PAs. However, during the 1930s, some Russian papers stating an efficiency improvement of 25%–30% in broadcasting radio transmitters by using a biharmonic mode for PAs were published. It was shown that the symmetrical anode voltage waveform and minimum level of its depression for a biharmonic PA shown in Fig. 3.3A can be provided with opposite phase conditions between the fundamental and third harmonic and optimum value of the ratio between their voltage amplitudes. Besides, it was noted that a high efficiency can be achieved even when impedance of the third-harmonic resonator is equal or slightly greater than impedance of the fundamental tank circuit. In addition, such an approach can slightly improve the modulation properties of the PA using either grid or anode modulation techniques because saturation for the fundamental frequency as a part of the flattened anode voltage waveform occurs later than that for the sinusoidal anode voltage.[9]

In the comprehensive research given in Ref. 10 it was confirmed that the second- or third-harmonic voltages introduced into the anode or grid circuits with the proper phase improve the vacuum-tube performance. The proper phasing can be done by various means, including an auxiliary tube, and the power output and overall efficiency of the main tube acting as a Class-C PA are increased. Fourth- and higher-order harmonics were at best of a little value in improving the path of operation. However, in view of the parasitic anode-cathode capacitance comprising the interelectrode and case capacitances and series plate inductance, the entire anode circuit should be tuned to the third harmonic, not only a single resonator. For example, such an anode circuit may include a parallel third-harmonic resonator, which is slightly mistuned in this case, and an additional series *LC* circuit connected in parallel to the tube, which has a capacitive reactance at the fundamental frequency and inductive reactance at the third-harmonic component tuned to the resonance with other elements in the anode circuit.[11]

The parallel resonator in the load network tuned to the third harmonic can be replaced by a low-pass filter with two series inductors and a shunt capacitor, as shown in Fig. 3.6A, designed to pass the third harmonic of the fundamental frequency, terminating in a parallel resonant circuit tuned to the fundamental.[12] In this case, the ratio between the series inductor $L/2$ and shunt capacitor C can be chosen to resonate the third-harmonic component $\omega = 3\omega_0 = \sqrt{2}/\sqrt{LC} = \omega_c/\sqrt{2}$, where $\omega_c = 2/\sqrt{LC}$ is the filter cutoff frequency, thus providing ideally infinite impedance seen by the device anode at the third harmonic when it is assumed an infinite quality factor for the parallel fundamentally tuned resonant circuit. The parallel resonators tuned to the third and fifth harmonics can be replaced by a three-section low-pass filter, as shown in Fig. 3.6B, whose elements are designed to pass the third and fifth harmonics of the fundamental frequency, terminating in a parallel resonant circuit tuned to the fundamental.[12] However, it is difficult to correctly specify the impedances at these harmonics seen by the anode circuit. This may result in a situation when a square-top anode voltage waveform cannot maintain its form in a circuit having inductive or capacitive reactance or both, even though, in the latter case, the reactive elements are so chosen that the circuit would be resonant for any one of the three frequencies, including

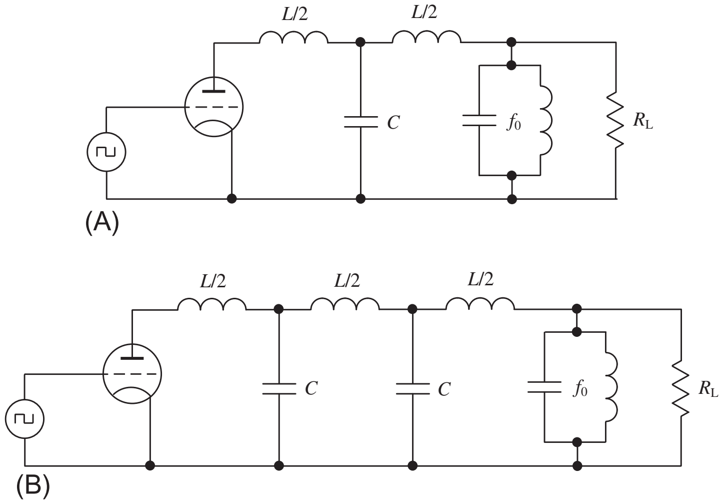


FIG. 3.6

Biharmonic and polyharmonic vacuum-tube PAs with low-pass filters.

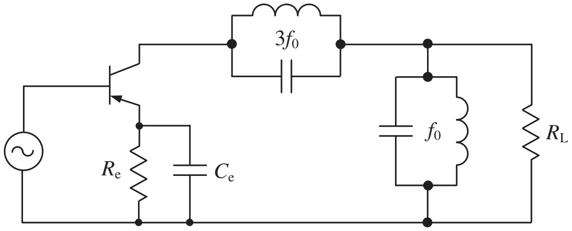


FIG. 3.7

Biharmonic bipolar-transistor PA.

the fundamental component. The reactances cause phase shifting of the component waves with subsequent distortion of the resultant wave and loss of efficiency.

Fig. 3.7 shows the biharmonic bipolar transistor PA with an additional resonant tank in the load network tuned to the third harmonic.[13] Because the third-harmonic current coefficient $\gamma_3(\theta)$ is positive for $\theta < 90$ degrees, it is necessary to operate partly in a slightly saturated mode to obtain $\gamma_3(\theta) < 0$. Besides, higher efficiency can be achieved in a Class-C with smaller half-conduction angle θ that can easily be provided by the emitter RC circuit. As a result, an output power of about 300 mW with a collector efficiency of 88% was achieved at the operating frequency of 106 kHz. It was then noted that an ideal solution requires the switchmode amplifying circuit when the current flows through the device at minimum collector voltage (switch is turned on), but the current is zero at maximum collector voltage (switch is turned off).

In practice, the effective driving waveform may differ from the idealized square wave depending upon what types of the harmonic resonators are used in the load network.[14] For example, applying the biharmonic driving signal containing the fundamental and second-harmonic components produces the signal amplification more efficiently because of the much steeper driving waveform.[8] The detailed mathematical explanation of the effect of the biharmonic driving signal consisting of the fundamental and third-harmonic components is given in Refs.[15, 16] Fig. 3.8 shows the simplified circuit of a vacuum-tube PA containing the tank and third-harmonic resonant circuits, both located in grid and anode circuits.

Consider the effect of the biharmonic input signal on the MOSFET transistor, whose simplified equivalent circuit is represented by an ideal voltage-controlled current source with transconductance g_m only. The biharmonic signal in the voltage form can be written as

$$v_g(\omega t) = V_g + V_{g1}(\cos\omega t - a_n \cos n\omega t), \tag{3.3}$$

where V_g is the gate bias voltage, and $a_n = V_{gn}/V_{g1}$ is the coefficient of nth harmonic injection.

By substituting Eq. (3.3) into the idealized device piecewise-linear transfer characteristic, an output current is written as

$$i(\omega t) = g_m\left(v_g - V_p\right) = I_0 + g_m V_{g1}(\cos\omega t - a_n \cos n\omega t), \tag{3.4}$$

where $I_0 = g_m(V_g - V_p)$ is the DC current and V_p is the device pinch-off voltage. The output current $i(\omega t)$ takes a zero value when $\omega t = \theta$, where θ is the half-conduction angle. Then,

$$I_0 = -g_m V_{g1}(\cos\theta - a_n \cos n\theta). \tag{3.5}$$

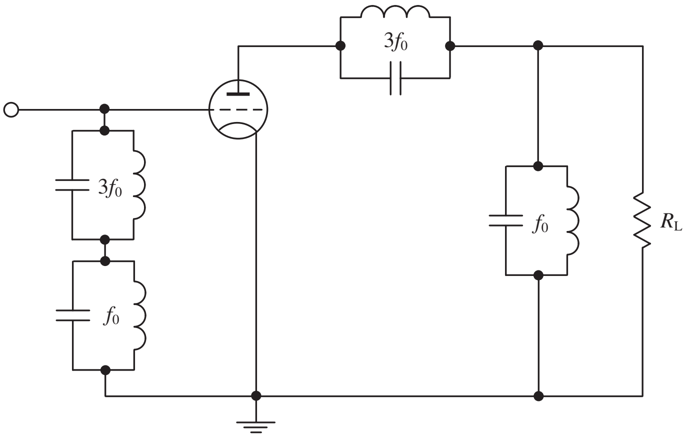


FIG. 3.8

Biharmonic PA with input harmonic control.

As a result, Eq. (3.4) can be rewritten in the form of

$$i(\omega t) = g_{\mathrm{m}} V_{\mathrm{g1}} [\cos\omega t - \cos\theta - a_n(\cos n\omega t - \cos n\theta)]. \tag{3.6}$$

In this case, the Fourier current-harmonic coefficients can be written as

$$\begin{aligned}\gamma_0'(\theta) &= \frac{1}{\pi}\left[\sin\theta - \theta\cos\theta + a_n\left(\theta\cos n\theta - \frac{\sin n\theta}{n}\right)\right] \\ &= \gamma_0(\theta) - \frac{a_n}{n}\gamma_0(n\theta),\end{aligned} \tag{3.7}$$

$$\begin{aligned}\gamma_1'(\theta) &= \frac{1}{\pi}\left[\theta - \frac{\sin 2\theta}{2} - na_n\left(\frac{\sin(n-1)\theta}{n-1} - \frac{\sin(n+1)\theta}{n+1}\right)\right] \\ &= \gamma_1(\theta) - n^2 a_n \gamma_n(\theta),\end{aligned} \tag{3.8}$$

$$\begin{aligned}\gamma_n'(\theta) &= \frac{1}{\pi}\left[\frac{\sin(n-1)\theta}{n(n-1)} - \frac{\sin(n+1)\theta}{n(n+1)} - a_n\left(\theta - \frac{\sin 2n\theta}{2n}\right)\right] \\ &= \gamma_n(\theta) - \frac{a_n}{n}\gamma_1(n\theta),\end{aligned} \tag{3.9}$$

where $\gamma_n(\theta)$ are the current-harmonic coefficients of an idealized Class-C PA with a single-carrier driving signal.

To compare the operation modes with the output sinusoidal voltage $v = V_{\mathrm{dd}} - V\cos\omega t$ and biharmonic voltage $v = V_{\mathrm{dd}} - V_1(\cos\omega t - a_n\cos n\omega t)$, where $a_n = V_n/V_1$, and V_{dd} is the DC supply voltage, consider the conduction angles and maximum output-current amplitudes to be equal. The latter condition implies that the minimum values of the saturation voltages for both cases are equal too, although appearing at different time moments depending upon the number of injected harmonic components. Then, the maximum drain voltage peak factor $\xi' = V_1/V_{\mathrm{dd}}$ in a biharmonic mode can be obtained by Ref. 15

$$\xi' = \frac{\xi}{\cos\dfrac{\pi}{2n}}, \tag{3.10}$$

where $\xi = V/V_{\rm dd}$ is the drain voltage peak factor corresponding to a cosinusoidal driving mode, when the voltage coefficient a_n takes an optimum value

$$a_n^0 = \frac{1}{n}\sin\frac{\pi}{2n}. \tag{3.11}$$

Generally, the drain efficiency η is written through the fundamental power P_1 and DC power P_0 in a single-carrier driving mode as.

$$\eta = \frac{1}{2}\frac{P_1}{P_0} = \frac{1}{2}\frac{V}{V_{\rm dd}}\frac{I_1}{I_0} = \frac{1}{2}\xi\frac{\gamma_1(\theta)}{\gamma_0(\theta)}. \tag{3.12}$$

By using Eqs. (3.7)–(3.12), the drain efficiency η' in a biharmonic mode can be calculated from

$$\eta' = \frac{1}{2}\frac{n^2}{\cos\dfrac{\pi}{2n}}\frac{\gamma_1(\theta) - n\gamma_n(\theta)\sin\dfrac{\pi}{2n}}{n^2\gamma_0(\theta) - \gamma_0(n\theta)\sin\dfrac{\pi}{2n}}\xi. \tag{3.13}$$

From Eq. (3.13), it follows that the drain efficiency in a biharmonic mode with third-harmonic injection ($n = 3$) in a Class-B bias condition with $\theta = 90$ degrees can achieve a value

$$\eta' = (0.85 - 0.86)\xi, \tag{3.14}$$

resulting in a maximum efficiency of 85%–86% in an ideal case of zero saturation voltage when $\xi = 1$. Similar efficiency improvement of about 8% compared with a cosinusoidal driving signal was achieved for the case of third-harmonic injection with $a_3 = 0.14$.[15] Moreover, the drain efficiency η' can be further improved by optimizing the conduction angle and voltage coefficient. For example, Eq. (3.14) can be rewritten as $\eta' = (0.95 - 0.96)\xi$ for optimum values $\theta_{\rm opt} \approx 63^\circ$ and $a_n^0 \approx 0.205$.[15]

However, it is difficult to achieve an optimum value of the voltage coefficient a_n in real practical conditions because its value significantly depends on the ratio between resonant circuit equivalent resistance R_n at nth harmonic component and equivalent resistance R_1 at fundamental frequency according to

$$a_n = \frac{V_n}{V_1} = \frac{I_n R_n}{I_1 R_1} = \frac{\gamma_n'(\theta) R_n}{\gamma_1'(\theta) R_1}. \tag{3.15}$$

From Eq. (3.15), it follows that, for a certain value of n and an optimum value of θ, the condition $a_n = a_n^0$ is satisfied with more accuracy for a greater ratio of $R_{\rm n}/R_1$. As a rule of thumb, it is enough to choose their ratio ≥ 10. In this case, the worsening of the drain efficiency η' will be equal to or less than 0.5%.

In previous input harmonic-control analysis, it was assumed that the active device represents an ideal voltage-controlled current source, which is a good approximation at sufficiently low frequencies for vacuum tubes or MOSFET devices. However, when using a high-frequency bipolar, MESFET, or high-electron-mobility transistor (HEMT) transistor as an active element, it is necessary to consider the significant nonlinearity of the device input capacitance. For example, the voltage-dependent input gate-source capacitance of a GaAs MESFET device can be modeled as a junction capacitance creating higher-order harmonics at the device input, each having a different phase. In this case, the proper relationships between amplitudes and phases of the harmonics at the transistor input are necessary to approximate the required symmetrical drain voltage and current waveforms.[17] The pseudomorphic high-electron-mobility transistor (pHEMT) device, in contrast to a conventional MESFET device, shows a very steep gradient in its gate-source capacitance versus gate-bias voltage. As a result, the efficiency enhancement up to 81% can be achieved for a microwave PA with ideal Class-F load network by input termination of all harmonics when input signal is purely sinusoidal compared with a nonterminated case with severely distorted input-voltage waveform.[18] This situation appears as the simplest and effective alternative to multiresonant input circuit, which is difficult to realize at very high frequencies in view of the device and circuit parasitics.

Generally, the biharmonic driving signal for the final stage is formed in preliminary amplifying stages by the proper harmonic tuning. However, if the driving signal source represents a sine-wave output voltage, the formation of the biharmonic driving signal can be done by subtracting the voltage of the harmonic component used in the anode circuit from the sinusoidal input voltage. Fig. 3.9A shows the biharmonic vacuum-tube PA, in which a low-reactance resonator compared with the anode resonator but tuned to the same third-harmonic frequency component is inserted into the cathode circuit.[14] The high degree of negative feedback developed makes it impossible for any significant third-harmonic current to develop, no matter what grid-voltage waveform is employed. In practice, with a sine-wave input correctly related in amplitude with the grid bias, the relative voltages developed between grid and cathode are self-adjusting to provide the flattened voltage waveforms.

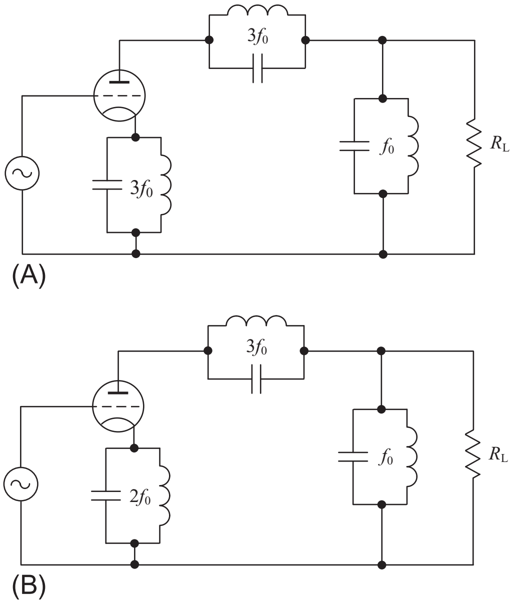


FIG. 3.9

Biharmonic PAs with cathode harmonic control.

Unfortunately, it is not always easy to realize the proper amplitude conditions because of the finite losses associated with two third-harmonic resonators because both resonators affect the voltage waveforms in the grid and anode circuits simultaneously. For example, the tubes with variable, weak, and small grid current characteristics cannot be used for such a biharmonic configuration. The effect of this problem can be significantly minimized if the resonant circuit in the cathode circuit tuned to the second harmonic together with a third-harmonic resonant circuit in the anode circuit is used, as shown in Fig. 3.9B, resulting in the input biharmonic voltage $v_g = V_{g1}\cos\omega t - V_2\cos 2\omega t$ and output voltage $v = V_1\cos\omega t + V_2\cos 2\omega t - V_3\cos 3\omega t$.[15] In this case, the maximum available anode efficiency can reach values of 85%–88%.

3.2 Idealized Class-F mode

Generally, an infinite number of odd-harmonic tank resonators can maintain a square voltage waveform with a half-sinusoidal current waveform at the device output. Fig. 3.10A shows such a Class-F PA with a multiple-resonator output filter to control the harmonic content of its collector (anode or drain) voltage and/or current waveforms, thereby shaping them to reduce dissipation and to increase efficiency.[19, 20]

To simplify an analysis of a Class-F PA, a simple equivalent circuit of which is shown in Fig. 3.10B, the following several assumptions are introduced:

- Transistor has zero saturation voltage, zero saturation resistance, and infinite off-resistance, and its switching action is instantaneous and lossless.
- RF choke allows only a DC current and has no resistance.
- Quality factors of all parallel resonant circuits have infinite impedance at the corresponding harmonic and zero impedance at other harmonics.

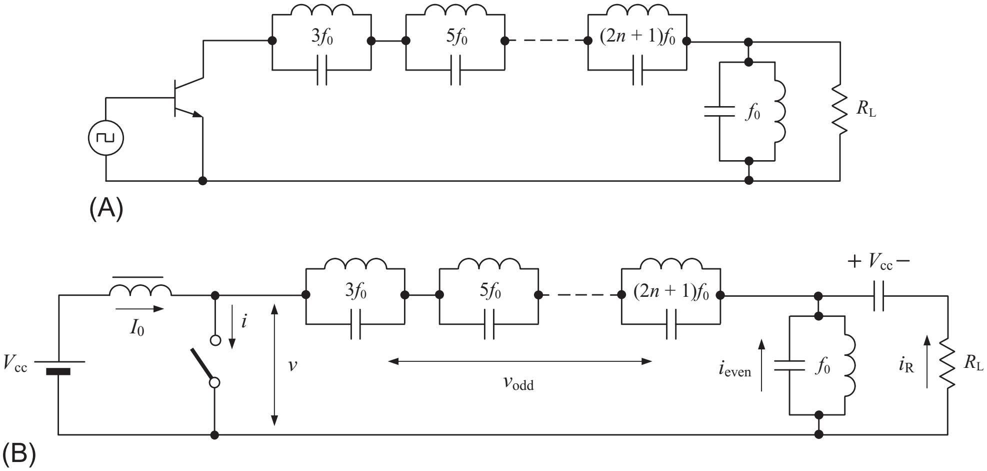


FIG. 3.10

Basic circuits of Class-F PA with parallel resonant circuits.

- There are no losses in the circuit except only into the load R_L.
- Operation mode with a 50% duty ratio.

To determine the idealized collector voltage and current waveforms, consider the distribution of voltages and currents in the load network assuming the sinusoidal fundamental current flowing into the load as $i_R(\omega t) = I_R \sin(\omega t)$, where I_R is its amplitude. The voltage $v(\omega t)$ across the switch can be represented as a sum of the DC voltage V_{cc}, fundamental voltage $v_R = i_R R_L$ across the load resistor, and voltage v_{odd} across the odd-harmonic resonators, written as

$$v(\omega t) = V_{cc} + v_{odd}[(2n+1)\omega t] + v_R(\omega t). \tag{3.16}$$

Because the time moment t was chosen arbitrarily, by introducing a phase shift of π, Eq. (3.16) can be rewritten for periodical sinusoidal functions as

$$v(\omega t + \pi) = V_{cc} - v_{odd}[(2n+1)\omega t] - v_R(\omega t). \tag{3.17}$$

Then, the summation of Eqs. (3.16), (3.17) yields

$$v(\omega t) = 2V_{cc} - v(\omega t + \pi). \tag{3.18}$$

From Eq. (3.18), it follows that maximum value of the collector voltage cannot exceed a value of $2V_{cc}$, and the time duration with maximum voltage of $v = 2V_{cc}$ coincides with the time duration with minimum voltage of $v = 0$. Because the collector voltage is zero when the switch is turned on, the only possible waveform for the collector voltage is a square wave composed of the DC, fundamental-frequency, and odd-harmonic components only.

During the interval $0 < \omega t \leq \pi$ when the switch is turned on, the current $i(\omega t)$ flowing through the switch can be written as

$$i(\omega t) = I_0 + i_{even}(2n\omega t) + i_R(\omega t), \tag{3.19}$$

whereas during the interval $\pi < \omega t \leq 2\pi$ when the switch is turned off, the current $i(\omega t + \pi)$ is equal to zero, resulting in

$$0 = I_0 + i_{even}(2n\omega t) - i_R(\omega t). \tag{3.20}$$

Then, substituting Eq. (3.20) into Eq. (3.19) yields

$$i(\omega t) = 2i_R(\omega t) = 2I_R \sin(\omega t), \tag{3.21}$$

from which it follows that the amplitude of the current flowing through the switch during interval $0 < \omega t \leq \pi$ is two times greater than the amplitude of the fundamental current. Thus, in a common case, Eq. (3.19) can be rewritten as

$$i(\omega t) = I_R\,(\sin\omega t + |\sin\omega t|), \tag{3.22}$$

which means that the switch current represents half-sinusoidal pulses with amplitude equal to double the load current amplitude.

Consequently, for a purely sinusoidal current flowing into the load shown in Fig. 3.11A, the ideal collector voltage and current waveforms can be represented by the appropriate normalized waveforms shown in Fig. 3.11B and C, respectively. Here, a sum of odd harmonics approximates a square voltage waveform, and a sum of the fundamental and even harmonics approximates a half-sinusoidal collector current waveform. As a result, the shapes of the collector current and voltage waveforms provide a

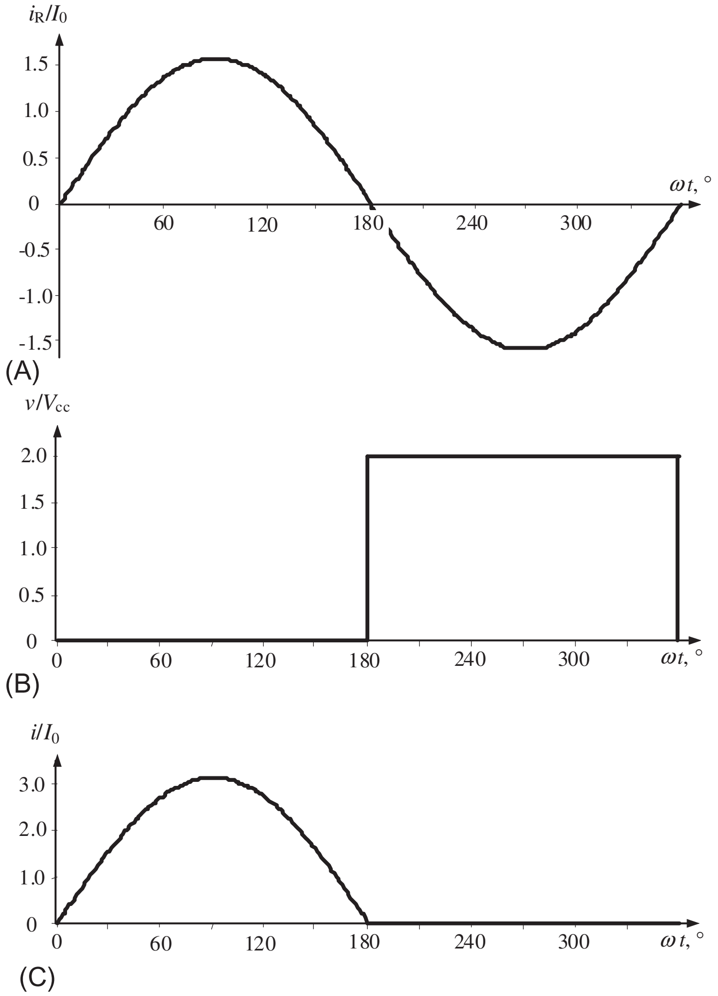


FIG. 3.11

Ideal waveforms of Class-F PA.

condition when the current and voltage do not overlap simultaneously. Such a condition, with symmetrical collector voltage and current waveforms, corresponds to an idealized Class-F operation mode with a collector efficiency of 100%.

A Fourier-series analysis of the current and voltage waveforms enables to obtain the equations for the DC current and fundamental voltage and current components in the collector voltage and current waveforms:

the DC current I_0 can be calculated from Eq. (3.22) as

$$I_0 = \frac{1}{2\pi}\int_0^{\pi} 2I_R \sin\omega t d\omega t = \frac{2I_R}{\pi}, \tag{3.23}$$

the fundamental current component can be calculated from Eq. (3.22) as

$$I_1 = \frac{1}{\pi}\int_0^{\pi} 2I_{\mathrm{R}} \sin^2 \omega t d\omega t = I_R, \tag{3.24}$$

and the fundamental voltage component can be calculated using Eq. (3.18) as

$$V_1 = V_{\mathrm{R}} = \frac{1}{\pi}\int_{\pi}^{2\pi} 2V_{\mathrm{cc}} \sin(\omega t + \pi) d\omega t = \frac{4V_{\mathrm{cc}}}{\pi}. \tag{3.25}$$

Then, the DC power and output power at the fundamental frequency are calculated from.

$$P_0 = V_{\mathrm{cc}} I_0 = \frac{2V_{\mathrm{cc}} I_{\mathrm{R}}}{\pi}, \tag{3.26}$$

and

$$P_1 = \frac{V_1 I_1}{2} = \frac{2\,V_{\mathrm{cc}} I_{\mathrm{R}}}{\pi}, \tag{3.27}$$

resulting in a theoretical collector efficiency with a maximum value of.

$$\eta = \frac{P_1}{P_0} = 100\%. \tag{3.28}$$

The impedance conditions seen by the device collector for an idealized Class-F mode using Eqs. (3.23)–(3.25) are obtained by

$$Z_1 = R_1 = \frac{V_1}{I_1} = \frac{8}{\pi^2}\frac{V_{\mathrm{cc}}}{I_0}, \tag{3.29}$$

$$Z_{2n} = 0 \quad \text{for even harmonics}, \tag{3.30}$$

$$Z_{2n+1} = \infty \quad \text{for odd harmonics}, \tag{3.31}$$

which are similar to that derived from the limiting case of the optimum efficiency Class-B mode.[21]

The collector square-voltage and half-sinusoidal current waveforms can be similarly obtained by using a multiple-resonator circuit shown in Fig. 3.12, where the parallel resonators tuned to the third, fifth, and higher-order odd harmonics are located between the voltage supply and collector, while the series resonant circuit tuned to the fundamental frequency f_0 provides the sinusoidal current flowing into the load.

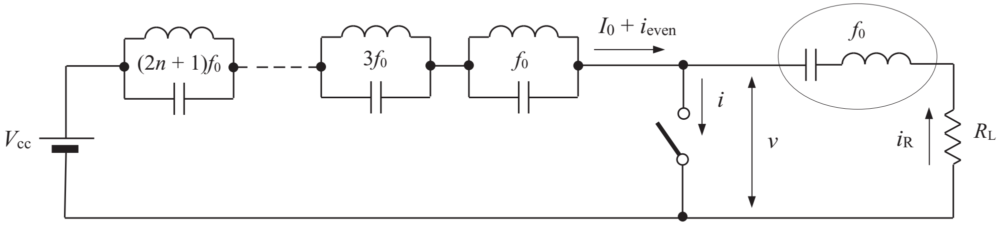


FIG. 3.12

Equivalent circuit of Class-F PA with series filter.

3.3 Class-F with maximally flat waveforms

Although it is impossible to realize the ideal harmonic-impedance conditions in real practice, the peaking of at least several current and voltage harmonic components should be provided to achieve high-efficiency operation of the PA. The more the voltage waveform provided by higher-order harmonic components can be flattened, the less power dissipation due to flowing of the output current—when output voltage is extremely small—occurs. To understand common design principles and to numerically calculate the PA efficiency according to the appropriate number of the frequency harmonic components of the voltage and current waveforms, it is useful to introduce a design technique applied to Class-F approximation with maximally flat waveforms.[22] The output network is assumed ideal to deliver only the fundamental-frequency power to the load without loss. The active device represents an ideal current source with zero saturation voltage and output capacitance. Flattening of the voltage and current waveforms to realize Class-F operation can be accomplished by using odd-harmonic components to approximate a square voltage waveform and even-harmonic components to approximate a half-sinusoidal current waveform, given by

$$v(\omega t) = V_{cc} + V_1 \sin\omega t + \sum_{n=3,5,7,\ldots}^{\infty} V_n \sin n\omega t, \tag{3.32}$$

$$i(\omega t) = I_0 - I_1 \sin\omega t - \sum_{n=2,4,6,\ldots}^{\infty} I_n \cos n\omega t. \tag{3.33}$$

For the symmetrical flattened voltage waveforms shown in Fig. 3.13, the medium points where the voltage waveform reaches its maximum and minimum values are at $\omega t = \pi/2$ and $\omega t = 3\pi/2$, respectively. Maximum flatness at the minimum voltage requires the even derivatives to be zero at $\omega t = 3\pi/2$. Because the odd-order derivatives are equal to zero because $\cos n\pi/2 = 0$ for odd n, it is necessary to define the even-order derivatives of the voltage waveform given by Eq. (3.32).

As a result, for a voltage spectrum including odd-frequency components up to the seventh component, the second, fourth, and sixth derivatives are.

$$\frac{d^2 v}{d(\omega t)^2} = -V_1 \sin\omega t - 9V_3 \sin 3\omega t - 25V_5 \sin 5\omega t - 49V_7 \sin 7\omega t, \tag{3.34}$$

$$\frac{d^4 v}{d(\omega t)^4} = V_1 \sin\omega t + 81V_3 \sin 3\omega t + 625V_5 \sin 5\omega t + 2401V_7 \sin 7\omega t, \tag{3.35}$$

$$\frac{d^6 v}{d(\omega t)^6} = -V_1 \sin\omega t - 729V_3 \sin 3\omega t - 15{,}625V_5 \sin 5\omega t - 117{,}649V_7 \sin 7\omega t. \tag{3.36}$$

At the minimum points, these derivatives must be equal to zero,

$$\left.\frac{d^2 v}{d(\omega t)^2}\right|_{\omega t = \frac{3}{2}\pi} = \left.\frac{d^4 v}{d(\omega t)^4}\right|_{\omega t = \frac{3}{2}\pi} = \left.\frac{d^6 v}{d(\omega t)^6}\right|_{\omega t = \frac{3}{2}\pi} = 0. \tag{3.37}$$

Consequently, a system of three equations to calculate the odd-harmonic voltage amplitudes (V_3, V_5, and V_7) through the DC component V_{cc} and fundamental voltage amplitude V_1 can be written as

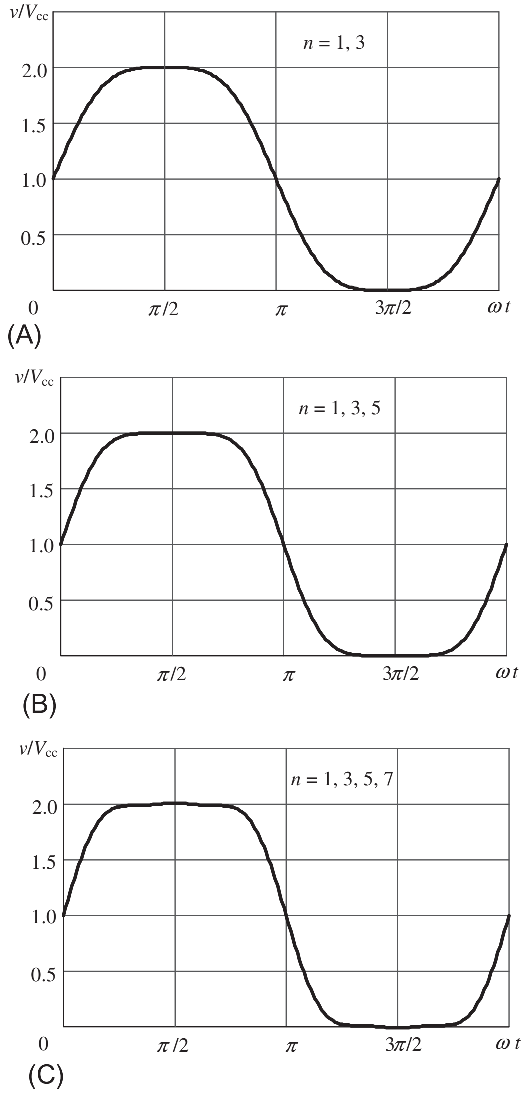


FIG. 3.13

Voltage waveforms for *n*th-harmonic peaking.

$$V_1 - 9V_3 + 25V_5 - 49V_7 = 0, \tag{3.38}$$

$$V_1 - 81V_3 + 625V_5 - 2401V_7 = 0, \tag{3.39}$$

$$V_1 - 729V_3 + 15{,}625V_5 - 117{,}649V_7 = 0. \tag{3.40}$$

For the third-harmonic peaking when only the third-harmonic component together with the fundamental one is present (assuming $V_5 = V_7 = 0$), Eq. (3.38) gives

$$V_3 = \frac{1}{9} V_1. \tag{3.41}$$

Then, from Eq. (3.32) at $\omega t = 3\pi/2$ when $v(\omega t) = 0$, the optimum amplitudes of the first and third harmonics are defined by

$$V_1 = \frac{9}{8} V_{cc} \quad V_3 = \frac{1}{8} V_{cc}. \tag{3.42}$$

For the biharmonic peaking with third- and fifth harmonic components (assuming $V_7 = 0$), simultaneous solution of Eqs. (3.38), (3.39) yields

$$V_3 = \frac{1}{6} V_1 \quad V_5 = \frac{1}{50} V_1, \tag{3.43}$$

and, consequently,

$$V_1 = \frac{75}{64} V_{cc} \quad V_3 = \frac{25}{128} V_{cc} \quad V_5 = \frac{3}{128} V_{cc}. \tag{3.44}$$

Similarly, for the triharmonic peaking with third, fifth, and seventh harmonic components, simultaneous solution of Eqs. (3.38)–(3.40) yields

$$V_3 = \frac{1}{5} V_1 \quad V_5 = \frac{1}{25} V_1 \quad V_7 = \frac{1}{245} V_1, \tag{3.45}$$

resulting for zero collector voltages in

$$\begin{aligned} V_1 &= \frac{1225}{1024} V_{cc} \quad V_3 = \frac{245}{1024} V_{cc}, \\ V_5 &= \frac{49}{1024} V_{cc} \quad V_7 = \frac{5}{1024} V_{cc}. \end{aligned} \tag{3.46}$$

The voltage waveforms for the third-harmonic peaking ($n = 1, 3$), odd biharmonic peaking ($n = 1, 3, 5$), and odd triharmonic peaking ($n = 1, 3, 5, 7$) are shown in Fig. 3.13.

For the symmetrical current waveforms shown in Fig. 3.14, the medium points where the current waveform reaches its minimum and maximum values are at $\omega t = \pi/2$ and $\omega t = 3\pi/2$, respectively. Because the odd-order derivatives are equal to zero because $\cos\pi/2 = 0$ and $\sin n\pi/2 = 0$ for even n, it is enough to determine the even-order derivatives of the current waveform given by Eq. (3.33). Maximum flatness at the minimum current requires the even derivatives to be zero at $\omega t = \pi/2$.

As a result, for a current spectrum including even-harmonic components up to the sixth component, the second, fourth, and sixth derivatives of the current waveform are.

$$\frac{d^2 i}{d(\omega t)^2} = I_1 \sin\omega t + 4I_2 \cos 2\omega t + 16I_4 \cos 4\omega t + 36I_6 \cos 6\omega t, \tag{3.47}$$

$$\frac{d^4 i}{d(\omega t)^4} = -I_1 \sin\omega t - 16I_2 \cos 2\omega t - 256I_4 \cos 4\omega t - 1296I_6 \cos 6\omega t, \tag{3.48}$$

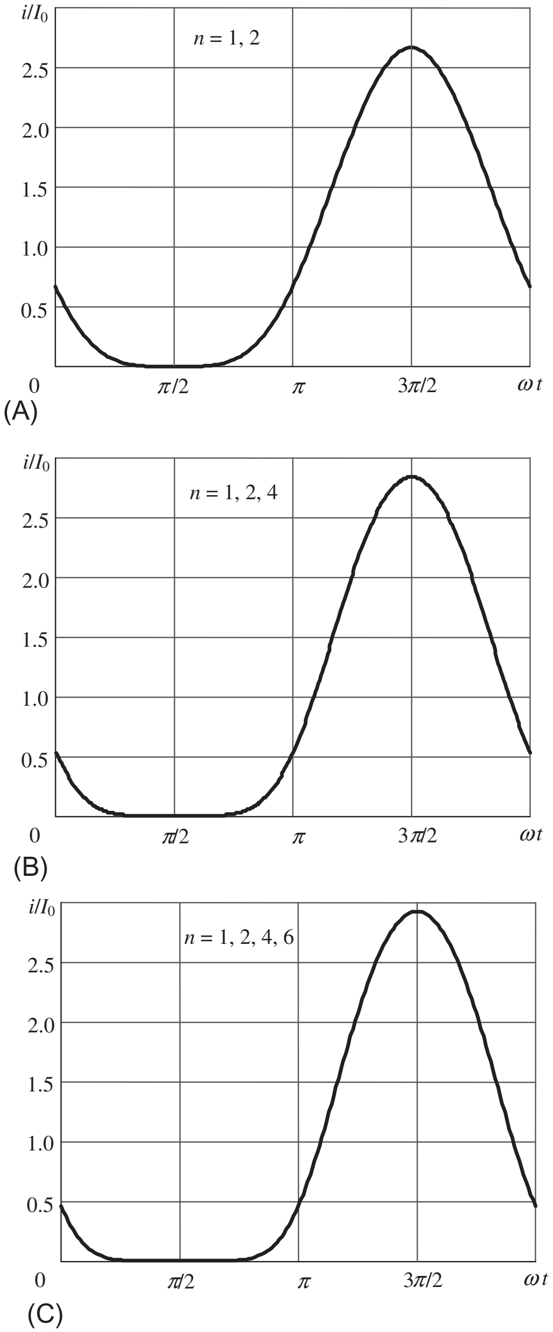


FIG. 3.14

Current waveforms for *n*th-harmonic peaking.

$$\frac{d^6 i}{d(\omega t)^6} = I_1 \sin\omega t + 64 I_2 \cos 2\omega t + 4096 I_4 \cos 4\omega t + 46{,}656 I_6 \cos 6\omega t. \tag{3.49}$$

At the minimum points, these derivatives must be equal to zero:

$$\left.\frac{d^2 i}{d(\omega t)^2}\right|_{\omega t=\frac{\pi}{2}} = \left.\frac{d^4 i}{d(\omega t)^4}\right|_{\omega t=\frac{\pi}{2}} = \left.\frac{d^6 i}{d(\omega t)^6}\right|_{\omega t=\frac{\pi}{2}} = 0. \tag{3.50}$$

Hence a system of three equations to calculate the even-harmonic current amplitudes (I_2, I_4, and I_6) through the DC component I_0 and fundamental current amplitude I_1 can be written as.

$$I_1 - 4I_2 + 16I_4 - 36I_6 = 0, \tag{3.51}$$

$$I_1 - 16I_2 + 256I_4 - 1296I_6 = 0, \tag{3.52}$$

$$I_1 - 64I_2 + 4096I_4 - 46{,}656I_6 = 0. \tag{3.53}$$

For the second-harmonic peaking when only the second harmonic component together with the fundamental one is present (assuming $I_4 = I_6 = 0$), Eq. (3.51) gives.

$$I_2 = \frac{1}{4} I_1. \tag{3.54}$$

Then, from Eq. (3.51) at $\omega t = \pi/2$ when $i(\omega t) = 0$, the optimum amplitudes are equal to

$$I_1 = \frac{4}{3} I_0 \quad I_2 = \frac{1}{3} I_0. \tag{3.55}$$

For the biharmonic peaking with second and fourth harmonic components (assuming $I_6 = 0$), simultaneous solution of Eqs. (3.51), (3.52) yields.

$$I_2 = \frac{5}{16} I_1 \quad I_4 = \frac{1}{64} I_1, \tag{3.56}$$

and, consequently,

$$I_1 = \frac{64}{45} I_0 \quad I_2 = \frac{4}{9} I_0 \quad I_4 = \frac{1}{45} I_0. \tag{3.57}$$

Similarly, for the triharmonic peaking with second, fourth, and sixth harmonic components, simultaneous solution of Eqs. (3.51)–(3.53) yields

$$I_2 = \frac{175}{512} I_1 \quad I_4 = \frac{7}{256} I_1 \quad I_6 = \frac{1}{512} I_1, \tag{3.58}$$

resulting for zero collector current in

$$\begin{gathered} I_1 = \frac{256}{175} I_0 \quad I_2 = \frac{1}{2} I_0, \\ I_4 = \frac{1}{25} I_0 \quad I_6 = \frac{1}{350} I_0. \end{gathered} \tag{3.59}$$

The current waveforms for the second-harmonic peaking ($n = 1$, 2), even biharmonic peaking ($n = 1$, 2, 4), and even triharmonic peaking ($n = 1$, 2, 4, 6) are shown in Fig. 3.14.

Table 3.1 Resultant efficiencies for various combinations of voltage and current harmonic components.

Current harmonic components	Voltage harmonic components				
	1	1, 3	1, 3, 5	1, 3, 5, 7	1, 3, 5, …, ∞
1	1/2 = 0.500	9/16 = 0.563	75/128 = 0.586	1225/2048 = 0.598	$2/\pi = 0.637$
1, 2	2/3 = 0.667	3/4 = 0.750	25/32 = 0.781	1225/1536 = 0.798	$8/3\pi = 0.849$
1, 2, 4	32/45 = 0.711	4/5 = 0.800	5/6 = 0.833	245/288 = 0.851	$128/45\pi = 0.905$
1, 2, 4, 6	128/175 = 0.731	144/175 = 0.823	6/7 = 0.857	7/8 = 0.875	$512/175\pi = 0.931$
1, 2, 4, …, ∞	$\pi/4 = 0.785$	$9\pi/32 = 0.884$	$75\pi/256 = 0.920$	$1225\pi/4096 = 0.940$	1 = 1.000

The effectiveness of the operations modes with different voltage and current harmonic peaking can be compared by calculating the collector (drain) efficiency η of each operation mode in accordance with

$$\eta = \frac{P_1}{P_0} = \frac{1}{2}\frac{V_1}{V_{cc}}\frac{I_1}{I_0}. \tag{3.60}$$

The resultant efficiencies for various combinations of voltage and current harmonic components, as presented in Table 3.1, show that the efficiency increases with an increase in the number of voltage and current harmonic components. To increase the efficiency, it is more desirable to provide harmonic peaking in consecutive numerical order—both for voltage and current harmonic components—than to increase the number of the harmonic components into only voltage or current waveforms. Class-F operation becomes mostly effective in comparison with Class-B operation if at least the third voltage harmonic peaking and fourth current harmonic peaking are realized. An inclusion of the fifth voltage harmonic component increases the efficiency up to 83.3%. An additional inclusion of the sixth-harmonic component into the current waveform and the seventh-harmonic component into the voltage waveform leads to efficiencies up to 94%. In this case, the efficiency of a Class-F mode with maximally flat waveform can be expressed as a simple explicit function of the number of even harmonics M in a current waveform and the number of higher odd harmonics K in a voltage waveform in the case when $M = K$ as

$$\eta = \frac{N}{N+1}, \tag{3.61}$$

where $N = 1 + M + K$ is the number of harmonics.[23]

Maximum efficiency for a given set of harmonics can be additionally increased if first to fix the fundamental-frequency amplitude and then to adjust the amplitude of the harmonics to minimize the downward excursion of the overall waveform.[24] Fixing the waveform minimum at zero gives the minimum supply voltage needed for full output power, thus maximizing efficiency. As a result, the maximum efficiency can be generally improved by 6%–8% compared to those for maximally flat waveforms. Analytically, the theoretical maximum efficiency depending only upon the terminating conditions can be written as

$$\eta = \frac{\pi}{2\,(m+1)}\cot\left[\frac{\pi}{2(m+1)}\right], \tag{3.62}$$

where m is the number of controlled harmonic components.[25] Moreover, when higher-order harmonic components are terminated in finite reactive impedances, the same maximum efficiency is obtained with the correct complex termination at the fundamental frequency.

Most Class-F PAs employ a conduction angle of 180 degrees when all odd harmonics of a half-sinusoidal current waveform are nulled, as are all even harmonics of a rectangular voltage waveform. However, conduction angles other than 180 degrees generally cause all harmonics to be present. In this case, a given harmonic is nulled at a specific conduction angle, but all or most others remain. Consequently, flattening of the voltage waveform during the time of conduction must be accomplished by the addition of a single harmonic.[26] For example, for a conduction angle of approximately 130 degrees, the use of the fourth harmonic increases the efficiency by about 6%, compared with that for a conventional Class-C PA.

3.4 Class-F with quarterwave transmission line

Ideally, a control of an infinite number of the harmonics maintaining a square voltage waveform and a half-sinusoidal current waveform at the drain can be provided using a serious quarterwave transmission line and a parallel-tuned resonant circuit, as shown in Fig. 3.15. This type of a Class-F PA was initially proposed to be used at higher frequencies where implementation of the load networks with only lumped elements is difficult and the parasitic device output (bondwire or package lead) inductance is sufficiently small.[19, 20] In this case, the quarterwave transmission line transforms the load impedance as

$$R = \frac{Z_0^2}{R_L}, \tag{3.63}$$

where Z_0 is the characteristic impedance of a transmission line.[27] For even harmonics, the short circuit on the load side of the transmission line is repeated, thus producing a short circuit at the drain. However,

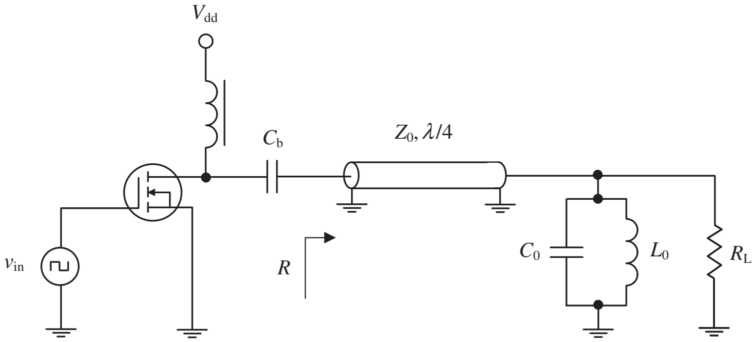


FIG. 3.15

Class-F PA with series quarterwave transmission line.

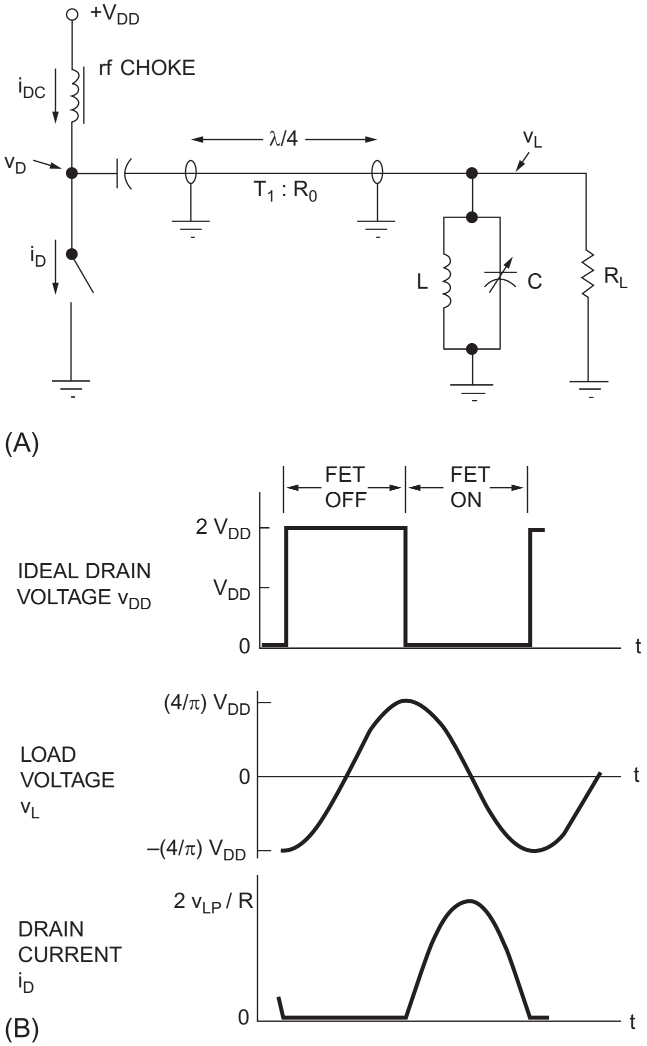

+V_{DD}
rf CHOKE
i_{DC}
v_D
$\lambda/4$
v_L
$T_1 : R_0$
i_D
L
C
R_L
(A)
FET OFF
FET ON
2 V_{DD}
IDEAL DRAIN VOLTAGE v_{DD}
V_{DD}
0
t
$(4/\pi)$ V_{DD}
LOAD VOLTAGE v_L
0
t
$-(4/\pi)$ V_{DD}
2 v_{LP} / R
DRAIN CURRENT i_D
0
t
(B)

FIG. 3.16

Load network with series quarterwave line and output waveforms of Class-F amplifier.

the short circuit at the load produces an open circuit at the drain for odd harmonics with resistive load at the fundamental.

The equivalent circuit of a Class-F load network with a series quarterwave transmission line is shown in Fig. 3.16A, where the parallel-tuned output circuit provides a short circuit to all harmonics, resulting in square-wave voltage and half-wave rectified sine-wave current shown in Fig. 3.16B.[27, 28] The first prototype of such a Class-F PA using two MOSFETs in parallel, as shown in Fig. 3.17, produced an output power of 300 mW with 73% efficiency at 25 MHz.[28]

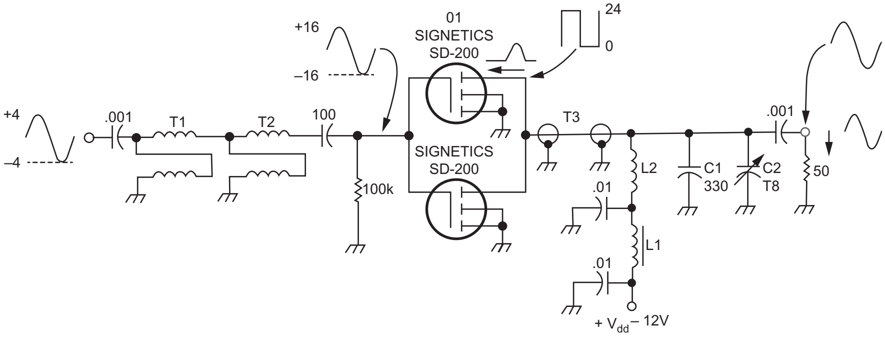


FIG. 3.17

Circuit schematic of high-efficiency Class-F MOSFET RF PA with series quarterwave transmission line.

These types of multiple-tuned RF PAs with odd-harmonic control have been given different names, such as biharmonic, polyharmonic, optimum-efficiency Class-B, multiple-resonator Class-C, single-ended Class-D, or even the Class-E.[19, 28] However, all of them were assigned by Raab to Class-F, which introduced the high-frequency PA with a quarterwave transmission line and parallel-tuned output circuit right after the introduction of the Class-E by Sokals in 1975.[29]

Generally, at low drive level, the active device acts as a current source (voltage-controlled in the case of the MOSFETs or MESFETs and current-controlled in the case of bipolar transistors). As input drive increases, the active device enters saturation resulting in a harmonic-generation process. Because the quarterwave transmission line presents the high impedance conditions to all odd harmonics, all odd harmonics provide a proper contribution to the output-voltage waveform. As a result, at high drive level, the output-voltage waveform becomes a complete square wave and the active device is saturated for a full half-cycle. In this case, the transistor acts as a switch rather than a saturating current source.

An alternative configuration of the Class-F PA with a shunt quarterwave transmission line located between the DC power supply and device collector is shown in Fig. 3.18A.[30] In this case, an RF choke and a series blocking capacitor can be eliminated because a series fundamentally tuned resonant circuit is used instead of a parallel fundamentally tuned resonant circuit. However, unlike the case with a series quarterwave transmission line, such a Class-F load network configuration with a shunt quarterwave transmission line does not provide an impedance transformation. Therefore the load resistance R, which is equal to the active device equivalent output resistance at the fundamental, must then be transformed to the standard load impedance. Let us now derive analytically some fundamental properties of a quarterwave transmission line. The transmission line in the time domain can be represented as an element with finite delay time depending upon its electrical length. Consider a simplified load network of the Class-F PA shown in Fig. 3.18B, which consists of a parallel quarterwave transmission line grounded at the end through power supply, a series fundamentally tuned L_0C_0 circuit, and a load resistance R. In an idealized case, the intrinsic device output capacitance is assumed negligible to affect the PA RF performance. The loaded quality factor Q_L of the series resonant L_0C_0 circuit is high enough to provide the sinusoidal output current i_R flowing into the load R. Based on this approach and using high-Q elements in the load network, high collector efficiencies of about 90% were achieved at operating frequencies and output powers up to 250 MHz and 10 W, respectively.

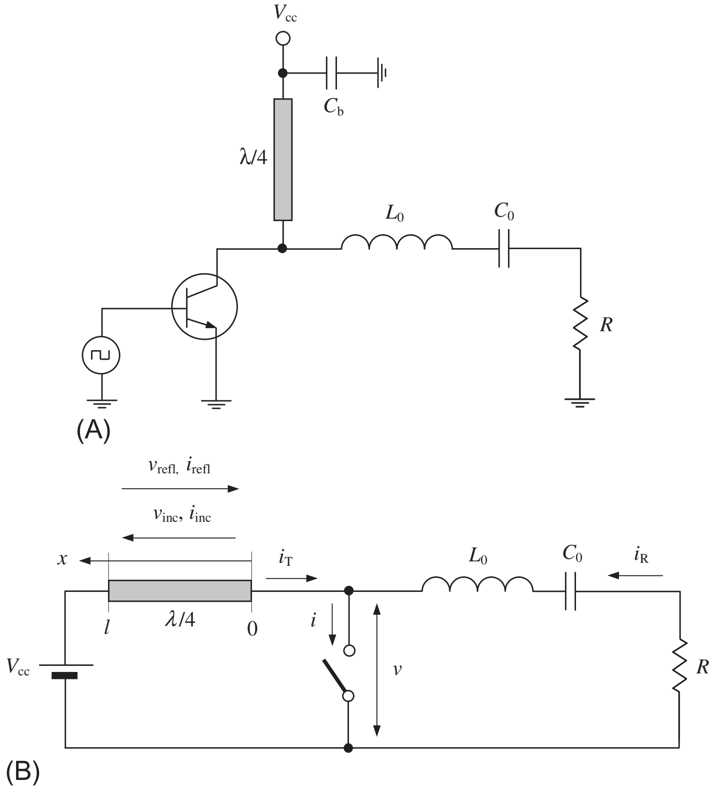


FIG. 3.18

Class-F PA with shunt quarterwave transmission line.

To define the collector voltage and current waveforms, consider the electrical behavior of a homogeneous lossless quarterwave transmission line connected to the DC voltage supply with RF grounding.[31] In this case, the voltage $v(t, x)$ in any cross-section of such a transmission line can be represented as a sum of the incident and reflected voltages, $v_{inc}(\omega t - 2\pi x/\lambda)$ and $v_{refl}\,(\omega t + 2\pi x/\lambda)$, respectively, generally with an arbitrary waveform. When $x = 0$, the voltage $v(t, x)$ is equal to the collector voltage

$$v(\omega t) = v(t, 0) = v_{inc}(\omega t) + v_{refl}(\omega t). \tag{3.64}$$

At the same time, at another end of the transmission line when $x = \lambda/4$, the voltage is constant and equal to

$$V_{cc} = v(t, \pi/2) = v_{inc}(\omega t - \pi/2) + v_{refl}(\omega t + \pi/2). \tag{3.65}$$

Because the time moment t was chosen arbitrarily, Eq. (3.65) can be rewritten using a phase shift of $\pi/2$ for each voltage by

$$v_{inc}(\omega t) = V_{cc} - v_{refl}(\omega t + \pi). \tag{3.66}$$

Substituting Eq. (3.66) into Eq. (3.64) yields.

$$v(\omega t) = v_{\text{refl}}(\omega t) - v_{\text{refl}}(\omega t + \pi) + V_{\text{cc}}. \tag{3.67}$$

Consequently, for the phase shift of π, the collector voltage can be obtained by.

$$v(\omega t + \pi) = v_{\text{refl}}(\omega t + \pi) - v_{\text{refl}}(\omega t + 2\pi) + V_{\text{cc}}. \tag{3.68}$$

For an idealized operation condition with a 50% duty ratio when within half a period the transistor is turned on and within another half a period the transistor is turned off with an overall period of 2π, the voltage $v_{\text{refl}}(\omega t)$ can be considered the periodical function with a period of 2π,

$$v_{\text{refl}}(\omega t) = v_{\text{refl}}(\omega t + 2\pi). \tag{3.69}$$

As a result, the summation of Eqs. (3.67), (3.68) using Eq. (3.69) results in the expression for collector voltage in the form

$$v(\omega t) = 2V_{\text{cc}} - v(\omega t + \pi). \tag{3.70}$$

From Eq. (3.70), it follows that the maximum value of the collector voltage cannot exceed a value of $2V_{\text{cc}}$, and the time duration with maximum voltage of $v = 2V_{\text{cc}}$ coincides with the time duration with minimum voltage of $v = 0$.

Similarly, equation for the current i_{T} that flows into the quarterwave transmission line can be obtained by

$$i_{\text{T}}(\omega t) = i_{\text{T}}(\omega t + \pi), \tag{3.71}$$

which means that the period of a signal flowing into the quarterwave transmission line is equal to π because it contains only even harmonics, because a quarterwave transmission line has an infinite impedance at odd harmonics.

Let the transistor operate as an ideal switch when it is turned on during the interval $0 < \omega t \leq \pi$ where $v = 0$ and turned off during the interval $\pi < \omega t \leq 2\pi$ where $v = 2V_{\text{cc}}$, according to Eq. (3.70). During the interval $\pi < \omega t \leq 2\pi$ when the switch is turned off, the load is connected directly to the transmission line and $i_{\text{T}} = -i_{\text{R}} = -I_{\text{R}} \sin\omega t$. Consequently, during the interval $0 < \omega t \leq \pi$ when the switch is turned on, $i_{\text{T}} = I_{\text{R}} \sin\omega t$ according to Eq. (3.71). Hence the current flowing into the quarterwave transmission line at any ωt can be represented by

$$i_{\text{T}}(\omega t) = I_{\text{R}} |\sin\omega t|, \tag{3.72}$$

where I_{R} is the amplitude of current flowing into the load.

Because the collector current is defined as $i = i_{\text{T}} + i_{\text{R}}$, then

$$i(\omega t) = I_{\text{R}}(\sin\omega t + |\sin\omega t|), \tag{3.73}$$

which means that the collector current represents a half-wave rectified sine-wave current with amplitude equal to double load-current amplitude.

Consequently, for a purely sinusoidal current flowing into the load because of infinite loaded quality factor of the series fundamentally tuned L_0C_0 circuit shown in Fig. 3.11A, the ideal collector voltage and current waveforms can be represented by the corresponding normalized square and half-sinusoidal waveforms shown in Fig. 3.11B and C, respectively, where I_0 is the DC current. Here, a sum of odd harmonics approximates a square voltage waveform, and a sum of the fundamental and even harmonics approximates a half-sinusoidal collector current waveform. The waveform corresponding to the normalized current flowing into the quarterwave transmission line shown in Fig. 3.19 consists of a sum of

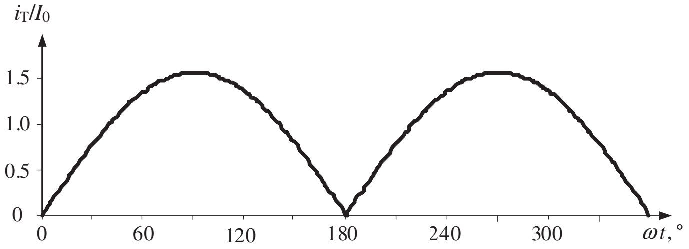


FIG. 3.19

Ideal current waveform in quarterwave transmission line.

even harmonics representing a full-wave rectified sine wave. As a result, the shapes of the collector current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously.

Fig. 3.20 shows a practical example of the circuit schematic of a Class-F PA with a shunt quarterwave line based on a 28-V, 10-W Cree GaN HEMT power transistor CGH40010. To better illustrate the drain voltage and current waveforms with minimum effect of the device parasitic output parameters, a sufficiently low operating frequency of 100 MHz was chosen. In this case, a simple lossy *RL* input shunt network is used to match the device input impedance to a 50-Ω source and to compensate for the device input gate-source capacitance C_{in} of about 5 pF at the fundamental frequency that resulted in a small-signal S_{11} better than −25 dB. The series 50-Ω resistor connected to the device gate is additionally included to provide an unconditional operation stability. The simulated drain voltage close to a square waveform and drain current close to a half-sinusoidal waveform are shown in Fig. 3.21A, where small waveform ripples (minimized by load-network parameter optimization) can be explained because of some effect of the device output drain-source capacitance C_{out} of about 1.3 pF and package parasitics at higher-order harmonic components. As a result, a maximum drain efficiency of 84.7% with a power gain of 20 dB and an output power of 40 dBm at a supply voltage of 28 V were obtained with a sine-wave driving signal, as shown in Fig. 3.21B. In this case, to better approximate the switchmode operation of a 10-W GaN HEMT device, it is necessary to slightly increase the input signal amplitude to operate in a saturated mode characterized by more than 3-dB gain compression point. Owing to the diode-based nonlinearity of the device input circuit, the amplitude harmonic ratio between the fundamental-frequency, second, and third harmonic components at the gate terminal is 8.2:1.3:1.

3.5 Effect of saturation resistance and shunt capacitance

It is useful to analytically estimate the effect of a saturation (or on-resistance) r_{sat} that is not equal to zero in a real transistor, and transistor, therefore, dissipates some amount of power due to the collector current flowing through this resistance when the transistor is turned on. The simplified equivalent circuit of a Class-F PA with a quarterwave transmission line where the transistor is represented by a non-ideal switch with the saturation resistance r_{sat} and parasitic output capacitance C_{out} is shown in Fig. 3.22. During the interval $0 < \omega t \leq \pi$ when the switch is turned on, the saturation voltage v_{sat} due to the current $i(\omega t)$ flowing through the switch can be written as

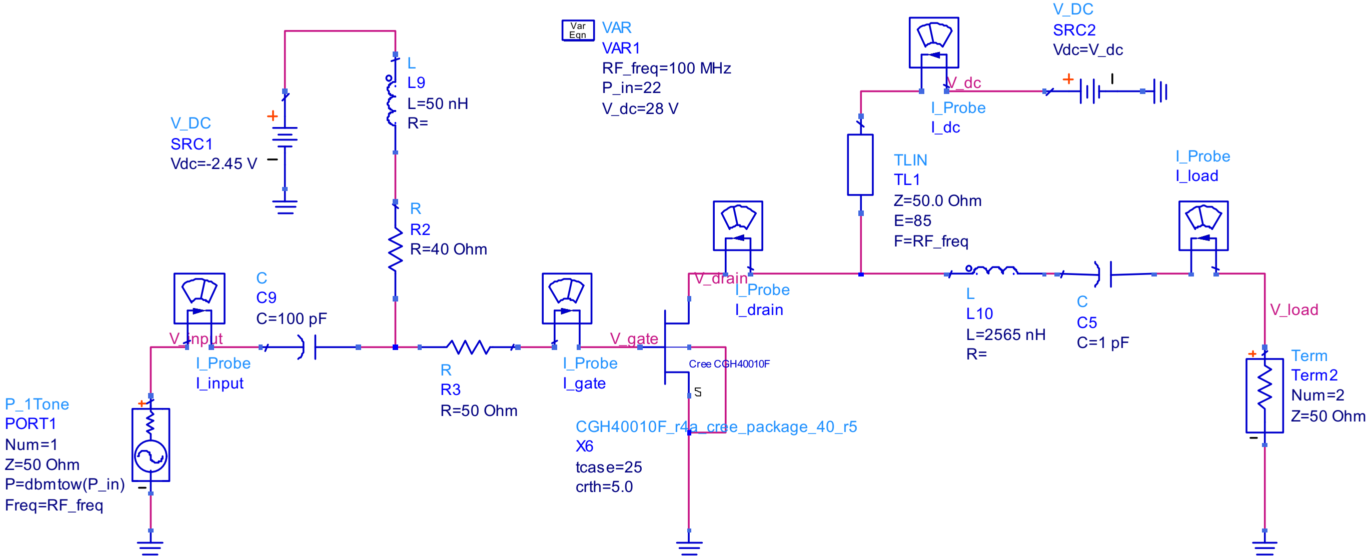
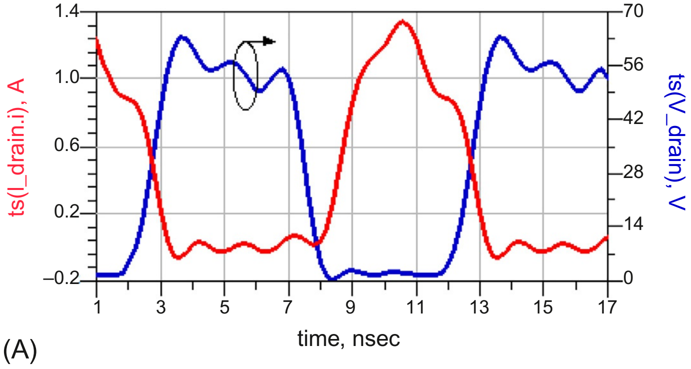

V_DC
SRC1
Vdc=-2.45 V
L
L9
L=50 nH
R=
Var
Eqn
VAR
VAR1
RF_freq=100 MHz
P_in=22
V_dc=28 V
V_DC
SRC2
Vdc=V_dc
V_dc
I_Probe
I_dc
TLIN
TL1
Z=50.0 Ohm
E=85
F=RF_freq
I_Probe
I_load
R
R2
R=40 Ohm
C
C9
C=100 pF
V_input
I_Probe
I_input
R
R3
R=50 Ohm
I_Probe
I_gate
V_gate
V_drain
I_Probe
I_drain
Cree CGH40010F
S
CGH40010F_r4a_cree_package_40_r5
X6
tcase=25
crth=5.0
L
L10
L=2565 nH
R=
C
C5
C=1 pF
V_load
Term
Term2
Num=2
Z=50 Ohm
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(P_in)
Freq=RF_freq

FIG. 3.20

Circuit schematic of a Class-F GaN HEMT PA with shunt quarterwave line.



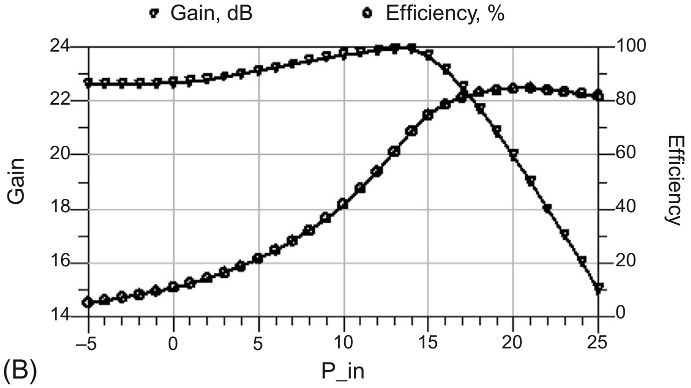


FIG. 3.21

Simulated waveforms and performance of a Class-F GaN HEMT PA.

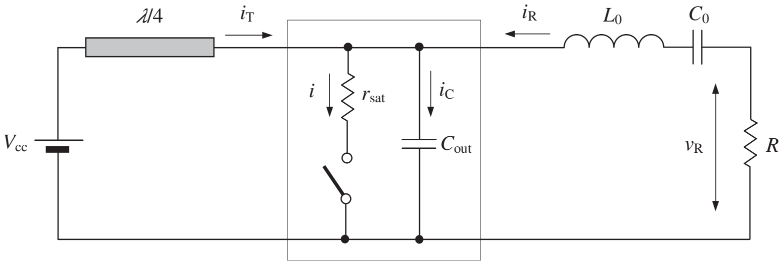

λ/4
i_T
i_R
L_0
C_0
i
r_{sat}
i_C
V_{cc}
C_{out}
v_R
R

FIG. 3.22

Effect of parasitic on-resistance and shunt capacitance.

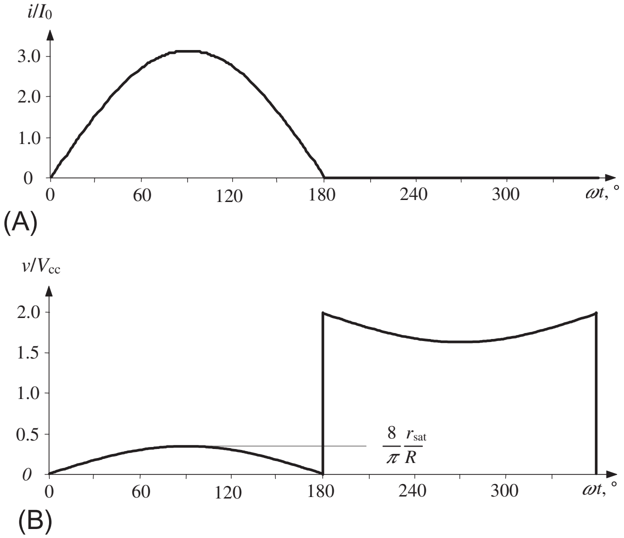


FIG. 3.23

Idealized collector current and voltage waveforms with nonzero on-resistance.

$$v_{\text{sat}}(\omega t) = V_{\text{sat}} \sin\omega t = 2I_{\text{R}}\, r_{\text{sat}} \sin\omega t, \tag{3.74}$$

where, by using Eq. (3.25), the saturation voltage amplitude V_{sat} can be obtained by

$$V_{\text{sat}} = 2V_{\text{R}}\frac{r_{\text{sat}}}{R} = \frac{8V_{\text{cc}}}{\pi}\frac{r_{\text{sat}}}{R}. \tag{3.75}$$

The corresponding collector current and voltage waveforms are shown in Fig. 3.23, where the half-sinusoidal current flowing through the saturation resistance r_{sat} causes the deviation of the voltage waveform from the ideal square waveform. In this case, the bottom part of the voltage waveform becomes sinusoidal with the amplitude V_{sat} during the interval $0 < \omega t \le \pi$. From Eq. (3.18), it follows that the same sinusoidal behavior will correspond to the top part of the voltage waveform during the interval $\pi < \omega t \le 2\pi$.

The power losses and collector efficiency due to presence of the saturation resistance r_{sat} can be evaluated using Eqs. (3.21), (3.23), (3.25) as

$$\begin{aligned}\frac{P_{\text{sat}}}{P_0} &= \frac{1}{2\pi}\int_0^{2\pi}\frac{i^2(\omega t)r_{\text{sat}}}{I_0V_{\text{cc}}}d\omega t = \frac{r_{\text{sat}}}{2\pi I_0V_{\text{cc}}}\int_0^{2\pi}(2I_{\text{R}})^2\sin^2\omega t d\omega t\\ &= \frac{r_{\text{sat}}I_{\text{R}}}{V_{\text{cc}}}\frac{I_{\text{R}}}{I_0} = \frac{r_{\text{sat}}}{R}\frac{I_{\text{R}}}{I_0}\frac{V_{\text{R}}}{V\text{cc}} = \frac{2r_{\text{sat}}}{R}.\end{aligned} \tag{3.76}$$

Hence the collector efficiency can be calculated from

$$\eta = 1 - \frac{P_{\text{sat}}}{P_0} = 1 - \frac{2r_{\text{sat}}}{R}. \tag{3.77}$$

In practice, the idealized collector voltage and current waveforms can be realized at low frequencies when the effect of the device collector capacitance is negligible. At higher frequencies, the effect of the collector capacitance contributes to a nonzero switching time, resulting in time periods when the collector voltage and collector current exist at the same time when $v > 0$ and $i > 0$. Consequently, such a load network with shunt capacitance cannot provide the switchmode operation with an instantaneous transition from the device pinch-off to saturation mode. Therefore during a nonzero time interval, the device operates in active region as a current source with the reverse-biased collector–base junction, and the collector current is provided by this current source.

The current flowing through the collector capacitance can be determined by differentiating both parts of Eq. (3.18), considering that voltage v is the voltage across the capacitance C, as

$$i_C(\omega t) = -i_C(\omega t + \pi), \tag{3.78}$$

which means that the current due to the capacitance charging process is equal to the current due to the capacitance discharging process with opposite sign, and the durations of the charging and discharging periods are equal.

From Fig. 3.22, it follows that the current flowing through the collector capacitance at the arbitrary time moment t can be written as

$$i_C(\omega t) = i_T(\omega t) + i_R(\omega t) - i(\omega t), \tag{3.79}$$

whereas at the time moment $(t + \pi/\omega)$, it can be obtained by

$$i_C(\omega t + \pi) = i_T(\omega t + \pi) + i_R(\omega t + \pi) - i(\omega t + \pi). \tag{3.80}$$

The output current flowing into the load is written as sinusoidal as

$$i_R(\omega t) = I_R \sin(\omega t + \varphi), \tag{3.81}$$

where φ is the initial phase shift due to the finite value of the collector capacitance.

Then, by considering Eqs. (3.71), (3.78), from Eq. (3.80), it follows that

$$-i_C(\omega t) = i_T(\omega t) - i_R(\omega t) - i(\omega t + \pi). \tag{3.82}$$

Adding Eqs. (3.79), (3.82) yields

$$i(\omega t) + i(\omega t + \pi) = 2 i_T(\omega t), \tag{3.83}$$

that specifies the relationship in the time domain between the collector current and current flowing into the transmission line.

The collector current and voltage waveforms are shown in Fig. 3.24 where the phase angle φ_1 corresponds to the beginning of the transistor saturation mode, and the phase angle φ_2 corresponds to the beginning of the active mode and collector capacitance charging process start-up.[31] During the saturation interval when $\varphi_1 < \omega t < \varphi_2$, the collector current $i(\omega t)$ can be defined using Eqs. (3.79), (3.81), (3.82) by

$$i(\omega t) = i_T(\omega t) + i_R(\omega t) = 2 i_R(\omega t) = 2 I_R \sin(\omega t + \varphi). \tag{3.84}$$

In active region when $0 \le \omega t \le \varphi_1$ and $\varphi_2 \le \omega t \le \pi$, the collector current flowing into the load network is defined by the input driving signal and for the conduction angle of 180 degrees, represents the periodic half-sinusoidal pulses written as

$$i(\omega t) = I_{\text{active}} \left(\sin \omega t + |\sin \omega t|\right), \tag{3.85}$$

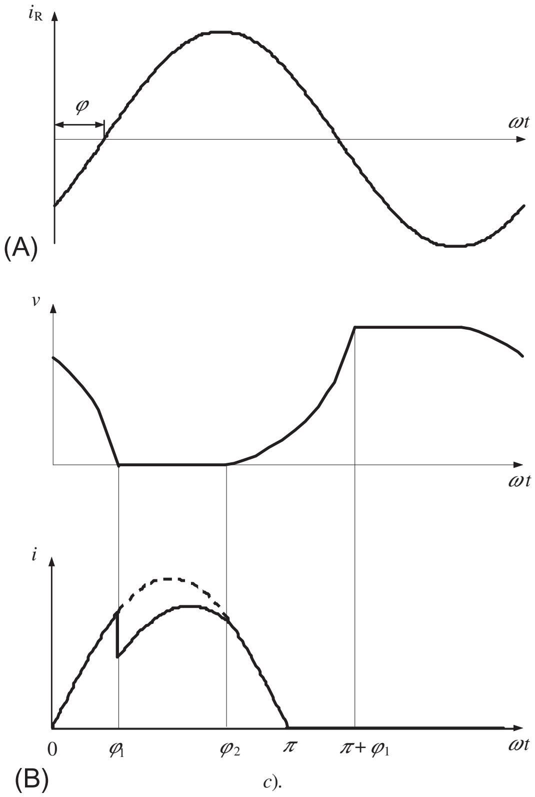


FIG. 3.24

Effect of shunt capacitance on voltage and current waveforms.

where the collector current amplitude I_{active} in active region is characterized by a higher value than the one in saturation mode when $I_{\text{sat}}=2I_R$, as follows from Eq. (3.85), because of the shunting effect of the forward-biased collector-base diode junction when device is saturated. The moment of the opening of the collector-base junction corresponds to the time moment φ_1 with instantaneous reduction in the collector current waveform, as shown in Fig. 3.24C. Physically, this effect can be explained by the carrier injection from the device collector to its base region as a result of forward-biasing of the collector-base junction. The saturation period is characterized by the diffusion capacitance of the forward-biased collector-base junction, whereas in active or pinch-off regions, the reverse-biased collector-base junction is described by the junction capacitance, the value of which is substantially smaller. The saturation period is ended at the time moment φ_2 corresponding to the beginning of the active mode and process of charging the collector junction capacitance is started up.

By using Eqs. (3.72), (3.84), (3.85), the current flowing into the transmission line i_T and current flowing through the collector capacitance i_C can be obtained by

$$i_T(\omega t)=I_{\text{active}}|\sin\omega t|, \tag{3.86}$$

$$i_C(\omega t) = 2[I_R \sin(\omega t + \varphi) - I_{\text{active}} \sin \omega t]. \tag{3.87}$$

Power losses due to the charging and discharging processes of the device collector capacitance can be calculated from

$$P_{\text{loss}} = \frac{1}{2\pi} \int_0^{\varphi_1} v(\omega t) i(\omega t) d\omega t + \frac{1}{2\pi} \int_{\varphi_2}^{\pi} v(\omega t) i(\omega t) d\omega t, \tag{3.88}$$

where the collector voltage v coincides with the voltage across the capacitance C. From Eq. (3.88), it follows that the longer active region because of the larger collector capacitance, the more power losses and less efficient operation of the PA. From the results of numerical calculations, the maximum operating frequency where the collector efficiency of a Class-F PA with the effect of the output capacitance C_{out} is higher than the collector efficiency of a conventional Class-B PA can be evaluated from

$$f_{\max} \cong \frac{0.47}{RC_{\text{out}}}, \tag{3.89}$$

where the output capacitance C_{out} is assumed a total collector capacitance (including the capacitances of the passive and active parts of the collector–base junction) corresponding to the DC bias operation point.[31]

3.6 Load networks with lumped elements

Theoretical results show that the proper control of only the second and third harmonics can significantly increase the collector efficiency of the PA by flattening the output voltage waveform. Because practical realization of a multielement high-order LC resonant circuit can cause a serious implementation problem, especially at higher frequencies, it is enough to be confined to a three- or four-element resonant circuit composing the load network of the PA. In addition, it is necessary to consider that, in practice, both extrinsic and intrinsic transistor parasitic elements such as output shunt capacitance or serious inductance have a substantial effect on the efficiency. The output capacitance C_{out} can represent the collector capacitance C_c in the case of the bipolar transistor or the sum of the drain-source and gate-drain capacitances, $C_{\text{ds}} + C_{\text{gd}}$, in the case of the FET device. The output inductance L_{out} is generally composed of the bondwire and lead inductances for a packaged transistor, the effect of which becomes significant at higher frequencies. The typical two-terminal reactive networks with series and parallel resonators used in a practical design procedure, which provide ideally infinite impedances at the fundamental and third harmonics and zero impedance at the second harmonic, are shown in Fig. 3.25.[32–34]

At microwave and millimeter-wave frequencies, it is required to minimize a number of elements to reduce the effect of any possible circuit parasitics. Fig. 3.26 shows the simple Class-F load network with the second- and third-harmonic controls, where C_{ds} is the drain-source capacitance of the MESFET device tuned together with inductance L_1 and capacitance C_1 for a parallel resonance at the third harmonic, while the series combination of L_1 and C_1 provides a series resonance at the second harmonic operating as a second-harmonic trap.[35] The load network input impedance Z_{net} can be written as.

$$Z_{\text{net}} = j\frac{\omega^2 L_1 C_1 - 1}{\omega C_1 - \omega C_{\text{ds}}(\omega^2 L_1 C_1 - 1)}. \tag{3.90}$$

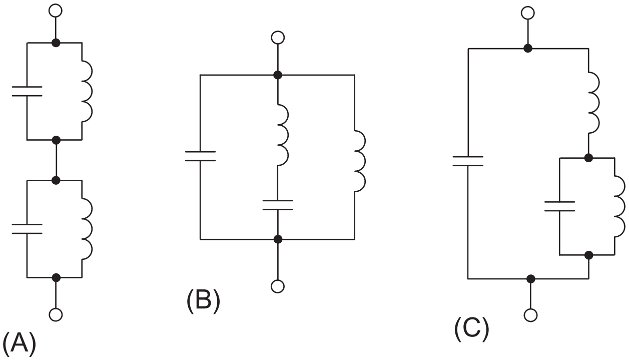


FIG. 3.25

Two-terminal reactive networks with series and parallel resonators.

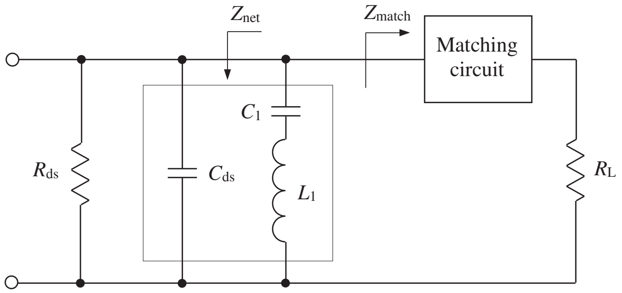


FIG. 3.26

Class-F load network with second- and third-harmonic controls.

As a result, by applying two harmonic-impedance conditions, open-circuited for the third harmonic $Z_{\rm net}(3\omega_0) = \infty$ and short-circuited for the second harmonic $Z_{\rm net}(2\omega_0) = 0$, where ω_0 is the fundamental angular frequency, the values of load-network elements as a function of $C_{\rm ds}$ can be calculated from.

$$C_1 = \frac{5}{4} C_{\rm ds}, \tag{3.91}$$

$$L_1 = \frac{1}{5\omega_0^2 C_{\rm ds}}. \tag{3.92}$$

However, because the resulting impedance at the fundamental frequency is capacitive, it is necessary to compensate for the capacitive reactance by choosing the parameters of the matching circuit having an inductive reactance of its input impedance $Z_{\rm match}$ at the fundamental and high impedance conditions at the third and higher-order harmonic components. The output matching circuit based on an L-type lumped transformer with a series inductor and a shunt capacitor implemented in a monolithic microwave design can be used to provide an impedance matching at the fundamental frequency and a high-impedance condition at the third harmonic together with a second-harmonic trap.[36]

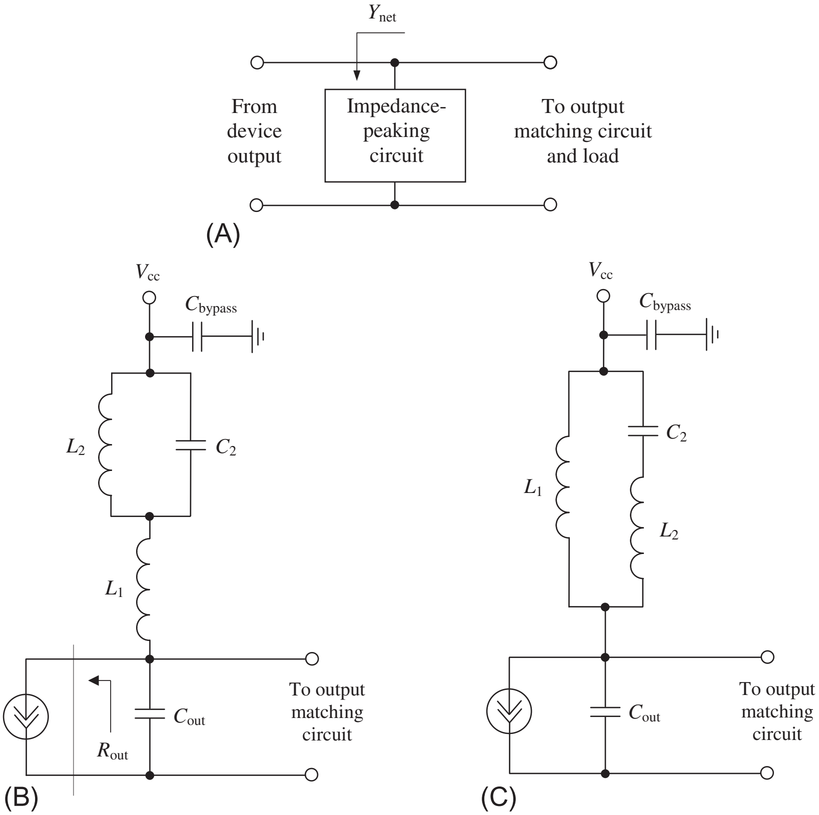

Y_{net}
From device output
Impedance-peaking circuit
To output matching circuit and load
(A)
V_{cc}
C_{bypass}
L_2
C_2
L_1
C_{out}
R_{out}
To output matching circuit
(B)
V_{cc}
C_{bypass}
C_2
L_1
L_2
C_{out}
To output matching circuit
(C)

FIG. 3.27

Load networks with parallel and series resonant circuits.

By adding an additional element to the load network shown in Fig. 3.26, it is possible to compensate for the capacitive reactance at the fundamental frequency, thus providing both high impedance at the fundamental and third harmonics and zero impedance at the second harmonic. Examples of such load networks with additional parallel and series resonant circuits located between the DC power supply and device output are shown in Fig. 3.27.[34, 37, 38] Here, the output circuit of the active device is represented by a multiharmonic current source, and R_{out} is the equivalent output resistance at the fundamental frequency defined as a ratio of the fundamental voltage at the device output to the fundamental current flowing into the device.

The reactive part of the output admittance (or susceptance) $B_{net} = \mathrm{Im}Y_{net}$ of the load network with a parallel resonant tank shown in Fig. 3.27B, including the device output capacitance C_{out}, can be written as

$$B_{net} = \omega C_{out} - \frac{1 - \omega^2 L_2 C_2}{\omega L_1 (1 - \omega^2 L_2 C_2) + \omega L_2}. \tag{3.93}$$

By applying three harmonic-impedance conditions $B_{\mathrm{net}}(\omega_0)=B_{\mathrm{net}}(3\omega_0)=0$ and $B_{\mathrm{net}}(2\omega_0)=\infty$ at the device output (collector or drain), determining an open circuit for the fundamental and third harmonic components and a short circuit for the second harmonic component, Eq. (3.93) can be rewritten in the form of three equations as

$$\left(1-\omega_0^2 L_1 C_{\mathrm{out}}\right)\left(1-\omega_0^2 L_2 C_2\right)-\omega_0^2 L_2 C_{\mathrm{out}}=0, \tag{3.94}$$

$$L_1\left(1-4\omega_0^2 L_2 C_2\right)+L_2=0, \tag{3.95}$$

$$\left(1-9\omega_0^2 L_1 C_{\mathrm{out}}\right)\left(1-9\omega_0^2 L_2 C_2\right)-9\omega_0^2 L_2 C_{\mathrm{out}}=0. \tag{3.96}$$

As a result, the ratios between elements of this impedance-peaking load network are

$$L_1=\frac{1}{6\omega_0^2 C_{\mathrm{out}}}, \tag{3.97}$$

$$L_2=\frac{5}{3}L_1, \tag{3.98}$$

$$C_2=\frac{12}{5}C_{\mathrm{out}}, \tag{3.99}$$

where the sum of the reactances of the parallel resonant tank, consisting of an inductor L_2 and a capacitor C_2, and inductor L_1 creates open-circuit parallel resonance conditions at the fundamental and third harmonic components, while the series capacitive reactance of the tank circuit in series with an inductance L_1 creates a short-circuit series resonance condition at the second harmonic component.[37, 38]

Applying the same conditions for the load network with a series-resonant circuit shown in Fig. 3.27C results in the ratios between elements given by

$$L_1=\frac{4}{9\omega_0^2 C_{\mathrm{out}}}, \tag{3.100}$$

$$L_2=\frac{9}{15}L_1, \tag{3.101}$$

$$C_2=\frac{15}{16}C_{\mathrm{out}}, \tag{3.102}$$

where an inductance L_2 and a capacitance C_2 create a short-circuit condition at the second harmonic, and all elements create the parallel-resonant tanks for the fundamental and third harmonic components.[34]

As an example, the frequency-response characteristic of the load network with a parallel resonant circuit shown in Fig. 3.27A, whose parameters are calculated based on the chosen fundamental frequency $f_0=500\,\mathrm{MHz}$, is shown in Fig. 3.28. In this case, the load-network parameters are $C_{\mathrm{out}}=2.2\,\mathrm{pF}$, $R_{\mathrm{out}}=R_{\mathrm{L}}=200\,\Omega$, $C_2=5.3\,\mathrm{pF}$, $L_1=7.7\,\mathrm{nH}$, and $L_2=12.8\,\mathrm{nH}$, with an inductor quality factor $Q_{\mathrm{ind}}=20$. It should be noted that the PA efficiency can be even higher if the first element of the output matching circuit adjacent to the transistor output is series and inductive to provide high-impedance conditions at higher-order harmonics.

The efficiency of Class-F PA can be further increased by terminating a greater number of voltage harmonics. According to Table 3.1, for Class-F PA with maximally flat waveform, its theoretical value

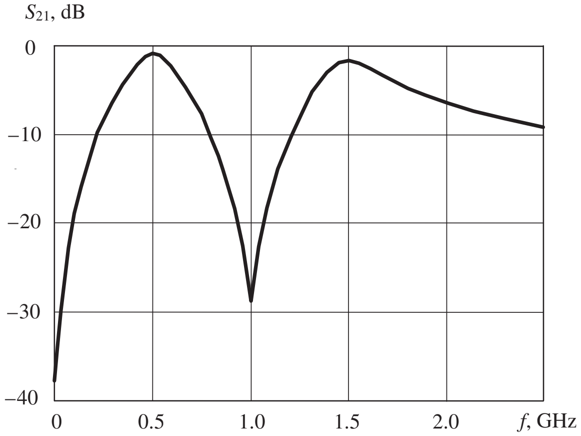


FIG. 3.28

Frequency response of load network with parallel resonant circuit.

can be improved from 88.4% to 92.0% by terminating up to the fifth voltage harmonic, assuming the half-sinusoidal drain current waveform. Fig. 3.29A shows the equivalent circuit of the harmonic termination network (HTN) representing an LC ladder circuit that includes the device output capacitance C_{out} as a first shunt capacitance.[39] In this case, the HTN provides short circuit at the even harmonics and open circuit at the odd harmonics of the fundamental frequency.

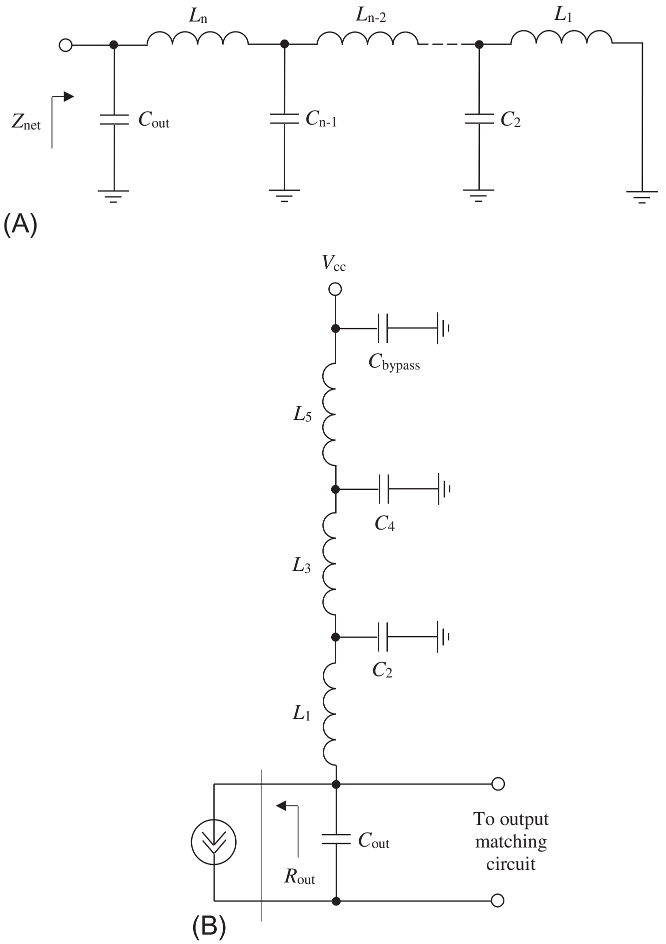
The equivalent impedance of the HTN shown in Fig. 3.29A is given by

$$Z_{\text{net}} = \frac{s\left(a_0 + a_2 s^2 + \cdots + a_{n-1} s^{n-1}\right)}{b_0 + b_2 s^2 + \cdots + b_{n+1} s^{n+1}}, \tag{3.103}$$

which provides $n+1$ imaginary poles and $n-1$ imaginary zeros, and zero at $s=0$ when n is an odd number. Thus the HTN can provide an open circuit at $(n+1)/2$ frequencies and a short circuit at $(n-1)/2$ frequencies. The HTN can be designed to terminate the total number of n harmonics. In the case of $n=3$, the HTN reduces to the circuit shown in Fig. 3.27B, while the HTN shown in Fig. 3.29B corresponds to the case of $n=5$.

For $n=5$, the coefficients of the numerator and denominator polynomials in Eq. (3.103) can be written as

$$\begin{aligned}
a_0 &= L_1 + L_3 + L_5,\\
a_2 &= L_1L_3C_2 + L_1L_5(C_2 + C_4) + L_3L_5C_4,\\
a_4 &= L_1L_3L_5C_2C_4,\\
b_0 &= 1,\\
b_2 &= L_1(C_2 + C_4 + C_{\text{out}}) + L_3(C_4 + C_{\text{out}}) + L_5C_{\text{out}},\\
b_4 &= L_1L_3C_2(C_4 + C_{\text{out}}) + L_1L_5C_{\text{out}}(C_2 + C_4) + L_3L_5C_4C_{\text{out}},\\
b_6 &= L_1L_3L_5C_2C_4C_6.
\end{aligned}$$



Ln
Ln-2
L1
Znet
Cout
Cn-1
C2
(A)
Vcc
Cbypass
L5
C4
L3
C2
L1
Cout
Rout
To output matching circuit
(B)

FIG. 3.29

Load networks with multiresonant circuit.

For Class-F operation, the HTN input impedance Z_{net} should include three pairs of imaginary poles at ω_0, $3\omega_0$, and $5\omega_0$, as well as two pairs of imaginary zeros at $2\omega_0$ and $4\omega_0$. By applying these conditions to Eq. (3.103), the ratios between the HTN elements are derived as

$$L_1 = \frac{7}{50\omega_0^2 C_{\text{out}}}, \tag{3.104}$$

$$L_3 = \frac{5}{9} L_1, \tag{3.105}$$

$$L_5 = \frac{6}{7} L_3, \tag{3.106}$$

$$C_2 = \frac{20}{7} C_{\text{out}}, \tag{3.107}$$

$$C_4 = \frac{15}{7} C_{\text{out}}, \tag{3.108}$$

with the total inductance of $0.28/\omega_0^2 C_{\text{out}}$.[39]

Fig. 3.30A shows the multiresonant load network that can provide an impedance transformation at the fundamental in addition to short circuit at the second harmonic and open circuit at the third harmonic seen by the device current source.[40] In this case, the inductance L_1 and capacitance C_1 are tuned to provide a short-circuit condition at the second harmonic, whereas the inductance L_2 and capacitance C_2 are tuned to provide an open-circuit condition at the third harmonic. Because the series L_1C_1 circuit has an inductive reactance at the third harmonic, the shunt circuit $C_{\text{out}}L_1C_1$ can be tuned to provide an open-circuit condition at the third harmonic when $C_1 = (5/4)C_{\text{out}}$ and $L_1 = 1/(5\omega_0^2 C_{\text{out}})$. The corresponding impedance matching at the fundamental is provided by adding the series capacitance $C_3 = 8C_2$ and the shunt inductance $L_3 = 1/(8\omega_0^2 C_{\text{out}})$ if the required value of C_2 is properly chosen. The fully integrated Class-F PA using the 4.8-mm LDMOS die and multiresonant load network shown in Fig. 3.30A achieved a drain efficiency of 54% with an output power of 36.4 dBm and a power gain of 15 dB at 1.8 GHz. Fig. 3.30B shows the intrinsic drain square-like voltage and current half-sinusoidal waveforms using the large-signal device model with on-wafer measured output termination. In view of realistic device model exhibiting a nonzero saturation voltage, care should be taken to optimize the device bias operating point in addition to the third-harmonic component of the drain voltage.[41]

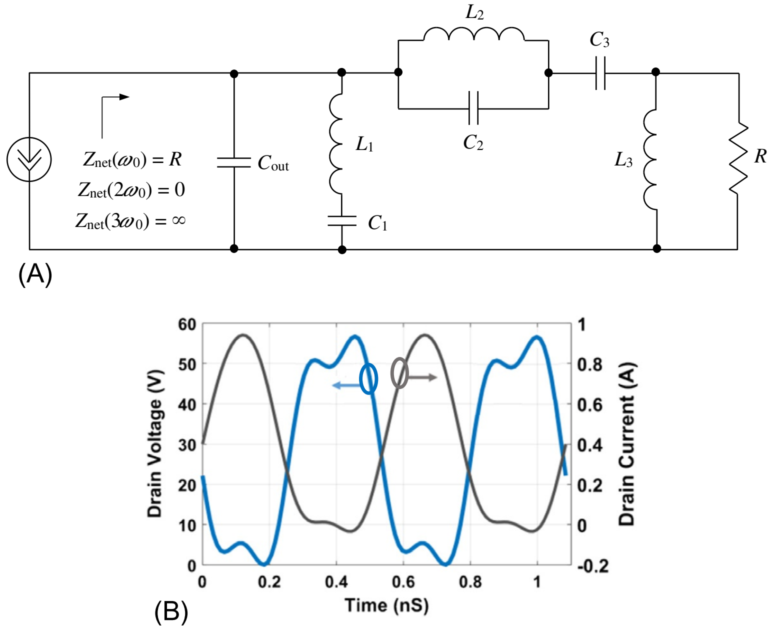


FIG. 3.30

Load network with second- and third-harmonic controls and drain voltage and current waveforms.

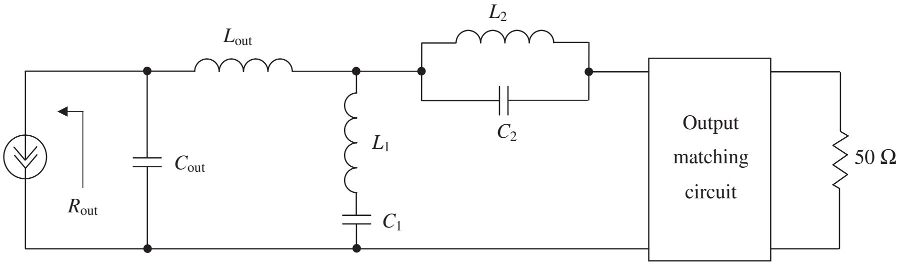


FIG. 3.31

Impedance-peaking load network including device output inductance.

Careful design must be provided at higher frequencies or in the case of high-power mode when the transistor equivalent output resistance at the fundamental frequency is sufficiently small. In this case, an effect of the output series inductance, including the bondwire and lead inductances for a packaged active device, becomes significant. The equivalent circuit of such an impedance-peaking load network is shown in Fig. 3.31. Here, the series circuit consisting of an inductor L_1 and a capacitor C_1 creates a short-circuit condition at the third harmonic. Because the output inductor L_{out} and capacitor C_{out} are tuned to create an open-circuit condition at the third harmonic, the device collector sees the resultant high impedance at the third harmonic.

To achieve the third-harmonic high impedance, an external series inductor may be added to interconnect the device output inductance L_{out} directly at the output terminal (collector or drain) if its value is smaller than required. In addition, the parallel resonant tank (L_2, C_2) is tuned to the second harmonic, while the series network (L_1+L_{out}, C_1) provides a short-circuit condition at the second harmonic.[38] As a result, the ratios between the load-network parameters are

$$L_{out} = \frac{1}{9\omega_0^2 C_{out}}, \tag{3.109}$$

$$L_1 = \frac{4}{5} L_{out}, \tag{3.110}$$

$$C_1 = \frac{5}{4} C_{out}, \tag{3.111}$$

$$L_2 = \frac{1}{4\omega_0^2 C_2}. \tag{3.112}$$

As a simple practical example, Fig. 3.32A shows the simplified circuit schematic of a two-stage GaAs HBT PA designed to use in cellphone transmitters in a frequency range of 698–716 MHz, where the final stage is operated in a Class-F mode with second-harmonic control. The second-harmonic short-circuit termination at the device collector is provided by the series circuit consisting of a bondwire and grounded external shunt capacitor that is connected to the device collector directly. At the same time, this second-harmonic short-circuit together with the RF choke and series load inductances implemented as narrow microstrip lines provide sufficiently high inductive impedance at the third harmonic. As a result, the collector efficiency of 73% was achieved at 710 MHz, corresponding to the collector voltage and current waveforms shown in Fig. 3.32B.

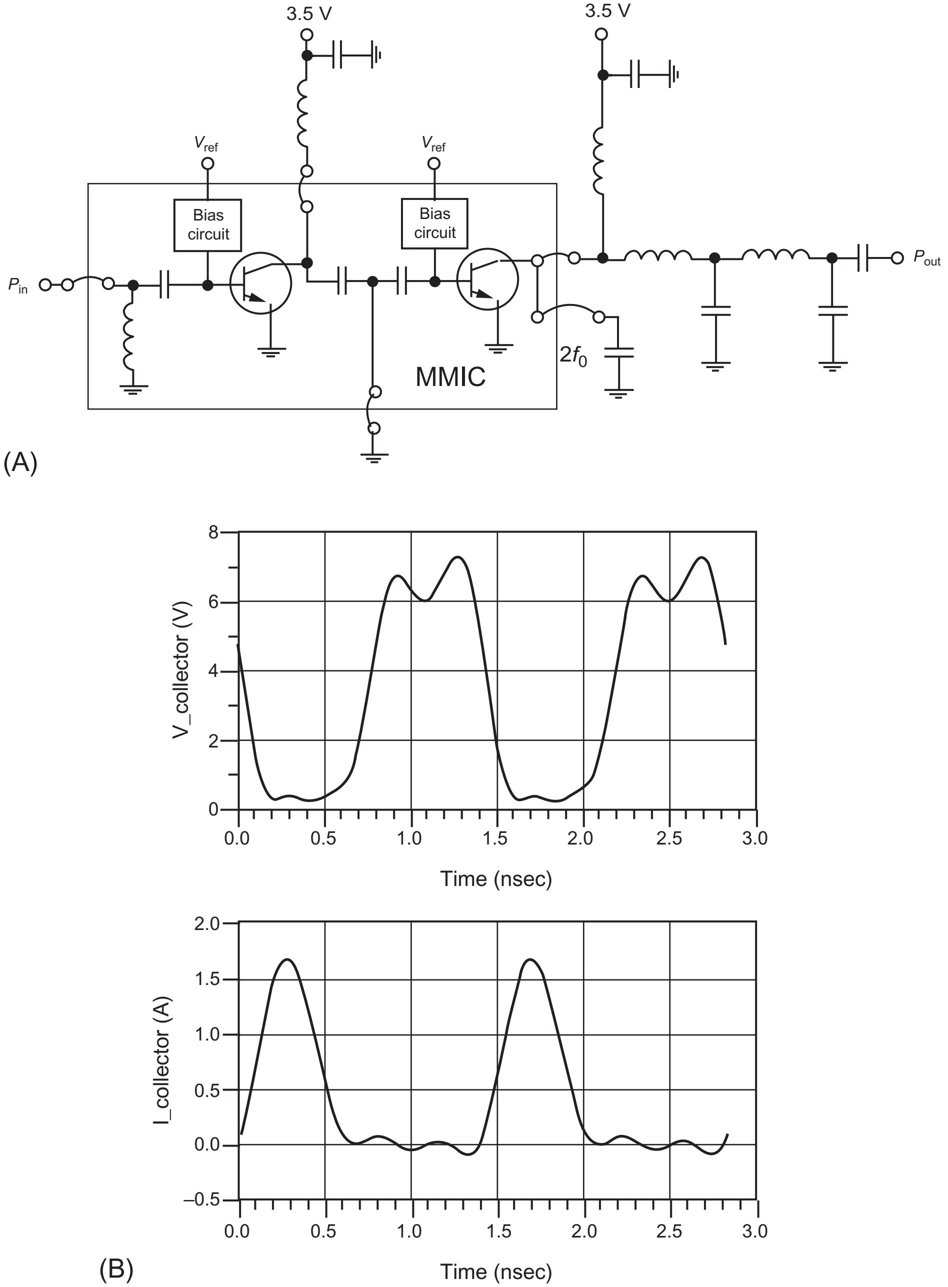

3.5 V
3.5 V
V_{ref}
V_{ref}
Bias circuit
Bias circuit
P_{in}
P_{out}
$2f_0$
MMIC
(A)
V_collector (V)
8
6
4
2
0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Time (nsec)
I_collector (A)
2.0
1.5
1.0
0.5
0.0
–0.5
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Time (nsec)
(B)

FIG. 3.32

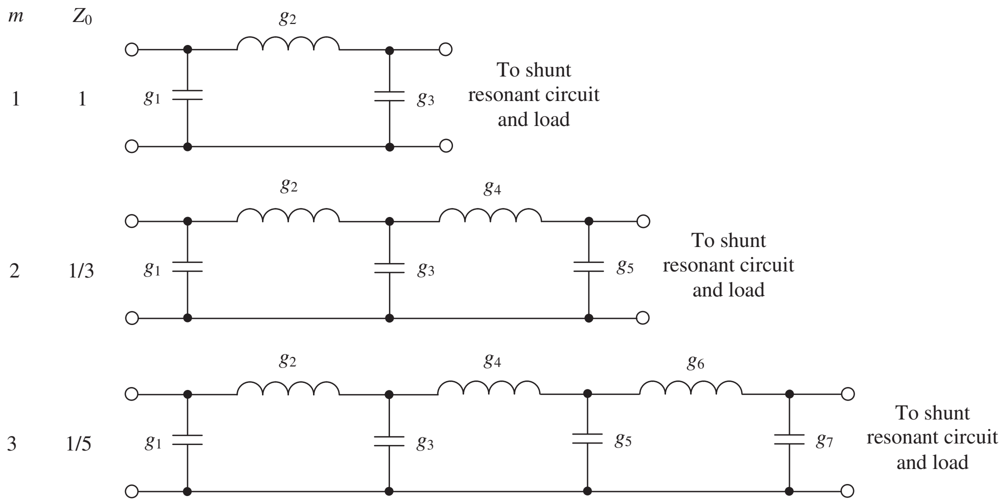
Schematic and collector voltage and current waveforms of two-stage GaAs HBT PA with second-harmonic control for handset application.

As a first approximation for comparison between different operation modes, the output device resistance R_{out} at the fundamental frequency required to realize a Class-F operation mode with third-harmonic peaking can be estimated as the equivalent resistance determined at the fundamental frequency for an ideal Class-F operation and written as $R_{\text{out}} = R_1^{(\text{F})} = V_1/I_1$, where V_1 and I_1 are the fundamental-frequency voltage and current amplitudes at the device output, respectively. Assuming zero saturation voltage and using Eqs. (3.23), (3.27) yield

$$R_1^{(\text{F})} = \frac{8}{\pi^2}\frac{V_{\text{cc}}}{I_0} = \frac{8}{\pi^2}\frac{V_{\text{cc}}^2}{P_1} = \left(\frac{4}{\pi}\right)^2 R_1^{(\text{B})}, \tag{3.113}$$

where $R_1^{(\text{B})} = V_{\text{cc}}/I_1 = V_{\text{cc}}^2/2P_1$ is the device equivalent output resistance at the fundamental frequency in an ideal Class-B mode.

The load network can represent a series low-pass *LC* ladder network commencing with a shunt capacitor and terminated with a narrowband shunt resonant circuit in parallel with the resistive load.[25] In this case, the device output capacitance can be a part of the external load network. This *LC* ladder-type load network should provide the correct complex impedance at the fundamental frequency, a short-circuit at the first $(2m - 2)$ even harmonics, an open circuit at the first $(2m - 1)$ odd harmonics, and reactive terminations at all harmonics $2m$ and above. The configurations of these networks for values of m up to the third degree with corresponding normalized coefficients g_i are shown in Fig. 3.33.


m
Z0
1
1
2
1/3
3
1/5
g1
g2
g3
g4
g5
g6
g7
To shunt resonant circuit and load
To shunt resonant circuit and load
To shunt resonant circuit and load

m	g_1	g_2	g_3	g_4	g_5	g_6	g_7
1	1	1	1				
2	1	1/6	12/5	5/18	9/5		
3	1	1/15	15/7	7/90	20/7	7/50	50/21

FIG. 3.33

Ideal ladder low-pass Class-F load networks and their parameters.

The general formulas for explicit values of the elements in the low-pass ladder load network with arbitrary degree based on a cutoff frequency $\omega_c = 1$ and a reference impedance of 1 Ω are derived from

$$\begin{aligned} g_1 g_2 &= \frac{1}{m(2m-1)}, \\ g_i g_{i+1} &= \frac{4}{(2m-1+i)(2m-i)}, \\ g_{2m} g_{2m+1} &= \frac{1}{m}, \end{aligned} \tag{3.114}$$

where $g_1 = 1$, and the characteristic impedance of the network operating as an impedance inverter which is obtained by

$$Z_0 = \frac{1}{2m-1}, \tag{3.115}$$

where $2 \le i \le 2m - 1$. By using such a low-order low-pass *LC* ladder network for input and output matching with second- and third-harmonic controls at the device input and output terminals simultaneously, a drain efficiency of 76% for a Class-F PA implemented in a 0.5-μm pHEMT process was achieved at an operating frequency of 1.84 GHz with 16 W of output power.[42]

3.7 Load networks with transmission lines

Instead of a quarterwave transmission line to provide short-circuit for even harmonics and open circuit for odd harmonics, a combination of short-length series microstrip lines and open-circuit stubs can be used to properly control a limited number of harmonics to approximate the Class-F mode that allows to reduce overall PA size and to increase efficiency of the operation. Fig. 3.34 shows the circuit schematic of a high-efficiency Class-F two-stage GaAs FET PA having a total efficiency of 70% and an output power of 2 W designed to operate at 900 MHz.[43] A drain efficiency of 80% was achieved at a low supply voltage of 6 V. These high efficiencies were obtained by using even-harmonic tuning of an output matching circuit. In this case, the harmonic impedance was short at even harmonics, and impedance at odd harmonics was not considered from the point of view of obtaining the maximum output power. The output circuit was designed under the assumption that the parasitic device parameters can be

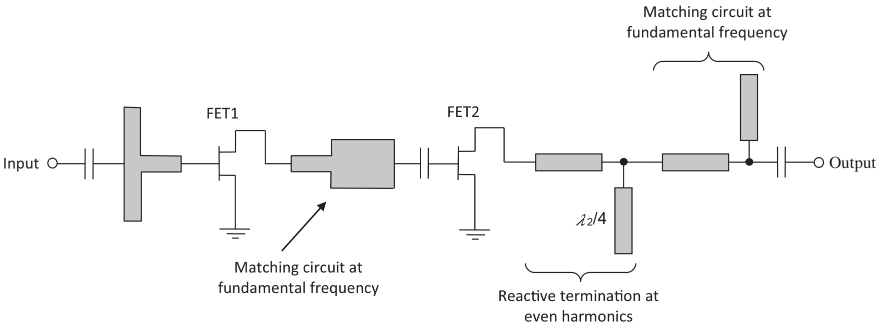

Matching circuit at fundamental frequency
FET1
FET2
Input
Output
$\lambda_2/4$
Matching circuit at fundamental frequency
Reactive termination at even harmonics

FIG. 3.34

Schematic of high-efficiency Class-F FET PA with even-harmonic short.

represented as a transmission line, and the GaAs FET consists of a current source and an equivalent transmission line at harmonic frequencies so that, when seen from the current source, a short circuit is observed for even harmonics. In Fig. 3.34, the transmission line between FET2 and the open-circuited $\lambda_2/4$ microstrip line, where $\lambda_2/4$ is the wavelength of the second-harmonic frequency, is a compensation line for the equivalent transmission line of the GaAs FET. The circuit between the output terminal and the open-circuited $\lambda_2/4$ microstrip line is a matching network that converts the FET output impedance containing the reactive component to $50\,\Omega$.

Generally, the design of a transmission-line or distributed matching circuit can be based on approximate equivalence between lumped and distributed elements that can be established by applying a Richards' transformation that provides a sequence of equal-length open- and short-circuited transmission lines representing redundant transmission-line sections as unit elements of $\lambda/8$ long at cutoff frequency ω_c.[44] The transmission-line impedances and electrical lengths of the load network can then be optimized and tuned to simultaneously provide the correct impedance at the fundamental frequency and the required complex terminations.[45] The shunt fundamentally tuned resonant circuit can be realized using a quarter-wavelength transmission line, which operates as a harmonic short at even harmonics.

It is problematic to realize the ladder *LC* load network by using commercially available lumped element chip capacitors and inductors due to their self-resonance frequency and insertion loss limitations. Therefore at higher frequencies, it is useful to transform a lumped ladder circuit to its distributed equivalent based on a multisection stepped-impedance transmission line. As an example shown in Fig. 3.35, the two-section lumped ladder *LC* circuit, including the device parasitic shunt output capacitance C_p and series bondwire inductance L_p, can equivalently be transformed to a corresponding Class-F load network with a series two-section stepped-impedance transmission line, whose transmission-line sections are characterized by the characteristic impedances $Z_i = \sqrt{L_i/C_i}$ and electrical lengths $\theta_i = \sin^{-1}\left(\omega_0\sqrt{L_iC_i}\right)$, where $i = 1, 2$.[46] Because poles of the input impedance of the stepped-impedance transmission line can vary depending on the ratio of the characteristic impedances and electrical lengths of the transmission-line sections, the entire circuit with parasitic elements can be optimized to provide a short-circuit condition at even harmonics and open-circuit condition at odd

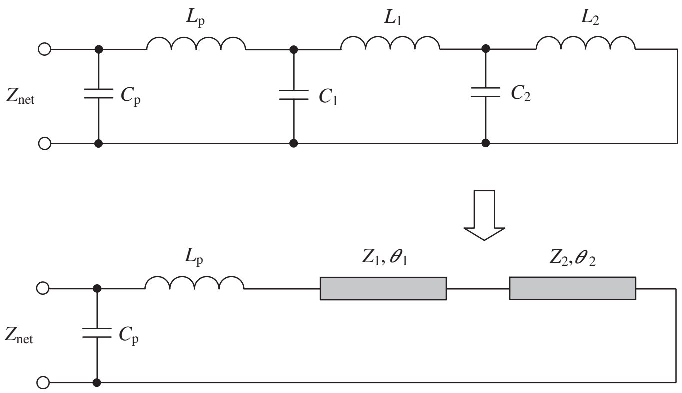


FIG. 3.35

Transformation from lumped to distributed Class-F load network.

harmonics. The experimental results of the fabricated 2-W 25-V microstrip GaN HEMT Class-F PA show a maximum drain efficiency of about 80% at an operating frequency of 5.86 GHz.

The optimum impedance matching at the fundamental frequency with the second- and third-harmonic tuning can be provided by using the series transmission-line sections and shunt open-circuit or short-circuit stubs to obtain open-circuit peaking and short-circuit termination seen by the device output at corresponding harmonic component.[47] Such an approach is very simple in terms of the load-network design and very convenient for practical implementation. Fig. 3.36A shows the idealized basic configuration of the transmission-line Class-F load network where a shunt quarter-wavelength transmission line providing a short-circuit termination for even voltage harmonic at the device output is connected to the DC power supply with a bypass capacitor.[48] The series transmission-line section and open-circuit stub, both having an electrical length of 30 degrees at the fundamental frequency, provide an open-circuit mode at the third harmonic because an open-circuit stub has a quarter wavelength at the third harmonic to realize a short-circuit condition at the right-hand side of the series transmission line

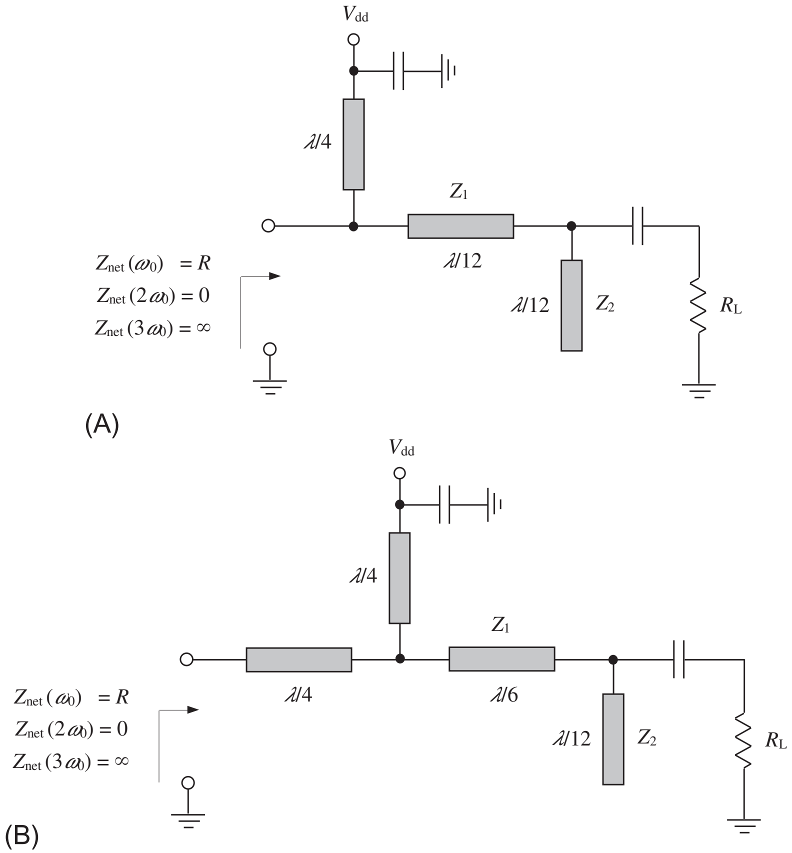

V_{dd}
$\lambda/4$
Z_1
$\lambda/12$
$Z_{net}(\omega_0) = R$
$Z_{net}(2\omega_0) = 0$
$Z_{net}(3\omega_0) = \infty$
$\lambda/12$
Z_2
R_L
(A)
V_{dd}
$\lambda/4$
Z_1
$\lambda/4$
$\lambda/6$
$Z_{net}(\omega_0) = R$
$Z_{net}(2\omega_0) = 0$
$Z_{net}(3\omega_0) = \infty$
$\lambda/12$
Z_2
R_L
(B)

FIG. 3.36

Idealized transmission-line Class-F load networks.

having a quarter wavelength at the third harmonic as well. The ideal Class-F PA with all even harmonic short-circuit termination and third harmonic peaking achieves a maximum drain efficiency of 88.4%. Such a Class-F load network implemented using coplanar lines into a 24-GHz MMIC GaAs pHEMT PA had contributed to a drain efficiency of 59% at an output power of 20 dBm.[49]

The load-network impedance Z_{net} seen by the device output at the fundamental frequency can be written as

$$Z_{\text{net}} = Z_1 \frac{R_L(Z_2 - Z_1 \tan^2\theta) + jZ_1Z_2\tan\theta}{Z_1Z_2 + j(Z_1 + Z_2)R_L\tan\theta}, \tag{3.116}$$

where $\theta = \theta_1 = \theta_2 = 30$ degrees, Z_1 and θ_1 are the characteristic impedance and electrical length of the series transmission line, and Z_2 and θ_2 are the characteristic impedance and electrical length of the open-circuit stub, respectively. Hence the impedance matching with the load at the fundamental can be provided by proper choice of the characteristic impedances Z_1 and Z_2.

Separating Eq. (3.116) into real and imaginary parts and taking into account that $\text{Re}Z_{\text{net}} = R$ and $\text{Im}Z_{\text{net}} = 0$, the system of two equations with two unknown parameters is obtained as

$$Z_1^2Z_2^2 - R_L^2(Z_1 + Z_2)\left(Z_2 - Z_1\tan^2\theta\right) = 0, \tag{3.117}$$

$$(Z_1 + Z_2)^2 R_L^2 R \tan^2\theta - Z_1^2Z_2^2\left[R_L\left(1 + \tan^2\theta\right) - R\right] = 0, \tag{3.118}$$

which enables the characteristic impedances Z_1 and Z_2 to be properly calculated. This system of two equations can be explicitly solved as a function of the parameter $r = R_L/R$ resulting in.

$$\frac{Z_1}{R_L} = \frac{\sqrt{4r - 3}}{r}, \tag{3.119}$$

$$\frac{Z_1}{Z_2} = 3\left(\frac{r - 1}{r}\right). \tag{3.120}$$

Consequently, for the specified value of the parameter r with the required Class-F optimum fundamental-frequency load resistance R and standard load resistance $R_L = 50\,\Omega$, the characteristic impedance Z_1 is calculated from Eq. (3.119), and then the characteristic impedance Z_2 is calculated from Eq. (3.120). For example, if the required Class-F optimum load resistance R is equal to 12.5 Ω, resulting in $r = 4$, the characteristic impedance of the series transmission line Z_1 is equal to 45 Ω and the characteristic impedance of the open-circuit stub Z_2 is equal to 20 Ω.

Fig. 3.36B shows the simplified Class-F load network with the second- and third-harmonic tuning using a series quarter-wavelength transmission line that provides zero impedance at the second-harmonic and infinite impedance at the third-harmonic components.[50] The short-circuit impedances at right-hand side of the series quarter-wavelength transmission line is provided by the short-circuited shunt quarter-wavelength transmission line at the second harmonic and an open-circuit $\lambda/12$ stub together with a series $\lambda/6$ transmission line at the third harmonic. In this case, an impedance matching at the fundamental frequency can be provided either using a separate matching circuit or by optimizing the characteristic impedances of the load-network transmission lines.

The close approximation to an ideal Class-F mode in the microwave region can be achieved by using a load network shown in Fig. 3.37, where each open-circuit stub has a quarter wavelength at each higher-order harmonic of the fundamental frequency providing zero impedance at the higher harmonic at point A.[51] The transmission line TL_{11} having a quarter wavelength at the fundamental frequency

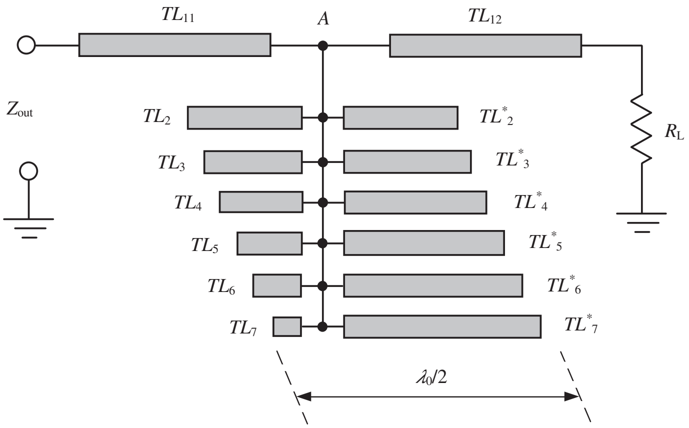


FIG. 3.37

Class-F load network with reactance compensation circuits.

transforms these zero impedances into open-circuit impedance at odd harmonics and short-circuit impedance at even harmonics seen from the device output. The quarterwave transmission line TL_{12} is necessary for impedance matching at the fundamental frequency of the output impedance $Z_{\rm out}$ with the standard load $R_{\rm L}$. To compensate for the reactive impedance at the fundamental frequency due to the open-circuit stubs TL_2, …, TL_7, the reactance compensation open-circuit stubs TL^*_2, …, TL^*_7 are added in series to form an overall half wavelength for each stub. However, such a Class-F load network can be effectively used at low power levels when the device parasitic output capacitance $C_{\rm out}$ is sufficiently small.

However, the efficiency of the PA can be limited by the transistor output capacitance $C_{\rm out}$ (mostly represented by the drain-source capacitance $C_{\rm ds}$ or collector capacitance $C_{\rm c}$) if this capacitance is not absorbed into a multiharmonic load network without compromising the ability to properly terminate the second- and third-harmonic components. Fig. 3.38A shows the simplified circuit schematic of the transmission-line transistor PA, whereas the equivalent load network corresponding to Class-F mode with a shunt short-circuited quarter-wavelength transmission line that provides a short circuit at even harmonics is shown in Fig. 3.38B.[37, 38]

In Class-F mode with a transmission-line load network shown in Fig. 3.38B, the electrical length of an open-circuit stub TL_3 is chosen to have a quarter wavelength at the third harmonic to realize short-circuit condition at the right-hand side of the series transmission line TL_2, whose electrical length θ_2 should provide an inductive reactance to resonate with the device output capacitance $C_{\rm out}$ at the third harmonic. In this case, a quarterwave transmission line TL_1, which is located between the DC power supply and drain terminal, provides short-circuit termination for even voltage harmonics. Such a load network is very practical when the DC drain voltage is very high to increase the device output impedance, or the operating frequency is sufficiently low, and bare die is used instead of packaged transistor to easily absorb bondwire inductances by the load network.[52] As a result, the electrical lengths of the transmission lines at the fundamental frequency can be obtained as

$$\theta_1 = \frac{\pi}{2}, \tag{3.121}$$

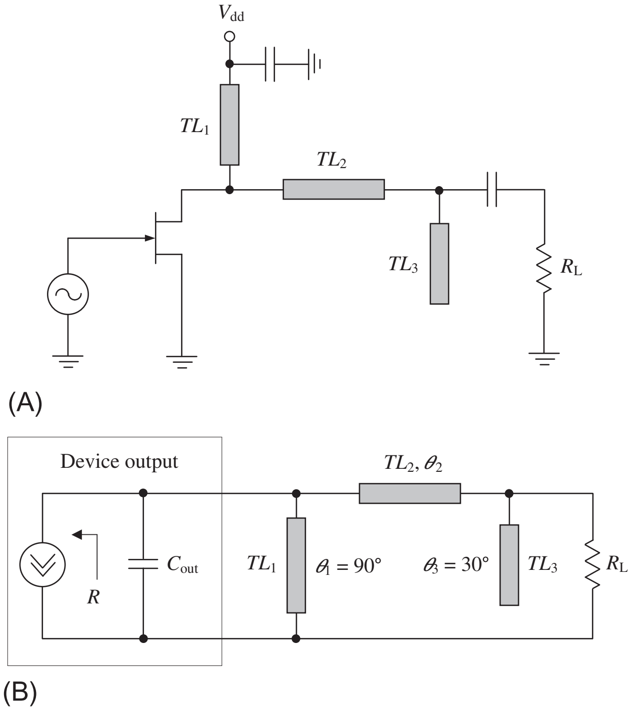


FIG. 3.38

Transmission-line Class-F load network with shunt capacitance.

$$\theta_2 = \frac{1}{3}\tan^{-1}\left(\frac{1}{3Z_0\omega_0 C_{out}}\right), \tag{3.122}$$

$$\theta_3 = \frac{\pi}{6}, \tag{3.123}$$

where Z_0 is the characteristic impedance of the series transmission line TL_2, and ω_0 is the fundamental radian frequency.

Fig. 3.39 shows an example of the frequency-response characteristic of the microstrip impedance-peaking circuit shown in Fig. 3.38B, assuming an alumina substrate for microstrip lines and the device equivalent output resistance $R = 50\,\Omega$ and output capacitance $C_{out} = 2.2\,\text{pF}$, microstrip-line characteristic impedance $Z_0 = 50\,\Omega$, and electrical length $\theta_2 = 15$ degrees, according to Eq. (3.122). From Fig. 3.39, it follows that the corresponding short-circuited conditions for all even harmonics and third-harmonic peaking have been provided. However, an additional output impedance matching to compensate for the reactive part and to match the real part of the equivalent output impedance with the standard 50-Ω load impedance at the fundamental frequency $f_0 = 500\,\text{MHz}$ is required by optimizing the characteristic impedances of the series microstrip line TL_2 and open-circuit stub TL_3.

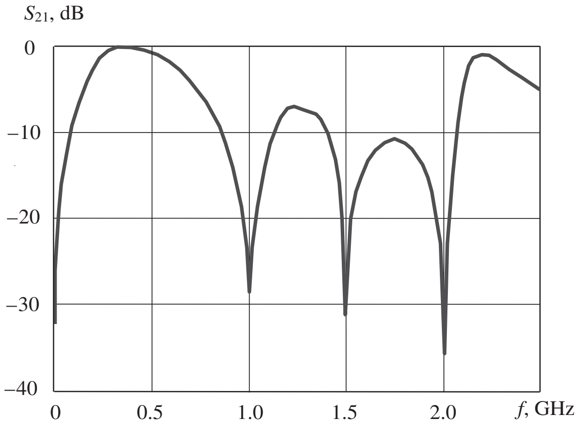


FIG. 3.39

Frequency response of microstrip impedance-peaking circuit.

When the Class-F PA is fabricated as a hybrid integrated circuit, there is a need to take into account the influence of the parasitic series bondwire inductance. In this case, it is possible to use either an additional series compensation line connected to the device output[53] or a load network with optimized parameters, as shown in Fig. 3.40A.[54] In the latter case, the open-circuit condition for the third harmonic can be satisfied by modifying Eq. (3.122) as

$$\theta_2 = \frac{1}{3}\tan^{-1}\left(\frac{1}{3Z_0\omega_0 C_{\text{out}}} - \frac{3\omega_0 L_{\text{out}}}{Z_0}\right), \tag{3.124}$$

where θ_2 is the electrical length of the series transmission line TL_2 at the operating frequency ω_0, with the characteristic impedance Z_0. However, the short-circuit condition for the second- and higher-order even harmonics cannot be met, and the performance of the Class-F PA is adversely affected as the operating frequency increases. Therefore the transistor drain voltage and current waveforms are not perfectly symmetrical, which are characterized by significant transition times from the saturation region to the pinch-off region and vice versa, mainly because of the effect of the second harmonic having the certain phase shift providing by the series bondwire inductance.

The more complicated impedance-peaking circuit to improve efficiency, including the output series parasitic inductance L_{out}, which can generally represent the bondwire and package lead inductances, is shown in Fig. 3.40B. Here, to create the second harmonic short-circuit condition and third-harmonic peaking, it is convenient to use a combination of the open-circuit and short-circuit transmission-line stubs in the load network. The device output elements L_{out} and C_{out} must create a parallel resonance at the third harmonic of the fundamental frequency as the short-circuit stub TL_1 has a half wavelength at the third harmonic with short-circuit conditions at its both ends. It should be mentioned that the open-circuit stub having a quarter wavelength at the third harmonic of the fundamental frequency can also be used.[55] The electrical length θ_2 of an open-circuit stub TL_2 is chosen to have less than a quarter wavelength at the second harmonic to realize an overall capacitive reactance together with the short-circuited transmission line TL_1 to be resonant with output inductance L_{out} at the second harmonic

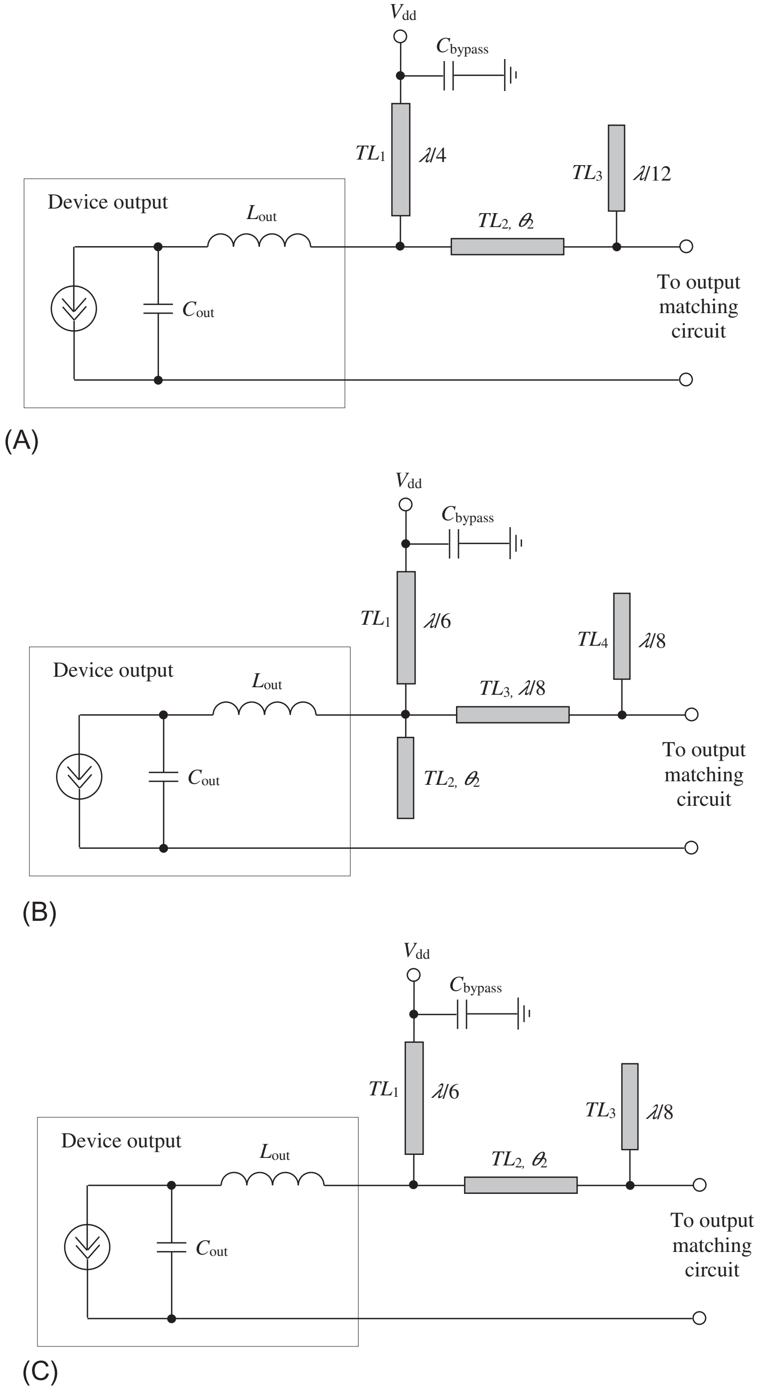

(A)
V_{dd}
C_{bypass}
TL_1
$\lambda/4$
TL_3
$\lambda/12$
Device output
L_{out}
TL_2, θ_2
C_{out}
To output matching circuit
(B)
V_{dd}
C_{bypass}
TL_1
$\lambda/6$
TL_4
$\lambda/8$
Device output
L_{out}
$TL_3, \lambda/8$
TL_2, θ_2
C_{out}
To output matching circuit
(C)
V_{dd}
C_{bypass}
TL_1
$\lambda/6$
TL_3
$\lambda/8$
Device output
L_{out}
TL_2, θ_2
C_{out}
To output matching circuit

FIG. 3.40

Transmission-line Class-F load networks, including device bondwire inductance.

of the fundamental frequency. In this case, it is preferable to use the transmission line TL_2 with a high characteristic impedance Z_0. The transmission lines TL_3 and TL_4 must be of quarter wavelengths at the second harmonic to provide the second-harmonic high impedance condition at the input of TL_3. As a result, the ratios between the load-network parameters are.[38]

$$L_{\mathrm{out}} = \frac{1}{9\omega_0^2 C_{\mathrm{out}}}, \tag{3.125}$$

$$\theta_2 = \frac{1}{2}\tan^{-1}\left(\frac{Z_0}{2\omega_0 L_{\mathrm{out}}} - \frac{1}{\sqrt{3}}\right), \tag{3.126}$$

where Z_0 is the characteristic impedance of both short-circuited and open-circuited transmission lines TL_1 and TL_2.

The impedance-peaking circuit shown in Fig. 3.40B, which provides short circuit at the second harmonic and open circuit at the third harmonic, can be simplified by removing the open-circuited transmission line TL_2 and properly setting the electrical length of the transmission line TL_3, which corresponds to the transmission line TL_2 with the electrical length θ_2, shown in Fig. 3.40C. As a result,

$$\theta_2 = \frac{1}{2}\tan^{-1}\left(\frac{1}{\sqrt{3}} - \frac{Z_0}{2\omega_0 L_{\mathrm{out}}}\right)^{-1}, \tag{3.127}$$

where Z_0 is the characteristic impedance of both short-circuited transmission lines TL_1 and TL_2. The electrical length θ_2 of a series transmission line TL_2 should be properly chosen according to Eq. (3.127) to provide an overall capacitive reactance together with the short-circuited transmission line TL_1 to be resonant with output inductance L_{out} at the second harmonic of the fundamental frequency. In this case, it is preferable to use the transmission line with low characteristic impedance Z_0.

3.8 LDMOSFET PA design examples

The effectiveness of the Class-F load-network design technique can be demonstrated based on the example of high-power LDMOSFET amplifiers. The small-signal equivalent circuit of the LDMOSFET cell with a gate length of 1.25 μm and a gate width of 1.44 mm is shown in Fig. 3.41A.[44] The device model parameters were extracted from pulsed current-voltage (I–V) and small-signal S-parameter measurements. The parameters of the small-signal device equivalent circuit are given at a bias voltage for Class-AB with a quiescent current $I_q = 15$ mA at a supply voltage $V_{\mathrm{dd}} = 28$ V. The measured and modeled output $I_{\mathrm{ds}} - V_{\mathrm{ds}}$ characteristics of the high-power device with a total gate width of 28 × 1.44 mm are shown in Fig. 3.41B. Based on these characteristics, it is easy to choose the peak drain current, which allows us to maximize the drain efficiency by minimizing the saturation voltage. For example, choosing a peak current of 3.5 A results in a DC current of approximately $3.5/\pi \approx 1.1$ A, according to Eqs. (3.21), (3.23), which leads to a saturation voltage of about 4 V. As a result, the maximum drain efficiency of about 80%, providing a delivery of the output power of more than 20 W into the load, can be achieved at a DC-supply voltage of 24 V.

The circuit schematic of the simulated 500-MHz single-stage lumped LDMOSFET PAs is shown in Fig. 3.42. In this case, the total gate width of a high-voltage LDMOSFET device is 7 × 1.44 mm to achieve 8 W of output power. The drain efficiency and power gain of the amplifier versus input power

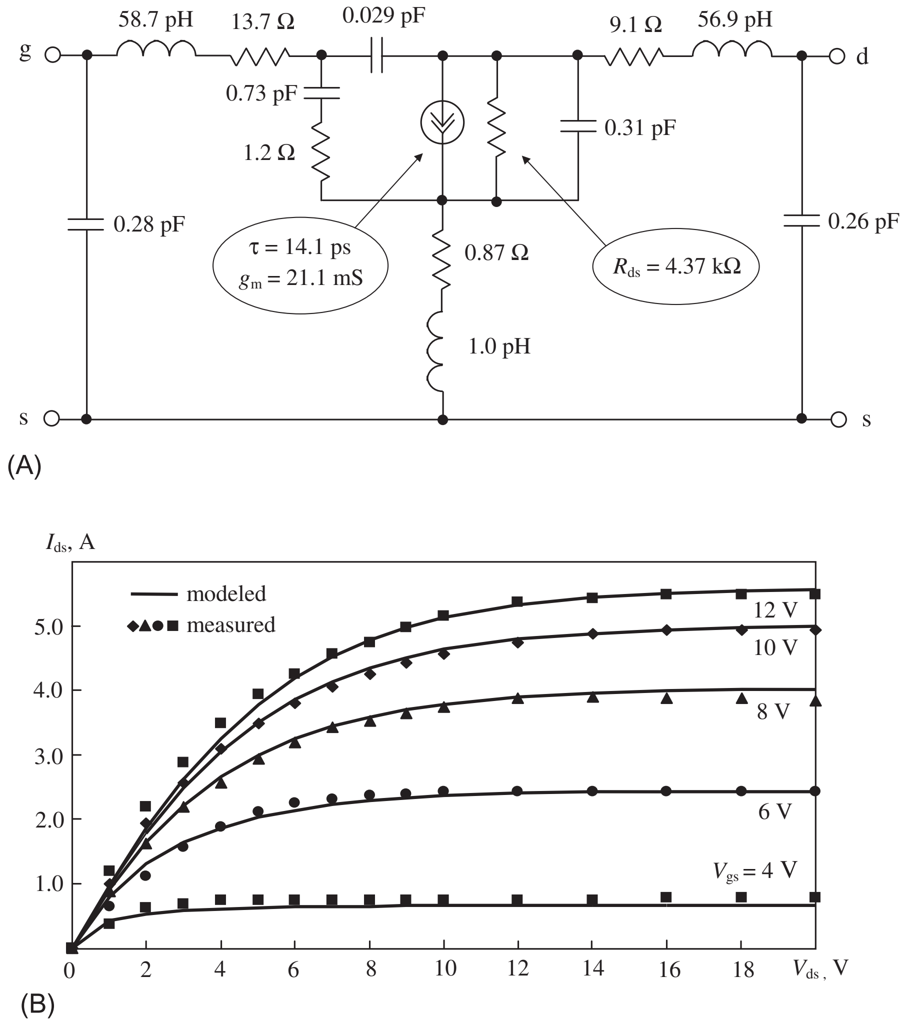

58.7 pH
13.7 Ω
0.029 pF
9.1 Ω
56.9 pH
g
d
0.73 pF
1.2 Ω
0.31 pF
0.28 pF
τ = 14.1 ps
g_m = 21.1 mS
0.87 Ω
R_{ds} = 4.37 kΩ
0.26 pF
1.0 pH
s
s
(A)
I_{ds}, A
modeled
◆▲●■ measured
5.0
4.0
3.0
2.0
1.0
12 V
10 V
8 V
6 V
V_{gs} = 4 V
0
2
4
6
8
10
12
14
16
18
V_{ds}, V
(B)

FIG. 3.41

Small-signal LDMOSFET equivalent circuit and output *I–V* curves.

P_{in} for the case of ideal inductors are given in Fig. 3.43A. The drain efficiency over 75% (curve 2) is obtained due to short-circuit condition at the second harmonic and open-circuit conditions at the third harmonic. Generally, it is important to provide high-impedance conditions at higher-order harmonics that can be readily obtained by using an output matching circuit with the series inductor as a first element. This shortens the switching time from pinch-off region to voltage-saturation region by better approximating the idealized drain voltage square waveform, as shown in Fig. 3.43C. It should be noted that the drain current waveform differs from a half-sinusoidal waveform because it includes

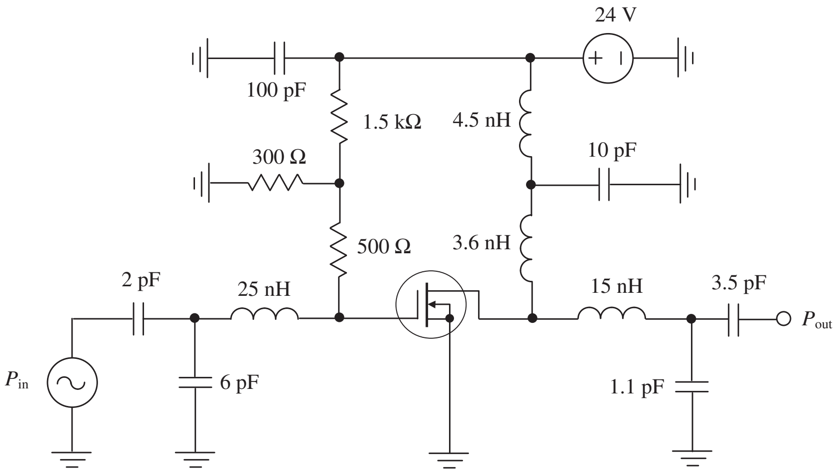


FIG. 3.42

Simulated lumped LDMOSFET Class-F PA.

higher-order odd harmonic components together with the current flowing through the device intrinsic equivalent circuit capacitors.

As follows from Eq. (3.32) for a symmetrical voltage waveform, the initial phases for the fundamental frequency and its harmonics should be equal, which is easy to realize by short-circuit and open-circuit conditions. However, according to Eq. (3.33) for a half-sinusoidal current waveform, the phases for any harmonic component should differ from the phase for the fundamental frequency by 90 degrees. This condition is easily realized in a Class-B load network where the fundamental component of the drain voltage is in phase with the fundamental component of the drain current, but for all higher-order current harmonics, the impedance of the resonant circuit will be capacitive because the drain current harmonics mostly flow through the shunt capacitor. Therefore the accurate harmonic phasing is very important to improve the effectiveness of a Class-F load network. The drain efficiency and power gain will be significantly reduced when the values of the quality factor of the load-network inductors are sufficiently small. For example, the maximum value of the drain efficiency can reach only 71% when an inductor quality factor at the fundamental frequency is $Q_{\text{ind}} = 30$, as shown in Fig. 3.43B.

Therefore at high power level, it is preferred to use the load networks that employ microstrip lines. The equivalent circuit of a simulated 500-MHz single-stage microstrip LDMOSFET PA using an active device with the same geometry is shown in Fig. 3.44. The input and output matching circuits represent a *T*-type matching circuit, each consisting of a series microstrip line, a parallel open-circuit stub, and a series capacitor. To provide even-harmonic short-circuit termination and third-harmonic peaking for a Class-F mode, an RF grounded quarterwave microstrip line and a combination of the series short-length microstrip line and open-circuit stub with electrical length of 30 degrees at the fundamental frequency each are used. Such an output-circuit configuration approximates the square drain voltage waveform with a good accuracy, as shown in Fig. 3.45A, and provides a drain efficiency over 75% with a maximum output power of 8 W, as shown in Fig. 3.45B. The smaller value of the drain efficiency

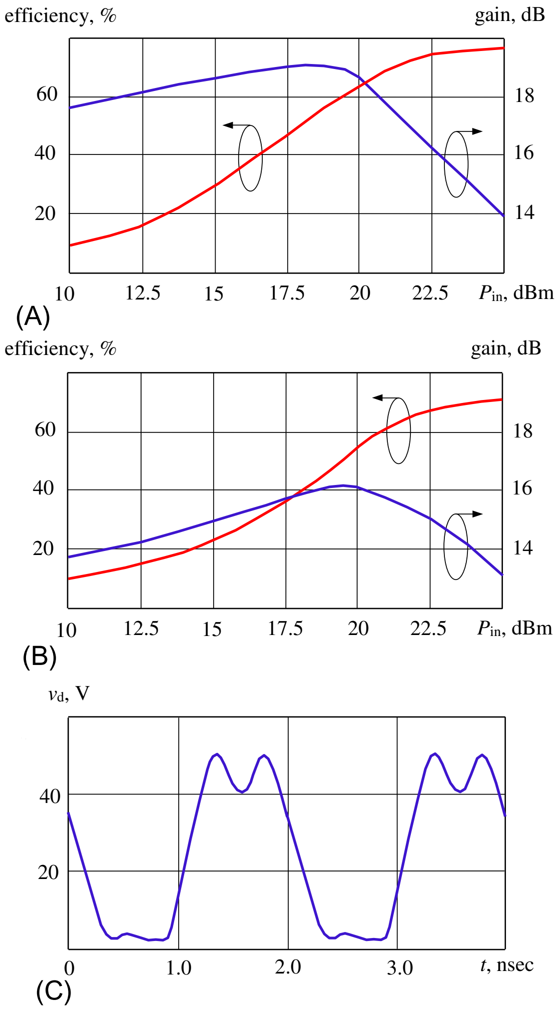


FIG. 3.43

Drain efficiency, power gain, and voltage waveform.

compared to the theoretically achievable value can be explained by the nonoptimized impedances at higher-order harmonics because, unlike a lumped inductor, the transmission line exhibits an equidistant impedance performance in the frequency domain with consecutive poles and zeros at the characteristic frequencies. This means that using a simple T-type transmission-line transformer does not provide high impedance conditions at all higher-order harmonics simultaneously.

It should be mentioned that, at frequencies close to the device transition frequency f_T, the drain (or collector) waveform becomes stretched due to a delay effect of the transistor input circuit with different

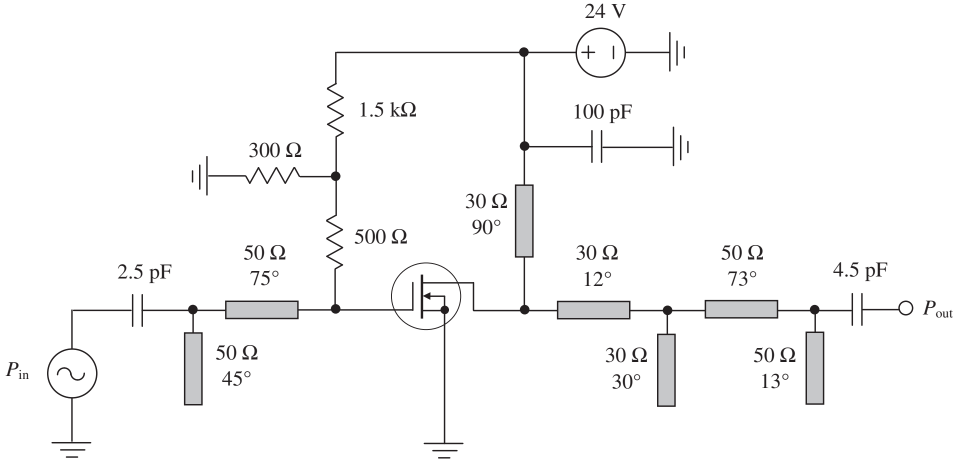

24 V
+
100 pF
1.5 kΩ
300 Ω
500 Ω
30 Ω
90°
2.5 pF
50 Ω
75°
30 Ω
12°
50 Ω
73°
4.5 pF
P_{out}
P_{in}
50 Ω
45°
30 Ω
30°
50 Ω
13°

FIG. 3.44

Simulated microstrip LDMOSFET Class-F PA.

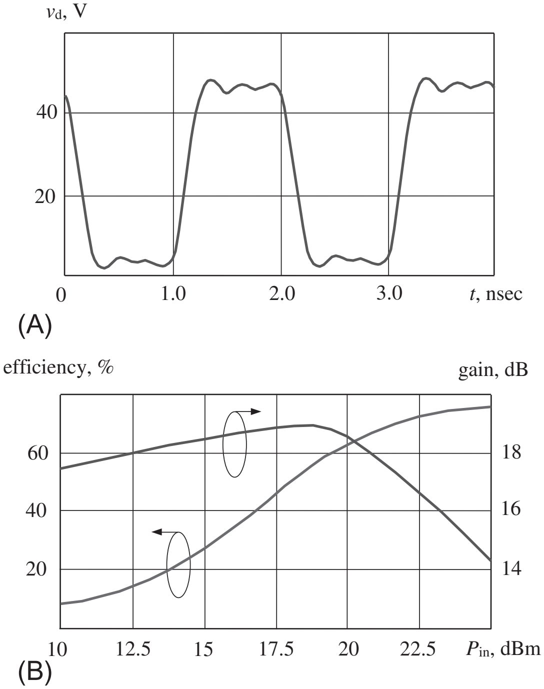


FIG. 3.45

Drain voltage waveform, efficiency, and power gain.

and significant phase shifts $\omega\tau_{\mathrm{in}} = \omega R_{\mathrm{in}} C_{\mathrm{in}}$ for higher-order harmonic components, where R_{in} is the series input resistance (gate resistance for field-effect transistor or base resistance for bipolar transistor) and C_{in} is the shunt input capacitance (gate-source capacitance for field-effect transistor or diffusion base–emitter capacitance for bipolar transistor). In this case, the concept of the low-frequency conduction angle is not valid anymore when the fundamental-frequency and third-harmonic components of the output voltage are 180 degrees out-of-phase for conduction angles above 180 degrees. In other words, the low-frequency or external conduction angle considered at the input of the transistor is different from the high-frequency or internal conduction angle considered at the transistor junction directly because of a transient effect of the device input circuit. Thus to achieve a 50% duty ratio of the collector voltage, the low-frequency conductance angles at the input may be significantly less than 180 degrees.[56] In addition, it is useful to introduce an additional phase shift at the third-harmonic component by tuning a third-harmonic component to make the collector voltage waveform more symmetrical.

3.9 Broadband capability of Class-F PAs

Generally, the high-efficiency Class-F performance can be realized across the relatively narrow frequency bandwidth because of high-*Q* resonant conditions at the fundamental-frequency and higher-order harmonic components. However, for a sufficiently low-power device when the real part of its input and load impedances is close to 50 Ω, it becomes possible to simplify the design of the broadband input matching circuit and load network. In this case, it is enough to use a simple lossy input matching circuit composed of a single series inductive element, which can be realized using a high-impedance microstrip line, and a series small-value resistor, with a shunt resistor added to the gate-bias circuit, whose value is sufficiently small. It is also important to include both resistors to provide unconditionally stable operating conditions. The load network can be designed primarily to achieve quasi-optimal Class-F loads at the fundamental-frequency and second-harmonic components. Such a design with broadband capability achieved a 21-dBm output power with a 0.5-dB flatness and a power-added efficiency (*PAE*) better than 65% from 575 to 915 MHz, corresponding to a relative bandwidth of 45%.[57] Another possibility to extend high-efficiency performance of a Class-F PA over a wider frequency range is to provide its operation in a deep saturation mode in the desired frequency range. For a two-stage 2-GHz Class-F GaN HEMT PA with a final stage operating in saturation mode with a 3-dB gain compression point or more, a *PAE* >60% is reached over 20% frequency bandwidth from 1.8 to 2.2 GHz, with an output power varying between 40 and 42 dBm.[58]

In handset applications where monolithic implementation for high-efficiency PAs is required, the microstrip lines are too bulky to be employed in a broadband Class-F load network. Fig. 3.46 shows the circuit schematic of a two-stage broadband monolithic Class-F PA for handset application, where the input and interstage matching circuits are based on two-section L-type *LC* matching circuits (high-pass and low-pass sections for input matching circuit and two high-pass sections for interstage matching circuit), and a load network includes several matching sections with the second- and third-harmonic resonators.[59, 60] By using a two-section L-type matching section where each section is characterized by the same quality factor, it is convenient to match a low device input impedance of about 2 Ω with a source impedance of 50 Ω through the intermediate impedance of 10 Ω when the matching circuit loaded quality factor Q_{L} is reduced to $Q_{\mathrm{L}} = \sqrt{(50/10)-1} = \sqrt{(10/2)-1} = 2$ (instead of $Q_{\mathrm{L}} = \sqrt{(50/2)-1} = 4.9$ for a single-section *LC* matching circuit), which ideally provides more than

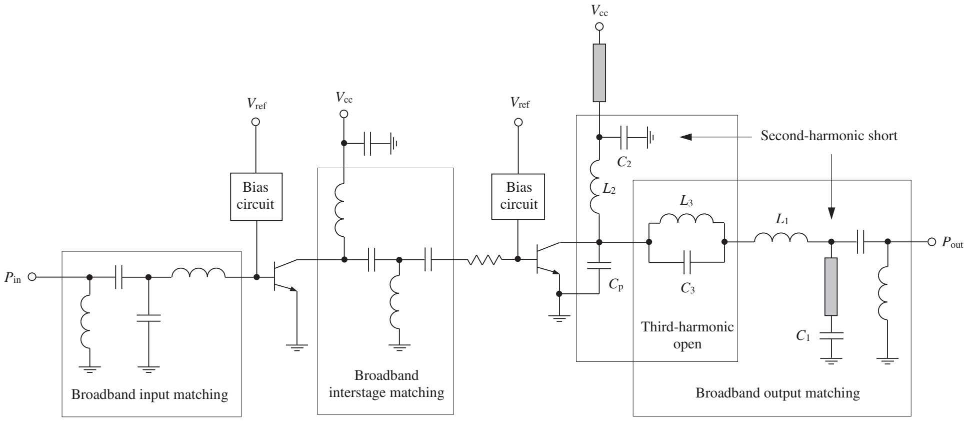


FIG. 3.46

Schematic of broadband Class-F PA for handset application.

two times wider frequency bandwidth Δf, according to $\Delta f = f_0/Q_L$, where f_0 is the center bandwidth frequency.[44] The interstage matching circuit comprises the bias-line inductance at the collector of the driver stage, and the series resistance is connected to the base of the final stage to increase the real part of the device input impedance and to improve the operating stability of the PA.

The load network comprises a broadband impedance matching at the fundamental frequency, the second-harmonic short circuits (L_2C_2 has a near zero impedance at the upper band of the second harmonic and C_1 with a short microstrip line has a near zero impedance at the lower band of the second harmonic), and the third-harmonic open circuit. The L_3C_3 tank resonator, which has an inductive reactance at the fundamental frequency, provides high impedance at the third-harmonic frequency, whereas the device output (collector) capacitance C_p is resonated out at the third-harmonic frequency by the inductance at the collector-bias line. The L_1 represents the series bondwire inductance, which is a part of the broadband matching circuit at the fundamental frequency. As a result, the proper second- and third-harmonic controls have contributed to enhance the *PAE* up to 48% across 300-MHz bandwidth from 1.8 to 2.1 GHz for a handset PA with an output power of 30 dBm, with less than 1-dB variations at a supply voltage of 3.4 V implemented in the InGaP/GaAs HBT process.

Fig. 3.47A shows the circuit schematic of a monolithic GaN HEMT Class-F PA with multiple resonant circuits to broaden the operating frequency bandwidth with high efficiency.[61] Here, the resonant frequencies are chosen such that the circuit can provide the required load impedances at the fundamental and harmonic frequencies. The parallel branch consisting of two inductors, kL_2 and $(k-1)L_2$, and capacitor C_2 is tuned to provide a short circuit at the third harmonic to provide an open-circuit condition at the device drain when the series inductance L_3 resonates with the device output capacitance C_{out}. At the same time, the inductor L_1 and capacitor C_1 are tuned to provide an open-circuit condition at the second harmonic, thus preventing the second harmonic from reaching the output. The parallel branch has a short-circuit impedance at $\omega_{short} = 1/\sqrt{k(1-k)L_2C_2}$ and an open-circuit impedance at $\omega_{open} = 1/\sqrt{kL_2C_2}$. In this case, the parallel branch appears as an inductor at the frequencies lower than ω_{open} and as a capacitor at the frequencies higher than ω_{open}. To satisfy the bandwidth requirements, the

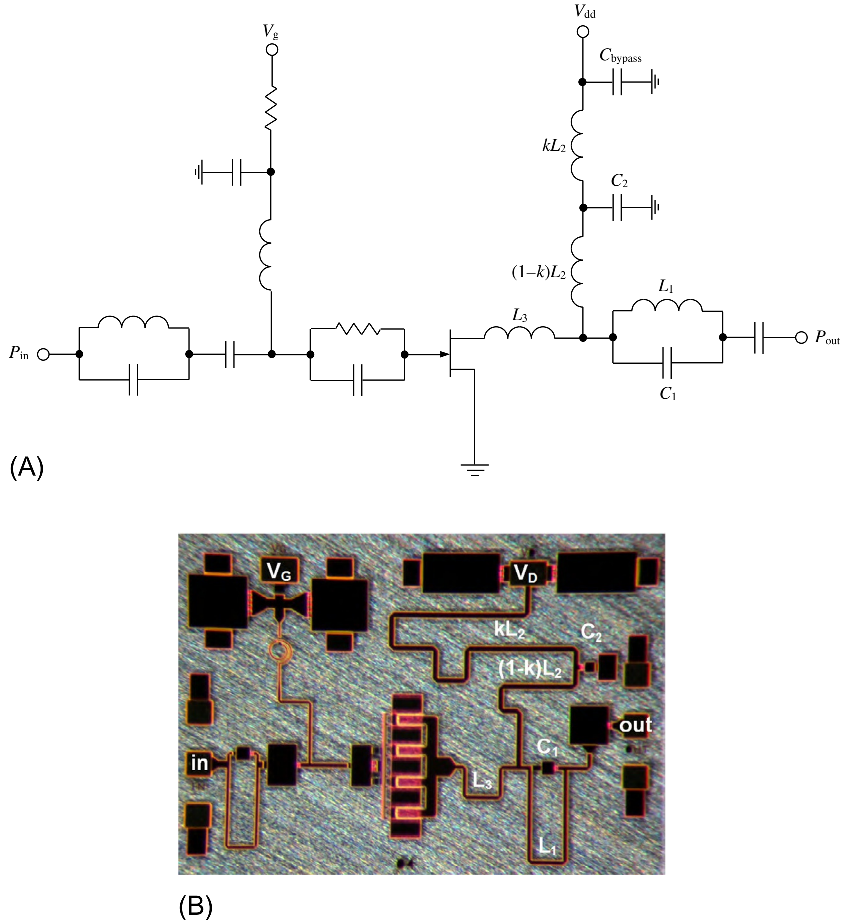


FIG. 3.47

Schematic and test chip of a GaN HEMT Class-F PA with broadband capability.[61]

parameter k should be chosen within the range of 5/9 to 8/9. At the second harmonic, the parallel branch provides the capacitive load impedance. As a result, the Class-F PA implemented in a 0.25-μm GaN HEMT on SiC process, as shown in Fig. 3.47B, achieved a drain efficiency >50% and an output power of 35.5 ± 0.5 dBm at 1-dB gain compression within the frequency bandwidth of 4.8 to 5.9 GHz for an input power of 23 dBm and at a DC-supply voltage of 28 V, with a die size of $1.2 \times 1.8\,\text{mm}^2$.

For a high-power base station or a low voltage cellphone application, the required device load impedance at the fundamental is sufficiently small, resulting in a high matching impedance ratio when an impedance matching network should be used in addition to the harmonic tuning network. Fig. 3.48A shows the circuit schematic of a load network consisting of a third-order harmonic network of Fig. 3.27B, including the device output capacitance and a two-section microstrip output matching network to match the device load of 3 Ω to the 50-Ω load. Here, the first series microstrip line and

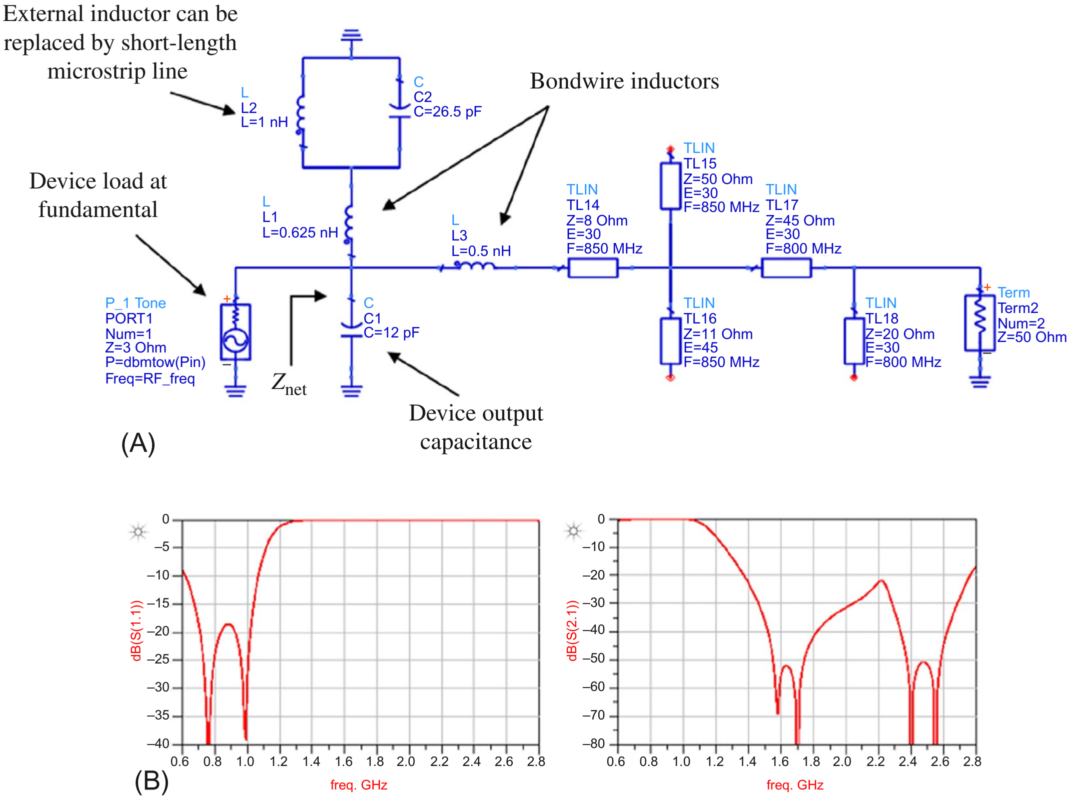

External inductor can be replaced by short-length microstrip line
L
L2
L=1 nH
C
C2
C=26.5 pF
Bondwire inductors
Device load at fundamental
L
L1
L=0.625 nH
L
L3
L=0.5 nH
TLIN
TL14
Z=8 Ohm
E=30
F=850 MHz
TLIN
TL15
Z=50 Ohm
E=30
F=850 MHz
TLIN
TL17
Z=45 Ohm
E=30
F=800 MHz
P_1 Tone
PORT1
Num=1
Z=3 Ohm
P=dbmtow(Pin)
Freq=RF_freq
C
C1
C=12 pF
Z_{net}
TLIN
TL16
Z=11 Ohm
E=45
F=850 MHz
TLIN
TL18
Z=20 Ohm
E=30
F=800 MHz
Term
Term2
Num=2
Z=50 Ohm
Device output capacitance
(A)
dB(S(1,1))
0
−5
−10
−15
−20
−25
−30
−35
−40
0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8
freq. GHz
dB(S(2,1))
0
−10
−20
−30
−40
−50
−60
−70
−80
0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8
freq. GHz
(B)

FIG. 3.48

Schematic of (A) Class-F load network with broadband capability and (B) its frequency response.

open-circuit stub with electrical lengths of 30 degrees provides an open-circuit condition at the third harmonic, the open-circuit stub with an electrical length of 45 degrees suppresses the second harmonic, and an L-type microstrip matching section provides the corresponding impedance matching at the fundamental. To broaden the frequency bandwidth, an electrical length of 30 degrees for microstrip lines in the harmonic and matching networks are chosen at the frequencies slightly shifted relatively to each other. In this case, the flat transfer function is observed from 700 to 900 MHz with significant attenuation in the region of the second and third harmonics, as shown in Fig. 3.48B.

Fig. 3.49A shows the impedance behavior at the fundamental from 700 to 900 MHz when the reactive part of the input impedance Z_{net} changes from capacitive at 700 MHz to inductive close to 900 MHz. At the same time, the second harmonic reactance varies from inductive at 1.4 GHz to capacitive at 1.8 GHz, as shown in Fig. 3.49B, similar to the third harmonic reactance varying from inductive to capacitive as well, as shown in Fig. 3.49C. The flattening of the real and imaginary parts of the load network impedance at the fundamental is mainly provided by the reactance compensation when the opposite reactances are provided by the harmonic and matching networks at the bandwidth edges.

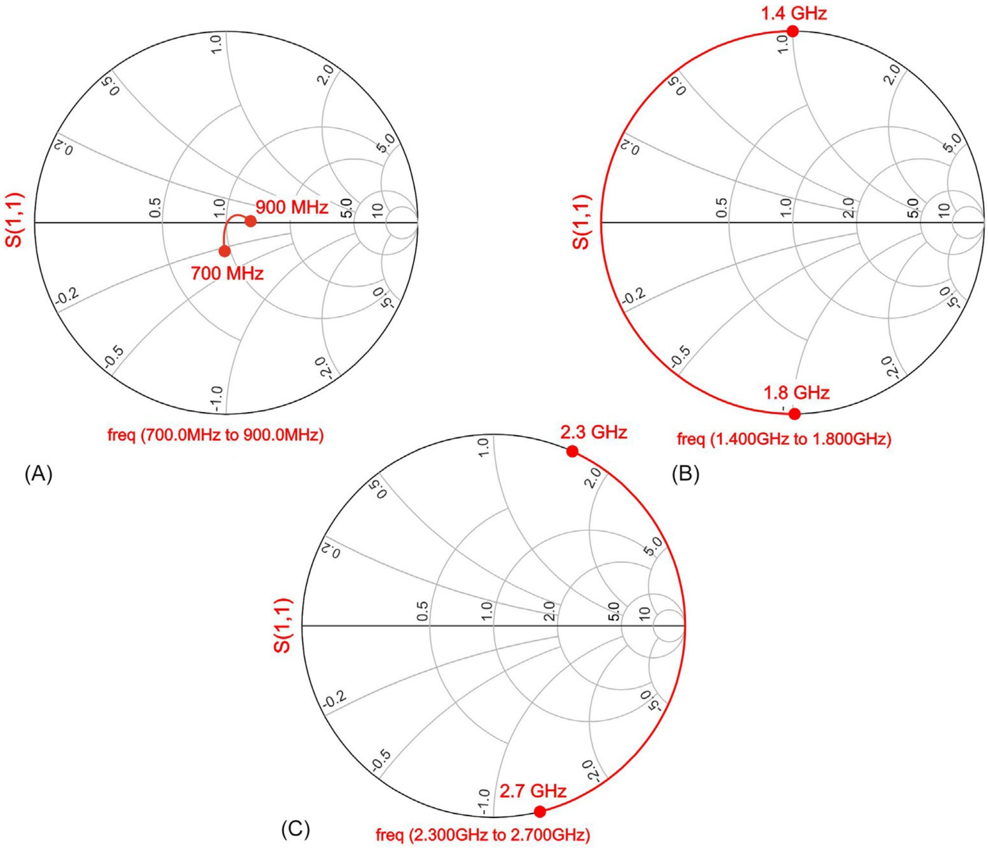


FIG. 3.49

Load network impedance response at (A) fundamental, (B) second, and (C) third harmonics.

In this case, $\text{Re}(Z_{\text{net}})$ varies from 2.2 to 3.8 Ω, as shown in Fig. 3.50A, whereas $\text{Im}(Z_{\text{net}})$ varies from −2.5 to 2.5 Ω, as shown in Fig. 3.50B.

In the Class-F with symmetrical drain voltage and current waveforms, the reactance is zero, which corresponds to the middle points of the impedance curves shown in Fig. 3.49 for the fundamental, second, and third harmonics. However, when moving to higher frequencies, the impedance distribution is different, becoming inductive at the fundamental and purely capacitive at the second and the third harmonics, which corresponds to the Class-E with asymmetrical drain voltage and current waveforms. At the same time, when moving to lower frequencies, the impedance becomes capacitive at the fundamental and purely inductive at the second and third harmonics, which corresponds to the inverse Class-E with asymmetrical drain voltage and current waveforms. This means that the broadband performance is obtained by using a mixed-mode Class-E^{-1}FE operation mode, which is called in some publications as

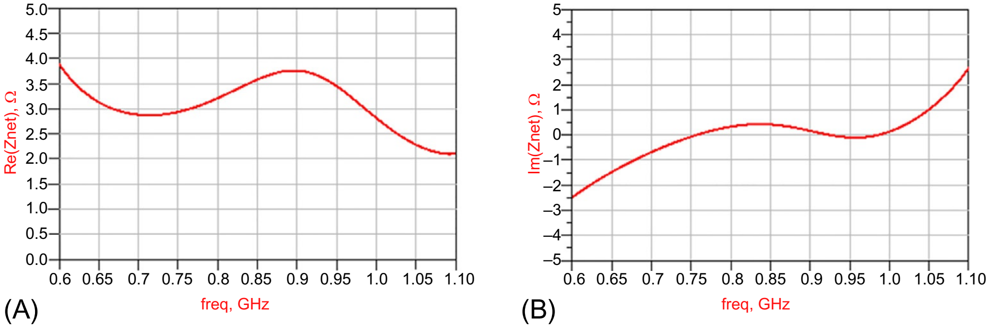


FIG. 3.50

Frequency response of (A) real and (B) imaginary part of input impedance.

a continuous Class-F, where the high-efficiency broadband performance is achieved at the expense of significant complications of the load network with multiple open-circuit stubs.[62, 63] Similarly, the broadband performance can be achieved using an inverse Class-F mode at the center bandwidth frequency and the Class-E mode with the inductive impedance at the fundamental and the capacitive reactances at the second and third harmonics (continuous inverse Class-F).[64] The broader performance over more than an octave can be obtained simultaneously using both continuous Class-F and continuous inverse Class-F.[65] The codesign of a high-efficiency PA and a ring-resonator microstrip bandpass filter with multiple open-circuit stubs based on a series of continuous modes can lead to very broadband or multiband impedance matching and cover frequency bandwidth up to two octaves when the frequency bandwidth of 0.8–3.2 GHz can be realized with an output power of 39.6–41.3 dBm and a drain efficiency from 62% to 68%.[66] However, in all these implementations with continuous Class-F and continuous inverse Class-F modes, the load networks contain a multiple number of the open-circuit stubs, and the matching impedance ratio is not so high. It should be noted that, for any set of harmonic reactances, the maximum efficiency can be achieved by proper adjustment of the waveforms and the fundamental-frequency load reactance.[67]

A simple to way to widen the frequency bandwidth with high efficiency is to reduce the characteristic impedance of the parallel quarterwave transmission line connected to the drain because the input impedance of the grounded quarterwave transmission line with smaller characteristic impedance varies less with frequency variations around fundamental frequency. The test board of a GaN HEMT Class-F PA with a wide quarterwave microstrip line is shown in Fig. 3.51A.[68] The series microstrip line connected to the quarterwave microstrip line and followed by the open-circuit $\lambda/12$ microstrip stub contributes to high-impedance conditions at the third harmonic. A three-section stepped-impedance microstrip line is used to match the resulting impedance at the fundamental. As a result, a drain efficiency of more than 74% with an output power of about 40.8 dBm and a power gain of about 12 dB was achieved at the center bandwidth frequency of 2.6 GHz, while maintaining more than 60% drain efficiency from 2.45 to 2.7 GHz, as shown in Fig. 3.51B.

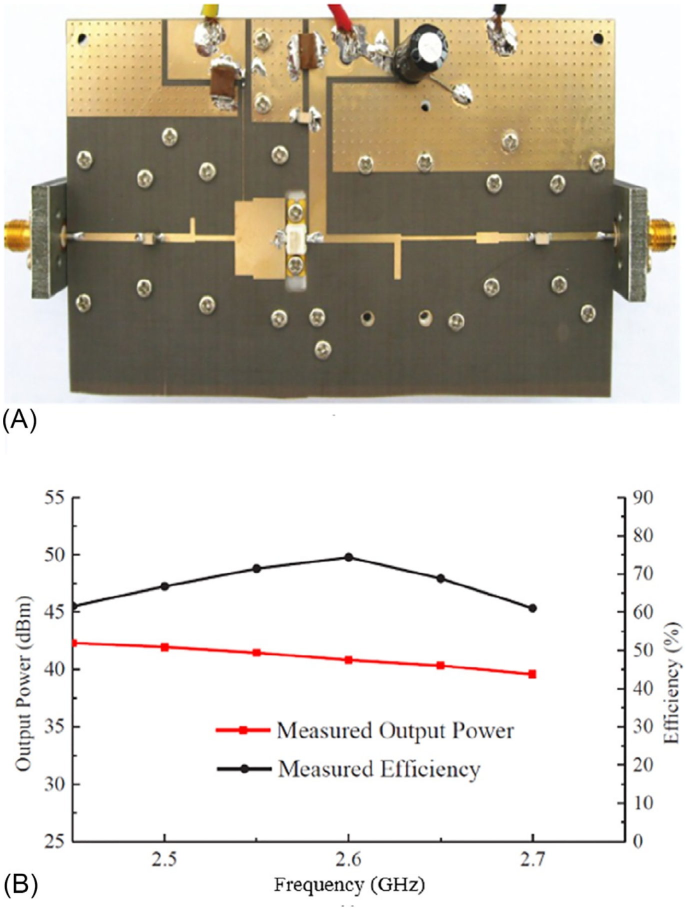


FIG. 3.51

Test board and performance of a GaN HEMT Class-F PA with expanding bandwidth.[68]

3.10 Practical Class-F power amplifiers and applications

A typical VHF high-efficiency lumped-element bipolar PAs, which can provide a 10-W output power with a PAE of about 60% in a zero-bias Class-C operation, is shown in Fig. 3.52A. Using a T-type output-matching *LC* transformer with a series inductor creates high-impedance conditions for the second and higher-order harmonics at the collector terminal, thereby improving the collector efficiency. In this case, the collector current waveform is close to the sinusoidal waveform, while the collector voltage waveform is characterized by a high value of its peak factor. To provide a reliable transistor operation, the maximum collector voltage amplitude should be less than the collector-emitter breakdown voltage. Owing to the small value of the transistor input impedance of about 1 Ω, the frequency bandwidth of such a bipolar PA is sufficiently narrow and normally does not exceed several percentage

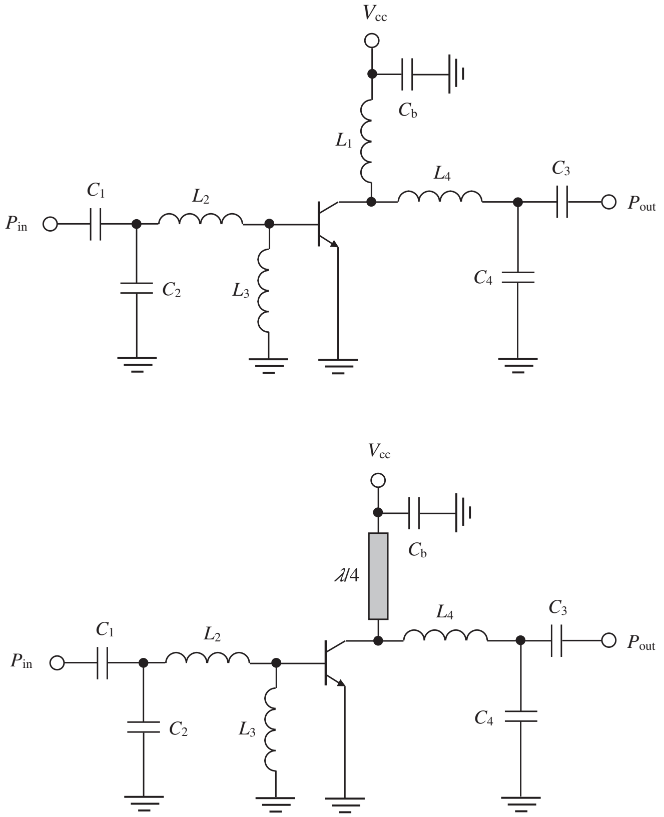


FIG. 3.52

Typical VHF high-efficiency bipolar PAs.

points. The inductor L_3 is required to provide a zero base-emitter bias voltage, while the inductor L_1 and bypass capacitor C_b are necessary to isolate DC power supply from RF signal. Their values are sufficiently large to influence the amplifier matching conditions. Such an RF PA in a slightly overdriven Class-B operation mode can provide a 10-W output power with a power gain of 8 dB and a *PAE* close to 70% at an operating frequency of 250 MHz.[21]

However, to improve the PA reliability by reducing a peak factor to a theoretical maximum value of 2, it is sufficient to use an RF grounded quarter-wavelength transmission line instead of an RF choke. Such an approach provides short-circuit conditions for collector voltage even harmonics, thus resulting in the square voltage and half-sinusoidal current waveform approximations typical for a Class-F operation mode. To increase the impedance conditions for higher-order harmonic components, it is necessary to use the series high-*Q* resonant circuit tuned to the fundamental frequency and followed by the output matching circuit. The typical schematic of such a high-efficiency Class-F VHF PA with a shunt quarterwave microstrip line is shown in Fig. 3.52B. In this case, a collector efficiency approaching 90% at an operating frequency of 250 MHz for a 10-W bipolar PA can be achieved.[44] At higher frequencies, when the load network is fabricated using the transmission-line technology replacing a lumped inductor by a series microstrip line and a shunt capacitor by an open-circuit stub, its input impedance is optimized to realize high impedance condition at the third harmonic, also taking into account the device parasitics.[69]

The simplified circuit topology of a microstrip two-stage 900-MHz GaAs MESFET PA is shown in Fig. 3.34, with the microstrip line between the MESFET device and open-circuit stub with an electrical length $\lambda_2/4$, where λ_2 is the second-harmonic wavelength, to compensate for the equivalent device output reactance and the *T*-type transmission-line impedance transformer to provide an output impedance matching with a 50-Ω load.[43] Similar load-network configuration of a single-stage 1.75-GHz MESFET PA is shown in Fig. 3.53.[53, 70] It consists of a short-circuited quarterwave microstrip line TL_2, having high-impedance conditions at the fundamental and third harmonic components at its input, and an open-circuit stub TL_4 of a quarter wavelength at the third harmonic, having low impedance at the third harmonic component at its input. To realize close to a square-wave voltage and half-sinusoidal current waveforms at the drain terminal, these short- and open-circuit conditions are transformed to the device output by two series microstrip lines TL_1 and TL_3. This has resulted in a drain efficiency of 75% and a power gain of 11 dB at an output power of 24.5 dBm with a drain bias voltage of 3 V. To better optimize impedance at the second harmonic, an additional short-circuited quarterwave line can be included further into the output matching circuit of the microwave *X*-band PA.[71] In a monolithic microwave integrated circuit (MMIC) design, the second harmonic short at the drain can be realized by using a series resonant circuit connected to the ground, while the high-impedance condition at the third harmonic is provided by a series spiral inductor being a part of the output matching circuit.[72]

Fig. 3.54A shows the circuit schematic of a monolithic GaAs pHEMT Class-F PA with a fifth-order harmonic termination network corresponding to its lumped equivalent shown in Fig. 3.29B.[39] Here, the load network provides a harmonic control up to fifth harmonic and transforms the transistor optimum load to a 50-Ω load. The PA is fully implemented in a 0.25-μm pHEMT process with a 100-μm substrate thickness having a chip size of 1.13 × 1.37 mm^2, as shown in Fig. 3.54B. To further improve the efficiency, a third-order harmonic termination is used in the input circuit. The transistor is stabilized by

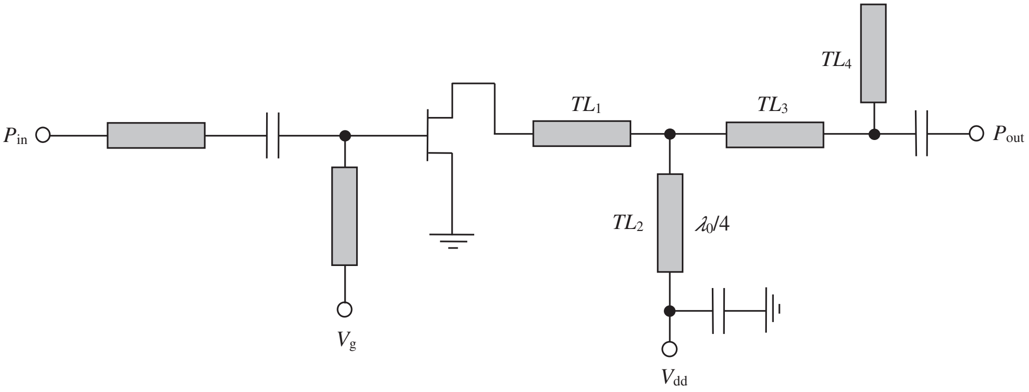


FIG. 3.53

Simplified schematics of a microstrip Class-F PA.

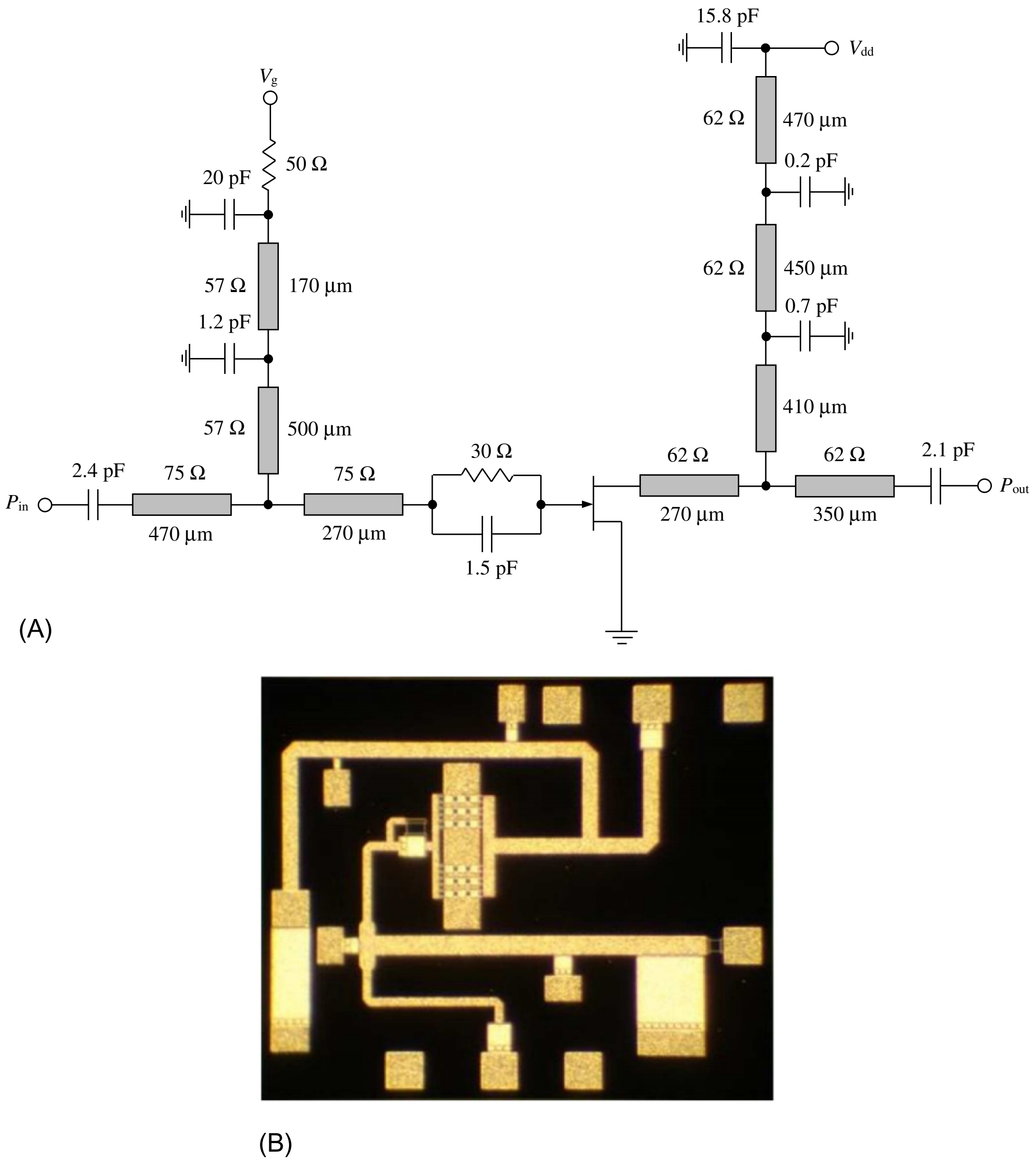

15.8 pF
V_{dd}
V_g
50 Ω
20 pF
62 Ω
470 μm
0.2 pF
57 Ω
170 μm
1.2 pF
62 Ω
450 μm
0.7 pF
57 Ω
500 μm
410 μm
30 Ω
62 Ω
62 Ω
2.1 pF
2.4 pF
75 Ω
75 Ω
P_{in}
P_{out}
470 μm
270 μm
270 μm
350 μm
1.5 pF
(A)
(B)

FIG. 3.54

Circuit schematic and test chip of monolithic Class-F PA.[39]

adding a parallel *RC* circuit connected in series to the gate. In this case, the resistor of 30 Ω reduces the transistor gain at low frequencies to improve the stability, whereas the capacitor of 1.5 pF avoids undesirable power gain degradation at higher frequencies where the transistor is inherently stable. As a result, at a supply voltage of 8 V, a *PAE* of 70% at the saturated output power of 27.5 dBm was achieved at 5.5 GHz.

One of the most important factors for high-efficiency Class-F operation mode is the value of the device saturation resistance r_{sat} (or on-resistance r_{on}), especially at a low supply voltage. Here, r_{sat} is the ratio of the drain-source voltage at the saturated drain current to the saturated drain current. It is difficult to improve the efficiency of a small-scale MESFET with a narrow gate width when, in a low-voltage operation, the ratio $r_{\mathrm{sat}}/R_{\mathrm{out}}$ (where R_{out} is the real part of the device equivalent output impedance) is not small enough. To provide a high-efficiency operation mode of the Class-F PA, it is required to increase this ratio as much as possible. For example, by decreasing r_{sat} by half, the drain efficiency can be improved by about 10%. A MESFET device with the saturation resistance r_{sat} of about 1 Ω can demonstrate a drain efficiency of 90% at a supply voltage of 6 V in a 900-MHz Class-F PA.[43]

The circuit schematic of a Class-F PA implemented in a deep submicron 0.2-μm CMOS technology is shown in Fig. 3.55.[73] Applying a Class-F operation mode has an advantage of substantially less drain voltage peak factor when compared with a Class-E mode. This helps to overcome the problem of a low oxide breakdown voltage, which limits the maximum output power and efficiency of the CMOS PA because of lower supply voltage required for the device protection. The Class-F operation mode is achieved by using an external quarter-wavelength transmission line together with a series on-chip

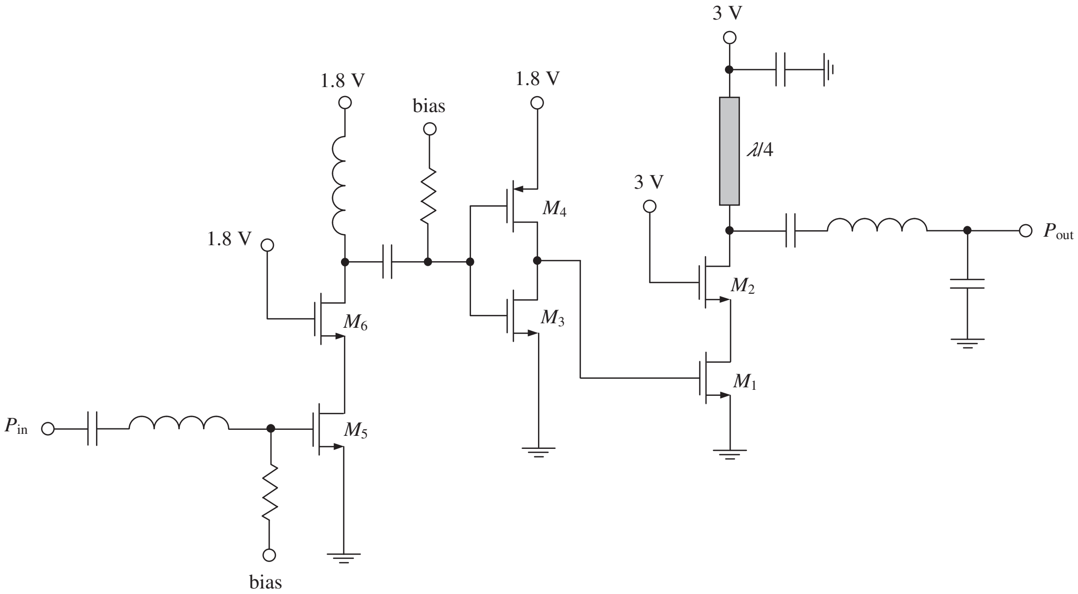


FIG. 3.55

Schematic of Class-F PA with quarterwave transmission line.

resonant circuit in the load network that provides high impedance at the second- and higher-order harmonics. In a cascode configuration of the final stage, the thin gate device M_1 is protected by a thick oxide (80 Å) device M_2 with no threat to oxide breakdown under a supply voltage of 3 V. The driver stage based on a complementary nMOS and pMOS pair eliminates the problem of negative voltage swing across the gate of the cascode device M_1, which is normally the case for a single-ended nMOS device and provides the driving signal waveform closer to a square wave. Such a CMOS Class-F PA operating at 900 MHz achieved a maximum output power of 1.5 W with a *PAE* of 43%.

Fig. 3.56 shows the simplified schematic of a parallel-amplifier architecture implemented in a 0.25-μm CMOS technology and intended to provide high efficiency at backoff output power levels.[74] This architecture employs three binary-weighted Class-F PAs, the output powers of which are combined in a power-combining network based on parallel quarterwave transmission lines loaded by parallel resonant tank tuned to the fundamental frequency. The capability to completely turn off each individual PA without interfering with the operation of other individual PAs is provided by the addition of pMOS shorting switches, resulting in high impedance at the end of the corresponding transmission line. The power-amplifier architecture operating at 1.4 GHz from a 1.5-V power supply occupies an active die size of 0.43 mm^2 and achieves a *PAE* of 49% at a maximum output power of 300 mW, while

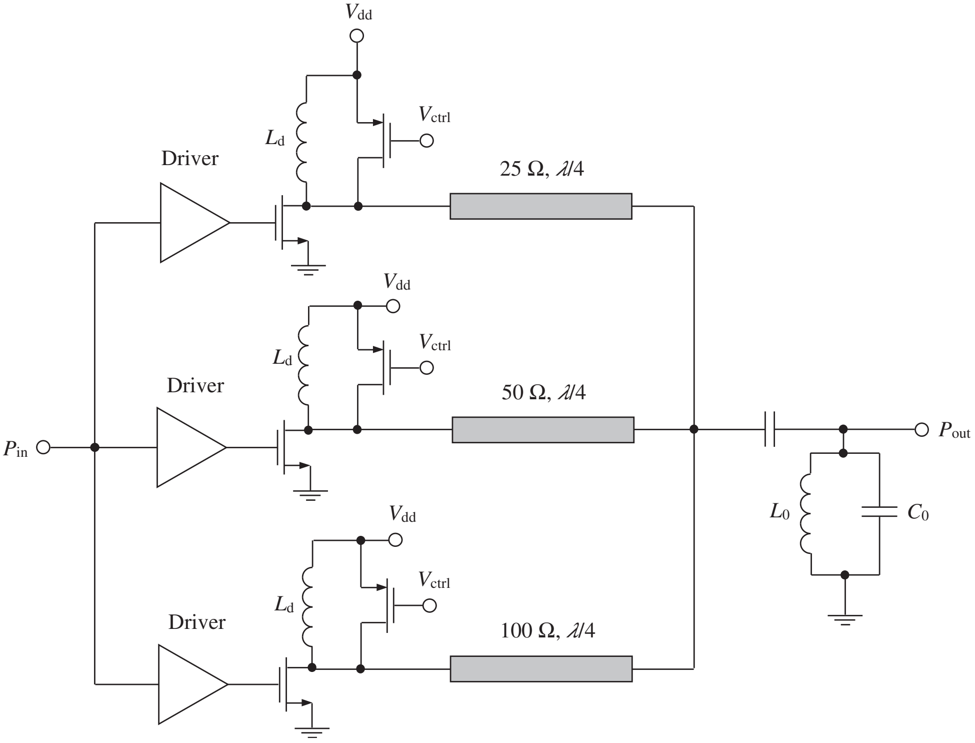


FIG. 3.56

Class-F parallel-PA architecture.

maintaining a *PAE* >43% over a lower output power range down to 100 mW. The transmission lines are implemented using the printed circuit board (PCB) microstrip lines. On-chip transmission-line fabrication in CMOS technology by using *LC* ladders makes it significantly shorter. For example, the frequency response of 10 sections containing a series inductor and a shunt capacitor each can approximate that of the transmission line within 5%, occupying the area of about 14 times shorter. In this case, it is enough to use a spiral inductor to implement both series inductor and shunt capacitor, which can be obtained with the bottom-plate parasitic capacitance of the spiral. However, the maximum *PAE* of the parallel on-chip PA architecture degrades by 10%–15%.

The bandwidth of a Class-F PA is limited in practice by the requirements to precisely terminate the second and third harmonics at the device output. In this case, a reconfigurable output matching network capable of providing a real-time tuning of the second and third harmonic terminations to support a wide tuning of the fundamental can be used. This reconfigurability can be achieved by using the integrated transformers and a bank of parallel capacitors that can support narrowband signals over a wide range of potential carrier frequencies. Fig. 3.57 shows the simplified circuit schematic of a fully integrated Class-F with reconfigurable harmonic termination using two transformer-based fourth-order resonators in the load network implemented in a standard 0.13-μm CMOS technology.[75] The first resonator consisting of L_1, L_2, C_1, and C_{T3} controls the location of the third-harmonic open-circuit termination, as well as provides the necessary impedance transformation from 50 Ω to the optimum load impedance. The second resonator consisting of L_{1f0}, L_{2f0}, C_{2f0}, and C_{T2} controls the location of the second harmonic short-circuit termination. The frequency location of the open-circuit and short-circuit terminations can then be controlled through variable capacitors C_{T3} and C_{T2}, which are realized using a bank of fixed capacitors and switches. The impact of the switches on the overall performance of the PA is minimized because they are partially isolated from the primary RF signal path by the coupling coefficients k_1 and k_2 of the corresponding transformers. By stacking four identical transistors, the power cell can allow a

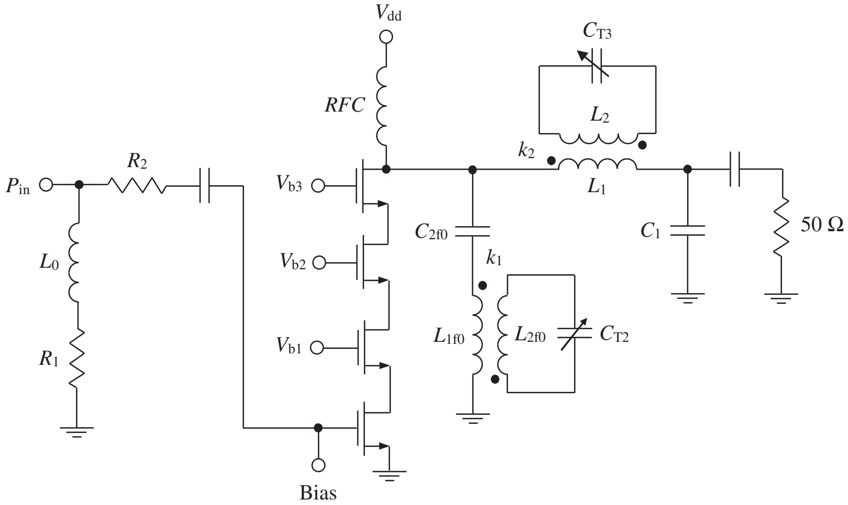


FIG. 3.57

Simplified schematic of Class-F PA with tunable harmonic terminations.

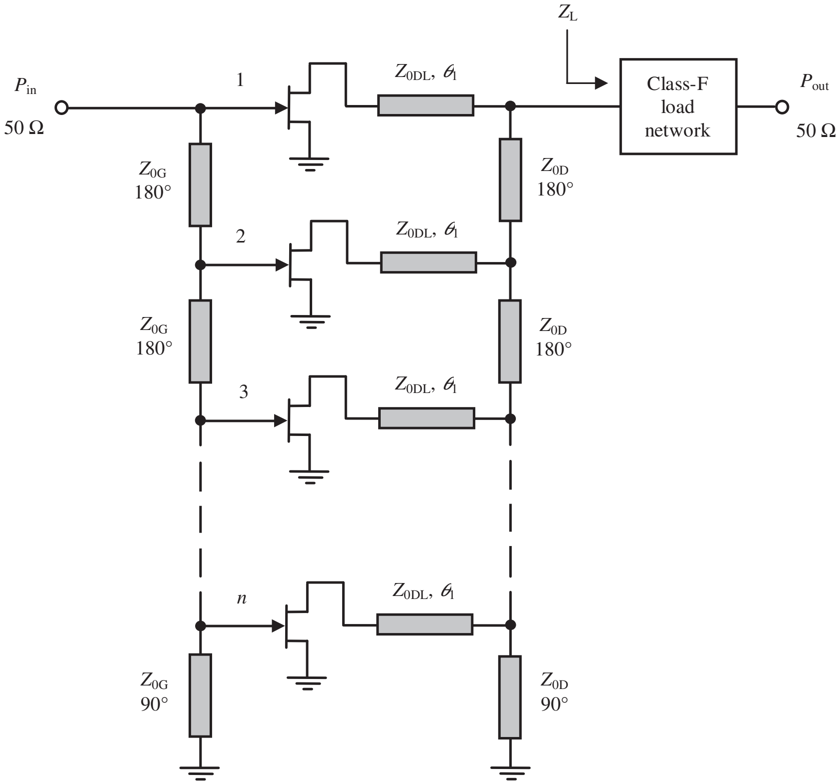


FIG. 3.58

Simplified schematic of a microstrip Class-F distributed amplifier.

supply voltage to be four times greater than that of a single transistor. The fabricated reconfigurable Class-F PA achieved a maximum *PAE* of 48.3%, 45.1%, and 30%, with a saturated output power ranging from 20.1 to 24.6 dBm for operation at 700, 900, and 1200 MHz, respectively, at a supply voltage of 4.8 V.

An efficient Class-F operation mode can also be applied to a distributed PA. Fig. 3.58 shows the simplified schematic of a modified Class-F single-ended dual-fed distributed MESFET PA with a device electrical spacing of 180 degrees at the center bandwidth frequency for optimum operation.[76] The two-port Class-F load network simultaneously provides impedance matching at the fundamental frequency, high impedance at the third and fifth harmonics, and low impedance at even harmonics; namely, Z_L is equal to Z_{0D} at the fundamental frequency but infinite at the third and fifth harmonic components. The open-circuit and short-circuit terminations of the output line are applied directly to the drain of each device through the half-wave transmission lines. For an idealized Class-F optimum operation, the impedance $Z_L(\omega_0)$ seen from the MESFET drain at the fundamental frequency considering both forward and reverse traveling waves can be obtained by

$$Z_L(\omega_0) = Z_{0D} = \frac{8}{n\pi^2}\frac{V_{dd}}{I_0}, \tag{3.128}$$

where V_{dd} is the drain bias voltage, I_0 is the total DC current, and n is the number of MESFETs.

To compensate for the device parasitics, an extra transmission line is cascaded with each device drain port. The characteristic impedance Z_{0DL} and electrical length θ_1 of this transmission line are

$$Z_{0DL} = \sqrt{\frac{L_d}{C_{ds}}}, \tag{3.129}$$

$$\theta_1 = \pi - \omega_0 \sqrt{L_d C_{ds}}, \tag{3.130}$$

where ω_0 is the fundamental angular frequency, L_d is the series drain inductance, and C_{ds} is the shunt drain-source capacitance. The combination of L_d and C_{ds} and extra transmission line, forming a simple low-pass filter section, behaves as a half-wave transmission-line transformer if $\omega\sqrt{L_d C_{ds}}$ is less than 36 degrees or one-tenth of wavelength at least up to the third harmonic. In a hybrid technology, such a 2-FET ($n=2$) Class-F distributed PA enables to achieve a drain efficiency of 71% and an output power of 22 dBm at an operating frequency of 1.75 GHz.

Modern wireless communication systems require feeding the signal with a nonconstant envelope through the PA. In this case, there is a tradeoff between power-amplifier efficiency and linearity with an improvement in one coming at the expense of the other. In a classical analog envelope elimination and restoration (EER) Kahn approach where special devices are required to separate amplitude (envelope) and RF phase-modulated signals, one type of a PA is responsible for envelope signal amplification, while another type of a PA is fed by a constant-envelope RF signal, as shown in Fig. 3.59. The constant-envelope RF signal can be amplified efficiently by a nonlinear PA using a Class-F operation mode. For example, at the operating frequency of 8.4 GHz, a Class-F MESFET PA was able to provide the maximum instantaneous efficiency of 55% with an output power of 610 mW.[77] Higher drain efficiency of about 73% at an average output power of 31 dBm can be achieved for a transmission-line Class-F GaN HEMT PA optimized to operate in the EER transmitter at 2.14 GHz.[50] Amplitude modulation of the final stage of the PA based on a Class-S modulator restores the envelope to the phase-modulated carrier signal creating an amplitude replica of the input signal.[19] In contrast to linear PAs, a

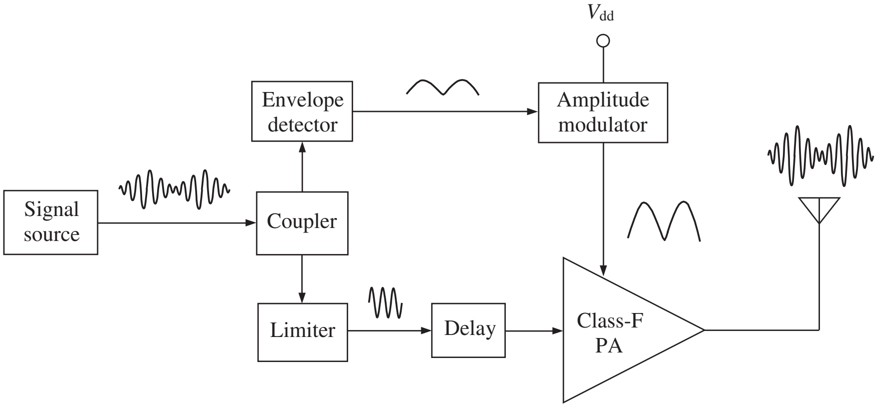


FIG. 3.59

Block diagrams of a Kahn EER transmitter with Class-F PA.

Kahn EER transmitter is potentially capable to operate with a high efficiency over a wide dynamic range of backoff output power levels and, therefore, to produce an average efficiency that is typically three to five times higher. To minimize misalignment between phase and amplitude, the delay line located in phase-modulated or envelope amplifying path is required.

In modern radio transmitters intended for wireless applications, both the envelope and phase-modulated signals can easily be generated separately using digital signal processing (DSP) technique.[44] The average efficiency of 26.4% for a multicarrier signal and 43.8% for a quadrature amplitude modulation (QAM) with better linearity were achieved in an *X*-band Class-F PA using the Kahn technique compared with 9.5% and 28.7% for a linear power-amplifier mode, respectively.[77] Average efficiency can even be increased by applying a modified Kahn technique using an additional drive modulation when dynamic RF input amplitude varies proportionally to the signal envelope.

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CHAPTER

Inverse Class-F

4

Highly efficient operation of the power amplifier can also be obtained by applying biharmonic or polyharmonic modes when an additional single-resonant or multi-resonant circuit tuned to the even harmonics of the fundamental frequency is added into the load network. An infinite number of even harmonic resonators results in an idealized inverse Class-F mode with a half-sinusoidal voltage waveform and a square current waveform at the device output terminal. In inverse Class-F power amplifiers analyzed in the frequency domain, the fundamental and harmonic load impedances are optimized by short-circuit termination and open-circuit peaking to control the voltage and current waveforms at the device output to obtain maximum efficiency. In this chapter, different inverse Class-F techniques using lumped and transmission-line elements, including a quarter-wave transmission line, are analyzed. Design examples and practical radio-frequency (RF) and microwave inverse Class-F power amplifiers for different wireless applications are described and discussed in detail in this chapter.

4.1 History of biharmonic and polyharmonic operation modes

Highly efficient biharmonic operation mode can be realized using a second-harmonic peaking when an additional parallel resonant circuit tuned to the second harmonic of the fundamental frequency is included in series into the load network. Similar to the load network with the third-harmonic peaking, the additional resonator creates a high impedance at the second harmonic, resulting in an efficiency improvement. In this case, by limiting to a biharmonic operation condition, the partial Fourier series of current $i(t)$ and voltage $v(t)$ in normalized form can be, respectively, written as

$$\frac{v(\omega t)}{V_0} = 1 - \frac{\pi}{2}\sin\omega t - \frac{2}{3}\cos 2\omega t, \tag{4.1}$$

$$\frac{i(\omega t)}{I_0} = 1 + \frac{4}{\pi}\sin\omega t + \frac{4}{3\pi}\sin 3\omega t, \tag{4.2}$$

where V_0 and I_0 are the DC voltage and current components, respectively. Note that an infinite number of the voltage and current harmonics presented in a Fourier-series expansion results in the ideal half-sinusoidal voltage and square current waveforms.

Fig. 4.1 shows that the shapes of the voltage and current waveforms can be significantly transformed by adding even one additional harmonic component with a proper phase. For example, the combination of the fundamental-frequency and third-harmonic components with 180 degrees out-of-phase shift at the center of symmetry results in a flattened current waveform with depression in its center, as shown in Fig. 4.1A, which can be minimized by using a proper ratio between the amplitudes of the

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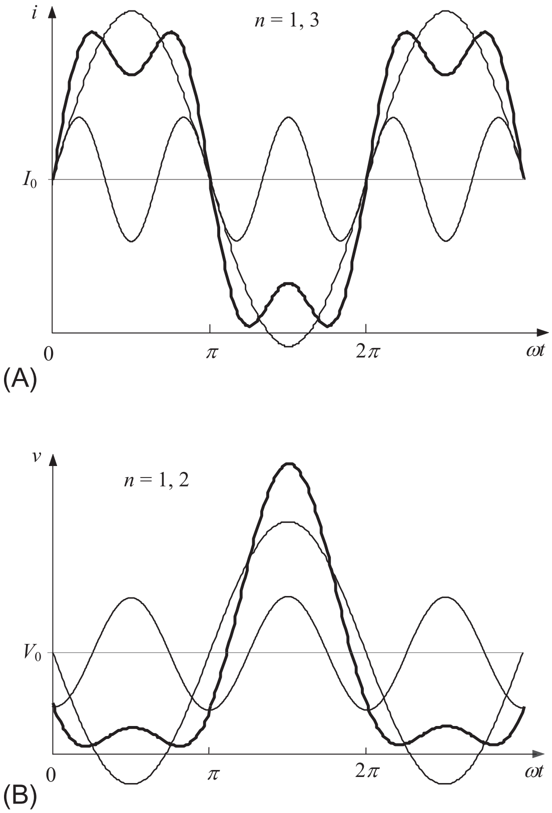


FIG. 4.1

Fourier current and voltage waveforms with third and second harmonics.

fundamental and third harmonics. Similarly, the combination of the fundamental-frequency and second-harmonic components, which are in phase at the center of symmetry, sharpens the voltage waveform corresponding to minimum values of the voltage waveform, as shown in Fig. 4.1B. The optimum ratio between the amplitudes of the fundamental and second current harmonics can maximize the current waveform in one half of the period and minimize the current waveform during the other half of the period determined by the device saturation resistance in a practical circuit. This means that the power loss due to the active device can be minimized because the results of the integration over the period when minimum current corresponds to maximum voltage will give a small value compared with the power delivered to the load.

The effect of the inclusion of the parallel resonant circuit tuned to the second harmonics and located in series at the anode, as shown in Fig. 4.2A, was first described and analyzed in early 1940s.[1–3] It was shown that the symmetrical anode current waveform and level of its depression can be provided with the opposite phase conditions between the fundamental-frequency and second-harmonic components for anode current and an optimum value of the ratio between their voltage amplitudes. It was also noted that a high operation efficiency can be achieved even when impedance of the parallel circuit to second

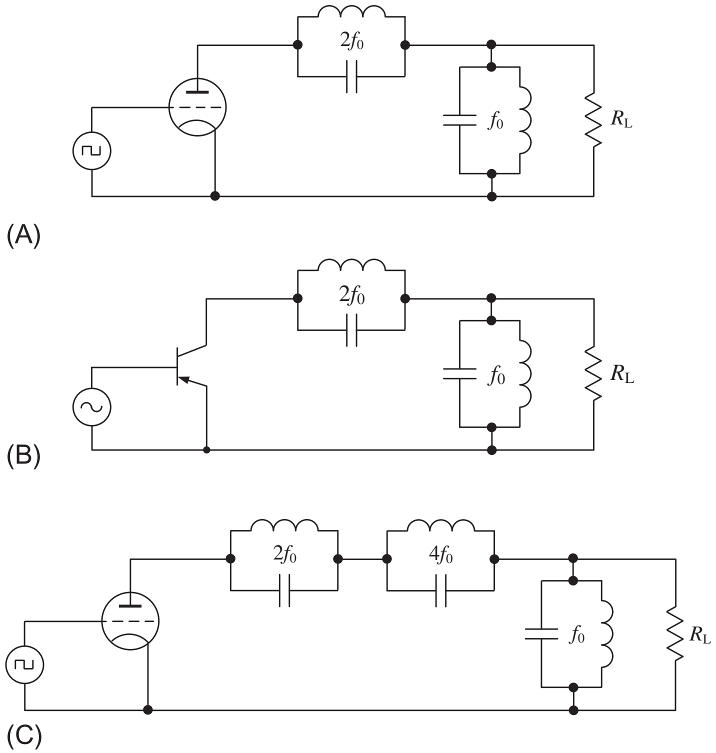


FIG. 4.2

Biharmonic and polyharmonic power amplifiers.

harmonic is equal to or slightly greater than the impedance of the tank circuit to fundamental frequency. In practical vacuum-tube power amplifiers intended for operation at very high frequencies, the peak output power and anode efficiency can, therefore, be increased by 1.15–1.2 times.[4] In addition, such an approach can improve the modulation properties of the power amplifier when the phase of the second voltage harmonic becomes negative when compared to that of the fundamental frequency.[1] However, generally, in view of the parasitic capacitance realized between anode and cathode, the entire anode circuit should be tuned to the second harmonic, not only a single resonator.

Fig. 4.2B shows the simplified schematic of a biharmonic bipolar-transistor power amplifier with an additional resonant tank in the load network tuned to the second harmonic, which achieved a collector efficiency of 92% and an output power of about 400 mW at an operating frequency of 106 kHz.[5] The required phase shift between the fundamental and second voltage harmonics at the collector is achieved due to the device inertia provided by its input capacitance and by operation in a slightly saturated mode. However, in this case, the collector voltage peak factor is higher compared to that for a power amplifier with the third-harmonic resonator. In addition, an additional resonator tuned to the fourth harmonic can be connected in series with the second-harmonic resonator, as shown in Fig. 4.2C, to maximize the anode efficiency of the vacuum-tube amplifier with a square voltage driving waveform.[6]

An efficiency improvement can also be significant in a Class-C power amplifier by using a single fourth-harmonic resonator in anode circuit. In this case, the grid driving voltage can represent a simple sinusoidal waveform because the current coefficients for the fundamental-frequency and fourth-harmonic components have opposite signs providing their 180 degrees out-of-phase voltage conditions at the anode at the center of waveform symmetry. For an idealized active device whose output is represented by the voltage-controlled current source only, the flattening of the anode voltage waveform can take place when the biharmonic signal, including the fundamental-frequency and fourth-harmonic components at the anode, can be written as

$$v = V_{\mathrm{a}} - V_{\mathrm{a}_1} \cos \omega t + V_{\mathrm{a}_4} \cos 4\omega t, \tag{4.3}$$

where V_{a} is the anode DC voltage, $V_{\mathrm{a}1}$ is the fundamental-frequency amplitude, and $V_{\mathrm{a}4}$ is the fourth-harmonic amplitude. For a piecewise linear approximation of the active device transfer current-voltage characteristic, the anode current will represent a sequence of pulses, the duration of which is defined by a conduction angle 2θ determined by the grid DC bias conditions. The opposite signs of the voltage amplitudes V_{a_1} and V_{a_4} cause the anode voltage waveform to be bottom flattened, thus reducing the power losses during the time interval when the anode current is high. Fig. 4.3 shows the simplified schematics of both (A) single-ended and (B) push-pull biharmonic vacuum tube high-power amplifiers, each having an additional harmonic resonator tuned to the fourth harmonic.[7]

The ratio of the fundamental-frequency and fourth-harmonic amplitudes expressed through the anode current coefficients $\gamma_1(\theta)$ and $\gamma_4(\theta)$ is defined by

$$\frac{V_{\mathrm{a}_1}}{V_{\mathrm{a}_4}} = \frac{I_{\mathrm{a}_1}}{I_{\mathrm{a}_4}} \frac{R_L}{R_{L_4}} = \frac{\gamma_1(\theta)}{\gamma_4(\theta)} \frac{R_L}{R_{L_4}}, \tag{4.4}$$

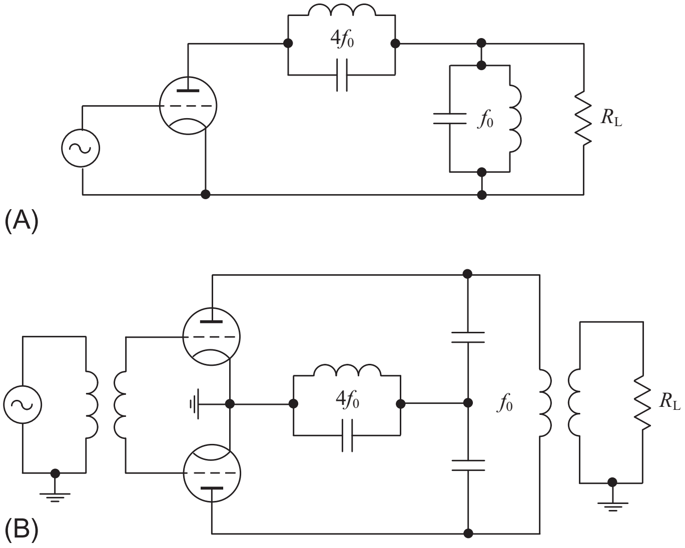


FIG. 4.3

Single-ended and push-pull power amplifiers with fourth harmonic peaking.

where I_{a1} is the amplitude of the fundamental current, I_{a4} is the amplitude of the fourth-harmonic current, and R_{L4} is the load resistance for the fourth-harmonic current due to a finite value of the quality factor of the fourth-harmonic resonator,

$$\gamma_1(\theta) = \frac{1}{\pi}\left(\theta - \frac{\sin 2\theta}{2}\right), \tag{4.5}$$

$$\begin{aligned}\gamma_4(\theta) &= \frac{\sin 4\theta \cos\theta - 4\cos 4\theta \sin\theta}{30\pi} \\ &= -\frac{2}{15\pi}\sin\theta\left(6\cos^4\theta - 7\cos^2\theta + 1\right)\end{aligned}. \tag{4.6}$$

From Eqs. (4.5), (4.6), the signs of the fundamental-frequency current coefficient $\gamma_1(\theta)$ and fourth-harmonic current coefficient $\gamma_4(\theta)$ are opposite when

$$\cos^{-1}\frac{1}{\sqrt{6}} < \theta < \pi - \cos^{-1}\frac{1}{\sqrt{6}}, \tag{4.7}$$

which results in 65.9 degrees $< \theta <$ 114.1 degrees, thus satisfying the required relationship between V_{a_1} and V_{a_4} in Eq. (4.3). This means that the bottom flattening of the anode voltage waveform can be achieved in Class-B or Class-C power amplifiers with a sinusoidal driving signal. Fig. 4.4A shows the anode voltage waveform where the amplitude of the fourth-harmonic component is one-eighth of the amplitude of the fundamental component, while the anode pulsed current waveform corresponding to a Class-C operation mode is shown in Fig. 4.4B. A higher anode efficiency can be achieved in a deep Class-C mode when θ is significantly smaller than 90 degrees because the bottom flattening of the voltage waveform occurs during the time interval shorter than half a period.

To further increase the efficiency of the biharmonic power amplifier, it makes sense to provide a biharmonic driving signal consisting of the fundamental frequency and its second-harmonic component.[8, 9] In this case, the fundamental-frequency and second-harmonic components should be 180 degrees out of phase at their maximum amplitudes, and the amplitude of the second harmonic is preferably chosen to have approximately three-eighths the amplitude of the fundamental. Fig. 4.5A shows the simplified circuit schematic of a vacuum-tube power amplifier containing the fundamental tank and second-harmonic resonant circuits, both in grid and anode circuits. From Eq. (3.13) given in Chapter 3, it follows that, for optimum values $\theta_{opt} \approx 80$ degrees and $a_n^0 \approx 0.41$, the anode efficiency in a biharmonic mode with second-harmonic injection when $n = 2$ can be increased up to $\eta' = (0.95\text{–}0.96)\xi$.[8]

A simple solution to realize 180 degrees out-of-phase conditions between the voltage fundamental-frequency and second-harmonic components at the device output is to use a second-harmonic tank resonator connected in series to the device input, as shown in Fig. 4.5B.[1] Such an approach gives a possibility to flatten the anode voltage waveform in active region avoiding the device saturation mode. Owing to the diode-type input of the vacuum tube, the resultant grid current pulse will contain a strong second-harmonic component, resulting in a second harmonic voltage component across the input resonator. The loaded quality factor of the second-harmonic resonator must be high enough to neglect the voltage drop at the fundamental frequency. As a result, the second-harmonic resonator has no effect on the voltage fundamental-frequency component. However, it provides a phase shift of 180 degrees for the second-harmonic component, because increasing in a voltage drop across the resonator results in decreasing of the voltage drop across the grid-cathode (base-emitter or gate-source) terminals.

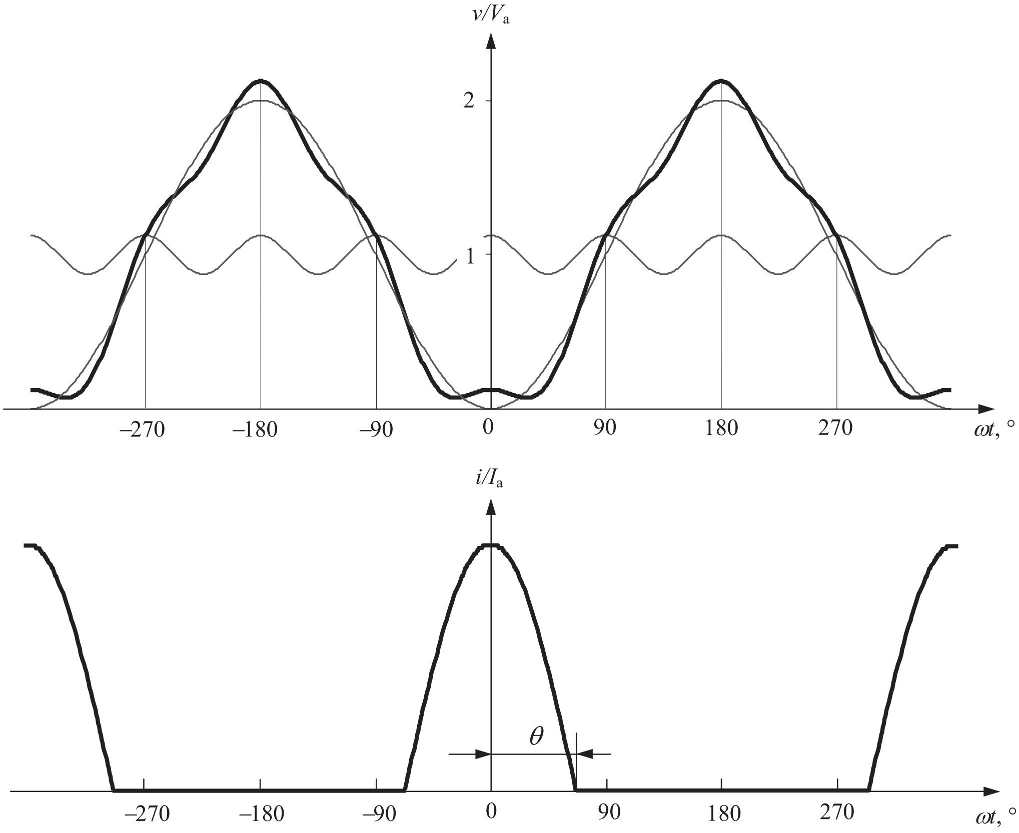


FIG. 4.4

Voltage and current waveforms of fourth-harmonic power amplifier.

Fig. 4.6A shows the combination of the fundamental-frequency and second-harmonic components shifted by 180 degrees. In comparison with Fig. 4.1B, where the fundamental-frequency and second-harmonic components are in phase at maximum point of the fundamental-frequency component, resulting in a waveform bottom flattening, this voltage waveform at the device input is characterized by its top flattening when the second harmonic has minimum value at maximum point of the fundamental-frequency component. Then, choosing the DC bias point V_g equal to the device pinch-off voltage V_p, the selection of which corresponds to Class-B mode with the conduction angle of 180 degrees for monoharmonic operation, will result in the anode biharmonic current pulses with conduction angle $2\theta > 180$ degrees, as shown in Fig. 4.6B. At the same time, using a second-harmonic resonator in the load network contributes to the anode voltage waveform, as shown Fig. 4.1B.

Similar biharmonic approach to affect individually the fundamental-frequency and second-harmonic conditions by using a transmission-line technique was applied to a two-stage microwave transistor power amplifier. In this case, the proper amplitude and phase conditions for the fundamental-frequency and second-harmonic components at the input of the final power stage

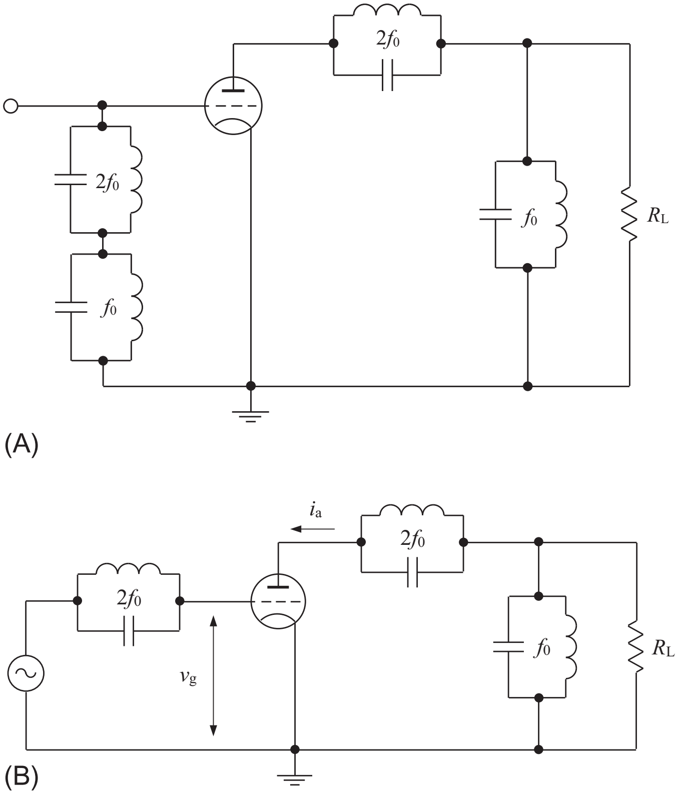


FIG. 4.5

Biharmonic power amplifier with input harmonic control.

separating from the driver stage output can be realized using the quarter-wavelength transmission lines in the form of the open-circuit and short-circuit stubs.[10] As a result, a drain efficiency of 77% was achieved for a microstrip biharmonic GaAs MESFET power amplifier operated at the carrier frequency of 1.62 GHz with an output power of 27.9 dBm.

4.2 Idealized inverse Class-F mode

Generally, an infinite number of even harmonic tank resonators can maintain a square current waveform, also providing a half-sinusoidal voltage waveform at the anode (collector or drain). Fig. 4.7 shows the basic schematics of an inverse Class-F power amplifier with a multiple-resonator output filter to control the harmonic content of its collector voltage and current waveforms, thereby shaping them to reduce dissipation and to increase efficiency, where the voltage v_{even} across the even-harmonic resonators and voltage i_{odd} is the current through the fundamental-frequency resonator which includes odd harmonics.

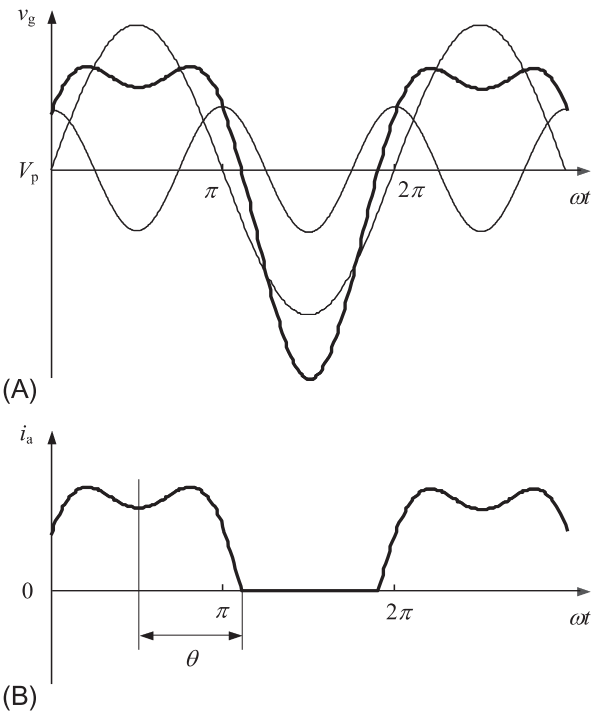


FIG. 4.6

Input and output voltage and current waveforms with second harmonic.

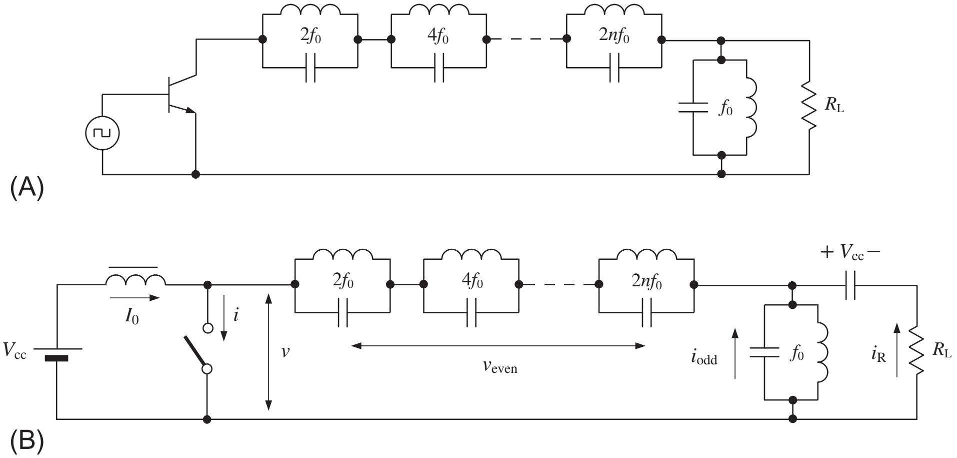

$2f_0$
$4f_0$
$2nf_0$
f_0
R_L
(A)
I_0
i
v
V_{cc}
$2f_0$
$4f_0$
$2nf_0$
v_{even}
$+ V_{cc} -$
i_{odd}
f_0
i_R
R_L
(B)

FIG. 4.7

Basic circuits of inverse Class-F power amplifier with parallel resonant circuits.

The term "inverse" means that the collector voltage and current waveforms are interchanged compared to a conventional case under the same idealized assumptions. Consequently, for a purely sinusoidal current flowing into the load, as shown in Fig. 4.8A, the ideal collector current waveform is composed by a fundamental-frequency and odd-harmonic components approximating a square waveform, as shown in Fig. 4.8B. At the same time, the collector voltage waveform is composed by the fundamental-frequency and even harmonic components approximating a half-sinusoidal waveform, as shown in Fig. 4.8C. As a result, the shapes of the collector current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously, similarly to a conventional

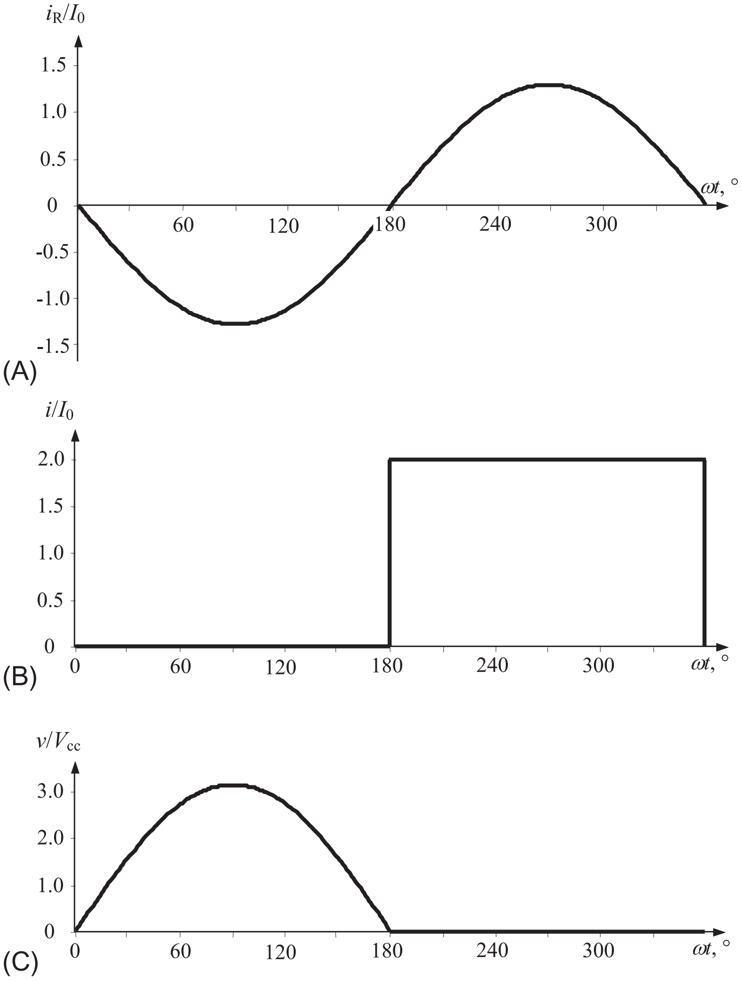


FIG. 4.8

Ideal waveforms of inverse Class-F power amplifier.

Class-F mode. Such a switchmode condition, with symmetrical collector voltage and current waveforms, corresponds to an idealized inverse Class-F operation mode with a 100% collector efficiency.

By using Eqs. (3.18), (3.22) given in Chapter 3 for a conventional Class-F mode, a similar analysis of the distribution of voltages and currents in the inverse Class-F load network results in equations for the collector current and voltage waveforms as

$$i(\omega t) = 2I_0 - i(\omega t + \pi), \tag{4.8}$$

where I_0 is the DC current and

$$v(\omega t) = V_\mathrm{R}\left(\sin\omega t + |\sin\omega t|\right), \tag{4.9}$$

where V_R is the fundamental-frequency amplitude. From Eq. (4.8), it follows that maximum value of the collector current cannot exceed a value of $2I_0$, and the time duration with maximum amplitude when $i = 2I_0$ coincides with the time duration with minimum amplitude when $i = 0$. Because the collector current is zero when the switch is turned off, the only possible waveform for the collector current is a square wave composing of only DC, fundamental-frequency, and odd-harmonic components.

By using a Fourier analysis of the current and voltage waveforms, the following equations for the DC voltage, fundamental voltage, and current components in the collector voltage and current waveforms can be obtained:

the fundamental current component can be calculated using Eq. (4.8) as

$$I_1 = I_\mathrm{R} = \frac{1}{\pi}\int_{\pi}^{2\pi} 2I_0 \sin(\omega t + \pi)\, d\omega t = \frac{4I_0}{\pi}, \tag{4.10}$$

the DC voltage V_cc can be calculated from Eq. (4.9) as

$$V_\mathrm{cc} = \frac{1}{2\pi}\int_0^{\pi} 2V_R \sin\,\omega t\; d\,\omega t = \frac{2V_\mathrm{R}}{\pi}, \tag{4.11}$$

the fundamental voltage component can be calculated from Eq. (4.9) as

$$V_1 = \frac{1}{\pi}\int_0^{\pi} 2V_\mathrm{R} \sin^2\omega t\; d\,\omega t = V_\mathrm{R}. \tag{4.12}$$

Then the ratio between the DC-supply power P_0 and the output power at the fundamental frequency P_1 can be written as

$$P_1 = \frac{V_1 I_1}{2} = \frac{1}{2}\frac{\pi V_\mathrm{cc}}{2}\frac{4I_0}{\pi} = P_0, \tag{4.13}$$

resulting in a theoretical collector efficiency of 100%.

The impedance conditions seen by the device collector for an idealized inverse Class-F mode are equal to

$$Z_1 = R_1 = \frac{\pi^2}{8}\frac{V_{cc}}{I_0}, \tag{4.14}$$

$$Z_{2n+1} = 0 \quad \text{for odd harmonics}, \tag{4.15}$$

$$Z_{2n} = \infty \quad \text{for even harmonics}. \tag{4.16}$$

Although it is impossible to realize the ideal harmonic impedance conditions in real practice, the peaking of at least several current and voltage harmonic components should be provided to achieve a high-efficiency operation of the power amplifier. The more the voltage waveform provided by higher order harmonic components can be flattened, the less power dissipation owing to flowing of the collector current—when the collector voltage is extremely small—occurs. Flattening of the collector voltage and current waveforms to realize an inverse Class-F operation with maximally flat waveforms can be accomplished by using odd-harmonic components to approximate a square current waveform, and even harmonic components to approximate a half-sinusoidal voltage waveform. For the symmetrical flattened current waveforms, the medium points where the current waveform reaches its minimum and maximum values are at $\omega t = \pi/2$ and $\omega t = 3\pi/2$, respectively. Maximum flatness at the minimum current requires the even derivatives to be zero at $\omega t = \pi/2$. At the same time, for the symmetrical voltage waveforms, the medium points where the current waveform reaches its maximum and minimum values are at $\omega t = \pi/2$ and $\omega t = 3\pi/2$, respectively. Maximum flatness at the minimum voltage requires the even derivatives to be zero at $\omega t = 3\pi/2$. In this case, efficiency of an inverse Class-F mode with maximally flat waveforms can be expressed as a simple explicit function of number of even harmonics M in a current waveform and number of higher odd harmonics K in a voltage waveform in the case when $M = K + 1$ as

$$\eta = \frac{N}{N+1}, \tag{4.17}$$

where $N = 1 + M + K$ is number of harmonics.[11]

4.3 Inverse Class-F with quarter-wave transmission line

An idealized inverse Class-F operation mode can also be represented by using a sequence of the series resonant circuits tuned to the fundamental and odd harmonics, as shown in Fig. 4.9A. In this case, it is assumed that each resonant circuit has zero impedance at the corresponding fundamental frequency f_0 and its odd-harmonic components $(2n + 1)f_0$ and infinite impedance at even harmonics $2nf_0$ realizing the idealized inverse Class-F square current and half-sinusoidal voltage waveforms at the device output. As a result, the active device that is driven to operate as a switch sees the load resistance R_L at the fundamental frequency, whereas the odd harmonics are shorted by the series resonant circuits.

An infinite set of the series resonant circuits tuned to the odd harmonics can be effectively replaced by a quarter-wavelength transmission line with the same operating capability. Such a circuit representation of an inverse Class-F power amplifier with a series quarter-wave transmission line loaded by the series resonant circuit tuned to the fundamental frequency is shown in Fig. 4.9B.[12, 13] The series-tuned

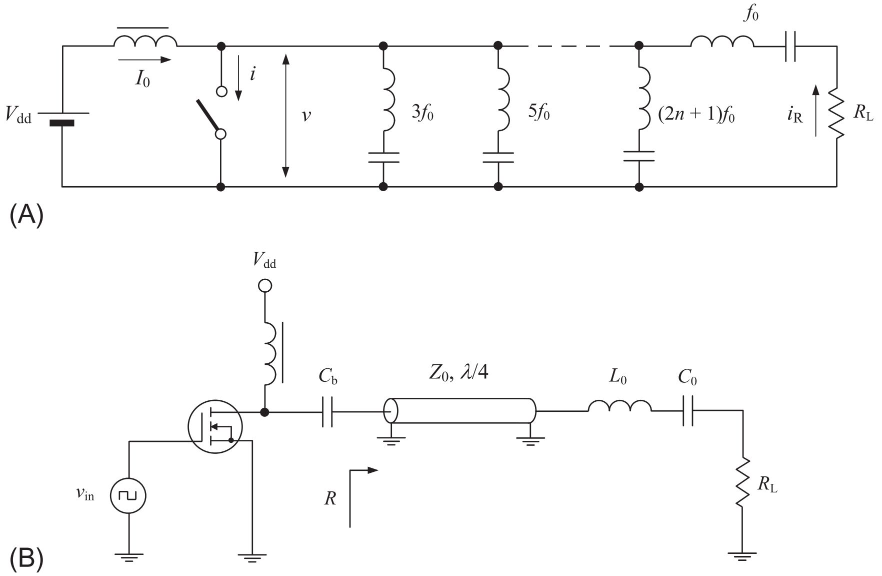


FIG. 4.9

Inverse Class-F power amplifier with series quarter-wave transmission line.

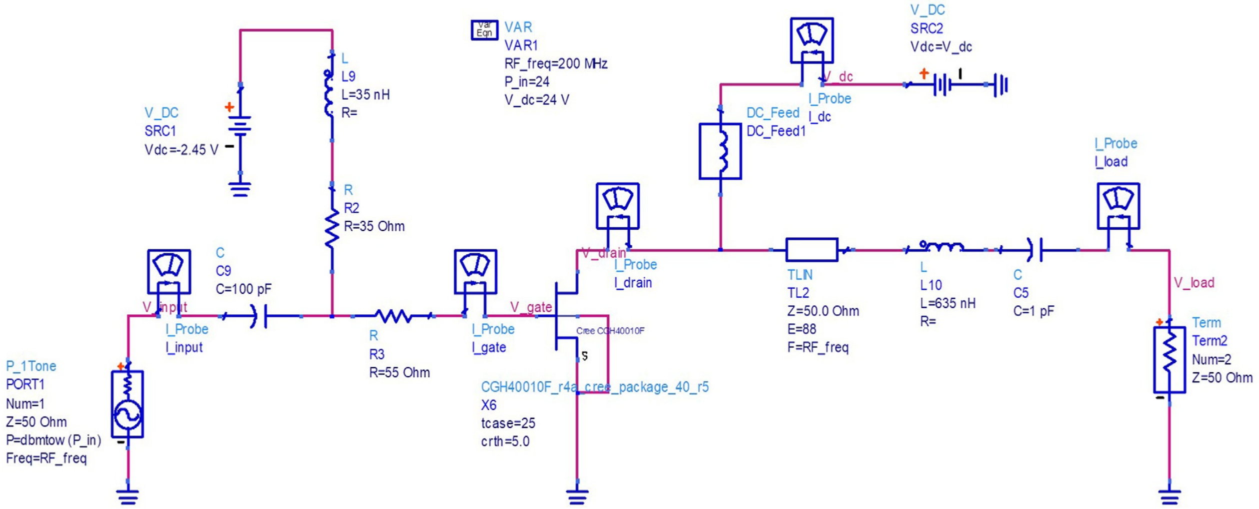
output L_0C_0 circuit presents to the transmission line a load resistance at the frequency of operation. At the same time, the quarter-wavelength transmission line transforms the load impedance according to

$$R = \frac{Z_0^2}{R_L}, \tag{4.18}$$

where Z_0 is the characteristic impedance of a transmission line. For even harmonics, the open circuit on the load side of the transmission line is repeated, thus producing an open circuit at the drain. However, the quarter-wavelength transmission line converts the open circuit at the load to a short circuit at the drain for odd harmonics with resistive load at the fundamental frequency.

Consequently, for a purely sinusoidal current flowing into the load because of infinite loaded quality factor of the series fundamentally tuned circuit, the ideal drain current and voltage waveforms can be represented by the corresponding normalized square and half-sinusoidal waveforms shown in Fig. 4.8B and C, respectively. Here, a sum of the fundamental and odd harmonics approximates a square current waveform and a sum of the fundamental and even harmonics approximates a half-sinusoidal drain voltage waveform. As a result, the shapes of the drain current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously. The quarter-wavelength transmission line causes the output voltage across the load resistor R_L to be phase-shifted by 90 degrees relative to the fundamental-frequency components of the drain voltage and current.

Fig. 4.10 shows a practical example of the circuit schematic of an inverse Class-F power amplifier with a series quarter-wave line based on a 28-V, 10-W Cree GaN high-electron-mobility transistor (HEMT) power transistor CGH40010. Similarly, to the conventional Class-F GaN HEMT power amplifier, a simple lossy *RL* input shunt network is also used to match the device input impedance



V_DC
SRC1
Vdc=-2.45 V
L
L9
L=35 nH
R=
R
R2
R=35 Ohm
VAR
VAR1
RF_freq=200 MHz
P_in=24
V_dc=24 V
V_DC
SRC2
Vdc=V_dc
V_dc
I_Probe
I_dc
DC_Feed
DC_Feed1
I_Probe
I_load
C
C9
C=100 pF
V_input
I_Probe
I_input
R
R3
R=55 Ohm
I_Probe
I_gate
V_gate
V_drain
I_Probe
I_drain
Cree CGH40010F
CGH40010F_r4a_cree_package_40_r5
X6
tcase=25
crth=5.0
TLIN
TL2
Z=50.0 Ohm
E=88
F=RF_freq
L
L10
L=635 nH
R=
C
C5
C=1 pF
V_load
Term
Term2
Num=2
Z=50 Ohm
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(P_in)
Freq=RF_freq

FIG. 4.10

Schematic of inverse Class-F GaN HEMT power amplifier with series quarter-wave line.

to a 50-Ω source and to compensate for the device input gate-source capacitance C_{gs} of about 5 pF at the fundamental frequency, providing a small signal mag(S_{11}) better than −20 dB at an operating frequency of 200 MHz. The series 55-Ω resistor is necessary to provide unconditional operation stability. The simulated drain voltage (close to half-sinusoidal) and current (close to square) waveforms are shown in Fig. 4.11A, where small deviations from the ideal waveforms (with optimized load network parameters) can be explained owing to the effect of the device output drain-source capacitance C_{ds} and package parasitics. In this case, a maximum drain efficiency of 84.8% with a power gain of 12.3 dB and an output power of 40.3 dBm at a supply voltage of 24 V were obtained with a sine-wave driving signal in a deep saturation condition at an input power of 28 dBm, as shown in Fig. 4.11B. Similar drain voltage and current waveforms were measured for a practical 200-MHz inverse Class-F GaN HEMT power amplifier with proper controlling of both third and fifth harmonics.[14]

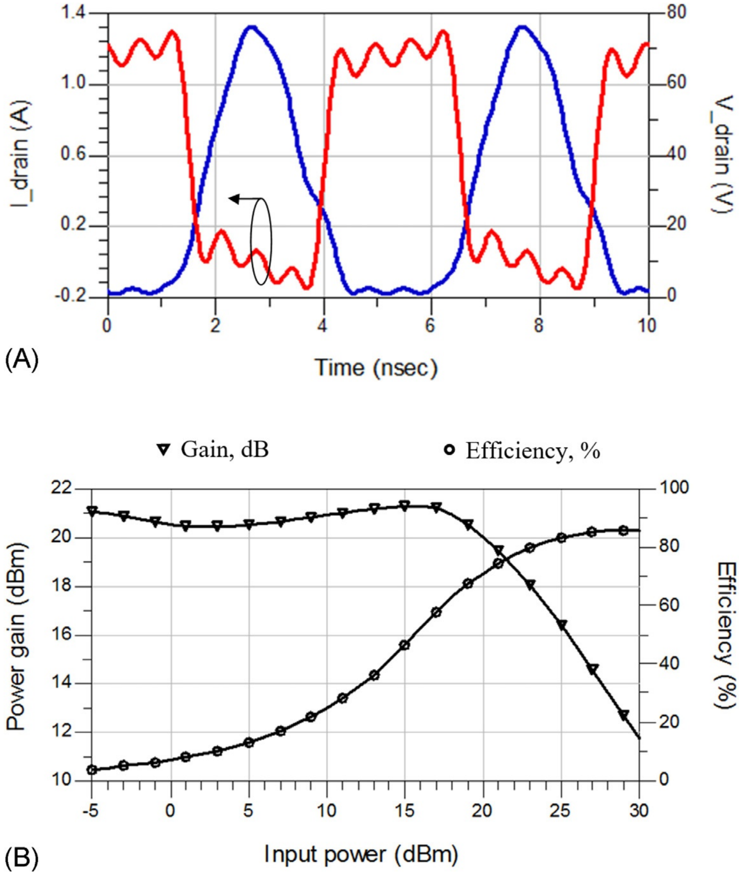


FIG. 4.11

Simulated waveforms, gain, and efficiency of an inverse Class-F GaN HEMT power amplifier.

4.4 Load networks with lumped elements

Theoretical results show that the proper control of the second harmonic can significantly increase the collector efficiency of the power amplifier by flattening the output current waveform and minimizing the product of integration of the voltage and current waveforms. Practical realization of a multielement high-order *LC* resonant circuit can cause a serious implementation problem, especially at higher frequencies and in monolithic integrated circuits, when only three harmonic components can be effectively controlled. Therefore it is enough to be confined to the three- or four-element resonant circuit comprising the load network of the power amplifier. In this case, the operation with the second-harmonic open circuit and third-harmonic short circuit is a promising concept for low-voltage power amplifiers.[15]

In addition, it is necessary to take into account that, in practice, both extrinsic and intrinsic transistor parasitic elements such as output shunt capacitance or serious inductance have a substantial effect on the efficiency. The output capacitance C_{out} can represent the collector capacitance C_{c} in the case of the bipolar transistor or the sum of drain-source capacitance and gate-drain capacitance $C_{\text{ds}} + C_{\text{gd}}$ in the case of the FET device. The output inductance L_{out} is generally composed of the bondwire and lead inductances for a packaged transistor, the effect of which becomes significant at higher frequencies. Fig. 4.12 shows the typical two-terminal lumped reactive networks with series and parallel resonators

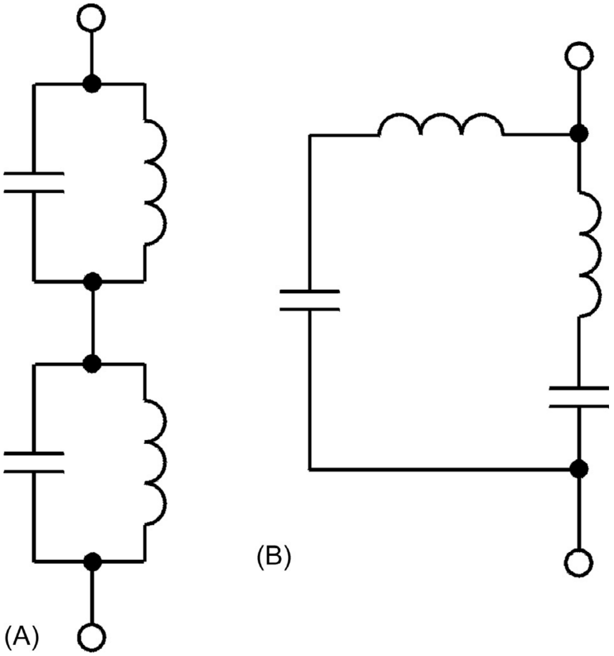


FIG. 4.12

Two-terminal reactive network with series and parallel resonators.

used in a practical design procedure, which provide ideally infinite impedances at the fundamental-frequency and second-harmonic components.

The load network with a second-harmonic impedance-peaking circuit is shown in Fig. 4.13A. Here, the series circuit consisting of an inductor L_1 and a capacitor C_1 creates a resonance at the second harmonic. Because the device output inductance L_{out} and capacitance C_{out} are tuned to create an open-circuited condition at the second harmonic, the device collector sees the resultant high impedance at the second harmonic. To achieve the second-harmonic high impedance, an external inductance can be added to interconnect the device output inductance L_{out} directly at the output if its value is not enough. As a result, the values of the load network parameters are

$$L_{\text{out}} = \frac{1}{4\omega_0^2 C_{\text{out}}}, \tag{4.19}$$

$$L_1 = \frac{1}{4\omega_0^2 C_1}. \tag{4.20}$$

The lumped load network with second-harmonic peaking, which was used in an inverse Class-F LDMOSFET power amplifier operated at 1 GHz with an output power of 13 W, is shown in Fig. 4.13B.[16] In this case, the capacitances C_1 and C_2 associated to inductance L_1 were optimized to present high impedance to the second harmonic and an optimal load resistance seen by the device

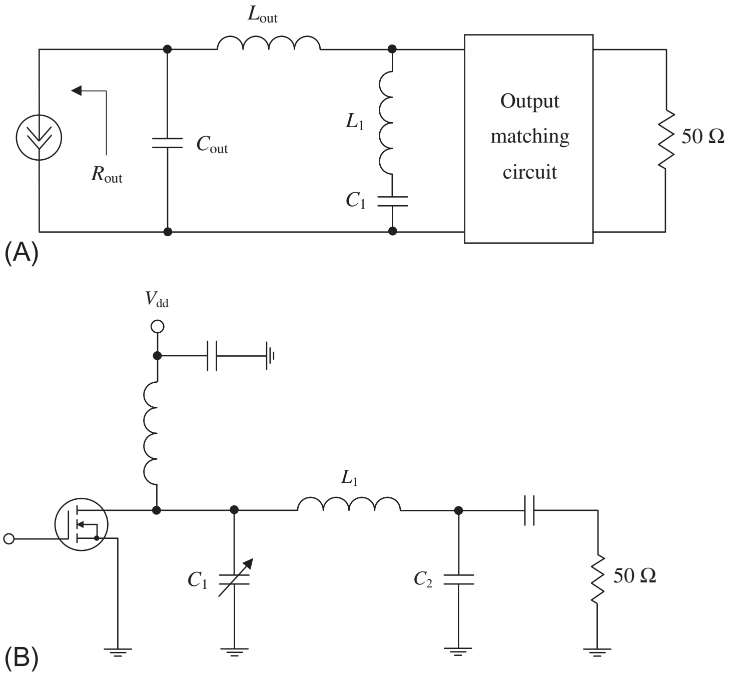


FIG. 4.13

Second-harmonic lumped impedance-peaking circuits.

output. The capacitance C_1 was chosen to be adjustable, taking into account the limited technology implementation accuracy. With accurate tuning of the load network parameters, the power-added efficiency can be increased by more than 10% when compared to the conventional Class-B mode.

There is a possibility to simultaneously control both the second and third harmonics by using a shunt series resonant circuit and a parallel resonant circuit connected in series to the output, as shown in Fig. 4.14. Here, the series resonant circuit consisting of an inductor L_1 and a capacitor C_1 creates a short-circuit condition at the second harmonic. Because the output inductor L_{out} and capacitor C_{out} are tuned to create an open-circuit condition at the second harmonic, the device collector sees the resultant high impedance at the second harmonic. In addition, the parallel resonant tank (L_2, C_2) is tuned to the third harmonic, whereas the series network ($L_1 + L_{\text{out}}$, C_1) provides a short-circuit condition at the third harmonic. If necessary, an external inductance can be added to increase the value of the device output inductance L_{out}.

As a result, in addition to Eq. (4.19), the ratios between the remaining load network parameters can be written as

$$L_1 = \frac{9}{5} L_{\text{out}}, \tag{4.21}$$

$$C_1 = \frac{5}{9} C_{\text{out}}, \tag{4.22}$$

$$L_2 = \frac{1}{9\omega_0^2 C_2}. \tag{4.23}$$

Fig. 4.15 shows the circuit configuration of a GaN HEMT inverse Class-F power amplifier considering up to the fourth-order harmonic control.[17] Here, the series reactance circuit has pole points at $2f_0$ and $4f_0$, and zero point at $3f_0$, whereas the shunt reactance circuit has pole point at f_0 and zero point at $3f_0$, where f_0 is the fundamental frequency. The output matching circuit is added between the inverse Class-F harmonic-control circuit and 50-Ω load. Because the upper limit for the self-resonant frequency of the commercially available chip capacitors and inductors is around 8 GHz, the operating frequency $f_0 =$ 860 MHz was chosen to demonstrate the drain efficiency over 75% at about 1-W output power.

As a first approximation for comparison between different operation modes, the output device resistance R_{out} at the fundamental frequency required to realize an inverse Class-F operation mode with second-harmonic peaking can be estimated as an equivalent resistance $R_{\text{out}} = R_1^{(\text{invF})} = V_1/I_1$ determined

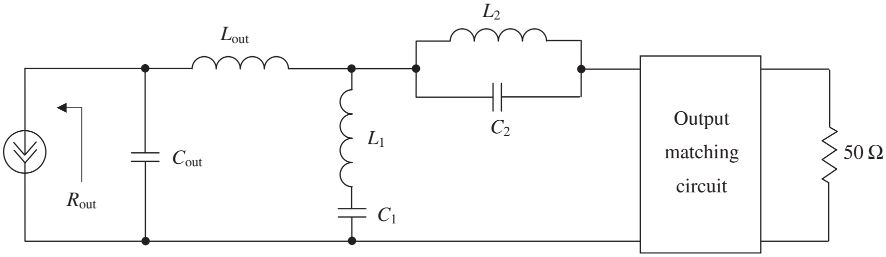


FIG. 4.14

Impedance-peaking load network, including device output inductance.

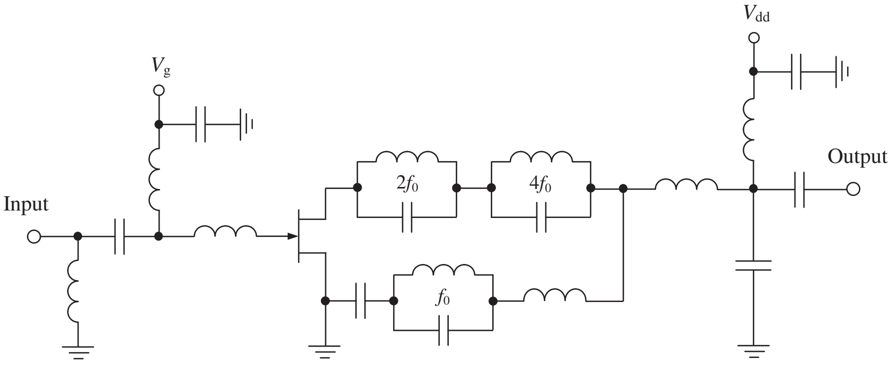


FIG. 4.15

Schematic of inverse Class-F power amplifier with up to the fourth-order harmonic control.

at the fundamental frequency for an ideal inverse Class-F operation. Assuming zero saturation voltage and using Eq. (3.29) from Chapter 3 and Eq. (4.14) yield

$$R_1^{(\text{invF})} = \frac{\pi^2}{8}\frac{V_{\text{cc}}}{I_0} = \left(\frac{\pi^2}{8}\right)^2 R_1^{(\text{F})} = \left(\frac{\pi}{2}\right)^2 R_1^{(\text{B})}, \tag{4.24}$$

where $R_1^{(\text{F})}$ is the equivalent output resistance in a conventional Class-F mode, and $R_1^{(\text{B})} = V_{\text{cc}}/I_1 = V_{\text{cc}}^2/2P_1$ is the equivalent output resistance in an ideal Class-B at the fundamental frequency. As follows from Eq. (4.24), the equivalent output resistance for an ideal inverse Class-F mode is of about 2.5 times higher compared to a conventional Class-B operation. Therefore using an inverse Class-F operation mode simplifies the load network design by minimizing the impedance transformation ratio. This is very important for a high output power level when the output resistance is sufficiently small. However, the maximum amplitude of the output voltage waveform can exceed the supply voltage by about three times.

4.5 Load networks with transmission lines

The ideal inverse Class-F power amplifier cannot provide all voltage third- and higher-order odd-harmonic short-circuit termination by the use of a single parallel transmission line, as can easily be realized by a quarter-wavelength transmission line for even harmonic shorting in the conventional Class-F power amplifier. In this case, with a sufficiently simple circuit schematic convenient for practical realization, applying the current second-harmonic peaking and voltage third-harmonic shorting can result in a maximum drain efficiency of more than 80%.[18, 19] For example, by providing a proper high-impedance second-harmonic peaking and load matching at the fundamental, the collector efficiency of 83% for a 425-MHz microstrip bipolar power amplifier and the drain efficiency of 68% for a 4-GHz MMIC GaN HEMT power amplifier have been achieved.[20, 21] Generally, to control the second and third harmonics at microwave frequencies, it is preferable to use the short-circuit and open-circuit stubs instead of lumped capacitors in the load network for better performance predictability and tuning accuracy.[22, 23]

Fig. 4.16A shows the idealized transmission-line inverse Class-F load network schematic where a shunt $\lambda/6$ transmission line grounded through the bypass capacitor provides a low impedance for the third harmonic and certain impedances for the fundamental and second harmonics at the device drain terminal.[19, 24] The second-harmonic peaking is achieved by using an open-circuit $\lambda/8$ stub, which creates a low impedance at the right-hand side of the series $\lambda/12$ transmission line at the second harmonic. As a result, this series $\lambda/12$ transmission line with an electrical length of 60 degrees at the second harmonic (combined in parallel with the shunt $\lambda/6$ transmission line with electrical length of 120 degrees at the second harmonic) represents a second-harmonic tank.

It is also useful and very practical for inverse Class-F power amplifiers to consider an alternative transmission-line load network with a series $\lambda/8$ transmission line as a first element, as shown in Fig. 4.16B.[25, 26] In this case, the series $\lambda/8$ transmission line short-circuited at its right-hand side by the shunt quarter-wavelength transmission line at the second harmonic provides an open circuit at the second harmonic seen by the device output, whereas the combined ($\lambda/8 + \lambda/24 = \lambda/6$) series transmission line short-circuited at its right-hand side by the open-circuit $\lambda/12$ stub provides a short circuit at

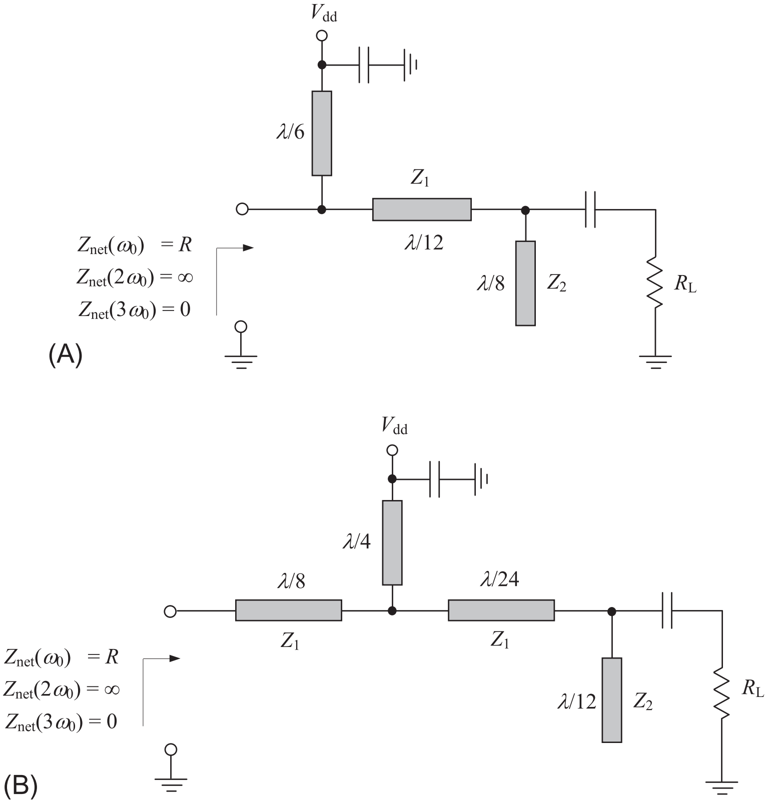

V_{dd}
$\lambda/6$
Z_1
$\lambda/12$
$Z_{net}(\omega_0) = R$
$Z_{net}(2\omega_0) = \infty$
$Z_{net}(3\omega_0) = 0$
$\lambda/8$
Z_2
R_L
(A)
V_{dd}
$\lambda/4$
$\lambda/8$
$\lambda/24$
Z_1
Z_1
$Z_{net}(\omega_0) = R$
$Z_{net}(2\omega_0) = \infty$
$Z_{net}(3\omega_0) = 0$
$\lambda/12$
Z_2
R_L
(B)

FIG. 4.16

Idealized transmission-line inverse Class-F load networks.

the third harmonic seen by the device output. By proper choice of the characteristic impedances of the transmission lines, the impedance matching conditions at the fundamental frequency can be realized.

The load network impedance Z_{net} seen by the device output at the fundamental can be written as

$$Z_{\text{net}} = Z_1 \frac{R_{\text{L}}(Z_2 - Z_1 \tan 30° \tan 60°) + jZ_1 Z_2 \tan 60°}{Z_1 Z_2 + j(Z_1 \tan 30° + Z_2 \tan 60°)R_{\text{L}}}, \tag{4.25}$$

where Z_1 is the characteristic impedance of the combined series transmission line, and Z_2 is the characteristic impedance of an open-circuit $\lambda/12$ stub. Separating Eq. (4.25) into real and imaginary parts and considering that $\text{Re}Z_{\text{net}} = R$ and $\text{Im}Z_{\text{net}} = 0$, the system of two equations with two unknown parameters is obtained by using the following expression:

$$(Z_1 + 3Z_2)^2 R_{\text{L}}^2 R - 3Z_1^2 Z_2^2 (4R_{\text{L}} - 3R) = 0, \tag{4.26}$$

$$3Z_1^2 Z_2^2 - R_L^2 (Z_2 - Z_1)(Z_1 + 3Z_2) = 0, \tag{4.27}$$

which allows direct calculation of the characteristic impedances Z_1 and Z_2. This system of two equations can be explicitly solved as a function of the parameter $r = R_{\text{L}}/R$ resulting in

$$\frac{Z_1}{R_{\text{L}}} = \frac{\sqrt{4r-1}}{\sqrt{3}r}, \tag{4.28}$$

$$\frac{Z_1}{Z_2} = \frac{r-1}{r}. \tag{4.29}$$

Consequently, if the required optimum load resistance and standard load resistance are equal to $R = 20\,\Omega$ and $R_{\text{L}} = 50\,\Omega$, respectively, resulting in $r = 2.5$, then the characteristic impedance of the series transmission line calculated from Eq. (4.28) is equal to $Z_1 = 35\,\Omega$, and the characteristic impedance of the open-circuit stub calculated from Eq. (4.29) is equal to $Z_2 = 58\,\Omega$.

Fig. 4.17 shows the simplified inverse Class-F load network with the second- and third-harmonic control using a series stepped-impedance transmission line, where θ_1 and θ_2 are the electrical lengths of the stepped-impedance transmission-line sections and M is the characteristic impedance ratio. In this

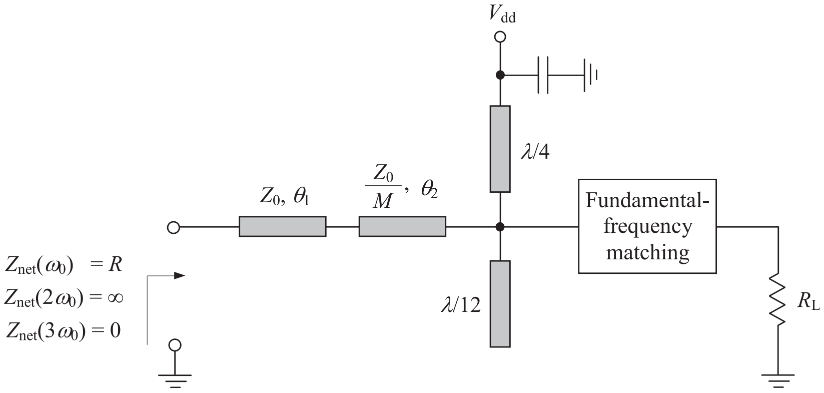

V_{dd}
$\lambda/4$
Z_0, θ_1
$\frac{Z_0}{M}$, θ_2
Fundamental-frequency matching
$Z_{\text{net}}(\omega_0) = R$
$Z_{\text{net}}(2\omega_0) = \infty$
$Z_{\text{net}}(3\omega_0) = 0$
$\lambda/12$
R_{L}

FIG. 4.17

Transmission-line inverse Class-F load network with stepped-impedance line.

case, a simple combination of two loaded transmission lines with high and low characteristic impedances can provide simultaneously the fundamental impedance matching and second-harmonic tuning to a high impedance nearby open-circuit condition.[21] However, by optimizing the characteristic impedances of the transmission-line sections, infinite impedance at the second harmonic and zero impedance at the third harmonic can be provided simultaneously. For the simplicity of analytical calculations, the transmission-line lengths can be set equal as $\theta = \theta_1 = \theta_2$.

The input network impedance Z_{net} as a function of electrical length θ of equal sections of the stepped-impedance transmission line is written as

$$Z_{\text{net}} = Z_0 \frac{Z_{\text{L}}(1 - M\tan^2\theta) + jZ_0\left(\frac{1}{M} + 1\right)\tan\theta}{Z_0\left(1 - \frac{\tan^2\theta}{M}\right) + jZ_{\text{L}}(M+1)\tan\theta}, \tag{4.30}$$

where Z_{L} is the load impedance including the short-circuit and open-circuit stubs.

For $Z_{\text{L}} = 0$,

$$Z_{\text{net}} = jZ_0 \frac{\frac{1}{M} + 1}{1 - \frac{\tan^2\theta}{M}} \tan\theta, \tag{4.31}$$

whose zeroes correspond to $\theta_{0\text{k}} = (\pi/2)k$ and poles correspond to

$$\theta_{pk} = k\pi \pm \tan^{-1}\sqrt{M}, \tag{4.32}$$

where $k = 0, 1, 2, \ldots$ Thus by choosing the proper characteristic impedance ratio M, the first pole θ_{p1} can be moved from initial value of 45 degrees for uniform line toward the second zero at $\theta_{02} = 90$ degrees and set at $\theta_{\text{p1}} = 60$ degrees for the stepped-impedance transmission line with $M = 3$. As a result, by using such a stepped-impedance transmission line, an open circuit at the second harmonic and short circuit at the third harmonic of the fundamental frequency can be provided if the fundamental frequency corresponds to $\theta = 30$ degrees.

Fig. 4.18A shows the design example of a stepped-impedance transmission-line inverse Class-F load network with harmonic tuning that provides an impedance matching at the fundamental frequency between the input impedance of 20 Ω and load impedance of 50 Ω at $f_0 = 2$ GHz.[23, 27] In this case, the stepped-impedance transmission line with equal section lengths of 30 degrees loaded by a short-circuited quarter-wavelength line and an open-circuit $\lambda/12$ stub creates an open circuit at the second harmonic and short circuit at the third harmonic seen by the 20-Ω source at its input. Using a subsequent short-length transmission line as an element of the output, fundamental-frequency matching circuit is required to compensate for the reactive part of the modified source impedance (any source impedance can be transformed to a real load impedance using a $\lambda/8$ transformer, whose characteristic impedance is equal to the magnitude of the source impedance[28]) followed by the quarter-wavelength transmission line that provides the transformation of the real part of the modified source impedance to the standard load of 50 Ω. The frequency response of such a stepped-impedance transmission-line inverse Class-F load network with harmonic tuning is shown in Fig. 4.18B, which demonstrates the fundamental-frequency impedance matching at 2 GHz, second-harmonic open circuit at 4 GHz, and third-harmonic short circuit at 6 GHz.

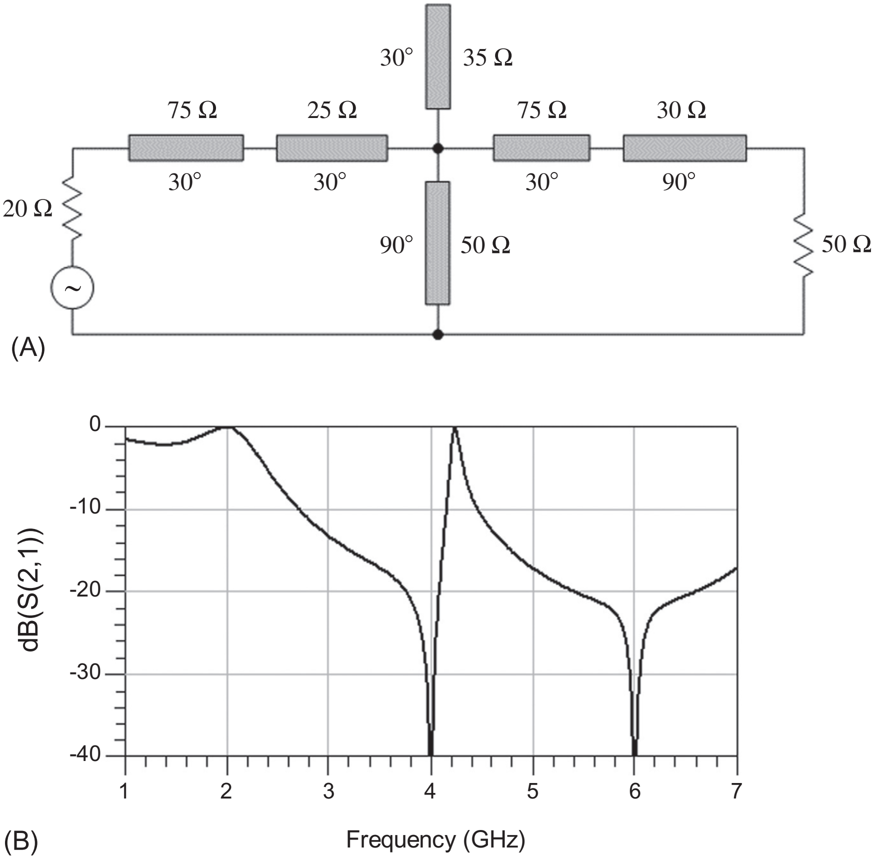


FIG. 4.18

Load network with second- and third-harmonic control and its frequency response.

However, the efficiency of the power amplifier can be limited by the transistor output capacitance C_{out} (mostly represented by drain-source capacitance C_{ds} or collector capacitance C_{c}) if this capacitance is not absorbed into multiharmonic load network without compromising the ability to properly terminate the second- and third-harmonic components. Fig. 4.19A shows the simplified circuit schematic of a transmission-line transistor power amplifier, whereas the equivalent load network corresponding to inverse Class-F mode with a shunt short-circuited $\lambda/3$ transmission line which provides a short circuit at the third harmonic at the device output is shown in Fig. 4.19B.[19] This circuit configuration is similar to that used to provide a conventional Class-F operation mode.

For such an inverse Class-F microstrip power amplifier, it is necessary to provide the following electrical lengths for the transmission lines at the fundamental frequency:

$$\theta_1 = \frac{\pi}{3}, \tag{4.33}$$

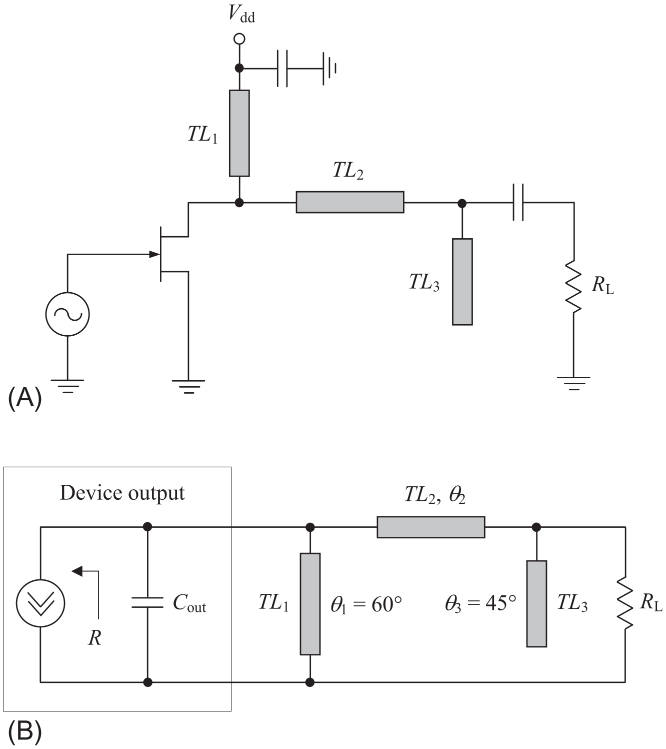


FIG. 4.19

Transmission-line inverse Class-F load network with shunt capacitance.

$$\theta_2 = \frac{1}{2}\tan^{-1}\left[\left(2Z_0\,\omega_0\,C_{out} + \frac{1}{\sqrt{3}}\right)^{-1}\right], \tag{4.34}$$

$$\theta_3 = \frac{\pi}{4}, \tag{4.35}$$

where Z_0 is the characteristic impedance of the microstrip lines. The transmission line TL_1 with electrical length $\theta_1 = 60$ degrees provides a short-circuited condition for the third harmonic, whereas all three transmission lines, together with the device output capacitance, form a parallel resonant circuit to realize an open-circuit condition for the second harmonic at the drain terminal. The open-circuit stub TL_3 with electrical length $\theta_3 = 45$ degrees creates a short-circuited condition at the end of the transmission line TL_2 at the second harmonic. Thus the series short-circuited transmission line TL_2 having an inductive reactance is tuned to the parallel resonance condition with the device output capacitance C_{out} and short-circuited transmission line TL_1.

As an example, Fig. 4.20 shows the frequency-response characteristic of the microstrip impedance-peaking circuit using an alumina substrate for the device equivalent output resistance $R_{out} = 50\,\Omega$ and

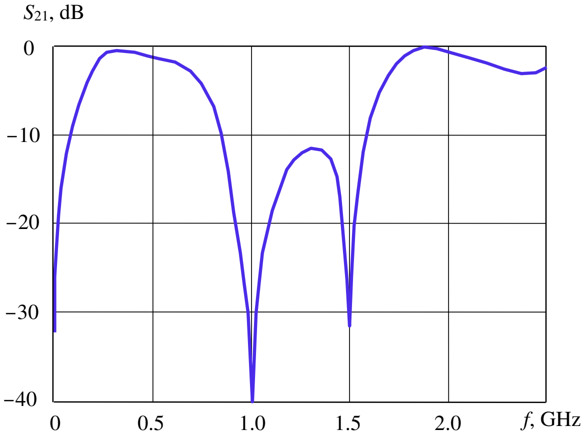


FIG. 4.20

Frequency response of the microstrip impedance-peaking circuit.

output capacitance $C_{out} = 2.2$ pF, characteristic impedance of microstrip lines $Z_0 = 50\,\Omega$, and electrical length $\theta_2 = 19$ degrees. From Fig. 4.20, it follows that, for the second-harmonic peaking and third-harmonic short-circuit termination, an additional output matching at the fundamental frequency $f_0 = 500$ MHz is required, taking into account the reactance introduced by the impedance-peaking load network.

Generally, to ensure that the fundamental matching did not affect the harmonic control, the load network can represent a separate fundamental matching circuit in addition to the harmonic-control circuit, as shown in Fig. 4.21.[29, 30] In this case, the harmonic-control circuit contains two shunt open-circuit stubs and two series transmission lines that provide the second- and third-harmonic control. The electrical length of each open-circuit stub is chosen to present a short circuit for the frequency of the corresponding harmonic at the junction with the series transmission line, in order not to be affected by tuning the fundamental matching network. The series transmission lines with electrical lengths θ_1 and θ_2 are used to provide the correct phase of the optimum harmonic reflection coefficient Γ_{opt} to the device drain.

Fig. 4.21A shows the load network configuration where the second-harmonic stub is closer to the drain than the third-harmonic stub. Because its electrical length is $\lambda/8$, which corresponds to $\lambda/4$ at the second harmonic, the second-harmonic stub transforms the open end to a short circuit, allowing for the achievement of a reflection coefficient independent of the fundamental matching and with a magnitude very close to unity at $2f_0$. Similarly, the third-harmonic stub with a length of $\lambda/12$ at f_0 is used to tune the third harmonic independently from the fundamental matching. The load network configuration with a third-harmonic stub placed closer to the transistor drain is shown in Fig. 4.21B. Even though both configurations present the same reflection coefficient to the transistor at the fundamental, second-harmonic, and third-harmonic frequencies, their resulting efficiencies can be different depending upon the difference in the conduction loss introduced by each topology. Despite high drain efficiencies provided by these load networks in implemented 10-W GaN HEMT inverse Class-F power amplifiers, greater than 80% at 1 GHz and about 75% at 2.45 GHz, the entire tuning procedure to properly match the impedances at the fundamental frequency and to provide the second- and third-harmonic control is quite complicated, and each load network requires a significant substrate space to be implemented.

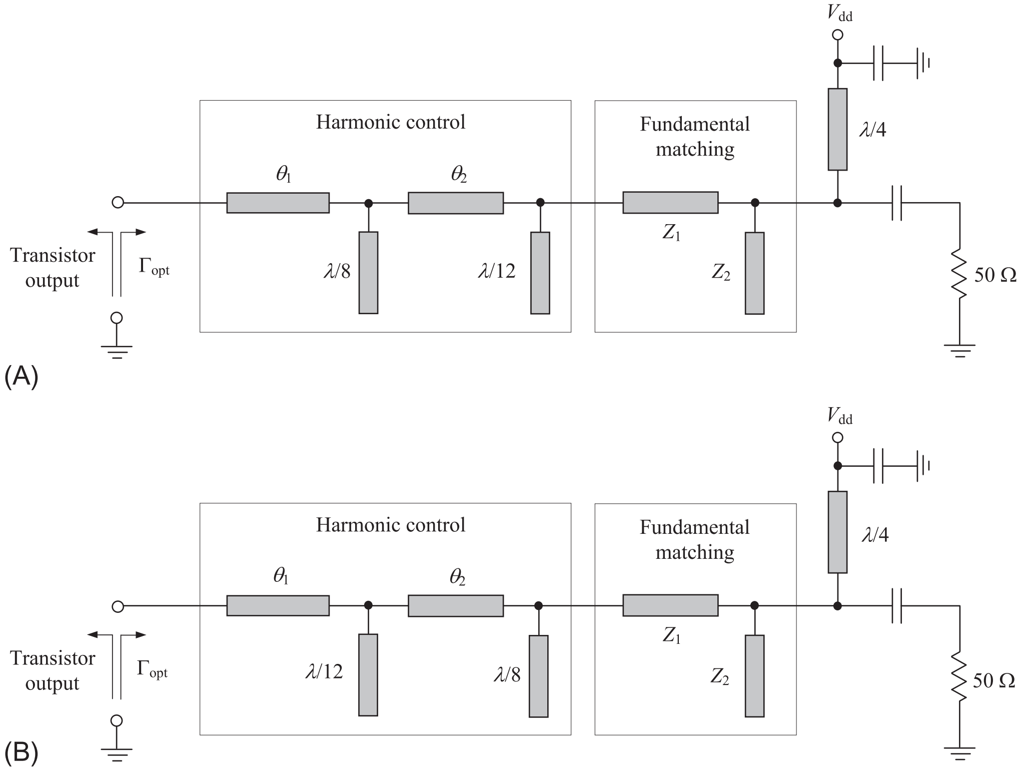

(A)
Harmonic control
Fundamental matching
V_{dd}
$\lambda/4$
θ_1
θ_2
$\lambda/8$
$\lambda/12$
Z_1
Z_2
Transistor output
Γ_{opt}
50 Ω
(B)
Harmonic control
Fundamental matching
V_{dd}
$\lambda/4$
θ_1
θ_2
$\lambda/12$
$\lambda/8$
Z_1
Z_2
Transistor output
Γ_{opt}
50 Ω

FIG. 4.21

Idealized transmission-line inverse Class-F load networks.

At higher frequencies, especially at microwaves, the effect of the output series inductance L_{out} (including a bondwire inductance and a lead inductance for the packaged device) becomes significant. Therefore it is useful to describe the relationship between the internal device parameters and parameters of the external harmonic-control circuit in a simple analytical way. The circuit schematic of a simple transmission-line impedance-peaking circuit is shown in Fig. 4.22A, where a combination of the series transmission line TL_1 and open-circuit stub TL_2, together with the output capacitance C_{out} and inductance L_{out}, is used to provide an open-circuited condition seen by the device multiharmonic current source at the second harmonic. Because the open-circuit stub at the second harmonic has zero impedance, the network admittance at the second harmonic can be written as

$$Y_{net}(2\omega_0) = j2\omega_0 C_{out} + \frac{1}{j2\omega_0 L_{out} + jZ_0 \tan 2\theta_0}. \tag{4.36}$$

Hence when $\text{Im}Y_{net}(2\omega_0) = 0$, the electrical length θ_0 of the series transmission line TL_1 is defined by

$$\theta_0 = \frac{1}{2}\tan^{-1}\left(\frac{1-4\omega_0^2 L_{out} C_{out}}{2\omega_0 C_{out} Z_0}\right), \tag{4.37}$$

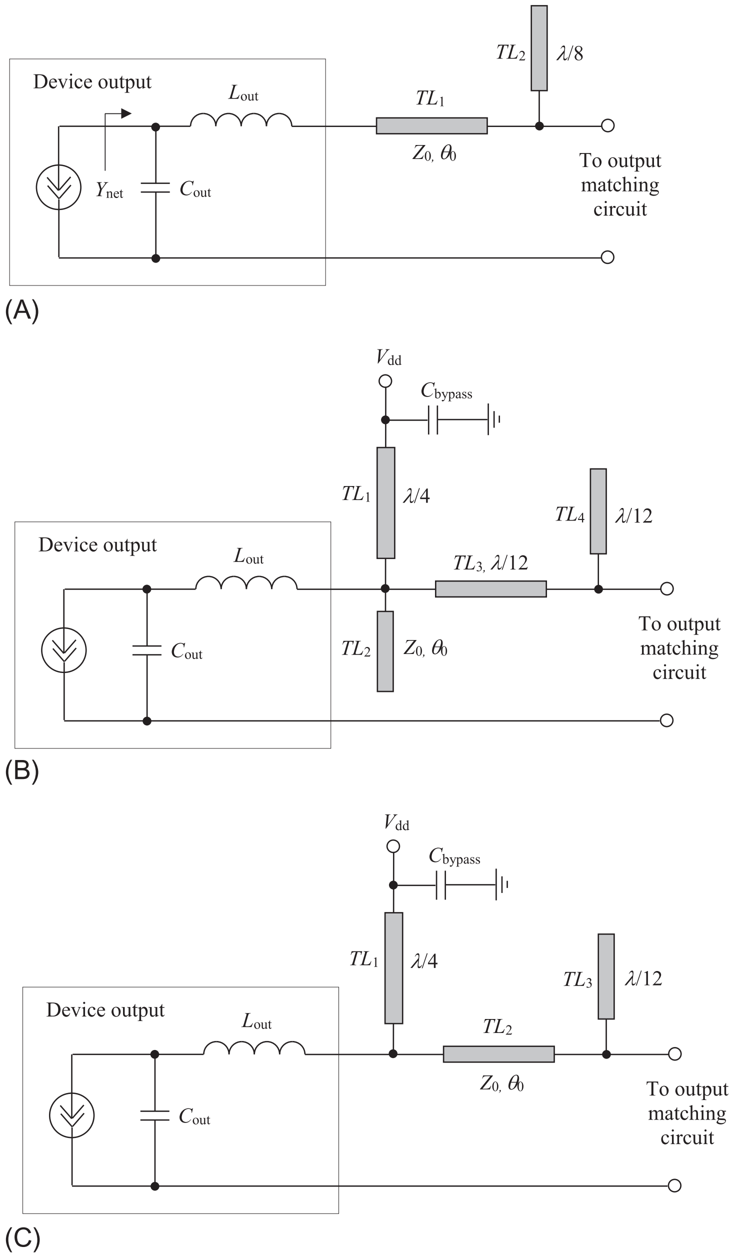

Device output
L_{out}
TL_1
TL_2
$\lambda/8$
Z_0, θ_0
Y_{net}
C_{out}
To output matching circuit
(A)
V_{dd}
C_{bypass}
TL_1
$\lambda/4$
TL_4
$\lambda/12$
Device output
L_{out}
$TL_3, \lambda/12$
C_{out}
TL_2
Z_0, θ_0
To output matching circuit
(B)
V_{dd}
C_{bypass}
TL_1
$\lambda/4$
TL_3
$\lambda/12$
Device output
L_{out}
TL_2
Z_0, θ_0
C_{out}
To output matching circuit
(C)

FIG. 4.22

Transmission-line inverse Class-F load networks with bondwire inductance.

resulting in a parallel resonant tank consisting of the shunt capacitance C_{out} and parallel inductance composed by the output inductance L_{out} and transmission line TL_1.

Another configuration of the impedance-peaking circuit, including the device output series inductance L_{out}, is shown in Fig. 4.22B, where the open-circuit and short-circuit transmission-line stubs are used to create both the third-harmonic short-circuit termination and second-harmonic peaking. The device output elements C_{out} and L_{out} (if necessary, an additional series inductor should be added) should create a parallel resonance at the second harmonic because the short-circuit stub TL_2 represents a half-wave line at the second harmonic with short-circuited conditions at its both ends. The electrical length θ_0 of an open-circuit stub TL_1 is chosen to have less than a quarter wavelength at the third harmonic to realize a capacitive reactance to be resonant with an output inductance L_{out} at the third harmonic of the fundamental frequency. The transmission lines TL_3 and TL_4 must be of quarter wavelengths at the third harmonic to provide a third-harmonic high-impedance condition at the input of TL_3. As a result, the ratios between the elements are

$$L_{\text{out}} = \frac{1}{4\omega_0^2 C_{\text{out}}}, \tag{4.38}$$

$$\theta_0 = \frac{1}{3}\tan^{-1}\left(\frac{Z_0}{3\omega_0 L_{\text{out}}}\right). \tag{4.39}$$

The impedance-peaking circuit shown in Fig. 4.22B, which provides open circuit at the second harmonic and short circuit at the third harmonic, can be simplified by removing the open-circuited transmission line TL_2 and properly setting the electrical length of the transmission line TL_3, which corresponds to the transmission line TL_2 with electrical length θ_0, as shown in Fig. 4.22C. To provide capacitive reactance to be resonant with output inductance L_{out} at the third harmonic of the fundamental frequency, the electrical length θ_0 of a series transmission line TL_2, which is short-circuited at the third harmonic, should be chosen to be longer than a quarter wavelength at the third harmonic. As a result,

$$\theta_0 = \frac{1}{3}\left(\pi - \tan^{-1}\frac{3\omega_0 L_{\text{out}}}{Z_0}\right), \tag{4.40}$$

where Z_0 is the characteristic impedance of the transmission lines TL_2.

As an alternative to this simple analytical approach, a complicated and time-consuming load-pull optimization procedure can be used to optimize impedance both at the fundamental frequency and second and third harmonics. Fig. 4.23A shows the transmission-line inverse Class-F load network which includes the device drain-source capacitance C_{ds} and package parasitics represented by a Π-type lowpass $C_1L_1C_2$ network.[31] By using load-pull optimization, the load network was designed to provide an open circuit at the second harmonic and a short circuit at the third harmonic at the intrinsic drain port. Moreover, the matching conditions between the 50-Ω standard load and 35-Ω equivalent output impedance required to realize an optimum inverse Class-F load at the fundamental frequency are provided by the load network as well. As a result, a drain efficiency of 66% and an output power of 13.8 W were obtained for a 2.14-GHz, 28-V LDMOSFET inverse Class-F power amplifier.

Fig. 4.23B shows the circuit schematic of a 3.5-GHz, 28-V GaN HEMT inverse Class-F power amplifier where a transistor bare die is used to reduce the parasitics of the package and facilitate harmonic impedance optimization at the transistor output reference plane.[32] Here, L_{bg} and L_{bd} are used to model the input and output bondwire inductances, respectively. The general optimization procedure consists

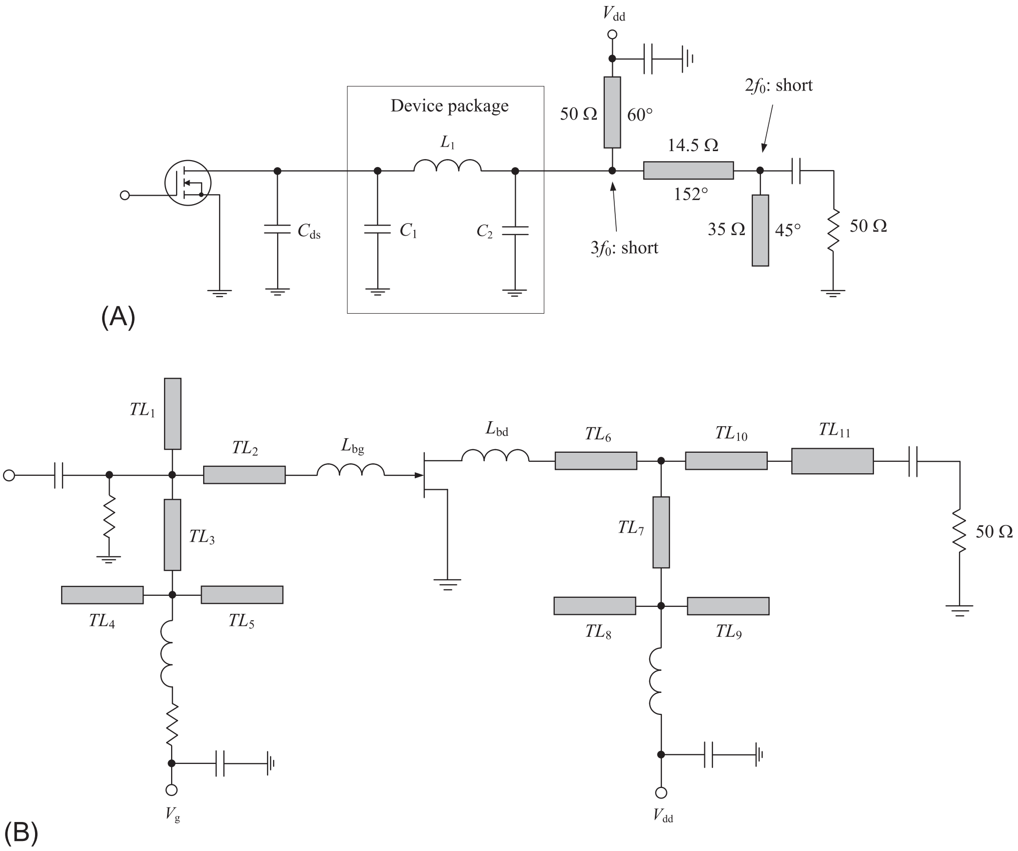

V_{dd}
Device package
50 Ω
60°
2f_0: short
14.5 Ω
L_1
152°
C_{ds}
C_1
C_2
35 Ω
45°
50 Ω
3f_0: short
(A)
TL_1
TL_2
L_{bg}
L_{bd}
TL_6
TL_{10}
TL_{11}
TL_3
TL_7
50 Ω
TL_4
TL_5
TL_8
TL_9
V_g
V_{dd}
(B)

FIG. 4.23

Circuit schematics of transmission-line inverse Class-F power amplifier.

of two steps: a source-pull/load-pull simulation to find the optimum source and load impedances at the fundamental frequency for efficiency and output power and then a harmonic load-pull simulation to define the optimum second- and third-harmonic load and source impedances for high-efficiency operation. The input matching circuit consists of the transmission lines from TL_1 to TL_5, and the load network is composed of the transmission lines from TL_6 to TL_{11}, which are all optimized to provide the optimum matching at the fundamental frequency and the corresponding second- and third-harmonic control. Finally, a maximum drain efficiency of 82% with a power gain of 12 dB was achieved at an output power of 40.4 dBm using a RO5870 substrate for board fabrication.

4.6 LDMOSFET power amplifier design examples

The effectiveness of the transmission-line load network design technique for inverse Class-F application can be demonstrated by the example of a 28-V high-power LDMOSFET amplifier with the device

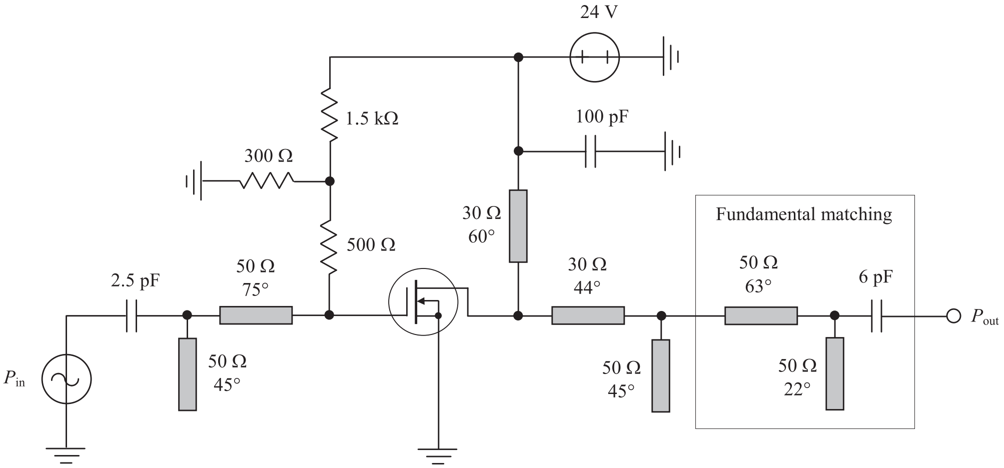


FIG. 4.24

Simulated 500-MHz single-stage microstrip power amplifier with *T*-transformer.

of the same geometry as for a conventional Class-F mode, the small signal equivalent circuit and output current-voltage characteristics of which are shown in Fig. 3.41 in Chapter 3. The circuit schematic of the simulated 500-MHz single-stage microstrip inverse Class-F power amplifier is shown in Fig. 4.24. In this case, both input and output matching circuits represent the T-type low-pass matching circuits, with a series microstrip line, a shunt open-circuit stub having a capacitive reactance, and a series capacitor. To provide the third-harmonic short-circuit termination and second-harmonic peaking corresponding to an inverse Class-F operation mode, the short-circuited microstrip line with electrical length of 60 degrees and a combination of a series microstrip line and an open-circuit stub with electrical length of 45 degrees for the second-harmonic termination are used.

Fig. 4.25A shows the drain voltage waveform which is only slightly different from the half-sinusoidal shape because of the fourth- and higher-order harmonics that are not properly controlled. Nevertheless, a drain efficiency of up to 71% with a maximum output power of 8 W was achieved, as shown in Fig. 4.25B. In this case, the peak value of the drain voltage is by more than two times greater than the drain supply voltage of 24 V, resulting in a peak factor approximately equal to $58/24 = 2.4$.

To minimize the number of the circuit elements, the output fundamental matching circuit of such a transmission-line power amplifier can also be realized in the form of a high-pass L-transformer with a series capacitor and a shunt transmission line grounded at its end, as shown in Fig. 4.26A. Simulation results indicate that, for this particular case, the length of a short-circuited transmission line in the output matching circuit is close to a quarter wavelength, corresponding to a significant inductive reactance at the fundamental frequency. Consequently, in this case, the load network designed to provide the second- and third-harmonic control can perform a function of the matching circuit as well, together with the series capacitance required for DC blocking. The simplified and slightly modified circuit schematic of the simulated 500-MHz single-stage microstrip inverse Class-F high-power amplifier with total LDMOSFET channel width of 28 × 1.44 mm is shown in Fig. 4.26B.

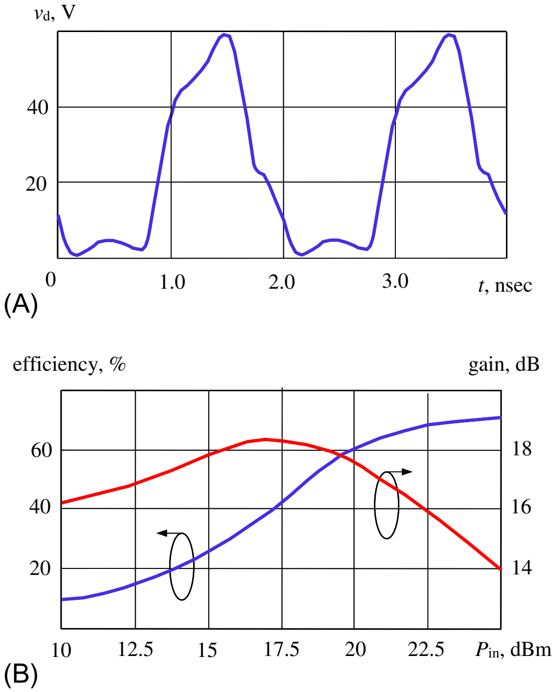


FIG. 4.25

Drain voltage waveform, efficiency, and power gain.

As a result, the drain efficiency up to 78% for an output power of about 25 W with a power gain of 14 dB can be achieved, as shown in Fig. 4.27A. An analysis of the drain voltage and current waveforms plotted in Fig. 4.27B indicates that the operation mode obtained is close to an inverse Class-F mode where the drain current waveform approximates a square wave, while the drain voltage waveform is close to a half-sinusoidal waveform. It should be noted that the negative current values are because of the current flowing through the intrinsic drain-source capacitance when the device multiharmonic voltage-controlled current source is pinched off. Besides, there is a small phase shift between voltage and current waveforms due to uncompensated phases at the harmonics using such a simple load network which provides both fundamental matching and second- and third-harmonic control. In this case, the maximum drain voltage amplitude does not reach even a value of 60 V.

Fig. 4.28 shows the (A) harmonic spectrum corresponding to the drain current waveform and (B) harmonic spectrum corresponding to the drain voltage waveform up to fifth harmonic components. As it is seen, both the second harmonic of a drain current waveform and the third harmonic of a drain voltage waveform are slightly increased than expected from the ideal waveforms. In addition, the higher order harmonic components also make their contribution to the shapes of the drain voltage and current waveforms. In practical design, it is possible to use chip capacitors instead of the open-circuit microstrip stubs to minimize the overall size of a power-amplifier board. In this case, the presence of a parasitic series inductance of the chip capacitor together with a parasitic via inductance can be useful to tune the capacitor's series self-resonance condition to the second harmonic.

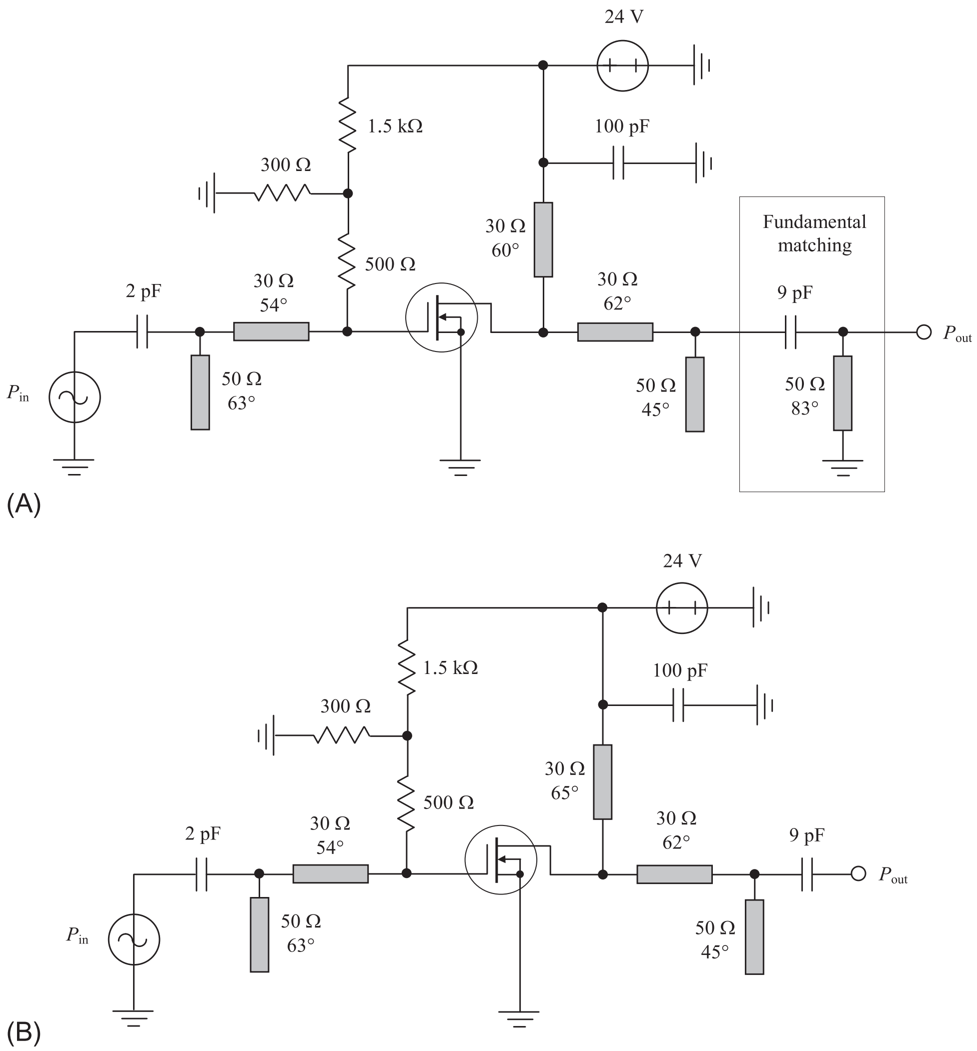

24 V
1.5 kΩ
100 pF
300 Ω
30 Ω
60°
Fundamental
matching
500 Ω
2 pF
30 Ω
54°
30 Ω
62°
9 pF
P_{out}
P_{in}
50 Ω
63°
50 Ω
45°
50 Ω
83°
(A)
24 V
1.5 kΩ
100 pF
300 Ω
30 Ω
65°
500 Ω
30 Ω
62°
2 pF
30 Ω
54°
9 pF
P_{out}
P_{in}
50 Ω
63°
50 Ω
45°
(B)

FIG. 4.26

Circuit schematics of simulated 500-MHz microstrip power amplifier.

4.7 Examples of practical implementation

The inverse Class-F concept can be successfully used in the design of low-voltage monolithic CMOS power amplifiers for wireless applications where lower current consumption is preferable because of on-chip inductors having low-quality factors. Fig. 4.29 shows the inverse Class-F CMOS power amplifier with second-harmonic peaking implemented in a 0.6-μm CMOS technology.[33] The MOSFET device was characterized by a gate length of 0.6 μm and a gate width of 1200 μm. The load network consists of a shunt on-chip capacitor C_1, a series bondwire inductor L_0, and a shunt off-ship chip

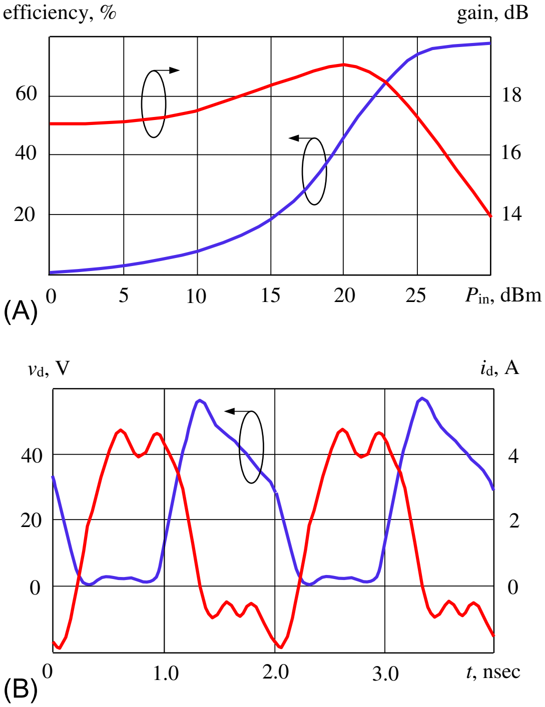


FIG. 4.27

Drain efficiency, power gain, voltage, and current waveforms.

capacitor C_2. At the second harmonic, the capacitor C_2 acts as a short circuit because of the self-resonance condition with its series parasitic inductance. At the same time, the capacitor C_1 and bond-wire inductor L_0 are tuned to the second harmonic providing a second-harmonic peaking at the device drain terminal. To stabilize the power amplifier operation, the feedback resistance R_2 is connected between the drain and the gate. The transistor was biased at half the maximum expected drain current. As a result, a small-signal power gain of 10.5 dB, a saturated output power of 22.8 dBm, and a maximum power-added efficiency (*PAE*) of 42% were achieved at an operating frequency of 1.9 GHz with a supply voltage of 3 V.

However, the level of the third-order intermodulation component IM_3 at high output powers is sufficiently high (approximately -20 dBc at $P_{out} = 18$ dBm) that this amplifier could not be directly used in an application that requires linear response to a varying envelope signal. The theoretical analysis and measurements of the intermodulation distortions for Class-AB operation show that, for the small-signal conditions, IM_3 follows a well-known 3 dB per dB slope. As a result of the different contribution of the device transfer function components, there are two sweet spots where IM_3 is minimal.[34] The first sweet spot appears because of the turn-on knee region contribution, whereas the second sweet spot close to the output-power compression point is because of the combined effect of the quadratic-to-linear and compression transitions of the device transfer function.

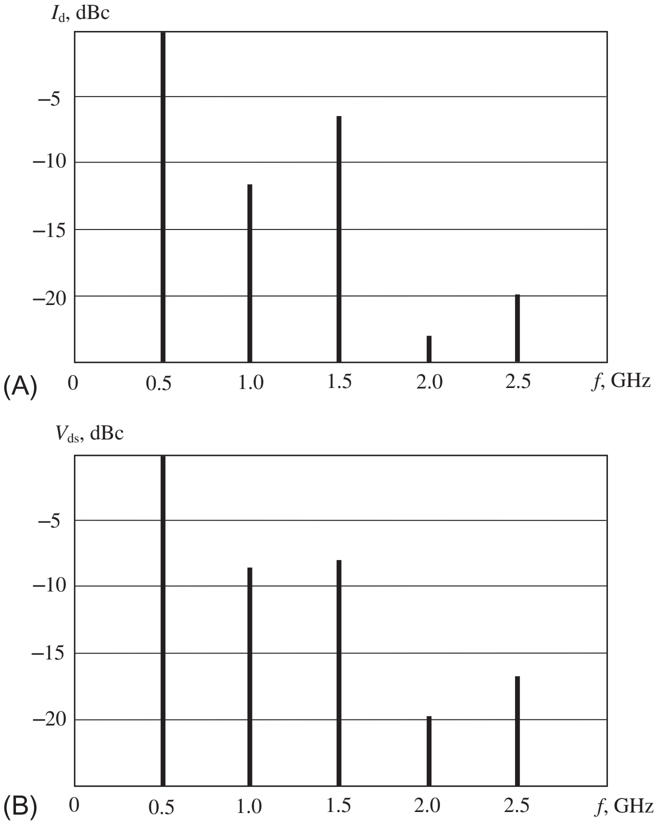


FIG. 4.28

Drain current and voltage waveform spectra.

Fig. 4.30 shows the inverse Class-F pulsed bipolar power amplifier operated at 425 MHz with a peak output power of 50 W.[20] The transmission lines in the load network serve two purposes, one is to match the low impedance of the device collector to the standard 50-Ω output and the other is to present the second-harmonic peaking required to produce the desired waveforms at the device collector for inverse Class-F operation. The electrical length θ of the first series microstrip line is calculated from Eq. (4.37) based on the value of the output device series inductance L_{out}. The first open-circuit microstrip stub having zero impedance at the second harmonic is necessary to provide high impedance seen by the device internal multiharmonic current source at the second harmonic. The second open-circuit microstrip stub is necessary to maximize the suppression of the even harmonic components. Both open-circuit stubs operate as capacitors at the fundamental frequency realizing a two-section low-pass output matching circuit. The inductor-resistor parallel circuit contains a ferrite core wire-wound inductor and 15-Ω resistor to provide a supply path while presenting an open circuit to the RF power. The right-hand capacitor on the supply branch is a 1500-μF charge storage capacitor to preserve the squareness of the current pulse at the collector by preventing pulse slum and poor rise time.

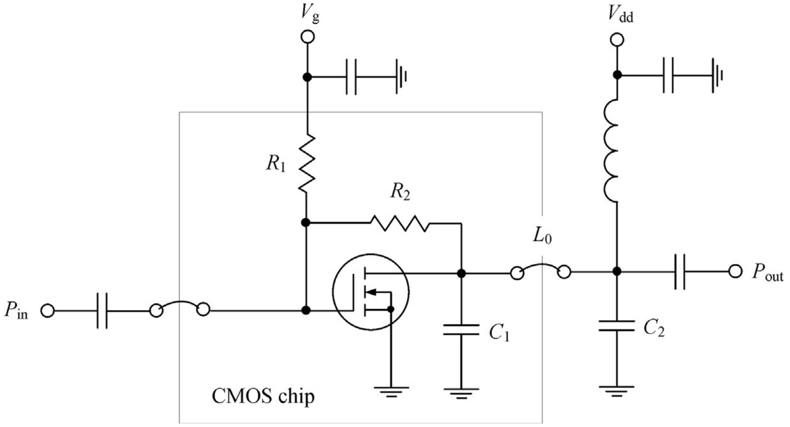

V_g
V_{dd}
R_1
R_2
L_0
P_{in}
P_{out}
C_1
C_2
CMOS chip

FIG. 4.29

CMOS inverse Class-F power amplifier schematic.

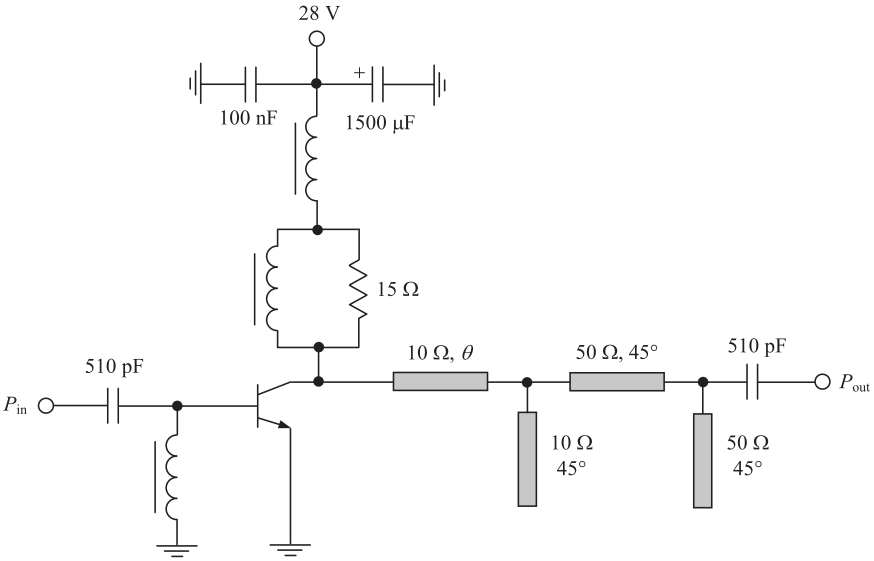

28 V
100 nF
1500 μF
+
15 Ω
510 pF
P_{in}
10 Ω, θ
50 Ω, 45°
510 pF
P_{out}
10 Ω
45°
50 Ω
45°

FIG. 4.30

Circuit schematic of a bipolar high-power amplifier.

The left-hand capacitor is a 100-nF parallel-plate bypass capacitor to bring RF ground to that node to prevent any RF power from entering the power supply.

In modern communication systems operating in frequency ranges from 225 MHz to 2.5 GHz, the silicon LDMOSFET devices are widely used in high-power transmitters due to their efficient and linear operation, simple bias-circuit realization, and cost-per-watt performance. Fig. 4.31 shows the schematic of a 1-GHz LDMOSFET power amplifier using lumped resonators.[35] Such an inverse Class-F schematic provides high impedance at the second harmonic of the fundamental frequency, low impedance at the third harmonic, and conjugate matching of the output equivalent device impedance at the fundamental frequency to a standard 50-Ω load. By using an LDMOSFET device with a gate length of 0.8 μm and a total gate width of 31.9 mm, a maximum drain efficiency of 77.8% with an output power of 12.4 W were achieved at a supply voltage of 28 V.

Fig. 4.32 shows the schematic of a 1.78-GHz LDMOSFET power amplifier using the same device which is based on a quarter-wave transmission line topology.[35] At the fundamental frequency, a quarter-wavelength transmission line operates as an impedance transformer followed by a series L_0C_0 filter tuned to the fundamental frequency and an L-type output matching circuit required to provide conjugate matching and additional harmonic suppression. For the second and higher-order harmonic components, the series filter presents an open circuit at the output of a quarter-wave transmission line. Hence an open circuit is presented at the device output for any even harmonic, and a short circuit is presented for any odd harmonic of the fundamental frequency due to the equidistant frequency properties of the input impedance of a loaded quarter-wave transmission line. The proper phasing of the second harmonic can be easily realized in practice when the active device is driven into a saturation mode. As a result, a drain efficiency of 60% with an output power of 13 W and a power gain of 10 dB were achieved at a supply voltage of 26 V.

To reduce the drain voltage and current overlapping resulting in an improved efficiency, a technique providing the gate driving with a quasi-half-sine-wave voltage by using a second-harmonic injection can be applied to a Class-F power amplifier. Fig. 4.33 shows the circuit schematic of a two-stage 2-GHz GaN HEMT power amplifier with an output power of 15 W, a power gain of 28 dB, and a *PAE* of 70%.[36] The driver stage is designed to operate in inverse Class-F mode and feeds the power stage with both fundamental and second-harmonic components having an optimized ratio of their amplitudes,

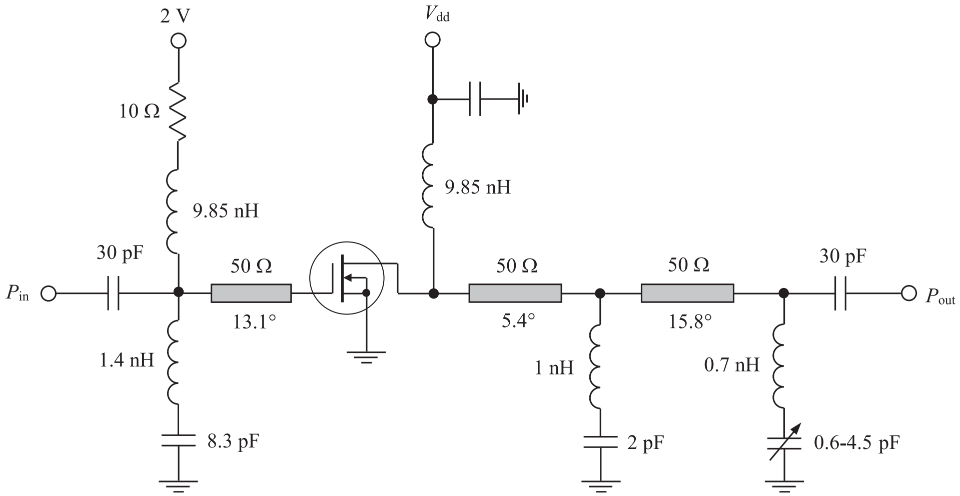


FIG. 4.31

Circuit schematic of a 1-GHz power amplifier with second-harmonic resonator.

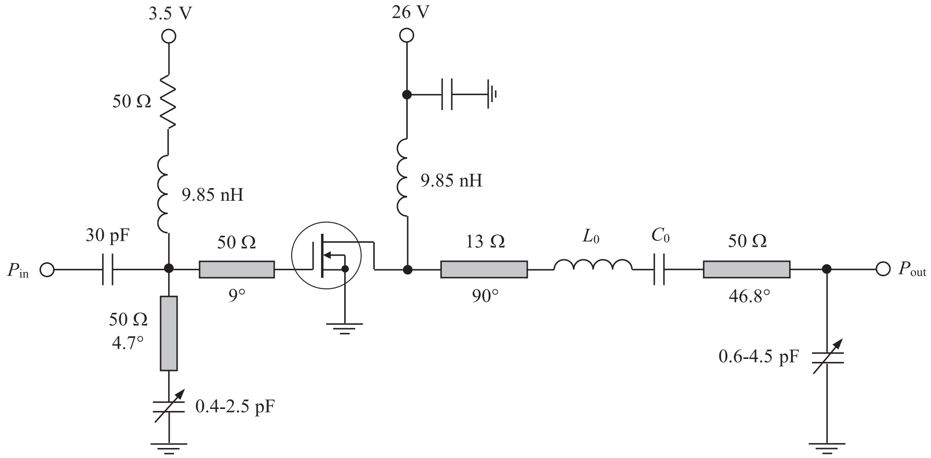

3.5 V
26 V
50 Ω
9.85 nH
9.85 nH
30 pF
P_{in}
50 Ω
9°
13 Ω
90°
L_0
C_0
50 Ω
46.8°
P_{out}
50 Ω
4.7°
0.4-2.5 pF
0.6-4.5 pF

FIG. 4.32

Circuit schematic of a 1.78-GHz power amplifier with quarter-wave transmission line.

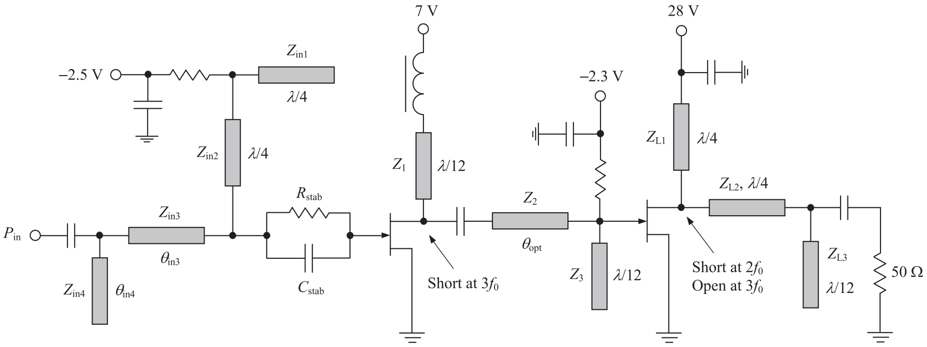

7 V
28 V
−2.5 V
Z_{in1}
λ/4
Z_{in2}
λ/4
−2.3 V
Z_1
λ/12
Z_{L1}
λ/4
Z_{L2}, λ/4
R_{stab}
Z_2
Z_{in3}
P_{in}
θ_{in3}
θ_{opt}
C_{stab}
Short at $3f_0$
Z_3
λ/12
Short at $2f_0$
Open at $3f_0$
Z_{L3}
λ/12
50 Ω
Z_{in4}
θ_{in4}

FIG. 4.33

Circuit schematic of high-efficiency two-stage transmission-line power amplifier.

equal to approximately 7:1, and zero phase shift between them. In this case, the driver transistor operating in inverse Class-F mode sees high impedance at the second harmonic and short impedance at the third harmonic due to the shunt $\lambda/12$ open-circuit stub and series microstrip line with optimum electrical length θ_{opt} connected to its drain port, thus providing a proper half-sine wave that directly feeds the gate port of the power stage. At the same time, low impedance at the second harmonic, due to the shunt $\lambda/4$ short-circuit stub, and high impedance at the third harmonic, due to the series $\lambda/4$ microstrip line and shunt $\lambda/12$ open-circuit stub, are provided at the drain port of the power transistor operating in a Class-F mode. The load network is synthesized to achieve impedance transformation at the fundamental frequency by optimizing the characteristic impedances Z_{L2} and Z_{L3}. A parallel RC network (R_{stab} and C_{stab}) is added in series at the input of the driver stage to ensure stability. It was observed that the active gate-source voltage-shaping technique offers significant improvement of PAE versus frequency that resulted in a *PAE* higher than 60% over a 400-MHz bandwidth around 2-GHz center bandwidth frequency at about 4-dB gain compression point.

Fig. 4.34A shows the circuit schematic of a monolithic single-stage 0.13-μm SiGe BiCMOS inverse Class-F with a harmonic load network using a quarterwave transmission line.[37] In this case, at the

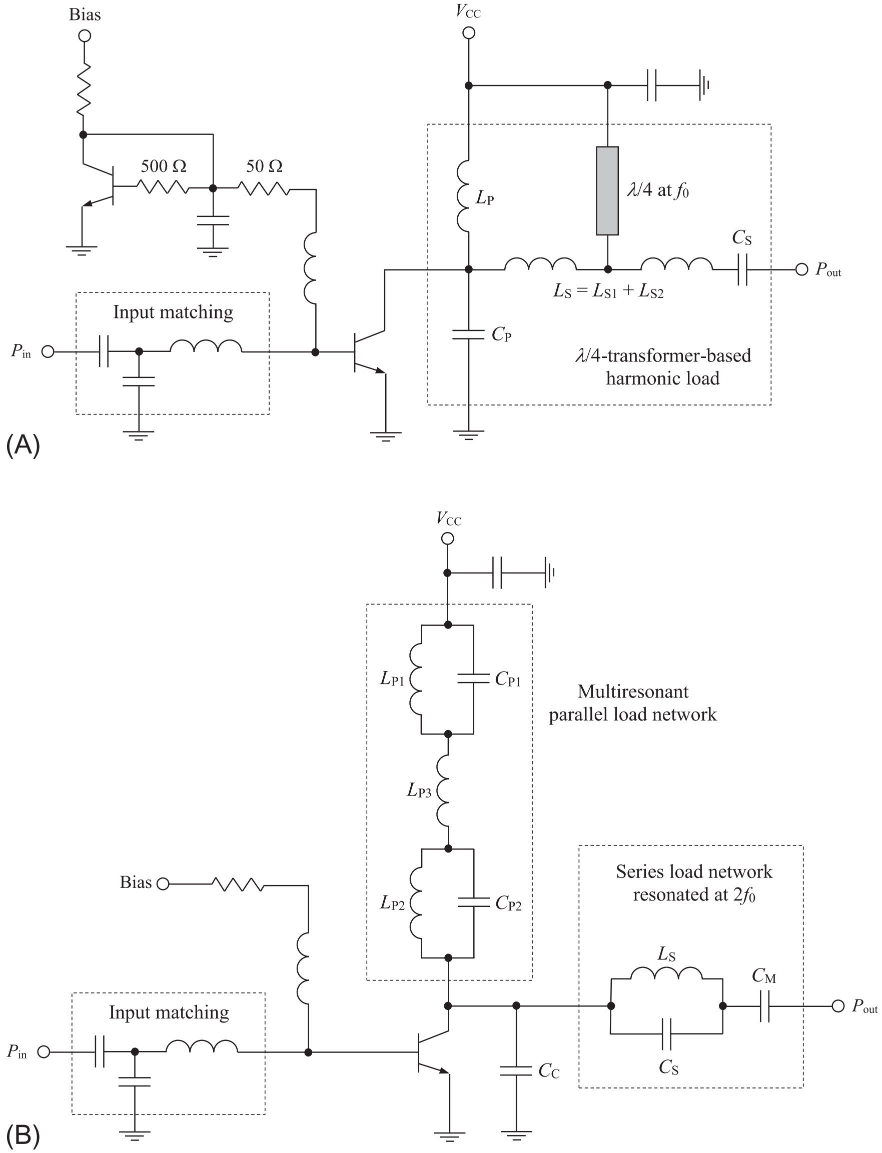

Bias
V_{CC}
500 Ω
50 Ω
L_P
λ/4 at f_0
C_S
P_{out}
$L_S = L_{S1} + L_{S2}$
Input matching
C_P
P_{in}
λ/4-transformer-based harmonic load
(A)
V_{CC}
L_{P1}
C_{P1}
Multiresonant parallel load network
L_{P3}
Bias
L_{P2}
C_{P2}
Series load network resonated at $2f_0$
L_S
C_M
Input matching
P_{out}
P_{in}
C_C
C_S
(B)

FIG. 4.34

Circuit schematics of (A) single-stage SiGe BiCMOS with λ/4 transmission line and (B) with multiresonance *LC* parallel load network.

f_0-band (39–42 GHz) due to an open-circuit impedance by the $\lambda/4$-line, the load network becomes a shunt L_PC_P—series L_SC_S dual f_0-resonator. However, at the $2f_0$-band (78–84 GHz), the $\lambda/4$-line becomes short, thus isolating the power amplifier from the output load and transforming the load network to a parallel $2f_0$-resonator composed of inductors L_P and L_{S1} and capacitor C_P, connecting in parallel. The $3f_0$ and higher-order harmonics (>117 GHz) will be filtered out through a low capacitive impedance formed by the capacitor C_P in parallel with the parasitic resistance R_x, which is contributed by the finite quality factor of the inductors and device output resistance. The capacitor C_P is composed of the transistor intrinsic capacitances and layout interconnect parasitic capacitance of about 70–80 fF. As a result, at a supply voltage of 2.4 V, the saturation output power of 18 dBm with a power gain of 6 dB and a *PAE* greater than 43% (including driver stage) was achieved at 40.5 GHz.

The fully lumped alternative of a 0.13-μm SiGe BiCMOS inverse Class-F with a harmonic load network which includes a multiresonance parallel load network is shown in Fig. 4.34B.[38, 39] In this case, the resonance frequency (50 GHz) of the parallel circuit $L_{P1}C_{P1}$ is set in between the fundamental frequency f_0 and its second harmonic $2f_0$, while the parallel circuit $L_{P2}C_{P2}$ resonates at 90 GHz in between the second and third ($3f_0$) harmonics. Therefore both resonators become inductive at f_0, which together with an inductance L_{P3} resonates out the shunt capacitance C_{C2} and makes an impedance peak at f_0. However, when approaching $2f_0$, the $L_{P1}C_{P1}$ resonator becomes capacitive, which provides four times smaller inductance at f_0 for multiresonance parallel load network, which resonates out the capacitance C_{C2} and makes impedance peak at $2f_0$. At the frequencies higher than 90 GHz, the $L_{P2}C_{P2}$ resonator becomes also capacitive, forming a series resonator that creates an impedance null at $3f_0$. The inductor L_S of 70 pH and capacitor C_S of 65 fF in the series load network provide an impedance peaking at $2f_0$, and the capacitor C_M of 120 fF cancels an inductive impedance provided by the L_SC_S resonator directly connecting the 50-Ω load to the device output at f_0. Therefore the overall load network, including both multiresonance parallel and series networks, provides composite load impedance, which is an optimum of 50 Ω at f_0, high impedance of greater than 150 Ω at $2f_0$, and low impedance of smaller than 10 Ω at $3f_0$, contributing to the corresponding collectors voltage and current waveforms corresponding to the inverse Class-F. As a result, at a supply voltage of 2.5 V, a peak *PAE* of 38.5% (including driver stage) with an output power of 15.5 dBm at 38 GHz was achieved while maintaining higher than 35% across the frequency bandwidth of 35–39 GHz.

For differential monolithic amplifier circuits at high microwave frequencies, the simultaneous fundamental matching and second/third-harmonic tuning can be achieved by using a harmonic-tuned output transformer with an embedded capacitor at its center tap, which enables an inverse Class-F operation.[40] In this case, an impedance seen at the device output at $2f_0$ is close to open circuit because of the resonant circuit formed by the even-mode primary and secondary winding inductances and the parasitic shunt capacitance at transformer input. At the same time, the third-harmonic tuning is realized because of the self-resonant frequency nature of the transformer. As a result, for a differential inverse Class-F cascode 0.13-μm SiGe BiCMOS power amplifier, a peak *PAE* of 51.1% with an output power of 25.8 dBm was achieved at 10 GHz when operated at a supply voltage of 3.0 V.

The design of RF power amplifier modules intended for use in cellular handsets is severely challenged by the continuing size and cost reduction goals. When the module size is reduced, the power amplifier efficiency is degraded due to the use of smaller passive components with a lower quality factor and closer proximity between components. Therefore it is so important that the final stage of the multistage power amplifier would operate in a high-efficiency mode. Fig. 4.35A shows the simplified circuit schematic of a three-stage GaAs HBT, where the final stage is operated in an inverse

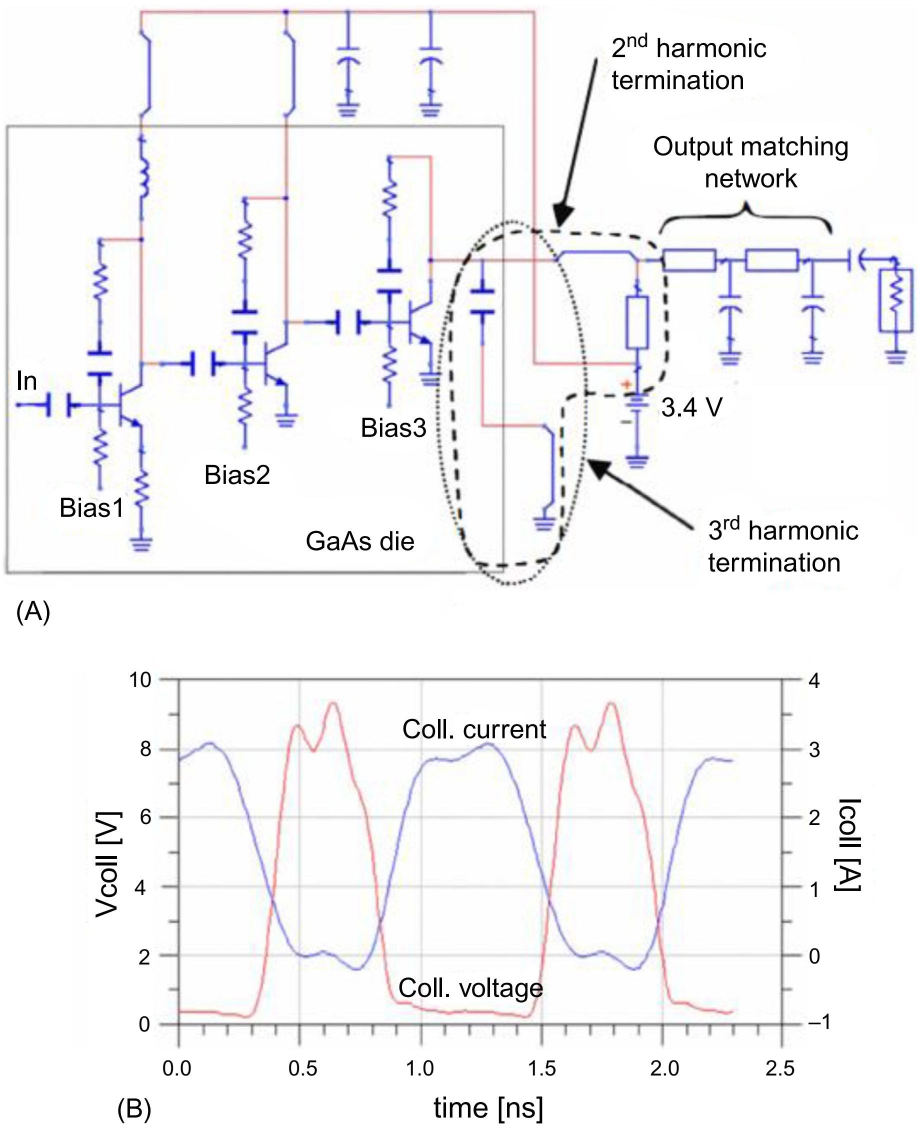

2nd harmonic termination
Output matching network
In
Bias1
Bias2
Bias3
GaAs die
3.4 V
3rd harmonic termination
(A)
Coll. current
Coll. voltage
Vcoll [V]
Icoll [A]
time [ns]
0.0
0.5
1.0
1.5
2.0
2.5
0
2
4
6
8
10
−1
0
1
2
3
4
(B)

FIG. 4.35

Circuit schematic and performance of a GaAs HBT three-stage power amplifier.[41]

Class-F mode with second- and third-harmonic controls.[41] Here, a two-section output matching network provides the load-line impedance of about $2.2 + j1.1\,\Omega$ at the fundamental to obtain a flat output power from 824 to 915 MHz. The third-harmonic termination is achieved by the series resonant circuit consisting of an on-die capacitor and a bondwire tuned to resonate at the third harmonic. At the same time, the reactance of these two elements, the collector bondwires and microstrip line in the drain

DC-supply circuit, provide the second-harmonic high-impedance termination. Fig. 4.35B shows the collector current and voltage waveforms, approximating an inverse Class-F operation mode with close to rectangular current waveform. As a result, the output power of 35 dBm with a flatness of ±0.125 dBm and a *PAE* of about 60% across the 824–915 MHz band were achieved, occupying an area of 12 mm^2.

For a high-power inverse Class-F GaN HEMT power amplifier, a simple parasitic compensation can be used when an external inductor with a decoupling capacitor is connected in parallel to the device output, thus providing close to open circuit second-harmonic impedance seen from the drain of the intrinsic device, in combination with the device shunt drain-source capacitance and series bondwire inductance.[42] At the same time, the load network consisting of a series microstrip line is used to adjust the load impedance followed by the shunt open-circuit stub having a length of $\lambda/8$ at the fundamental frequency for the second-harmonic short. The characteristic impedances of the series and shunt microstrip lines implemented in a high-dielectric substrate are chosen to provide the optimum impedance at the fundamental frequency. The power amplifier exhibited an output power of 95 W, a *PAE* of 72.2%, and a high linear gain of 19.8 dB at 2.6 GHz under 100-μs pulsed conditions at a supply voltage of 40 V.

Fig. 4.36A shows the basic circuit topology of a high-power inverse Class-F GaN HEMT power amplifier for *L*-band GPS (global positioning system) applications where the input and output matching networks are implemented by using the microstrip lines of different electrical lengths and characteristic impedances.[43] In this case, the series microstrip lines TL_2, TL_4, and TL_6 are mainly used to match the required device output impedance at the fundamental frequency f_0 to 50-Ω load. However, the electrical lengths of these microstrip lines also impact the harmonic resonator performance at $2f_0$ and $3f_0$. All required optimum impedances corresponding to maximum efficiency for GaN HEMT CGHV14250 device at the fundamental, second, and third harmonics were obtained by load-pull simulations. The shunt open-circuit stubs TL_3 and TL_5 are employed to resonate the second and third harmonics. All matching networks are implemented using a 20-mil Rogers substrate RO4350B. The simulated performance of the power amplifier biased in Class-B achieving the saturated output power of 54.6 dBm, *PAE* of 81%, and power gain of 12 dB at 1.227 GHz is shown in Fig. 4.36B, whereas the time-domain drain current and voltage waveforms corresponding to an inverse Class-F operation mode are shown in Fig. 4.36C.

4.8 Load-pull tuning of inverse Class-F GaN HEMT power amplifier

Usually, the nonlinear transistor models do not predict accurately the transistor behavior at harmonic frequencies, at high output power levels with very low output impedance, and under heavy gain compression. Therefore load-pull tuning is a commonly used approach in conjunction with analytical methods in the design of high-power amplifiers. Traditional load-pull tuning procedure makes use of mechanical tuners to vary drain and gate impedances. The transistor performance is measured over a constellation of the fundamental-frequency impedances, whereas the harmonic impedances are allowed to vary arbitrarily. A simple, low-cost method for control and systematic variation of harmonic impedances is based on the block diagram shown in Fig. 4.37A, where the fundamental-frequency output impedance is referenced to plane P3 and harmonic-frequency impedances are referenced to plane P1.[44] This reference plane is intrinsic to the device at the output of the drain current source and is referred to as the virtual drain. The harmonic terminations must be referenced to this plane to achieve the

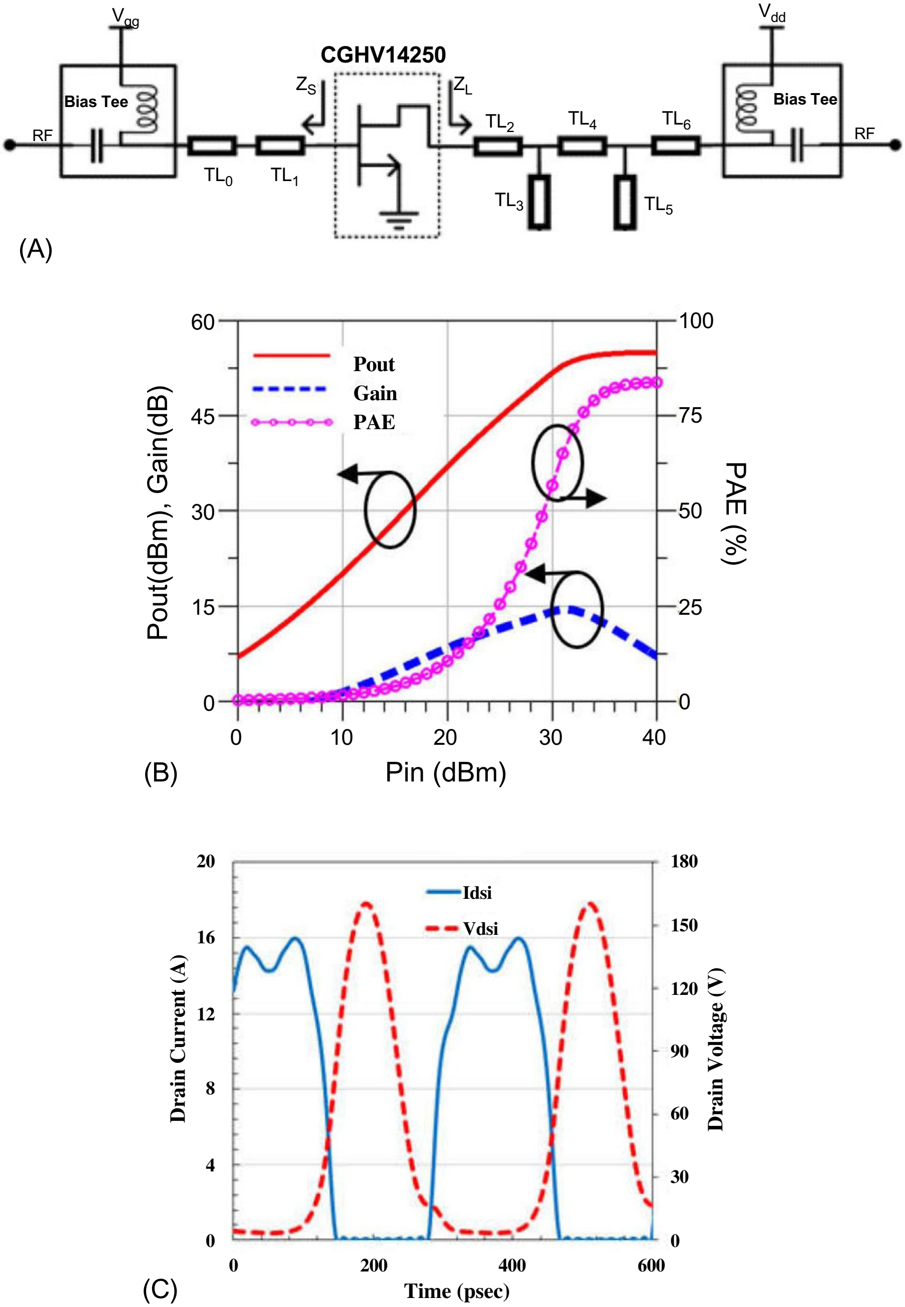


FIG. 4.36

Schematic of 1.78-GHz power amplifier with quarter-wave transmission line.[43]

high-efficiency modes. The goal is to determine what impedance must be presented by the prematch circuit at plane P3 to achieve a harmonic short or open at the virtual drain, including package parasitics and the device output capacitance C_{out}.

The harmonic prematch circuit shown in Fig. 4.37A performs the following tuning functions:

- Transforms the 50-Ω fundamental constellation to a lower impedance (in this case, 5 Ω), with the small signal gain contours for six prematch harmonic terminations used for validating load-pull calibration.
- Supplies DC bias near the device drain to avoid the large-signal oscillations.
- Constrains the second harmonic impedance to a single high-reflection coefficient for the whole fundamental-impedance constellation.
- Increases the angle of the second-harmonic termination by decreasing the length of a tuning stub, with only a small impact on the fundamental-frequency impedance transformation.

The two-port *S*-parameters of the output prematch, mechanical tuner, and output attenuators are separately measured to allow de-embedding of resistive and reflection losses at each fundamental impedance in the load-pull constellation. The input and output prematch blocks are built as break-apart fixtures, enabling *S*-parameter measurement using a microstrip TRL (Thru, Reflect, Line) calibration kit.

Two identical prematch circuits were constructed, one for *S*-parameter measurement (CKTA) and one to remain permanently wire bonded to the device (CKTB), thus eliminating parasitic variations and limiting potential for damage to the device. The second harmonic stubs in both prematch circuits are tuned identically so that *S*-parameters from CKTA can be de-embedded from the load-pull measurements using CKTB. The accuracy of this method is verified after tuning the second harmonic termination by measuring the small signal gain contours.

The 50-W GaN HEMT device TGF-2023-10 was biased at 28-V drain supply with a Class-AB bias current of 300 mA. Source pull was first performed to optimize the small signal gain, then followed by the large-signal load-pull measurements at six second-harmonic termination angles shown by different dots in Fig. 4.37B, referenced to plane P1 or virtual drain. At each impedance point, the input power was increased until gate current measured 20 mA, corresponding to an approximately consistent level of gain compression. Fig. 4.37B shows the fundamental-frequency drain efficiency contours (referenced to plane P3) that correspond to six second-harmonic terminations. The drain efficiency and maximum output power of each contour is indicated next to the corresponding harmonic termination dot. Fig. 4.37B also illustrates the required modification to the prematch circuit to achieve each harmonic termination. The highest efficiency region (77%) is achieved with the second harmonic nearest to an open circuit. In this case, the third harmonic was not explicitly controlled but was fixed at a capacitive impedance. Another output prematch circuit was designed to terminate the second and third harmonics in an open and a short circuit at plane P1, respectively (the inverse Class-F mode). Intentional termination of the third harmonic increases the transistor drain efficiency by 8% without reducing output power.

A prototype inverse Class-F power amplifier designed using the corresponding measured load-pull tuning results is shown in Fig. 4.37C. The fundamental load impedance of $(10.2 + j6.20)\ \Omega$ was presented at plane P3 with 0.27-dB insertion loss in the output matching circuit. In this case, the second-harmonic and third-harmonic impedances approximate an open and a short circuit at plane P1,

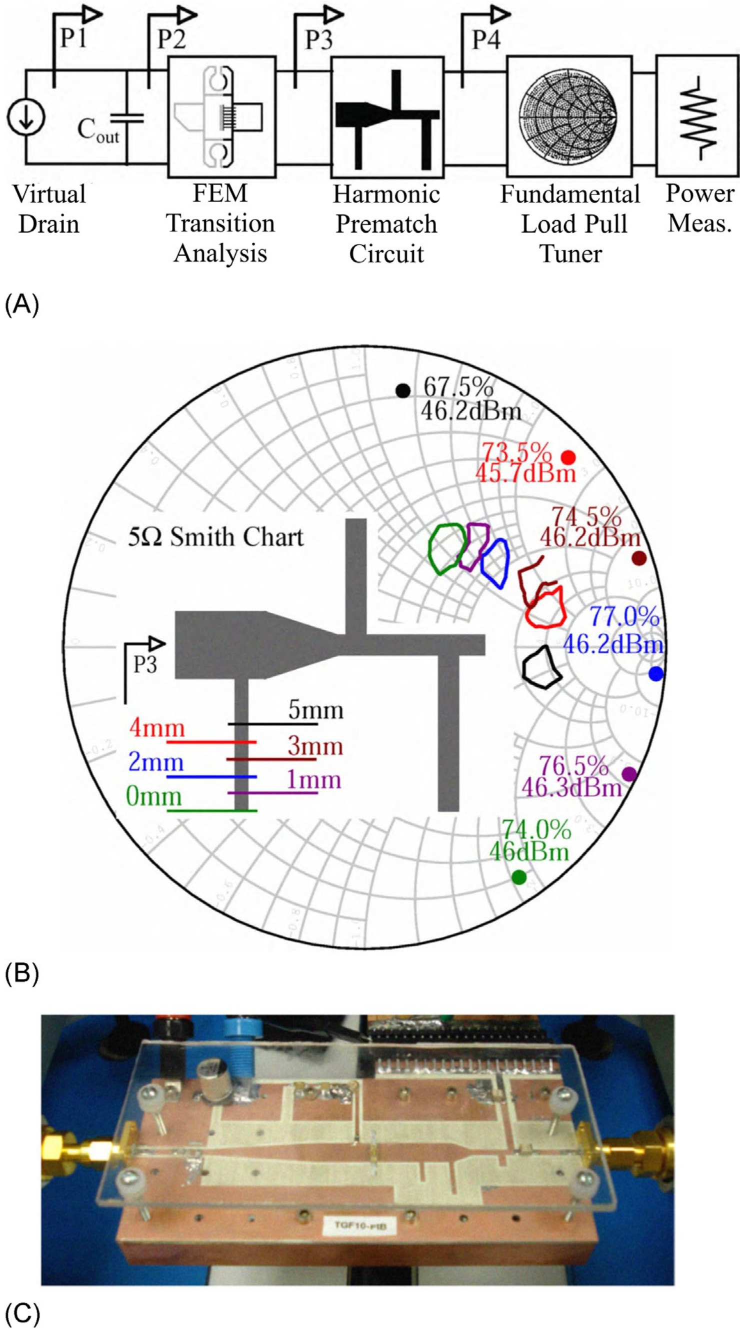

P1
P2
P3
P4
C$_{out}$
Virtual Drain
FEM Transition Analysis
Harmonic Prematch Circuit
Fundamental Load Pull Tuner
Power Meas.
(A)
67.5%
46.2dBm
73.5%
45.7dBm
74.5%
46.2dBm
5Ω Smith Chart
77.0%
46.2dBm
P3
5mm
4mm
3mm
2mm
1mm
0mm
76.5%
46.3dBm
74.0%
46dBm
(B)
TGF10-#1B
(C)

FIG. 4.37

(A) Block diagram of an output load-pull system, (B) drain efficiency contours, and (C) a fabricated inverse Class-F power amplifier.[44]

respectively. The output power of 36 W was measured with a power gain of 14.5 dB, a drain efficiency of 81%, and a *PAE* of 78% at 2.14 GHz, which are consistent with load-pull characterization results.[44]

4.9 Inverse Class-F GaN HEMT power amplifiers for cellular systems

In modern wireless communication systems, it is required that the power amplifier could operate with a high efficiency, high linearity, and low-harmonic output level simultaneously. To increase the efficiency of the power amplifier, it is possible to apply a switchmode inverse Class-F mode technique that can ideally provide a drain efficiency of 100% with rectangular drive. This kind of a power amplifier requires an operation in deep saturation mode, resulting in a poor linearity and therefore is not suitable to directly replace linear power amplifiers in modern and future generation WCDMA/LTE transmitters with nonconstant envelope signal in 4G/5G telecommunication systems for small-cell multiple-input multiple-output (MIMO) or high-power base station applications. However, to obtain both high efficiency and good linearity, such kind of a nonlinear high-efficiency power amplifier operating in an inverse Class-F mode can be used in advanced transmitter architectures such as Doherty, LINC (linear amplification using nonlinear components), or EER (envelope elimination and restoration) with digital predistortion.[26, 45]

In a power amplifier using the packaged device at high frequencies or having high output power, the presence of a transistor output series bondwire and lead inductance L_{out} creates some problems in providing an acceptable second- or third-harmonic open- or short-circuit termination. In this case, it is convenient to use a series transmission line as a first element of the load network connected to the device output, as shown in Fig. 4.38A, where the transmission line TL_1 is placed between the device drain and shunt short-circuited quarter-wavelength transmission line TL_3. However, if the length of combined series transmission line $TL_1 + TL_2$ becomes very long in Class-F mode with a short circuit at the second harmonic and an open circuit at the third harmonic and an additional fundamental-frequency matching circuit is required, then such a load network in inverse Class-F mode is compact, convenient for harmonic tuning, and very practical. Fig. 4.38B shows the equivalent circuit of a transmission-line inverse Class-F load network, where the complex conjugate load matching is provided at the fundamental, and both high reactance at the second harmonic and low reactance at the third harmonic are created at the device output by using two series transmission lines TL_1 and TL_2, the electrical lengths of which depend on the values of the device output shunt capacitance C_{out} and series inductance L_{out}, a quarter-wavelength short-circuit stub TL_3, and an open-circuit stub TL_4 with electrical length of 30 degrees.[23, 46] The output shunt capacitance C_{out} can represent both intrinsic bias-dependent drain-source capacitance C_{ds} and extrinsic bias-independent drain pad-contact capacitance C_{dp} of the nonlinear large-signal equivalent circuit for GaN HEMT device, whereas the series output inductance L_{out} model combined the effects of metallization, bond wire, and package inductances.[47]

The harmonic conditions for an inverse Class-F load network seen by the device multiharmonic current source derived from Eqs. (4.14)–(4.16) for the first three harmonic components, including fundamental, are

$$\text{Re}Z_{net}(\omega_0) = R, \tag{4.41}$$

$$\text{Im}Z_{net}(2\omega_0) = \infty, \tag{4.42}$$

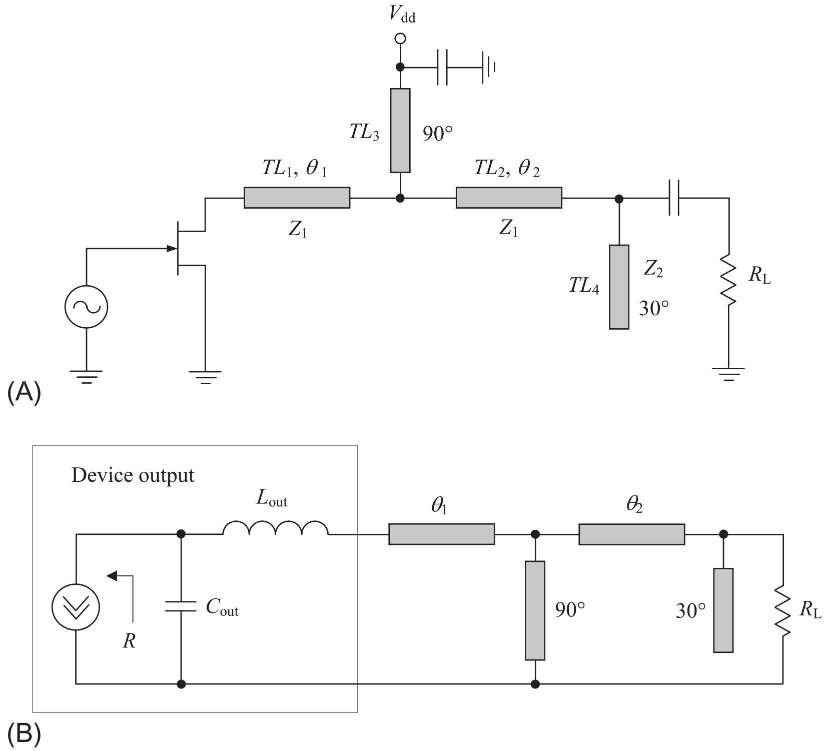


FIG. 4.38

Transmission-line inverse Class-F power amplifier and its equivalent circuit.

$$\mathrm{Im}Z_{\mathrm{net}}(\omega_0) = \mathrm{Im}Z_{\mathrm{net}}(3\omega_0) = 0, \tag{4.43}$$

where the load resistance (or equivalent output resistance) R seen by the device output at the fundamental frequency can be written in inverse Class-F mode as

$$R = \frac{\pi^2}{4} R^{(B)} = \frac{\pi^2}{8} \frac{(V_{dd} - V_{sat})^2}{P_{out}}, \tag{4.44}$$

where $R^{(B)} = (V_{dd} - V_{sat})^2/2P_{out}$ is the equivalent output resistance obtained in Class-B bias mode, V_{dd} is the DC supply voltage, V_{sat} is the saturation voltage, and P_{out} is the fundamental output power.

Fig. 4.39A shows the transmission-line load network seen by the device multiharmonic current source at the fundamental frequency, where the combined series transmission line $TL_1 + TL_2$ (together with an open-circuit capacitive stub TL_4 with electrical length of 30 degrees) provides an impedance matching between the optimum equivalent output device resistance R and the standard load resistance R_L by proper choice of the transmission-line characteristic impedances Z_1 and Z_2, where C_{out} and L_{out} are the elements of the matching circuit. For simplicity of calculation, the characteristic impedances of the transmission lines TL_1 and TL_2 are set to be equal to Z_1.

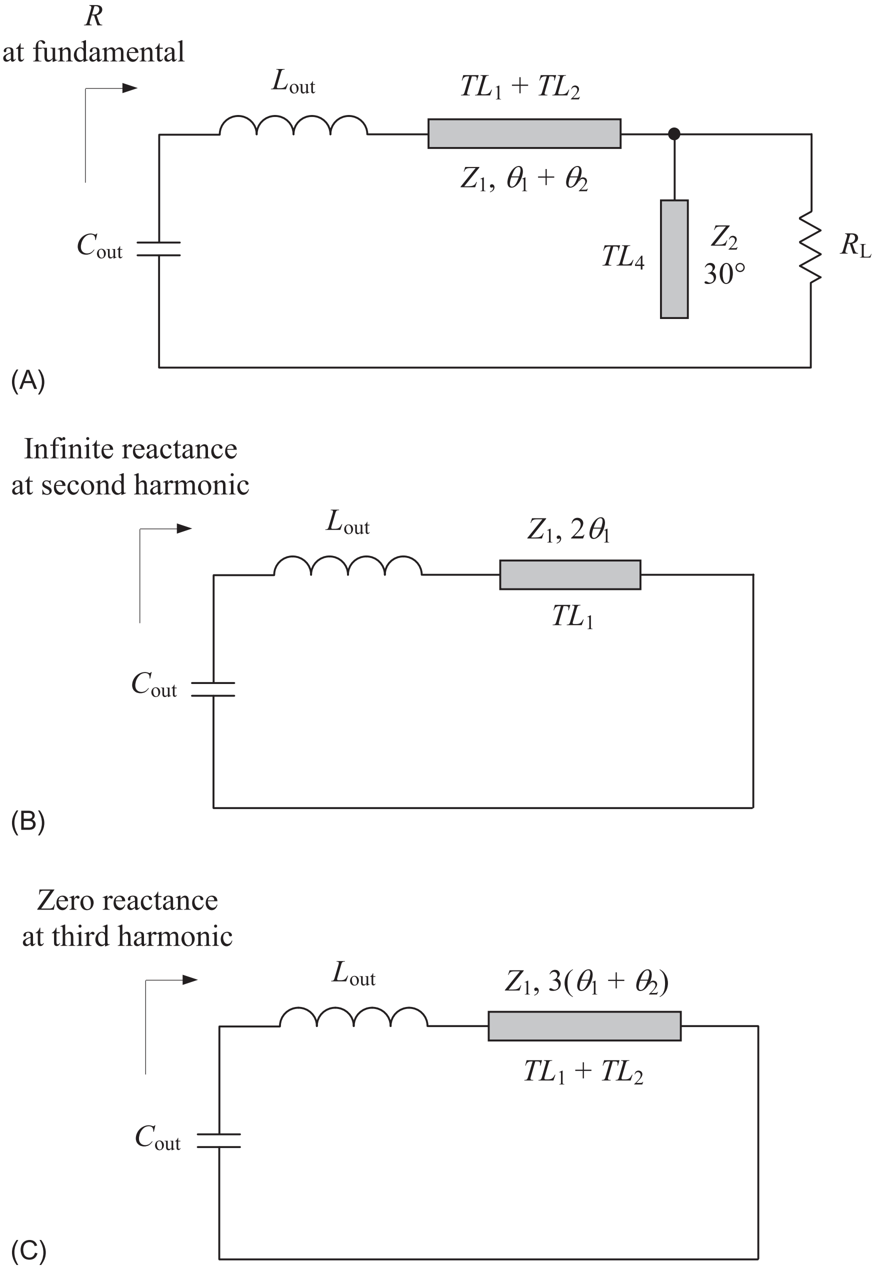

R
at fundamental
L_{out}
$TL_1 + TL_2$
$Z_1, \theta_1 + \theta_2$
C_{out}
TL_4
Z_2
30°
R_L
(A)
Infinite reactance
at second harmonic
L_{out}
$Z_1, 2\theta_1$
TL_1
C_{out}
(B)
Zero reactance
at third harmonic
L_{out}
$Z_1, 3(\theta_1 + \theta_2)$
$TL_1 + TL_2$
C_{out}
(C)

FIG. 4.39

Load networks seen by the device output at corresponding harmonics.

The load network seen by the device current source at the second harmonic (taking into account the short-circuit effect of the RF grounded quarter-wavelength transmission line TL_3) is shown in Fig. 4.39B, where the transmission line TL_1 provides an open-circuit condition for the second harmonic at the device output by forming a second-harmonic tank, together with the shunt capacitor C_{out} and series inductance L_{out}. A similar load network at the third harmonic is shown in Fig. 4.39C, where the open-circuit effect of the RF grounded quarter-wavelength transmission line TL_3 and short-circuit effect of the open-circuit stub TL_4 at the third harmonic are used. In this case, the combined transmission line $TL_1 + TL_2$ short-circuited at its right-hand side and connected in series with an inductance L_{out} provides a short-circuit condition for the third harmonic at the device output. Depending on the actual physical length of the device output electrode, the on-board adjusting of the transmission lines TL_1 and TL_2 can easily provide the required open-circuit and short-circuit conditions, as well as an impedance matching at the fundamental frequency, due to their series connection to the device output.

By using Eqs. (4.42), (4.43), the electrical lengths of the transmission lines TL_1 and TL_2, assuming the same characteristic impedance Z_1 for both series transmission-line sections, can be defined from

$$2\omega_0 C_{\text{out}} - \frac{1}{2\omega_0 L_{\text{out}} + Z_1 \tan 2\theta_1} = 0, \tag{4.45}$$

$$3\omega_0 L_{\text{out}} + Z_1 \tan 3(\theta_1 + \theta_2) = 0, \tag{4.46}$$

with the maximum total electrical length $\theta_1 + \theta_2 = \pi/3$ or 60 degrees at the fundamental frequency or 180 degrees at the third harmonic component when $L_{\text{out}} = 0$.

As a result, the electrical lengths of the transmission lines TL_1 and TL_2 as analytical functions of the device output series inductance L_{out} and shunt capacitance C_{out} are obtained as

$$\theta_1 = \frac{1}{2}\tan^{-1}\frac{1-(2\omega_0)^2 L_{\text{out}} C_{\text{out}}}{2 Z_1 \omega_0 C_{\text{out}}}, \tag{4.47}$$

$$\theta_2 = \frac{\pi}{3} - \frac{1}{3}\tan^{-1}\frac{3\omega_0 L_{\text{out}}}{Z_1} - \theta_1, \tag{4.48}$$

where the transmission-line characteristic impedance Z_1 can be set in advance.

To omit an additional matching section at the fundamental, the inverse Class-F load network can also be used to match the equivalent device fundamental-frequency impedance R with the standard load impedance R_{L} (usually equal to $50\,\Omega$). In this case, it is necessary to properly optimize both characteristic impedances Z_1 and Z_2. Fig. 4.40 shows the equivalent representation of an inverse Class-F load network (including the device output parameters L_{out} and C_{out}) by a lumped low-pass Π-type matching circuit, where $C = \tan[(30\text{ degrees})/\omega_0 Z_2)$ and $L \approx (Z_1/\omega_0)\sin(\theta_1 + \theta_2) + L_{\text{out}}$ owing to sufficiently short length of the combined transmission line $TL_1 + TL_2$, typically much less than 60 degrees at the fundamental frequency depending upon the device output parameters. As a result,

$$Z_1 \cong \frac{\omega_0 (L - L_{\text{out}})}{\sin(\theta_1 + \theta_2)}, \tag{4.49}$$

$$Z_2 = \frac{1}{\omega_0 C \sqrt{3}}. \tag{4.50}$$

For a lumped low-pass Π-type matching circuit with $R_{\text{L}} > R$ and $Q = \omega_0 C_{\text{out}} R$,

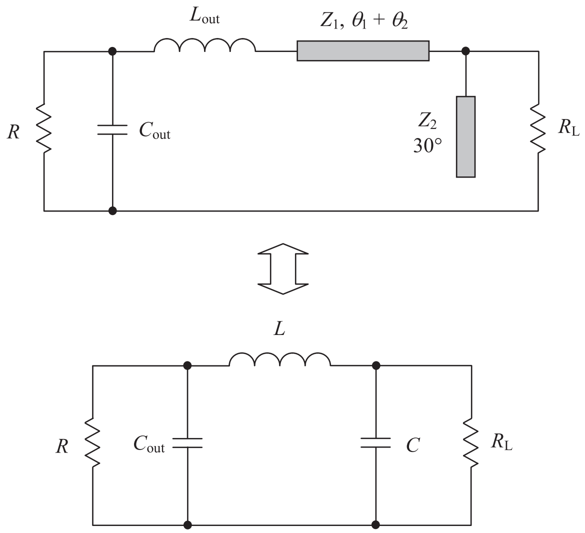


FIG. 4.40

Equivalent representations of load network at fundamental frequency.

$$Q_L = \sqrt{\frac{R_L}{R}(1+Q^2) - 1}, \tag{4.51}$$

$$C = \frac{Q_L}{\omega_0 R_L}, \tag{4.52}$$

$$L = \frac{Q + Q_L}{1 + Q_L^2} \frac{R_L}{\omega_0}, \tag{4.53}$$

where the parameters L_{out}, C_{out}, R, and R_L are fixed.[19] By subsequent calculation of the load quality factor Q_L from Eq. (4.51) and then the capacitance C from Eq. (4.52), the characteristic impedance Z_2 can be directly obtained from Eq. (4.50). After calculating the inductance L from Eq. (4.53), the remaining parameters, including the electrical lengths θ_1 and θ_2 and characteristic impedance Z_1 can be finally obtained from a system of three equations given by Eqs. (4.47)–(4.49).

For most practical cases when $\omega_0 L_{out}/Z_1 < 0.1$, from Eqs. (4.48), (4.49), it follows that the characteristic impedance Z_1 can simply be calculated from

$$Z_1 = \frac{\omega_0 (2L - L_{out})}{\sqrt{3}}. \tag{4.54}$$

Fig. 4.41A shows the simulated circuit schematic that approximates a transmission-line inverse Class-F power amplifier based on a 28-V, 10-W Cree GaN HEMT power transistor CGH40010 and transmission-line load network with the second- and third-harmonic tuning, as shown in Fig. 4.38A. The input matching circuit provides a fundamental-frequency complex-conjugate matching with the standard 50-Ω source. The load network was slightly modified by optimizing the parameters of the series transmission line for implementation convenience. In this case, the device input and

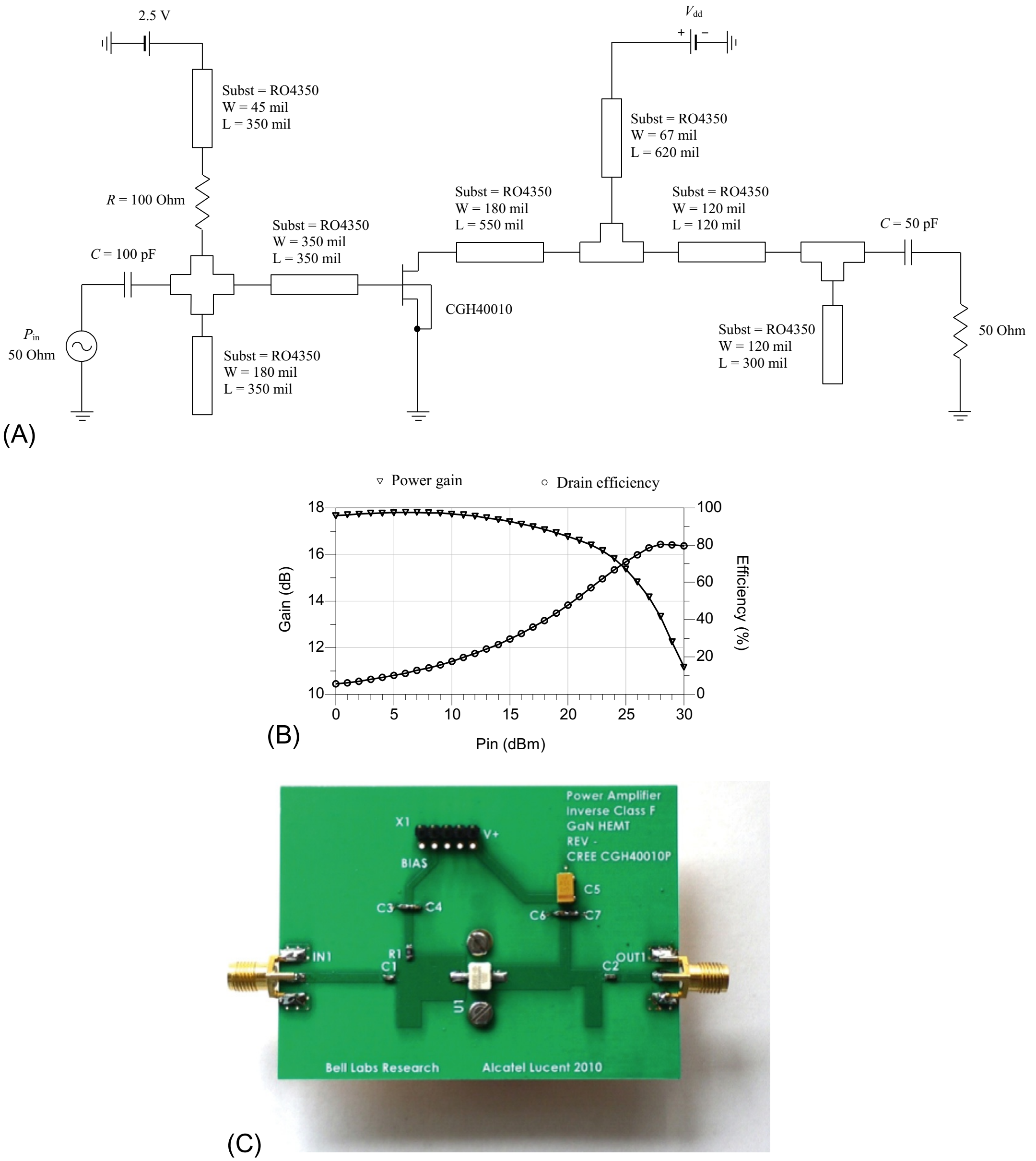

2.5 V
Subst = RO4350
W = 45 mil
L = 350 mil
R = 100 Ohm
C = 100 pF
Subst = RO4350
W = 350 mil
L = 350 mil
Pin
50 Ohm
Subst = RO4350
W = 180 mil
L = 350 mil
CGH40010
Subst = RO4350
W = 180 mil
L = 550 mil
Vdd
+ −
Subst = RO4350
W = 67 mil
L = 620 mil
Subst = RO4350
W = 120 mil
L = 120 mil
C = 50 pF
Subst = RO4350
W = 120 mil
L = 300 mil
50 Ohm
(A)
Power gain
Drain efficiency
Gain (dB)
Efficiency (%)
Pin (dBm)
18
16
14
12
10
100
80
60
40
20
0
0
5
10
15
20
25
30
(B)
Power Amplifier
Inverse Class F
GaN HEMT
REV -
CREE CGH40010P
X1
V+
BIAS
C3
C4
C5
C6
C7
IN1
R1
C1
C2
OUT1
Bell Labs Research
Alcatel Lucent 2010
(C)

FIG. 4.41

Transmission-line 10-W inverse Class-F GaN HEMT power amplifier.

output package leads as external elements were properly modeled to take into account the effect of their inductances, and their models were then added to the simulation setup.

The simulation results of a transmission-line inverse Class-F GaN HEMT power amplifier shown in Fig. 4.41B are based on a nonlinear device model supplied by Cree and technical parameters for a 30-mil RO4350 substrate. The maximum output power of 41.3 dBm, power gain of 13.3 dB (linear gain of about 18 dB), drain efficiency of 80.3%, and *PAE* of 76.5% are achieved at an operating frequency of 2.14 GHz with a supply voltage of 28 V and a quiescent current of 40 mA. The experimental results of the test board of this transmission-line inverse Class-F GaN HEMT power amplifier using a 28-V, 10-W Cree GaN HEMT power transistor CGH40010P in a metal-ceramic pill package shown in Fig. 4.41C were very close to the simulated results with a maximum output power of 41.0 dBm, a drain efficiency of 76.0%, a *PAE* of 72.2%, and a power gain of 13.0 dB at an operating frequency of 2.14 GHz (gate bias voltage $V_g = -2.8$ V and drain supply voltage $V_{dd} = 28$ V), achieved without any tuning of the input matching circuit and load network.[23]

Fig. 4.42A shows the simulated circuit schematic of a transmission-line inverse Class-F power amplifier based on a 25-W Cree GaN HEMT power transistor CGH40025F.[48, 49] The input matching circuit provides a complex conjugate matching with the standard 50-Ω source. Similarly, the load network approximates the transmission-line structure with the second- and third-harmonic control shown in Fig. 4.38A. In this case, the characteristic impedances of the shunt and series transmission lines were optimized for better performance and convenience of practical implementation. Special care was taken for modeling of the device input and output package leads to account for finite values of their inductances. Fig. 4.42B shows the simulated results of an inverse Class-F power amplifier using a 30-mil RO4350 substrate. The maximum output power of 43.4 dBm, drain efficiency of 84.6%, and *PAE* of 78.5% with a power gain of 11.4 dB (linear gain of about 17 dB) at $V_g = -2.5$ V and $V_{dd} = 28$ V were achieved at an operating frequency of 2.14 GHz. Fig. 4.42C shows the test board of a 25-W GaN HEMT power amplifier implemented in RO4350 substrate, where physical dimensions of all transmission lines correspond to the simulation setup shown in Fig. 4.42A.[49] The measured results of such an inverse Class-F GaN HEMT power amplifier with a maximum output power of 43.5 dBm, a drain efficiency of 82.1%, and a power gain of 12.2 dB at 2.14 GHz (quiescent current $I_q = 100$ mA and drain supply voltage $V_{dd} = 32$ V) were achieved without any tuning of the input matching circuit and load network.

For particular values of the parameters C_{out} and L_{out} when C_{out} is sufficiently small and L_{out} is large enough, the electrical length θ_2 can be set to zero, thus resulting in a special simplified case of the inverse Class-F load network, as shown in Fig. 4.43A. In a common case, Eqs. (4.45), (4.46) can be rewritten in a generalized form of

$$4pq + 2q\tan 2\theta_1 - 1 = 0, \tag{4.55}$$

$$3p + \tan 3\theta_1 = 0, \tag{4.56}$$

where $q = Z_1\omega_0 C_{out}$ and $p = \omega_0 L_{out}/Z_1$. Substituting Eq. (4.56) into Eq. (4.55) results in a transcendental equation to define implicitly the required electrical length θ_1 for proper q, which is written as

$$2q(2\tan 3\theta_1 - 3\tan 2\theta_1) + 3 = 0. \tag{4.57}$$

Then, the characteristic impedance Z_1 can be obtained from Eq. (4.56), which provides explicit calculation of the load network parameter p for given electrical length θ_1.

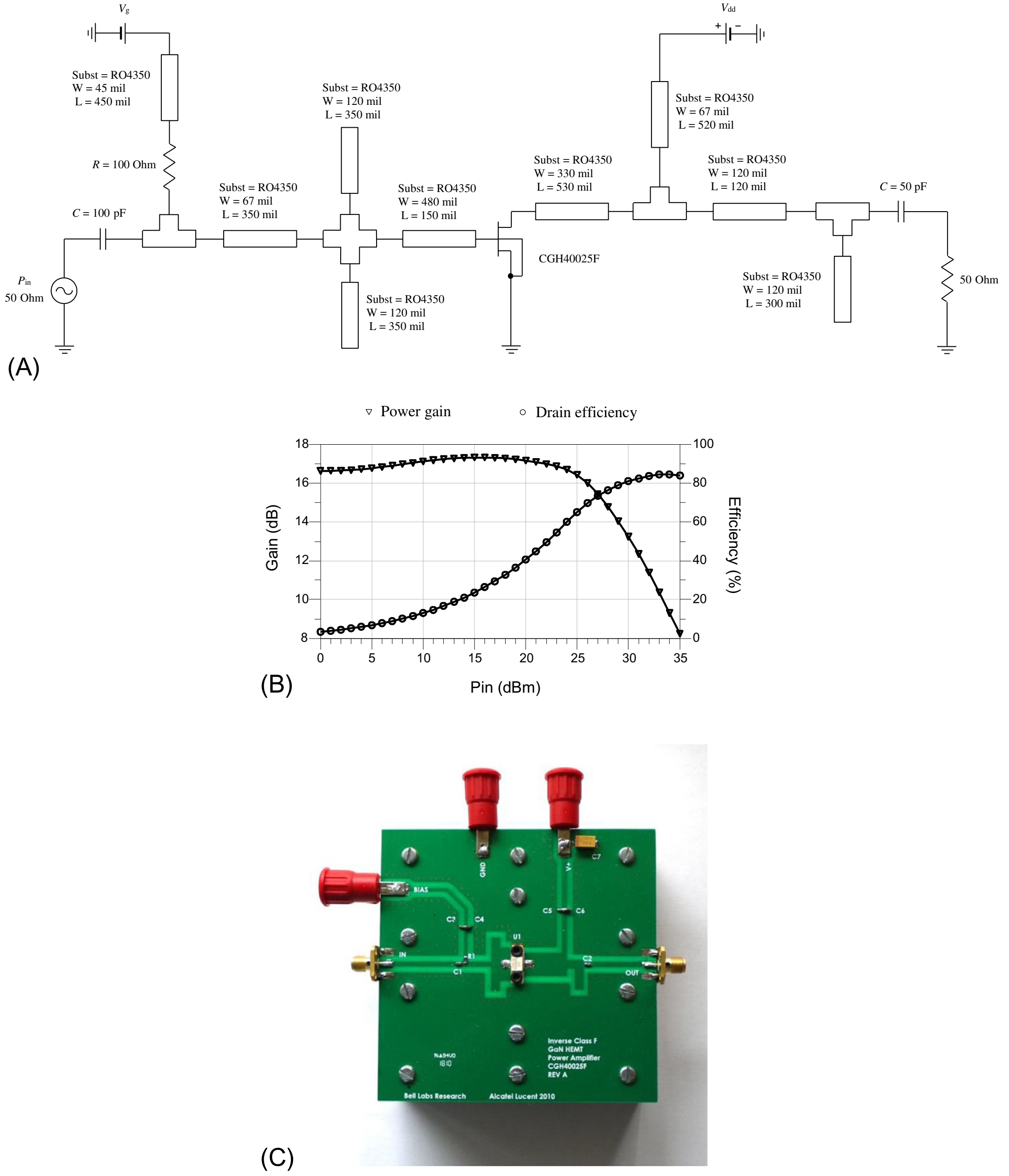

V_g
Subst = RO4350
W = 45 mil
L = 450 mil
R = 100 Ohm
C = 100 pF
P_{in}
50 Ohm
Subst = RO4350
W = 67 mil
L = 350 mil
Subst = RO4350
W = 120 mil
L = 350 mil
Subst = RO4350
W = 120 mil
L = 350 mil
Subst = RO4350
W = 480 mil
L = 150 mil
CGH40025F
Subst = RO4350
W = 330 mil
L = 530 mil
V_{dd}
Subst = RO4350
W = 67 mil
L = 520 mil
Subst = RO4350
W = 120 mil
L = 120 mil
Subst = RO4350
W = 120 mil
L = 300 mil
C = 50 pF
50 Ohm
(A)
▿ Power gain
○ Drain efficiency
Gain (dB)
Efficiency (%)
Pin (dBm)
8
10
12
14
16
18
0
20
40
60
80
100
0
5
10
15
20
25
30
35
(B)
BIAS
GND
V+
C7
C3
C4
C5
C6
U1
IN
R1
C1
C2
OUT
Inverse Class F
GaN HEMT
Power Amplifier
CGH40025F
REV A
Bell Labs Research
Alcatel Lucent 2010
(C)

FIG. 4.42

Transmission-line 25-W inverse Class-F GaN HEMT power amplifier.

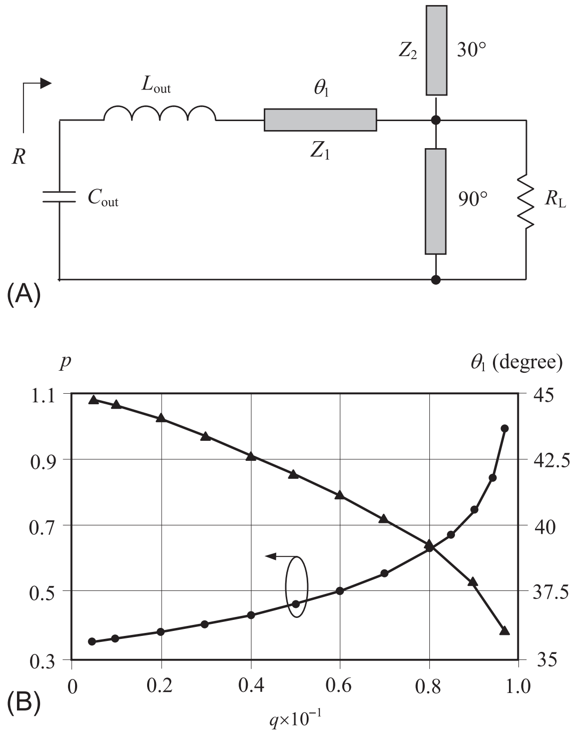


FIG. 4.43

Special case of inverse Class-F load network and its parameters.

Fig. 4.43B shows the frequency behavior of the normalized parameters p and q, which characterize a transmission-line inverse Class-F load network with a uniform series transmission line. In this case, a transmission-line network solution can be found for p varying from 0.34 to 1.02 when $q < 0.1$, resulting in values of electrical length θ_1 within 35–45 degrees. For example, for $q = 0.09$, which gives $p = 0.74$ and $\theta_1 = 38°$, as follows from Fig. 4.43B, the characteristic impedance Z_1 and series inductance L_{out} are calculated for $C_{out} = 0.3\,\text{pF}$ as $Z_1 = 22\,\Omega$ and $L_{out} = 1.2\,\text{nH}$ at an operating frequency of 2.14 GHz.

Fig. 4.44A shows the simulated circuit schematic of an inverse Class-F GaN HEMT power amplifier based on a 28-V, 5-W Nitronex RF power transistor NPTB00004 where the input matching circuit provides a complex conjugate matching with a 50-Ω source, and the load network represents the transmission-line circuit shown in Fig. 4.43A. The simulated results of an inverse Class-F power amplifier using a 30-mil RO4350 substrate are shown in Fig. 4.44B. The maximum output power of 37.1 dBm, drain efficiency of 73.1%, and *PAE* of 70.7% at an operating frequency of 2.14 GHz are achieved with a power gain of 15.1 dB (linear gain of around 20 dB) and a supply voltage of 25 V. Considering the parasitic effect of the device output lead, the length of adjacent series microstrip line can be slightly reduced. As a result of practical implementation, a drain efficiency of 74.6% and a *PAE* of

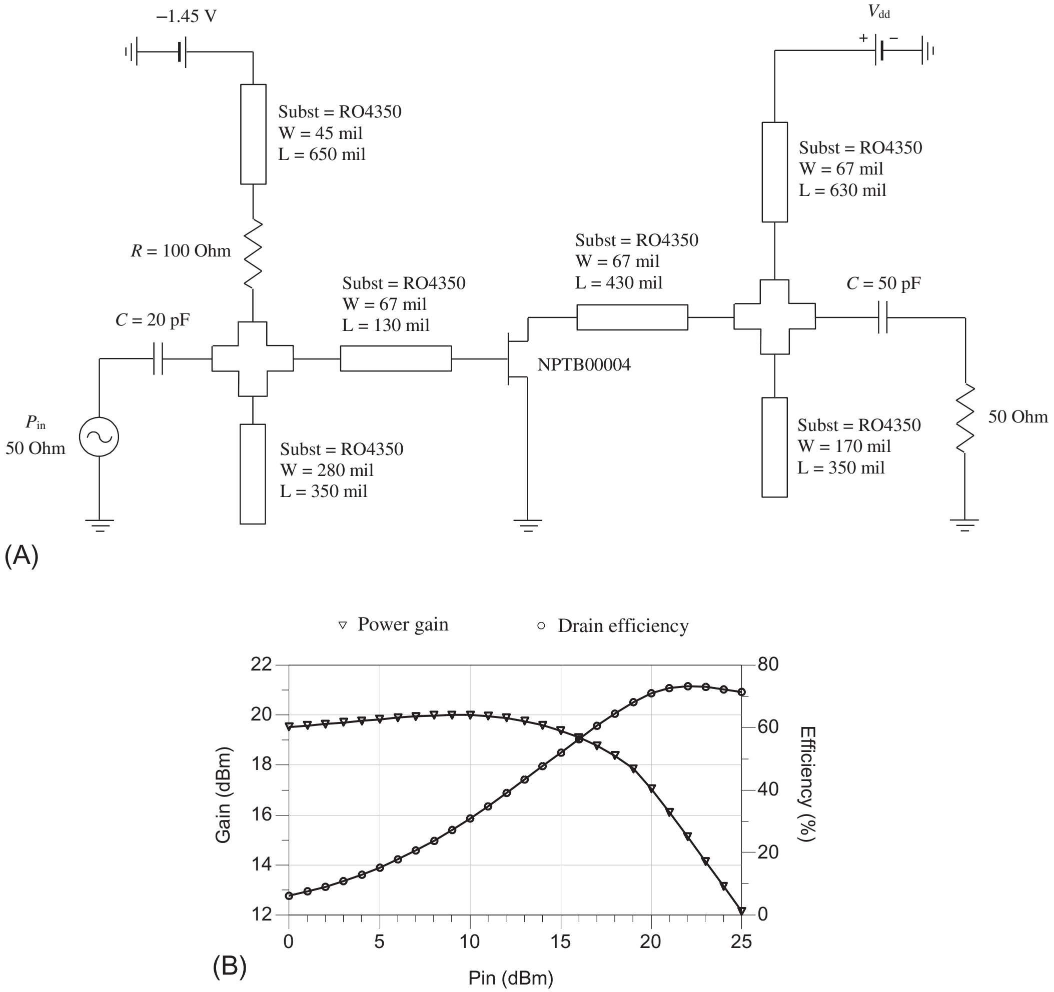

−1.45 V
Subst = RO4350
W = 45 mil
L = 650 mil
R = 100 Ohm
C = 20 pF
Subst = RO4350
W = 67 mil
L = 130 mil
Subst = RO4350
W = 67 mil
L = 430 mil
NPTB00004
Vdd
+ −
Subst = RO4350
W = 67 mil
L = 630 mil
C = 50 pF
Pin
50 Ohm
Subst = RO4350
W = 280 mil
L = 350 mil
Subst = RO4350
W = 170 mil
L = 350 mil
50 Ohm
(A)
▿ Power gain
○ Drain efficiency
Gain (dBm)
22
20
18
16
14
12
Efficiency (%)
80
60
40
20
0
0
5
10
15
20
25
Pin (dBm)
(B)

FIG. 4.44

Transmission-line 5-W inverse Class-F GaN HEMT power amplifier.

70.5% with a power gain of 12.5 dB were achieved at 2.14 GHz (gate bias voltage $V_g = -1.4\,\text{V}$, quiescent current $I_q = 20\,\text{mA}$, and drain supply voltage $V_{dd} = 25\,\text{V}$).[46] In this case, deeper saturation mode with increased input power results in lower DC supply current that contributes to increased drain efficiency (78.5% and higher) with almost constant fundamental output power. The fundamental output power is varied almost linearly from 33 dBm at $V_{dd} = 20\,\text{V}$ up to 37.5 dBm at $V_{dd} = 35\,\text{V}$, and a maximum drain efficiency of about 82% is achieved at a DC supply voltage of 32.5 V. Owing to

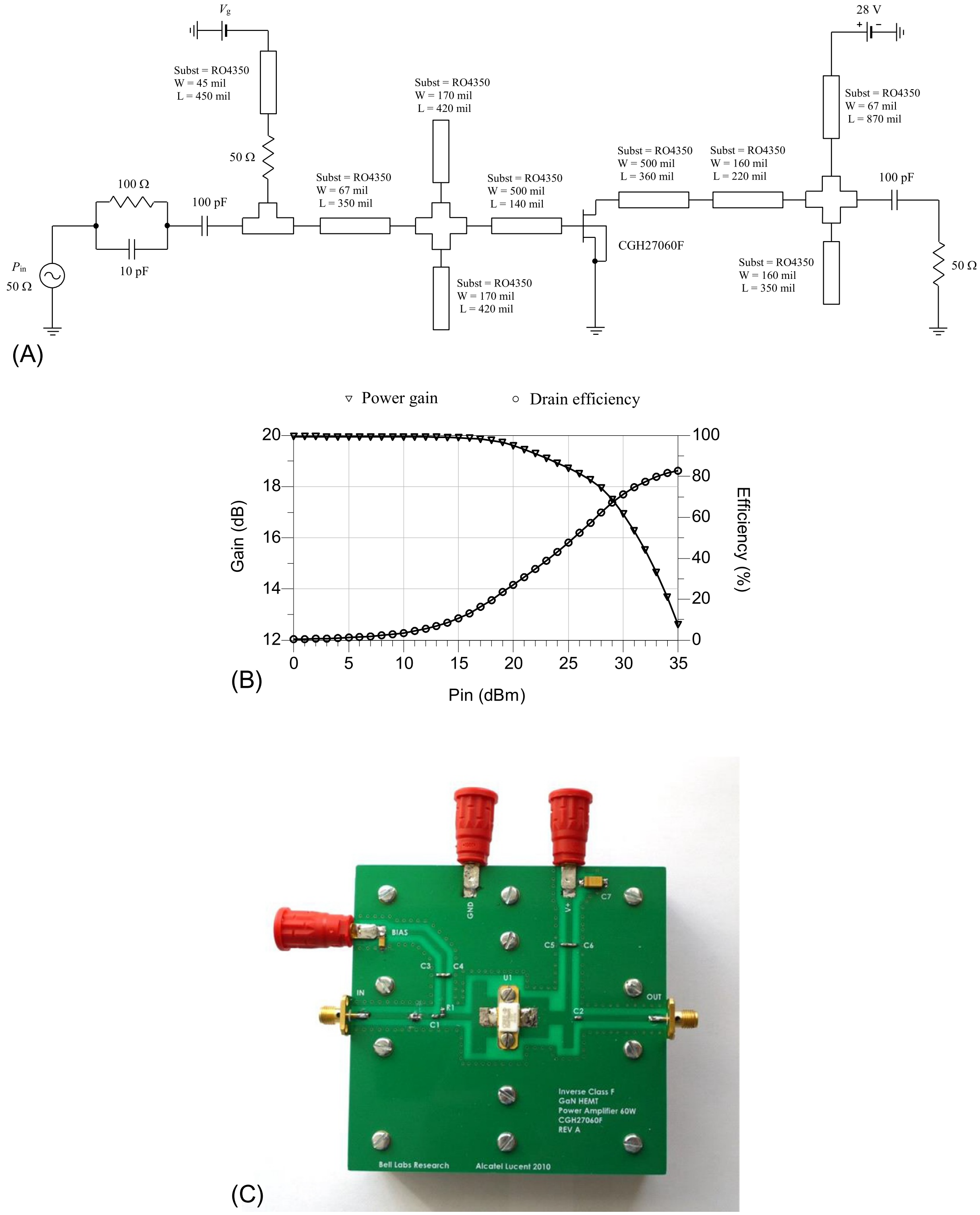

V_g
Subst = RO4350
W = 45 mil
L = 450 mil
50 Ω
100 Ω
100 pF
10 pF
P_{in}
50 Ω
Subst = RO4350
W = 67 mil
L = 350 mil
Subst = RO4350
W = 170 mil
L = 420 mil
Subst = RO4350
W = 170 mil
L = 420 mil
Subst = RO4350
W = 500 mil
L = 140 mil
CGH27060F
Subst = RO4350
W = 500 mil
L = 360 mil
Subst = RO4350
W = 160 mil
L = 220 mil
28 V
Subst = RO4350
W = 67 mil
L = 870 mil
Subst = RO4350
W = 160 mil
L = 350 mil
100 pF
50 Ω
(A)
▿ Power gain
○ Drain efficiency
Gain (dB)
Efficiency (%)
Pin (dBm)
20
18
16
14
12
100
80
60
40
20
0
0
5
10
15
20
25
30
35
(B)
GND
V+
C7
BIAS
C5
C6
C3
C4
IN
U1
OUT
R1
C1
C2
Inverse Class F
GaN HEMT
Power Amplifier 60W
CGH27060F
REV A
Bell Labs Research
Alcatel Lucent 2010
(C)

FIG. 4.45

Transmission-line 50-W inverse Class-F GaN HEMT power amplifier.

the short-circuit and open-circuit effects of the corresponding quarterwave transmission-line stubs, the second- and third-harmonic components are suppressed by more than 25 dB.

Fig. 4.45A shows the simulated circuit schematic of an inverse Class-F GaN HEMT power amplifier based on a 28-V, 60-W Cree RF power transistor CGH27060F. The input matching circuit provides a complex conjugate matching with a 50-Ω source at the fundamental frequency. The load network represents the corresponding microstrip-line implementation of the transmission-line load circuit shown in Fig. 4.43A, where a uniform series transmission line is replaced by the stepped-impedance series transmission line, which is required for convenience of practical implementation and results in shorter overall length.[50] Special stripline models in air substrate for the device input and output package leads are added to the simulation setup to take into account their inductances. For stability reason, a parallel connection of a 10-pF capacitor and a 100-Ω resistor are inserted in series into the input circuit.

Fig. 4.45B shows the simulated results of a transmission-line 50-W inverse Class-F GaN HEMT power amplifier implemented on a 30-mil RO4350 substrate. The maximum output power of 47.6 dBm, drain efficiency of 82.4%, and *PAE* of 78.8% at an operating frequency of 2.14 GHz are achieved with a power gain of 13.6 dB (linear gain of around 20 dB) at a supply voltage of 32 V. A high drain efficiency of more than 80% is achieved in a strong saturation mode when the power gain is compressed by more than 5 dB. In this case, the measured results demonstrate a saturated output power of 47.3 dBm, a drain efficiency of 82.3%, and a power gain of 14.3 dB, resulting in a *PAE* of 79.8% (gate bias voltage $V_g = -3.35$ V, quiescent current $I_q =$ 230 mA, and drain supply voltage $V_{dd} = 32$ V), which was achieved without any tuning of the load network.[50] The test PCB board of a 50-W GaN HEMT power amplifier implemented on a 30-mil RO4350 substrate is shown in Fig. 4.45C. The output power of 46.5–47.0 dBm is provided over the frequency bandwidth of 2.11–2.17 GHz, with drain efficiencies greater than 72% at the input signal of 32 dBm.

Fig. 4.46A shows the simulated circuit schematic of an inverse Class-F LDMOSFET power amplifier based on a 28-V, 75-W NXP RF power transistor BLF6G22LS-75. The input matching circuit provides a complex conjugate matching with a 50-Ω source at the fundamental frequency. The load network represents the corresponding microstrip-line implementation of the simplified transmission-line load network shown in Fig. 4.43A, where a uniform series transmission line is replaced by the stepped-impedance series transmission line. Special stripline models for the device input and output package leads are added to the simulation setup to take into account their inductances. The output power of 48.1 dBm, drain efficiency of 77.6%, and *PAE* of 76.2% at an operating frequency of 2.14 GHz were simulated with a power gain of 17.1 dB (linear gain of about 20 dB) at a supply voltage of 28 V.[50] The test PCB board of a 28-V inverse Class-F LDMOSFET power amplifier implemented on a 30-mil RO4350 substrate is shown in Fig. 4.46B. The measured results for a transmission-line LDMOSFET inverse Class-F power amplifier demonstrate an output power of 48.0 dBm, a drain efficiency of 70.2%, and a power gain of 18.0 dB, resulting in a *PAE* of 69.1% (gate bias voltage $V_g =$ 1.73 V, quiescent current $I_q = 200$ mA, and drain supply voltage $V_{dd} = 28$ V). In this case, an additional tuning of the short-circuited and open-circuited stubs in the load network was necessary to optimize the performance. Note that the maximum drain efficiency of about 60% was achieved in a Class-AB operation mode with the fundamental tuning only.[51]

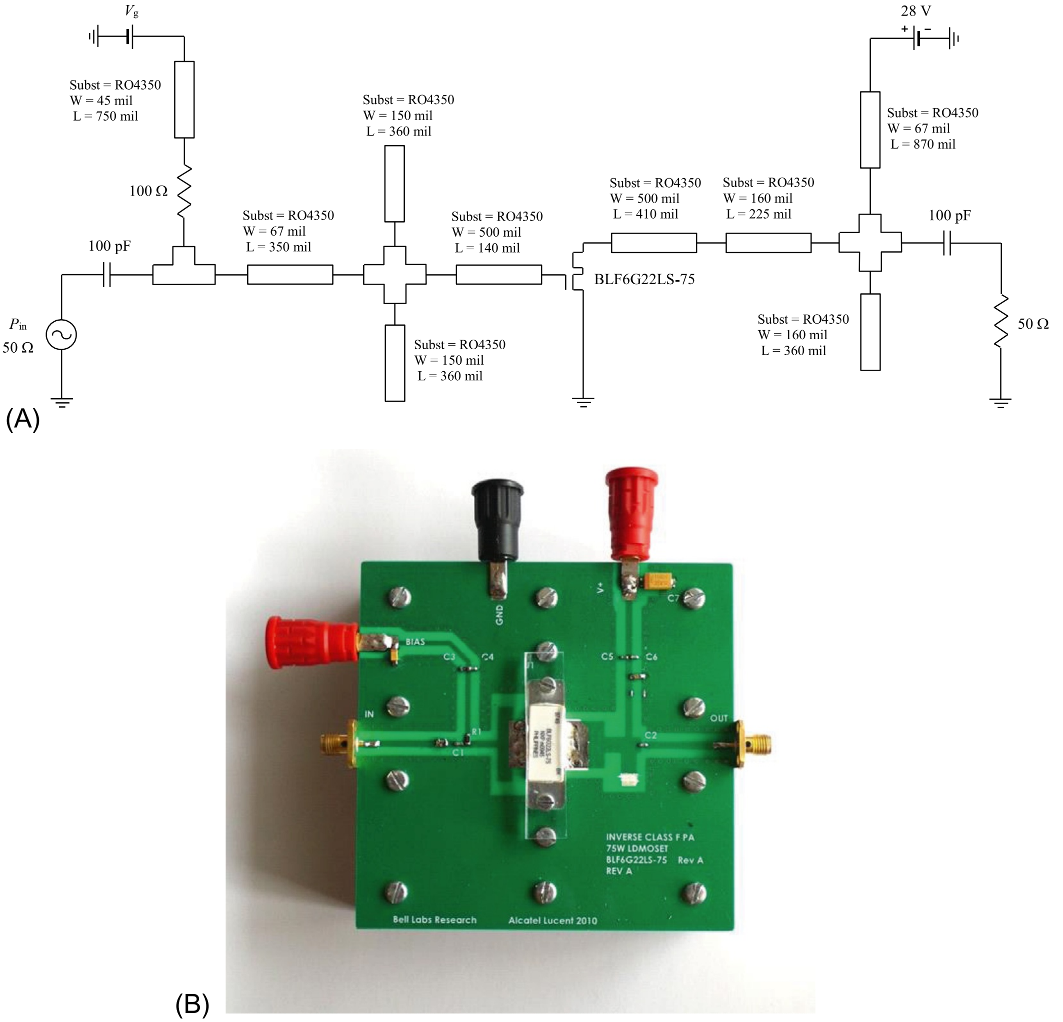

V_g
Subst = RO4350
W = 45 mil
L = 750 mil
100 Ω
100 pF
P_{in}
50 Ω
Subst = RO4350
W = 67 mil
L = 350 mil
Subst = RO4350
W = 150 mil
L = 360 mil
Subst = RO4350
W = 500 mil
L = 140 mil
Subst = RO4350
W = 150 mil
L = 360 mil
BLF6G22LS-75
Subst = RO4350
W = 500 mil
L = 410 mil
Subst = RO4350
W = 160 mil
L = 225 mil
28 V
+
−
Subst = RO4350
W = 67 mil
L = 870 mil
100 pF
Subst = RO4350
W = 160 mil
L = 360 mil
50 Ω
(A)
GND
V+
BIAS
C3
C4
C5
C6
C7
IN
OUT
R1
C1
C2
INVERSE CLASS F PA
75W LDMOSET
BLF6G22LS-75 Rev A
REV A
Bell Labs Research
Alcatel Lucent 2010
(B)

FIG. 4.46

Simulation setup and test board of inverse Class-F LDMOSFET power amplifier.

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CHAPTER

Class-E power amplifiers with shunt capacitance

5

The switchmode Class-E power amplifiers with shunt capacitance have found widespread application because of their design simplicity and high-efficiency operation. Their load-network configuration consists of a shunt capacitor, a series inductor, and a series filter tuned to fundamental frequency to provide a high level of harmonic suppression. In the Class-E power amplifier, the transistor operates as an on-to-off switch, and the shapes of the current and voltage waveforms provide a condition in which the high current and high voltage do not occur simultaneously, which minimizes the power dissipation and maximizes the power-amplifier efficiency. In this chapter, the historical aspects and modern trends of a Class-E power amplifier design are presented. Different circuit configurations and load-network techniques using the push-pull mode, lumped elements, and transmission lines are analyzed. The effects of the transistor saturation resistance, finite switching time, and nonlinear shunt capacitance are described. The practical radio-frequency (RF) and microwave Class-E power amplifiers and their applications are given and discussed.

5.1 History of Class-E techniques

Using resonant circuits in the load network tuned to the odd and/or even harmonics of the fundamental frequency can generate biharmonic or polyharmonic operation modes of vacuum-tube or transistor power amplifiers, which is a very effective approach to increase their operating efficiency. This implies ideally the in-phase or out-of-phase harmonic conditions when symmetrical flattened voltage or current waveforms can be formed by inserting harmonic resonators in the anode circuit and tuning them to the odd and/or even harmonics of the fundamental frequency. However, as it turned out yet in the late 1940s and early 1950s, this is not the only way to improve the power amplifier efficiency, when during experimental tuning of the vacuum-tube amplifiers operating in a saturated mode, it was observed that the efficiency significantly increases when the second- and higher-order harmonics are properly phased.[1–3] In this case, the load must present reactive impedances at the harmonics, thus causing the proper shapes of the anode voltage and current to be formed. The resonant circuit is detuned in the direction of frequencies higher than the operating frequency. The anode efficiencies of 93%–94% were achieved in some cases by simply tuning the resonant circuit to higher frequencies so that the phase angle of the load was in the range of 30–40 degrees. This resulted in the proper inductive impedance at the fundamental frequency and capacitive reactances at the second- and higher-order harmonics.[1, 4]

Independently, in the early 1960s, Rudi de Buda found that the efficiency of a power amplifier can be significantly improved if, instead of conventional Class-C operation, the tube is operated as a

Switchmode RF and Microwave Power Amplifiers. https://doi.org/10.1016/B978-0-12-821448-0.00005-7
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switch.[1, 5] The bias point, drive, and load impedance must be coordinated so that current flows during the conduction interval, but the plate voltage is zero. When the plate voltage is positive, the tube is cut off so that no current flows. Fig. 5.1 shows the circuit schematic of this vacuum-tube switching-mode amplifier with series capacitance C and shunt filter jY having infinite admittance (short circuit) at all harmonics. The optimal parameters for the load network were derived analytically by integrating $i(t)$ flowing through C and assuming pure sine-wave voltage (with the phase selected as reference phase) across load G, with the voltage derivative set to zero at the corresponding time. The load-network parameters C, G, and Y were obtained from a Fourier analysis when the fundamental current component was derived using a Fourier integral from $i(t)$. The theoretical conversion efficiency of an ideal tube of 100% is achieved when load impedance is approximately 35 degrees inductive at the fundamental and is equivalent to a small capacitance at harmonics.

Fig. 5.2 shows the circuit schematic of a vacuum-tube power amplifier with a parallel-tuned LC circuit inserted between the anode and the output matching circuit, which has a resonant frequency

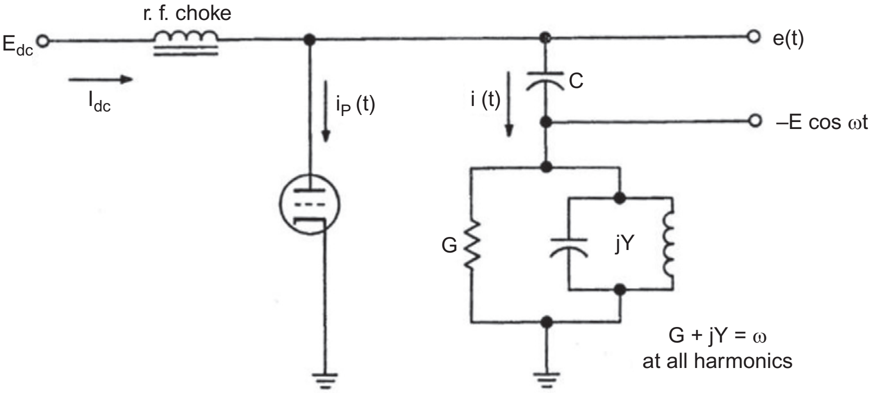

FIG. 5.1

Schematic of a vacuum-tube switching-mode amplifier with series capacitance and shunt filter.

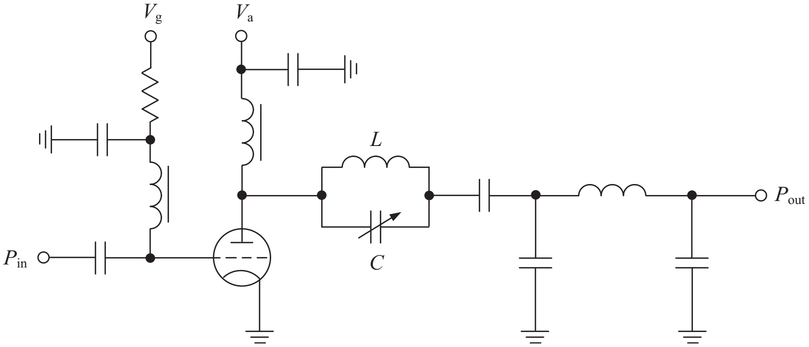

FIG. 5.2

Class-C power amplifier with detuned resonant circuit.

equal to about 1.5 times the carrier frequency of the signal to be amplified.[6] In other words, if the carrier signal is transmitting at a fundamental frequency f_0, the parallel resonant circuit will have a resonant frequency of about $1.5f_0$ followed by a filter or output matching circuit to suppress the harmonics of the fundamental frequency and to maximize the output power at the fundamental frequency delivered to the standard load. As a result, an efficiency of 89% was achieved for a 3.2-MHz vacuum-tube high-power amplifier. Although it was assumed that such a parallel resonant circuit introduces considerable impedance to its own second harmonic (which is the third harmonic $3f_0$ of the carrier frequency) and can result in a flattened anode voltage waveform, another interesting and nontrivial conclusion can be derived from this circuit topology. In this case, provided the output low-pass Π-type matching circuit has purely resistive impedance at the fundamental frequency and capacitive reactances at the harmonic components, the device anode sees inductive impedance at the fundamental frequency and capacitive reactances at the second- and higher-order harmonic components. This means that the voltage and current waveforms are not symmetrical anymore, thus representing an alternative mechanism of the efficiency improvement.

At the same time, it was also discovered that very high efficiencies can be obtained with a series-tuned *LC* circuit connected to a transistor, as shown in Fig. 5.3A.[7] The reasons for this high efficiency are that the transistor operates in a pure switching mode, and that the voltage across the transistor and the current flowing through it can both be made equal to zero during the switch-on transient when a proper choice of the transistor and circuit parameters are provided. To satisfy such a high-efficiency condition of the transistor power amplifier, the collector voltage and voltage derivative should be zero at the time just prior to the conduction interval when the transistor goes into the saturation mode. The series-tuned circuit, consisting of a capacitor C_0 and an inductor L, must appear inductive at the operating frequency. In this case, a loaded quality factor Q_L of the series-tuned circuit of about 10 will give a good sinusoidal shape to the load current. As a result, a 20-W 500-kHz bipolar power amplifier was built, having a collector efficiency of 94% with a conduction angle of 180 degrees.

To realize the high-operation efficiency of the power amplifier, the ideal switch should represent the transistor, and the impedance seen from the collector into the matched circuit should not correspond to a short circuit for the second harmonic over the whole frequency range.[8] The simplified collector circuit of a switchmode power amplifier is shown in Fig. 5.3B, where C is the collector-emitter capacitance (assumed to be independent of voltage), C_0 is the DC-blocking capacitor, L is the series inductor, and R is the load resistor. When the voltage across the capacitor C crosses zero, the switch will be closed. The basic switching operation can be described by two sets of linear first-order differential equations, one set for the on-state and another set for the off-state, with an approximate solution. It was assumed that a high collector efficiency is a result of a zero collector-emitter voltage at the end of the off-state cycle due to transient without the need for any current when only a small power is dissipated in the switching slopes. Collector efficiencies up to 85% were achieved in the frequency range of 48–70 MHz.

The exact theoretical analysis of the operation conditions of a single-ended switchmode power amplifier using its simplified equivalent circuit shown in Fig. 5.3B, with the calculation of the circuit parameters first given in Refs. 9,10. Here, the active device is considered an ideal switch that is driven to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the switch when it is turned on and by the transient response of the load network when the switch is turned off. To simplify a theoretical analysis, the following assumptions were introduced:

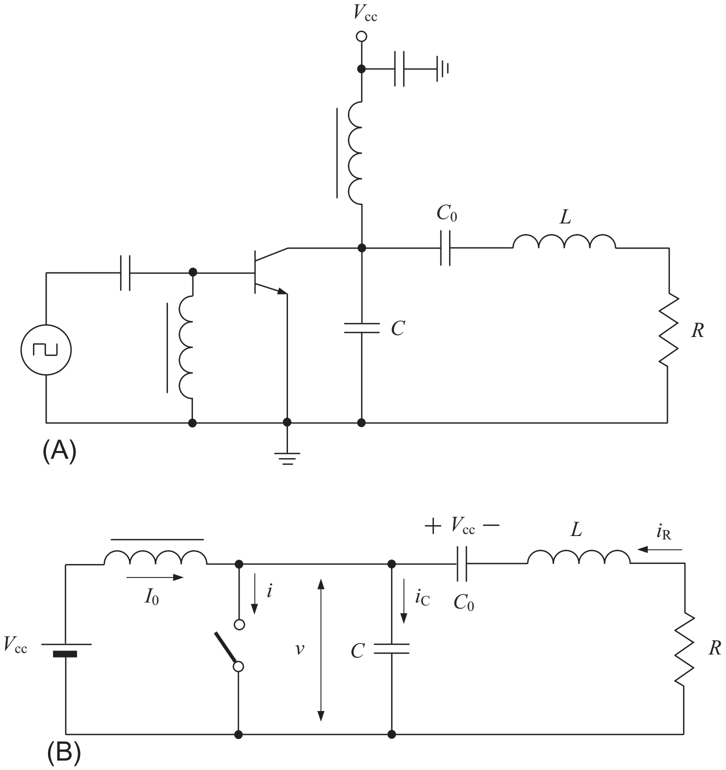

FIG. 5.3

Basic circuits of a switchmode power amplifier with nonsinusoidal output voltage.

- Transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless (except when discharging the shunt capacitance).
- Total shunt capacitance is independent of the collector and is assumed linear.
- RF choke allows only a constant DC current and has no resistance.
- There are no losses in the circuit except only into the load R.

For a lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch at turn-on time moment $t=T$, when the transistor is saturated:

$$v(t)\big|_{t=T}=0 \tag{5.1}$$

$$\left.\frac{dv(t)}{dt}\right|_{t=T}=0 \tag{5.2}$$

where T is the period of input driving signal, and $v(t)$ is the voltage across the switch. The second optimum condition given by Eq. (5.2) means that the collector current $i(t)$ has no jump and is equal to zero at this moment because the collector capacitor C is completely discharged.

The derivation of the load-network parameters is based on the consideration of the processes during on-state and off-state transistor operation modes separately.[10, 11] When the switch is turned on, the equivalent amplifier system is described by a system of the first-order differential equations in the form

$$V_{\text{cc}} = L\frac{di_{\text{R}}(t)}{dt} + i_{\text{R}}(t)R \tag{5.3}$$

$$i(t) = I_0 + i_{\text{R}}(t) \tag{5.4}$$

where the voltage V_{cc} is applied to the plates of the blocking capacitor C_0. By taking into account the initial condition $i(0)=0$, the current $i(t)$ flowing through the switch can be obtained by

$$i_{\text{s}}(t) = \frac{V_{\text{cc}} + I_0R}{R}\left[1 - \exp\left(-\frac{R}{L}t\right)\right] \tag{5.5}$$

When the switch is turned off at the time moment $t=t_1$, another system of the first-order differential equations can be written by

$$V_{\text{cc}} = v(t) + L\frac{di_{\text{R}}(t)}{dt} + i_{\text{R}}(t)R \tag{5.6}$$

$$C\frac{dv(t)}{dt} = I_0 + i_{\text{R}}(t) \tag{5.7}$$

with the initial conditions $i_{\text{R}}(t_1) = i(t_1) - I_0$ and $v(t_1) = 0$.

Hence the voltage $v(t)$ across the switch can be obtained by

$$v(t) = (V_{\text{cc}} + I_0R)\left[1 + \frac{1}{\omega}\sqrt{d^2 + \omega^2}\exp(-\delta t)\sin(\omega t + \varphi)\right] \tag{5.8}$$

where

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad \delta = \frac{R}{2L} = \frac{\omega_0}{2Q_{\text{L}}}$$

$$d = \frac{i(t_1)}{(V_{\text{cc}} + I_0R)}\frac{1}{C} - \delta$$

$$\varphi = \tan^{-1}\left(\frac{\omega}{d}\right) \qquad \omega = \sqrt{\omega_0^2 - \delta^2}$$

In an optimum operation mode when the collector (A) voltage and (B) current waveforms shown in Fig. 5.4 do not overlap each other resulting in a zero power loss on the transistor, the voltage $v(t)$ in Eq. (5.8) should satisfy the optimum zero-voltage and zero-voltage-derivative conditions given by Eqs. (5.1) and (5.2). As a result, the analytical relationships between the load-network components can be properly obtained, whose values for different duty ratio or saturation time $\tau_{\text{sat}} = \omega t_1$ are given in Table 5.1, where $P_{\text{out}} = I_0V_{\text{cc}}$ is the output power corresponding to the idealized lossless operation conditions.[12]

However, to provide such an idealized switching operation mode, the loaded quality factor of this L-type circuit should be sufficiently small, for example, $Q_{\text{L}} = 2.8656$ for a 50% duty ratio, increasing at smaller duty ratios. This leads to the variation of the harmonic coefficient from 15% at $\tau_{\text{sat}} = 216$ degrees to 3% at $\tau_{\text{sat}} = 144$ degrees. As a result, such a switchmode bipolar power amplifier designed

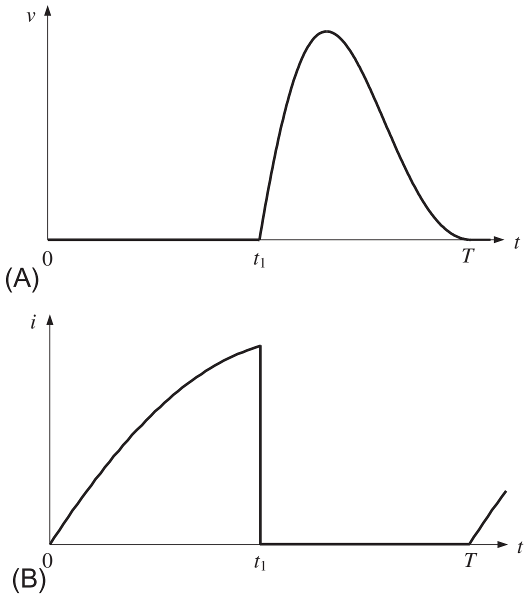

FIG. 5.4

Idealized collector voltage and current waveforms of switchmode power amplifier with nonsinusoidal output voltage.

Table 5.1 Load-network parameters of a switchmode power amplifier.

Parameters	τ_{sat} (degrees)				
	108	**144**	**180**	**216**	**252**
$\frac{\omega L}{R}$	3.4872	2.4083	1.7879	1.3494	0.9887
ωCR	0.2063	0.2280	0.2177	0.1865	0.1437
$\frac{P_{out}R}{V_{cc}^2}$	0.0732	0.1788	0.3587	0.6622	1.1953

to operate at 1 MHz and supply voltage of 15 V with a total output power of 3 W could provide a collector efficiency of 95.9% under optimum switching conditions with a 50% duty ratio.[12]

5.2 Load network with shunt capacitor and series filter

For additional harmonic suppression, it is necessary to connect the load through the series filter tuned to the fundamental frequency, for example, a simple L_0C_0 filter shown in Fig. 5.5A.[9, 13] The loaded quality factor Q_L of the series resonant circuit consisting of an inductor L_0 and a capacitor C_0 tuned to the

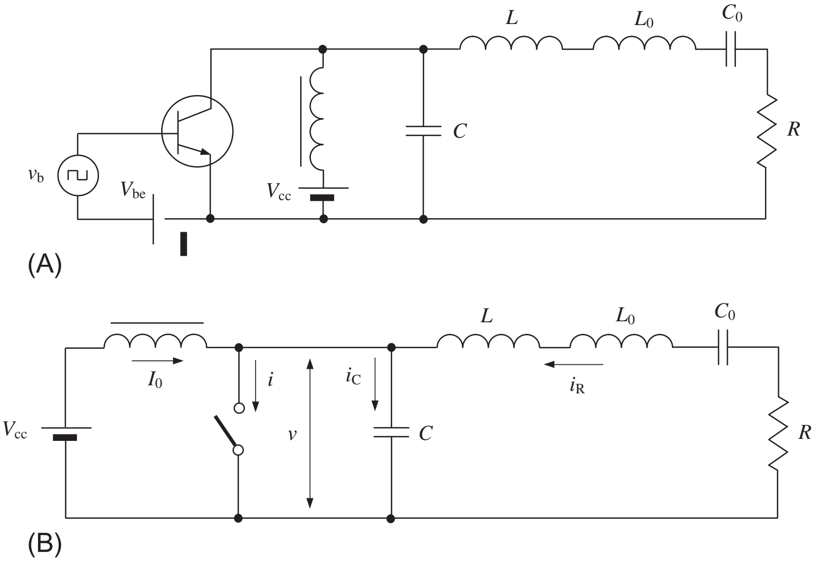

FIG. 5.5

Basic circuits of a Class-E power amplifier with shunt capacitance.

fundamental frequency $\omega_0 = 1/\sqrt{L_0C_0}$ should be sufficiently high for the output current to be sinusoidal. The single-ended switchmode power amplifier with a shunt capacitor and series filter was introduced by the Sokals in 1975 as a Class-E power amplifier and has found widespread application because of their design simplicity and high operation efficiency.[14, 15] This type of high-efficiency power amplifiers was then widely used in different frequency ranges and output power levels, ranging from several kilowatts at low RF frequencies up to about 1 W at microwaves.[16]

The characteristics of a Class-E power amplifier can be determined by finding its steady-state collector voltage and current waveforms. The simplified equivalent circuit of a Class-E power amplifier with shunt capacitance is shown in Fig. 5.5B, where the load network consists of a capacitor C shunting the transistor output, a series inductor L, a series fundamentally tuned L_0C_0 circuit, and a load resistor R. In a common case, the shunt capacitor C represents the transistor output capacitance and an external circuit capacitor. The collector of the transistor is connected to the supply voltage by an RF choke with a high reactance at the fundamental frequency. The transistor is considered an ideal switch that is driven in such a way as to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the switch when it is turned on and by the transient response of the load network when the switch is turned off.

To simplify the analysis of a Class-E power amplifier, the following assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.
- The total shunt capacitance is independent of the collector and is assumed to be linear.
- The RF choke allows only a constant DC current and has no resistance.

- The loaded quality factor $Q_L = \omega L_0/R = 1/\omega C_0 R$ of the series resonant L_0C_0 circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal at the switching frequency.
- There are no losses in the circuit except only in the load R.
- For simplicity, a 50% duty ratio is used.

For a lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch (just prior to the start of switch on) at the moment $\omega t = 2\pi$, when the transistor is saturated:

$$v(\omega t)|_{\omega t=2\pi} = 0 \tag{5.9}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0 \tag{5.10}$$

where $v(\omega t)$ is the voltage across the switch.

A detailed theoretical analysis of a Class-E power amplifier with shunt capacitance, for any duty ratio, is given in Ref. 17, where the load current is assumed to be sinusoidal:

$$i_R(\omega t) = I_R \sin(\omega t + \varphi) \tag{5.11}$$

where φ is the initial phase shift.

When the switch is turned on for $0 \leq \omega t < \pi$, the current through the capacitance

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = 0 \tag{5.12}$$

and, consequently,

$$i(\omega t) = I_0 + I_R \sin(\omega t + \varphi) \tag{5.13}$$

under the initial on-state condition $i(0) = 0$. Hence the DC current can be defined as

$$I_0 = -I_R \sin\varphi \tag{5.14}$$

and the current through the switch can be rewritten by

$$i(\omega t) = I_R[\sin(\omega t + \varphi) - \sin\varphi] \tag{5.15}$$

When the switch is turned off for $\pi \leq \omega t < 2\pi$, the current through the switch $i(\omega t) = 0$, and the current flowing through the capacitor C can be written as

$$i_C(\omega t) = I_0 + I_R \sin(\omega t + \varphi) \tag{5.16}$$

producing the voltage across the switch by the charging of this capacitor according to

$$v(\omega t) = \frac{1}{\omega C}\int_{\pi}^{\omega t} i_C(\omega t)\, d\omega t = -\frac{I_R}{\omega C}[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi] \tag{5.17}$$

Applying the first optimum condition given by Eq. (5.9) enables the phase angle φ to be determined as

$$\varphi = \tan^{-1}\left(-\frac{2}{\pi}\right) = -32.482° \tag{5.18}$$

Consideration of trigonometric relationships shows that

$$\sin\varphi = \frac{-2}{\sqrt{\pi^2+4}} \quad \text{and} \quad \cos\varphi = \frac{\pi}{\sqrt{\pi^2+4}} \tag{5.19}$$

Then, the steady-state voltage waveform across the switch using Eqs. (5.14) and (5.19) can be obtained by

$$v(\omega t) = \frac{I_0}{\omega C}\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{5.20}$$

By using a Fourier series expansion, the expression to determine the supply voltage V_{cc} can be written as

$$V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)d\omega t = \frac{I_0}{\pi\omega C} \tag{5.21}$$

As a result, the normalized steady-state collector voltage waveform for $\pi \le \omega t < 2\pi$ and current waveform for period of $0 \le \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{cc}} = \pi\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{5.22}$$

$$\frac{i(\omega t)}{I_0} = \frac{\pi}{2}\sin\omega t - \cos\omega t + 1 \tag{5.23}$$

Fig. 5.6 shows the normalized (A) load current, (B) collector voltage, and (C) collector current waveforms for an idealized optimal Class-E mode with shunt capacitance. From the collector voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch and current $i(\omega t)$, consisting of the load sinusoidal current and DC current, which flows through the transistor. However, when the transistor is turned off, this current flows through the shunt capacitor C. The jump in the collector current waveform at the instant of switching off is necessary to obtain nonzero output power at the fundamental frequency delivered to the load, which can be defined as an integration of the product of the collector voltage and current derivatives over the entire period.[18] Therefore, dv/dt and di/dt must both be nonzero during at least one of the switching transitions.

As a result, there is no nonzero voltage and current simultaneously, which means a lack of the power losses, and gives an idealized collector efficiency of 100%. This implies that the DC power and fundamental-frequency output power delivered to the load are equal,

$$I_0 V_{cc} = \frac{I_R^2}{2}R \tag{5.24}$$

Consequently, the value of the DC supply current I_0 using Eqs. (5.14) and (5.19) can be determined by

$$I_0 = \frac{V_{cc}}{R}\frac{8}{\pi^2+4} = 0.577\frac{V_{cc}}{R} \tag{5.25}$$

Then, the amplitude of the output voltage $V_R = I_R R$ can be obtained from

$$V_R = \frac{4V_{cc}}{\sqrt{\pi^2+4}} = 1.074V_{cc} \tag{5.26}$$

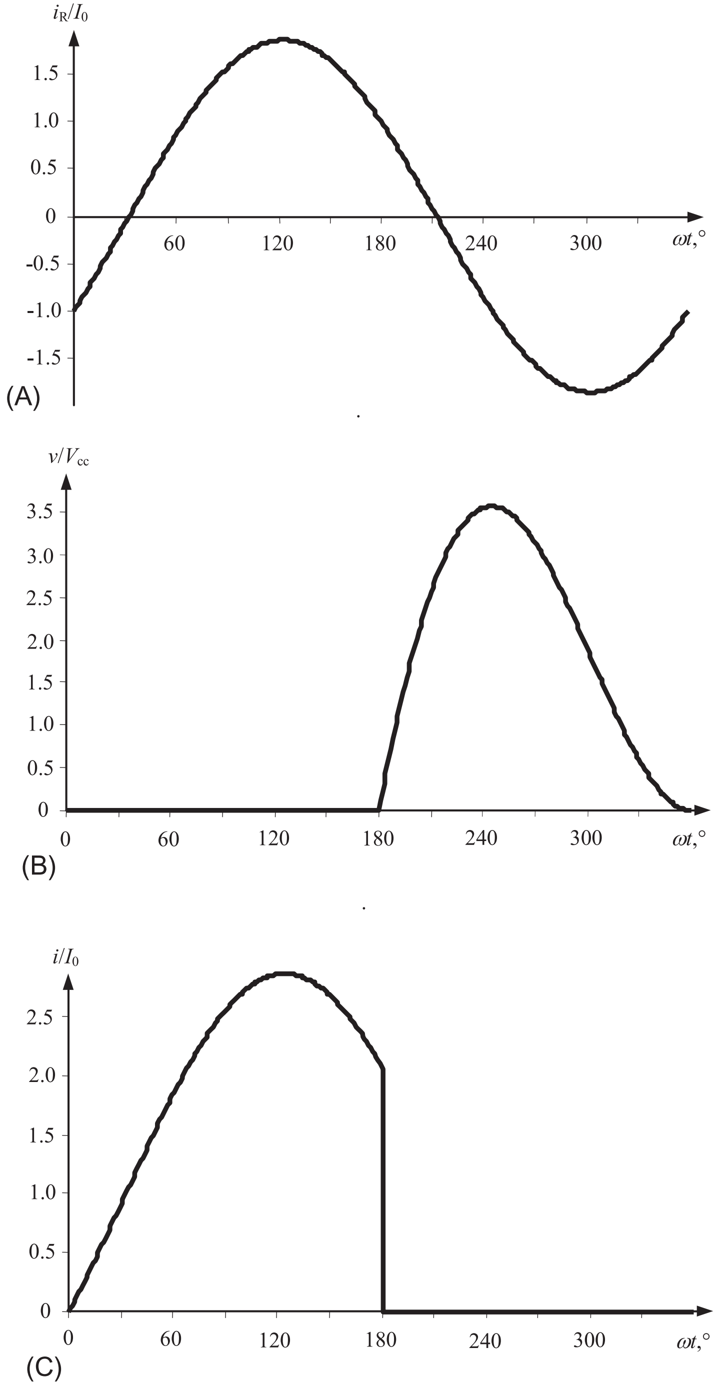

FIG. 5.6

Normalized load current, collector voltage, and collector current waveforms for nominal Class-E with shunt capacitance.

The peak collector voltage $V_{\max}$ and current $I_{\max}$ can be determined by differentiating the appropriate waveforms given by Eqs. (5.22) and (5.23), respectively, and setting the results equal to zero, which gives

$$V_{\max} = -2\pi\varphi V_{\mathrm{cc}} = 3.562 V_{\mathrm{cc}} \tag{5.27}$$

and

$$I_{\max} = \left(\frac{\sqrt{\pi^2+4}}{2}+1\right) I_0 = 2.8621 I_0 \tag{5.28}$$

The fundamental-frequency voltage $v_1(\omega t)$ across the switch consists of the two quadrature components shown in Fig. 5.7, whose amplitudes can be found using Fourier formulas and Eq. (5.22) as

$$V_{\mathrm{R}} = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin(\omega t+\varphi)d\omega t = \frac{I_{\mathrm{R}}}{\pi\omega C}\left(\frac{\pi}{2}\sin 2\varphi + 2\cos 2\varphi\right) \tag{5.29}$$

$$V_{\mathrm{L}} = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t+\varphi)d\omega t = -\frac{I_{\mathrm{R}}}{\pi\omega C}\left(\frac{\pi}{2} + \pi\sin^2\varphi + 2\sin 2\varphi\right) \tag{5.30}$$

As a result, the optimum series inductance L and shunt capacitance C can be calculated from

$$\frac{\omega L}{R} = \frac{V_{\mathrm{L}}}{V_{\mathrm{R}}} = 1.1525 \tag{5.31}$$

$$\omega CR = \frac{\omega C}{I_{\mathrm{R}}} V_{\mathrm{R}} = 0.1836 \tag{5.32}$$

The optimum load resistance R for the supply voltage V_{cc} and fundamental-frequency output power P_{out} delivered to the load using Eqs. (5.24) and (5.26) can be obtained by

$$R = \frac{8}{\pi^2+4}\frac{V_{\mathrm{cc}}^2}{P_{\mathrm{out}}} = 0.5768\frac{V_{\mathrm{cc}}^2}{P_{\mathrm{out}}} \tag{5.33}$$

Finally, the phase angle of the load network seen by the switch and required for an idealized optimum (or nominal) Class-E mode with shunt capacitance can be determined through the load-network parameters using Eqs. (5.31) and (5.32) as

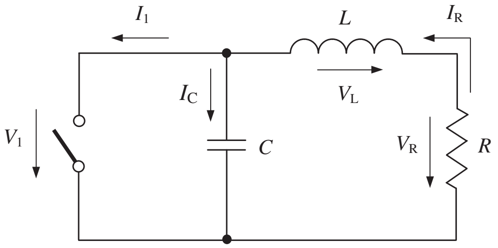

FIG. 5.7

Equivalent Class-E load network at fundamental frequency.

$$\varphi = \tan^{-1}\left(\frac{\omega L}{R}\right) - \tan^{-1}\left(\frac{\omega CR}{1 - \frac{\omega L}{R}\omega CR}\right) = 35.945° \tag{5.34}$$

When realizing a Class-E operation mode, it is very important to know up to which maximum frequency such an idealized efficient operation mode can be extended. In this case, it is important to establish a relationship between the maximum operation frequency $f_{\max}$, shunt capacitance C, output power P_{out}, and supply voltage V_{cc} by using Eqs. (5.32) and (5.33) when

$$f_{\max} = 0.0507\left(P_{\text{out}}/CV_{\text{cc}}^2\right) \tag{5.35}$$

where $C = C_{\text{out}}$ is the device output capacitance limiting the maximum operation frequency of an idealized optimum Class-E power amplifier with shunt capacitance.

The high-Q_{L} assumption for the series-resonant L_0C_0 circuit can lead to considerable errors if its value is substantially small in real circuits.[19] For example, for a 50% duty ratio, the values of the load-network parameters for the loaded quality factor Q_{L} less than unity can differ by several tens of percentages. At the same time, for $Q_{\text{L}} \geq 7$, the errors are found to be less than 10%, and they become less than 5% for $Q_{\text{L}} \geq 10$. A detailed overview of Class-E power amplifiers with shunt capacitance, including explicit design equations, applicable frequency ranges, optimization principles, and experimental results, is given in Ref. 20.

5.3 Matching with standard load

For most practical applications, it is necessary to match the required Class-E optimum load resistance R with a standard load resistance R_{L}, usually equal to 50 Ω. Fig. 5.8A shows the equivalent circuit of a Class-E power amplifier with shunt capacitance, where the series L_0C_0 filter is followed by an L-type low-pass matching circuit consisting of a series inductor L_1 and a shunt capacitor C_1.[21] Such a connection of this matching circuit when its shunt capacitor C_1 is connected in parallel to the load resistor R_{L} assumes that $R < R_{\text{L}}$. This is normally the case for the high-power or low-voltage power amplifiers. The main goal of the matching circuit is to provide a maximum delivery of the output power at the fundamental frequency $f_0 = \omega_0/2\pi$ to the standard load of 50 Ω because it is assumed that the series L_0C_0 filter has sufficiently high Q-factor to suppress the harmonic components of the fundamental frequency.

In this case, the Class-E optimum resistance R generally can be defined through the parameters of the L-type low-pass impedance-matching circuit and the load resistance R_{L} as

$$R = \frac{R_{\text{L}}}{1 + (\omega_0 R_{\text{L}} C_1)^2} + j\left[\omega L_1 - \frac{\omega_0 C_1 R_{\text{L}}^2}{1 + (\omega_0 R_{\text{L}} C_1)^2}\right] \tag{5.36}$$

Because it is necessary to provide the complex-conjugate matching conditions to maximize the output power in the load, the imaginary part of Eq. (5.36) must be equated to zero. Then, Eq. (5.36) can be resolved separately for the real and imaginary parts as

$$R_{\text{L}} = R\left(1 + Q_{\text{L}}^2\right) \tag{5.37}$$

$$\frac{1}{\omega_0 C_1} = \omega_0 L_1\left(1 + Q_{\text{L}}^{-2}\right) \tag{5.38}$$

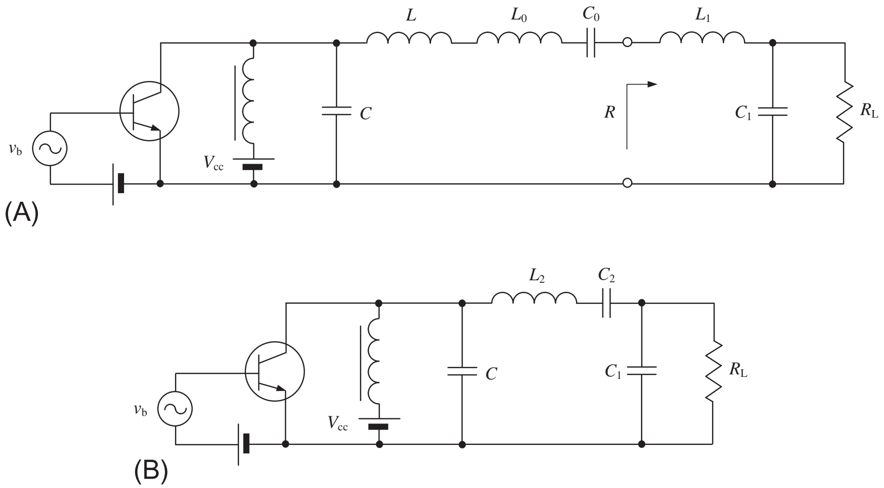

FIG. 5.8

Schematics of Class-E power amplifiers with impedance-matching circuits.

where

$$Q_L = \omega_0 C_1 R_L = \frac{\omega_0 L_1}{R} \tag{5.39}$$

is the loaded quality factor that is equal for both the series and parallel circuits at the fundamental frequency.

As a result, the loaded quality factor Q_L can be expressed through the load resistances R and R_L as

$$Q_L = \sqrt{\frac{R_L}{R} - 1} \tag{5.40}$$

while the matching circuit parameters can be calculated from

$$L_1 = \frac{R Q_L}{\omega_0} \tag{5.41}$$

$$C_1 = \frac{Q_L}{\omega_0 R_L} \tag{5.42}$$

The series high-Q_L filter and L-type matching circuit can be combined into a Π-type circuit with two shunt capacitors and series L_2C_2 circuit, where $L_2 = L + L_0 + L_1$ and $C_2 = C_0$, as shown in Fig. 5.8B. Generally, a tandem connection of any type of low-pass or band-pass matching sections can be used for different ratios between the required optimum Class-E load resistance R and the standard load resistance R_L. In this case, to simplify the matching design procedure, it is best to cascade the low-pass L-type matching sections with equal values of their Q_L-factors.[22, 23]

Fig. 5.9A shows the circuit schematic of a lumped-elements Class-E HBT power amplifier operated in a frequency bandwidth of 5–6 GHz and based on a single-section low-pass output matching circuit.[24] Here, the capacitor C_2 and inductor L_2 are determined to obtain the appropriate Class-E load impedance at the fundamental frequency. Owing to its low-pass characteristic, the impedance seen at the collector terminal tends to approximate an open circuit with increasing frequency. The input network was designed to match the transistor input impedance to the 50-Ω source impedance, where the ballasting resistor R_1 and large capacitance C_1 are used to improve low-frequency stability. In a monolithic power amplifier based on an AlGaN/GaN HEMT technology with $f_T = 18$ GHz, whose circuit schematic is shown in Fig. 5.9B, a shunt capacitor C_2 is fabricated using parallel-plate technology with silicon nitride (SiN) passivation dielectric layer, and a series multiturn inductor L_2 is implemented using air-bridges and a 3-μm-thick gold interconnected layer, resulting in a power-added efficiency (*PAE*) of 61% and an output power of 33.8 dBm at an operating frequency of 4 GHz.[25]

In the case of monolithic implementation of the Class-E power amplifier, the large value of an inductor L_0 shown in Fig. 5.8A results in significant ohmic losses and low self-resonant frequency that is

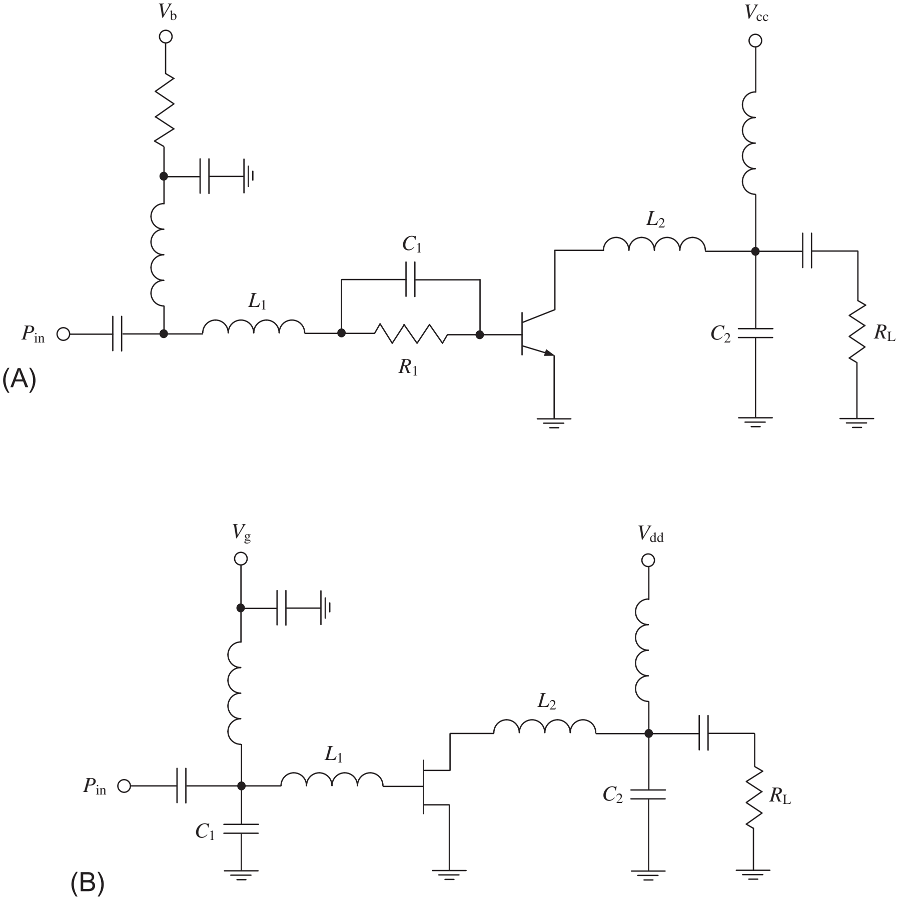

FIG. 5.9

Schematics of a lumped-elements Class-E power amplifiers with shunt capacitance.

crucial at microwave frequencies. Therefore to minimize the inductance value of the monolithically implemented spiral inductor, the Class-E load network can represent the alternative topology shown in Fig. 5.10A with an optimized second-harmonic peaking and a simultaneous impedance transformation at the fundamental frequency.[24] Here, the parallel tank formed by capacitor C_1 and inductor L_1 is designed to resonate at $2f_0$. The net impedance of the second-harmonic resonator must represent an inductive reactance at the fundamental frequency f_0, similar to the contribution of inductance L in the Class-E load network shown in Fig. 5.8A. In this case, it is assumed that the capacitive reactances of the parallel tank at the third and higher-order harmonic components are relatively high when compared with that provided by the shunt capacitance C.

Consequently, the design equations for the load-network elements L_2, C_1, and C_2 in Fig. 5.10A can be derived by using Eq. (5.31) as

$$L_2 = \frac{3R}{4\omega_0}\left(Q_L + 1.1525\right) \tag{5.43}$$

$$C_2 = \frac{1}{4\omega_0^2 L_2} \tag{5.44}$$

$$C_1 = \frac{Q_L}{\omega_0 R_L} \tag{5.45}$$

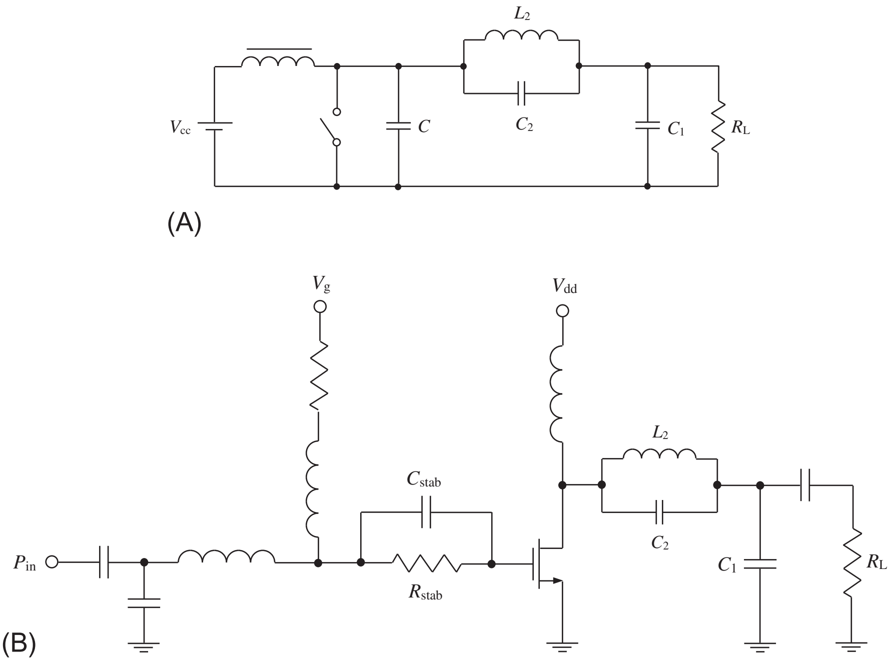

FIG. 5.10

Schematics of a lumped-elements Class-E power amplifier with second-harmonic peaking.

where Q_L is obtained from Eq. (5.40).

Fig. 5.10B shows the circuit schematic of a lumped 2.55-GHz Class-E power amplifier with a tank resonant circuit in the load network tuned to the second harmonic. Based on a 90-nm CMOS process, this power amplifier achieved a simulated drain efficiency of 57.4% at an output power of 22.7 dBm when operated from a supply voltage of 2.5 V.[26]

5.4 Effect of saturation resistance

In practical power amplifier design, especially when a value of the supply voltage is sufficiently small, it is very important to predict the overall degradation of power amplifier efficiency due to the finite value of the transistor saturation resistance. Fig. 5.11 shows the simplified equivalent circuit of a Class-E power amplifier with shunt capacitance, including the saturation resistance (on-resistance) $r_{\rm sat}$ connected in series to the ideal switch. To obtain a quantitative estimate of the losses due to the contribution of $r_{\rm sat}$, the saturated output power $P_{\rm sat}$ can be obtained with a simple approximation when the current $i(\omega t)$ flowing through the saturation resistance $r_{\rm sat}$ is determined in an ideal case by Eq. (5.23).

An analytical expression to calculate the power losses due to the saturation resistance $r_{\rm sat}$, whose value is assumed constant, can be represented in the normalized form as

$$\frac{P_{\rm sat}}{P_0} = \frac{r_{\rm sat}}{2\pi I_0 V_{\rm cc}} \int_0^{\pi} i^2(\omega t)\, d\omega t \tag{5.46}$$

where $P_0 = I_0 V_{\rm cc}$ is the DC power. As a result, by using a linear approximation of the collector current waveform for the Class-E load network with one inductor and one capacitor whose equivalent circuit without saturation resistance $r_{\rm sat}$ is shown in Fig. 5.3B, the averaged dissipated power $P_{\rm sat}$ normalized to the DC power P_0 can be evaluated by

$$\frac{P_{\rm sat}}{P_0} = \frac{8}{3} \frac{r_{\rm sat} P_0}{V_{\rm cc}^2} \tag{5.47}$$

for the required DC power P_0 and supply voltage $V_{\rm cc}$.[21]

For a Class-E power amplifier with shunt capacitance represented by equivalent circuit shown in Fig. 5.11, by taking into account that

$$\int_0^{\pi} \left(\frac{\pi}{2} \sin \omega t - \cos \omega t + 1 \right)^2 d\omega t = \frac{\pi}{8} (\pi^2 + 28) I_0^2 \tag{5.48}$$

Eq. (5.46) can be finally rewritten using Eq. (5.25) by

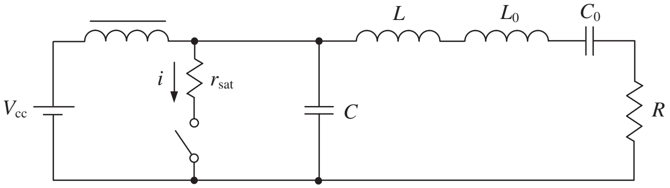

FIG. 5.11

Equivalent Class-E load network with transistor saturation resistance.

$$\frac{P_{\text{sat}}}{P_0} = \frac{r_{\text{sat}}}{2\pi} \frac{I_0}{V_{\text{cc}}} \frac{\pi}{8} \left(\pi^2 + 28 \right) = \frac{r_{\text{sat}}}{2R} \frac{\pi^2 + 28}{\pi^2 + 4} = 1.365 \frac{r_{\text{sat}}}{R} \tag{5.49}$$

The collector efficiency η can be calculated from

$$\eta = \frac{P_{\text{out}}}{P_0} = \frac{P_0 - P_{\text{sat}}}{P_0} = 1 - \frac{P_{\text{sat}}}{P_0} \tag{5.50}$$

Hence the presence of the saturation resistance results in the finite value of the saturation voltage V_{sat}, which can be defined from

$$\frac{V_{\text{sat}}}{V_{\text{cc}}} = 1 - \frac{1}{1 + 1.365 \dfrac{r_{\text{sat}}}{R}} \tag{5.51}$$

where V_{sat} is normalized to the DC collector voltage V_{cc}.[27]

In an optimum switching mode when both Class-E conditions given by Eqs. (5.9) and (5.10) are satisfied, the second optimum condition is equivalent to

$$\left. \frac{di(\omega t)}{d\omega t} \right|_{\omega t = 2\pi} = 0 \tag{5.52}$$

when the collector current at the end of each period must start with zero derivative because $v(\omega t) = r_{\text{sat}}\, i(\omega t)$. Fig. 5.12 shows the collector voltage and current waveforms by solid lines corresponding to an optimum operation mode.[13] Here, the shape of the saturation voltage shown in Fig. 5.12A is determined by the collector current waveform. However, if the first optimum condition is not satisfied when, for example, some positive value of the collector voltage at the time when the transistor is turned on is assumed, this results in the switching losses accompanied by the proper transient response of the current waveform shown in Fig. 5.12B by dashed lines in the impulse form, with a finite amplitude whose duration is determined by the time constant $\tau_s = r_{\text{sat}}C$.[28] In this case, the peak collector voltage reduces compared to the optimal case.

In addition to the saturation resistance r_{sat}, the power losses in the elements of the load network are also very important for predicting the efficiency of the Class-E power amplifier. The contribution of each circuit element to the overall power loss and drain efficiency was experimentally validated on the example of a 300-W MOSFET Class-E power amplifier developed to operate at a switching frequency of 7.29 MHz and a DC supply voltage of 130 V with a sinusoidal driving signal.[29] Being calculated at 42.5% duty ratio, the individual component losses of the elements of the equivalent Class-E load network shown in Fig. 5.13 are listed in Table 5.2. A power MOSFET transistor IRFP440 was used as a switch, and its saturation resistance r_{sat} was obtained from the manufacturer's data sheet. As a result, the total calculated power loss was 29.3 W, resulting in a drain efficiency of 91.1%, which is very close to the measured drain efficiency of 90.1%. As it was expected, more than 40% of the total power loss is contributed by the power transistor because of its nonzero value of the saturation resistance.

5.5 Driving signal and finite switching time

An analysis of the idealized operation of the Class-E power amplifier is based on a preliminary assumption of instant transistor switching of the saturation mode with zero on-resistance to the pinch-off mode

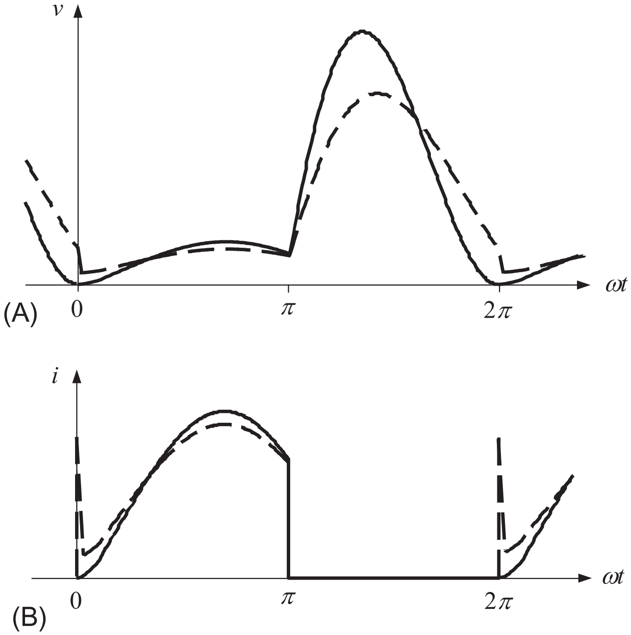

FIG. 5.12

Collector voltage and current waveforms for an idealized Class-E with saturation resistance.

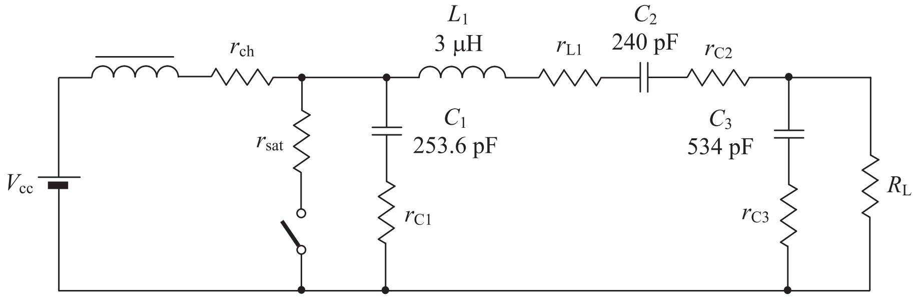

FIG. 5.13

Equivalent Class-E load network with lossy elements.

with zero current. However, real transistors are characterized by nonzero transition times when switching time may constitute a significant part of the period, especially at high frequencies. In this case, there are different contributions of the nonzero switching conditions during the on-to-off and off-to-on transitions. If the power loss during the off-to-on transition is negligible because the collector voltage drops to zero at the end of pinch-off mode with collector (or drain) current starting from zero value, the power loss becomes significant during the on-to-off transition because the collector (or drain) current must

Table 5.2 Component resistance and predicted power loss.

Component	Resistance (Ω)	Predicted power loss (W)
r_{sat}	0.85	12.75
r_{C2}	0.42	6.29
r_{L1}	0.28	4.19
r_{C3}	0.42	3.77
r_{C1}	0.23	1.22
r_{ch}	0.2	1.07

decrease instantly to zero from a significant value that it achieves at the end of the saturation mode. Physically, the finite switching time can be explained by the device inertia when the base charge reduces to zero value with some finite time delay τ_s. Owing to the device inertia, mostly owing to the time delay in its input circuit, there is an active state where the collector (or drain) current is determined by the base (or channel) charge process but not by the load network.

The input port characteristics of bipolar, MOSFET, or MESFET transistors are so different that generally a different driver circuit should be used for each transistor type. In this case, the best gate voltage drive should represent a trapezoidal waveform, with the falling transition occupying 30% or less of the period. A shorter transition time is difficult to achieve because of the effect of the transistor equivalent circuit parameters, among which the most important are the gate resistance R_g, the gate-source capacitance C_{gs}, and the gate-drain capacitance C_{gd}, providing an input time delay $\tau_{in} = R_g(C_{gs} + C_{gd})$. For both MOSFET and MESFET transistors, the optimum drive minimizes the sum of the output stage power dissipation and the driver stage power consumption. The peak of the drive waveform should be safely below the transistor maximum gate-source voltage rating. For MESFET devices, it should be less than the gate-source voltage, at which the gate-source diode conducts enough current to cause either of two undesired effects:

- Metal migration of the gate metallization at an undesirably rapid rate, making the transistor operating lifetime shorter than desired.
- Enough power dissipation to reduce the overall efficiency more than the efficiency is increased by the lower dissipation in the lower on-resistance that results from a higher upper level of the drive waveform.

The lower level of the trapezoid should be low enough to result in a satisfactorily small current during the off-state of the transistor operation. A sine wave is a usable approximation to the trapezoidal waveform, though not optimum. To obtain the transistor duty ratio of 50% that is usually the best choice, the zero level of the sine wave should be positioned slightly above the transistor turn-on threshold voltage. It is a better approximation to remove the part of the sine waveform that goes below the value of the gate-source bias voltage that ensures fully off-state operation, replacing it with a constant voltage at that gate-source bias voltage. This reduces the input drive power by slightly less than 50%, almost doubling the power gain.

Fig. 5.14 shows the simplified equivalent transistor model, where both capacitances C_{in} and C_{out} include the feedback base-collector (or gate-drain) capacitance. Despite the simplification, such an equivalent model can describe with a sufficient accuracy the behavior of the bipolar, MOSFET, or

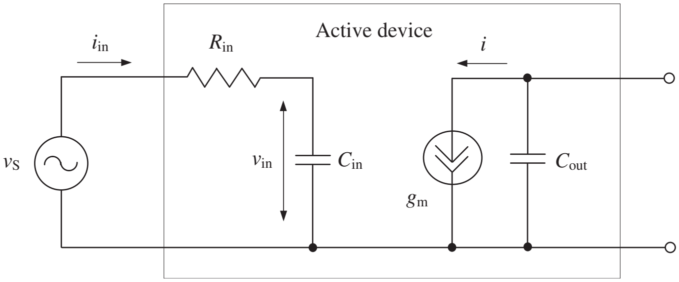

FIG. 5.14

A simplified equivalent transistor model.

MESFET transistor up to approximately $0.1f_T$, where f_T is the transition frequency. Moreover, for a MOSFET transistor, the gate-source capacitance varies insignificantly over a wide range of the gate-bias voltages, whereas the feedback gate-drain capacitance is sufficiently small, normally by an order of less than the gate-source capacitance. Let us assume that the transistor is driven from the signal source with a sinusoidal voltage,

$$v_S(\omega t) = V_0 + V_S \sin(\omega t + \psi_0) \tag{5.53}$$

where V_0 is the base-emitter (or gate-source) bias voltage, and ψ_0 is the initial phase shift.

For the input transistor circuit, the linear first-order differential equation can be given by

$$\omega C_{in} \frac{dv_{in}}{dt} = \frac{v_S - v_{in}}{R_{in}} \tag{5.54}$$

By considering that $i = g_m v_{in}$, where g_m is the device transconductance (assuming it is constant when the device is turned on and is equal to zero when the device is turned off), Eq. (5.54) can be rewritten as

$$\frac{di}{d\omega t} + \frac{i}{\omega\tau_{in}} - \frac{V_0 + V_S \sin(\omega t + \psi_0)}{\omega\tau_{in}} = 0 \tag{5.55}$$

whose general solution can be obtained by

$$i(\omega t) = C_0 \exp\left(-\frac{\omega t}{\omega\tau_{in}}\right) + A_1 \sin(\omega t + \psi_0) + A_2 \cos(\omega t + \psi_0) + A_3 \tag{5.56}$$

where $\tau_{in} = R_{in}C_{in}$.

The coefficients A_1, A_2, and A_3 are defined by substituting Eq. (5.56) into Eq. (5.55) and equating the corresponding components. Then, by setting the boundary conditions $i(0) = i(\pi) = 0$ to determine the remaining unknown coefficient C_0 and bias voltage V_0, we can finally write

$$i(\omega t) = \frac{g_m V_S}{\sqrt{1 + (\omega\tau_{in})^2}} \left[\frac{1 - 2\exp\left(-\frac{\omega t}{\omega\tau_{in}}\right) + \exp\left(-\frac{\pi}{\omega\tau_{in}}\right)}{\exp\left(-\frac{\pi}{\omega\tau_{in}}\right) - 1} \times \sin(\psi - \psi_0) + \sin(\omega t - \psi + \psi_0) \right] \tag{5.57}$$

where $\psi = \tan^{-1}(\omega\tau_{\text{in}})$ is the input phase angle. It should be noted that the collector (or drain) current waveforms can have different characteristics, depending upon the boundary conditions, initial phase shift, and base-emitter (or gate-source) bias voltage. For example, a 50% duty ratio of the input signal is realized with the bias voltage calculated from

$$V_0 = -\frac{V_{\text{S}}}{\sqrt{1 + (\omega\tau_{\text{in}})^2}} \frac{1 + \exp\left(-\dfrac{\pi}{\omega\tau_{\text{in}}}\right)}{1 - \exp\left(-\dfrac{\pi}{\omega\tau_{\text{in}}}\right)} \sin(\psi - \psi_0) \tag{5.58}$$

which can take positive, zero, and negative values when the transistor can be biased for Class-AB, Class-B, or Class-C operation modes, respectively, depending upon its input circuit parameters.

For the sinusoidal input voltage with initial phase $\psi_0 = 30$ degrees shown in Fig. 5.15A, the resulting collector (or drain) current waveforms for several values of the parameter $\omega\tau_{\text{in}}$ are plotted in Fig. 5.15B, from which it follows that generally the collector current waveforms are asymmetrical, and the degree of this asymmetry depends on the input circuit phase angle ψ. In this case, close to symmetrical waveform can be obtained with $\omega\tau_{\text{in}} = 0.6$. At higher frequencies, the waveform asymmetry is shifted to the right-hand side, thus contributing to shorter switching time of the transistor. However, a larger value of $\omega\tau_{\text{in}}$, which is the time delay due to the input RC circuit, contributes to the smaller output current amplitude with an appropriately smaller fundamental-frequency component, resulting in a power gain reduction. The input voltage amplitude V_{in} across the capacitance C_{in} can be defined as a frequency-dependent function by

$$\frac{V_{\text{in}}}{V_{\text{S}}} = \frac{1}{\sqrt{1 + (\omega\tau_{\text{in}})^2}} \tag{5.59}$$

From Eq. (5.59), it follows that, for the same input capacitance C_{in}, the voltage across the capacitance C_{in} reduces with an increase of R_{in} or τ_{in}, thus resulting in a smaller output fundamental current amplitude. For zero input resistance R_{in} when there is no power loss in the transistor input circuit, the power gain becomes infinite. The input power for a nonzero value of R_{in} can be calculated from

$$P_{\text{in}} = \frac{I_{\text{in}}^2 R_{\text{in}}}{2} = \frac{(\omega\tau_{\text{in}})^2}{1 + (\omega\tau_{\text{in}})^2} \frac{V_{\text{S}}^2}{2R_{\text{in}}} \tag{5.60}$$

where I_{in} is the input current amplitude.

Generally, the switching time is sufficiently small. Certainly, for an ideal active device without any memory effects due to intrinsic phase delays, the switching time is equal to zero when the rectangular input drive results in a rectangular output response with the required amplitude, as shown in Fig. 5.16A by rectangular curve 1, where curve 2 corresponds to an ideal Class-E collector current waveform. Such an ideal case assumes zero feedback capacitance and zero input resistance R_{in}. Otherwise, if R_{in} is not equal to zero, the input low-pass $R_{\text{in}}C_{\text{in}}$ filter section provides the suppression of higher-order harmonics of the fundamental frequency, resulting in the finite rise and fall times of the driving rectangular pulse in the time domain. This means that, during this finite on-time and off-time operation conditions, an active device cannot be instantly switched from the saturation mode to the pinch-off mode and operates in the active region when simultaneously output current and output voltage are positive corresponding to the output power dissipation inside the transistor.

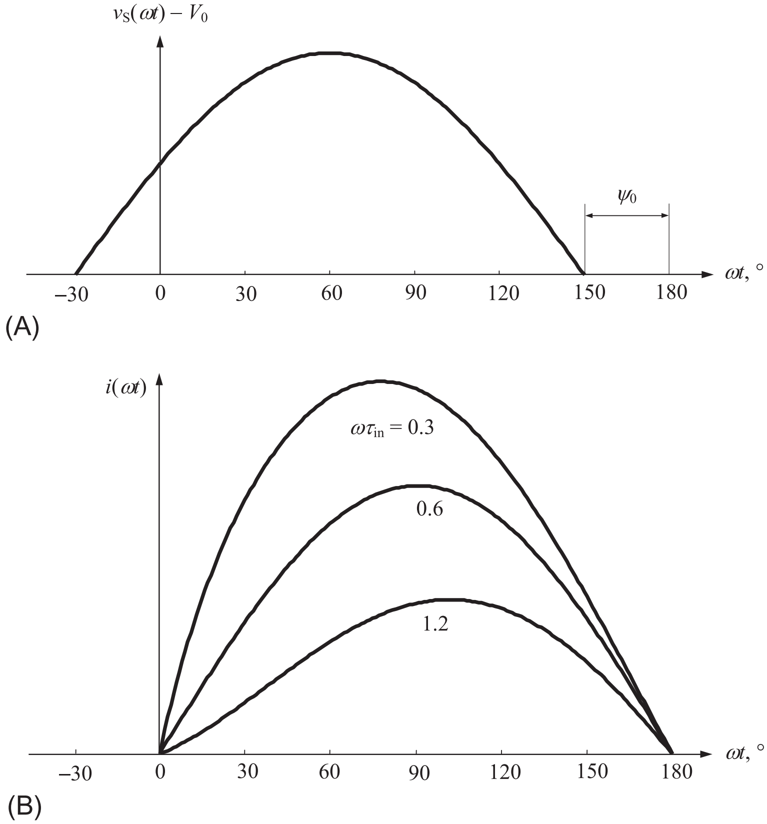

FIG. 5.15

Collector current waveforms versus input parameter $\omega\tau_{in}$.

However, in a real situation, especially at higher frequencies, it is very difficult to realize the driving signal close to the rectangular form because it leads to significant circuit complexity and requires the minimum device input delay (R_{in} should be as small as possible) and transition frequency $f_T = g_m/2\pi C_{in}$ to be as high as possible (C_{in} should be as much smaller as possible). Fortunately, to realize high-efficiency operation conditions, it is sufficient to drive the power amplifier simply with a sinusoidal signal. The finite-time transition from the saturation mode to the pinch-off mode through the device active mode takes place at the point of the intersection of the curve corresponding to the base (or channel) charge process (curve 1) and the curve corresponding to the required ideal collector-current waveform provided by the load network (curve 2), as shown in Fig. 5.16B. To minimize the switching time interval, it is sufficient to slightly overdrive the active device with signal amplitude by 20%–30% higher than is required for a conventional Class-B power amplifier, as shown in Fig. 5.16C. As an alternative, the second-harmonic component (to approximate a half-sinusoidal waveform) or third-harmonic component (to approximate a rectangular waveform with close to trapezoidal waveform) with proper phasing can be added to the input driving signal. In both cases, the overall driving signal

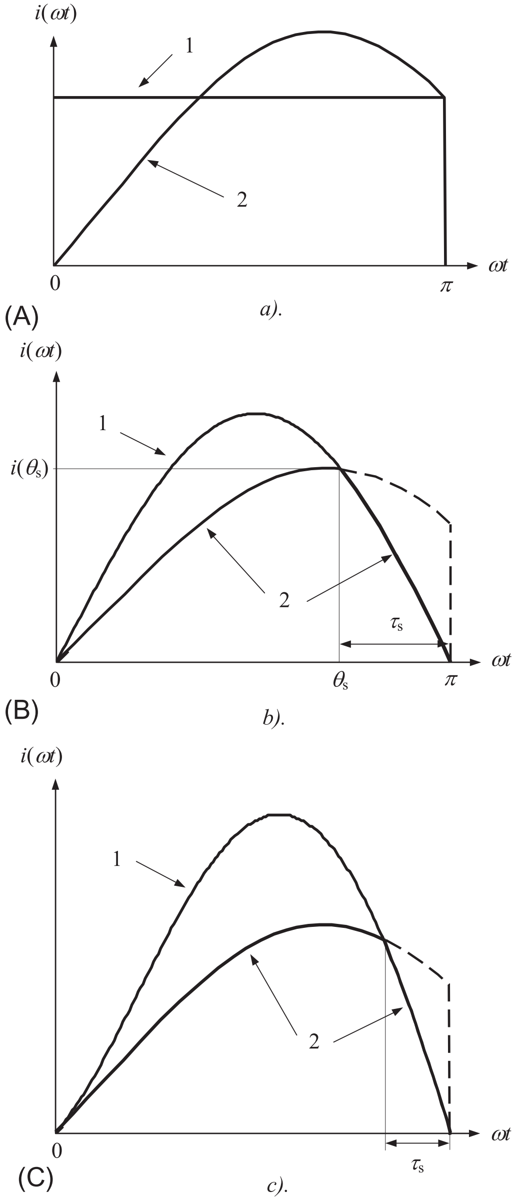

FIG. 5.16

Collector current waveforms due to nonzero values of switching time.

amplitude will be increased when compared with simply sinusoidal driving signal, thus resulting in a faster switching operation time.

The power dissipated during this on-to-off transition can be calculated assuming zero on-resistance as

$$P_{\mathrm{s}} = \frac{1}{2\pi}\int_{\theta_{\mathrm{s}}}^{\pi} i(\omega t)v(\omega t)d\omega t \tag{5.61}$$

where the collector voltage during the transition time $\tau_{\mathrm{s}} = \pi - \theta_{\mathrm{s}}$ is defined by

$$v(\theta_{\mathrm{s}}) = \frac{1}{\omega C}\int_{\theta_{\mathrm{s}}}^{\pi} i_{\mathrm{C}}(\omega t)d\omega t \tag{5.62}$$

The short duration of the switching time and the proper behavior of the resulting collector (or drain) waveform allows us to make an additional assumption of a linearly decreasing collector current during fall time $\tau_{\mathrm{s}} = \pi - \theta_{\mathrm{s}}$, starting at $i(\theta_{\mathrm{s}})$ at time θ_{s} and decaying to zero at time π, which can be written as

$$i(\omega t) = i(\theta_{\mathrm{s}})\left(1 - \frac{\omega t - \theta_{\mathrm{s}}}{\tau_{\mathrm{s}}}\right) \tag{5.63}$$

where $i(\theta_{\mathrm{s}})$ corresponds to the peak collector current shown in Fig. 5.16B.[21, 27] In this case, the capacitor-charging current $i_{\mathrm{C}}(\omega t) = i(\theta_{\mathrm{s}}) - i(\omega t)$, being zero during saturation mode, varies linearly between zero and $i(\theta_{\mathrm{s}})$ during on-to-off transition, according to

$$i_{\mathrm{C}}(\omega t) = i(\theta_{\mathrm{s}})\frac{\omega t - \theta_{\mathrm{s}}}{\tau_{\mathrm{s}}} \tag{5.64}$$

The collector voltage produces a parabolic voltage waveform during the switching interval, according to Eq. (5.62), as

$$v(\omega t) = \frac{i(\theta_{\mathrm{s}})}{2\omega C\tau_{\mathrm{s}}}(\omega t - \theta_{\mathrm{s}})^2 \tag{5.65}$$

As a result, the power dissipated during transition, according to Eq. (5.61), is then

$$P_{\mathrm{s}} = \frac{i^2(\theta_s)\tau_{\mathrm{s}}^2}{48\pi\omega C} \tag{5.66}$$

For an optimum Class-E power amplifier by assuming in view of a short transition time that $i(\theta_{\mathrm{s}}) = i(\pi)$, from Eq. (5.23), it follows that $i(\pi) = 2I_0$; hence

$$P_{\mathrm{s}} = \frac{I_0^2\tau_{\mathrm{s}}^2}{12\pi\omega C} \tag{5.67}$$

By taking into account Eq. (5.35), the switching loss power P_{s} normalized to the DC power P_0 can be obtained by

$$\frac{P_{\mathrm{s}}}{P_0} = \frac{I_0\tau_{\mathrm{s}}^2}{12\pi\omega CV_{\mathrm{cc}}} = \frac{\tau_{\mathrm{s}}^2}{12} \tag{5.68}$$

As a result, the collector efficiency η can be estimated as

$$\eta = 1 - \frac{P_{\mathrm{s}}}{P_0} = 1 - \frac{\tau_{\mathrm{s}}^2}{12} \tag{5.69}$$

As follows from Eq. (5.68), the power losses due to nonzero switching time are sufficiently small and, for example, for $\tau_s = 0.35$ or 20 degrees, they are only about 1%, whereas they are approximately equal to 10% for $\tau_s = 60$ degrees. A more exact analysis assuming a linear variation of the collector current during on-to-off transition results in similar results when efficiency degrades to 97.72% for $\tau_s = 30$ degrees and to 90.76% for $\tau_s = 60$ degrees.[30] Considering an exponential collector current decay rather than linear during the fall time shows the similar result for $\tau_s = 30$ degrees when $\eta = 96.8\%$, but the collector efficiency degrades more significantly at longer fall times when, for example, $\eta = 86.6\%$ for $\tau_s = 60$ degrees.[31]

It should be noted that all these results were obtained for a particular case of the infinite Q_L factor of the series-tuned resonant circuit. However, for the loaded quality factors Q_L having finite and sufficiently small values with the assumption of harmonic distortion in the output signal, the collector efficiency increases by several percent.[32] As a result, in terms of efficiency and linearity, the most desirable range of Q_L is from 5 to 10. In terms of practical implementation, the smaller the gate length of the transistor, the lower the fall-time angles can be expected, and the loaded quality factor becomes of less importance for collector efficiency. For example, by using a 0.6-μm CMOS device, the lower decay time with the drain efficiency greater by about 10% than that when using a 0.8-μm CMOS device can be achieved.[32] Similarly, using a 1.0-μm GaN HEMT device results in an output power of 93 mW and a drain efficiency of 72% at an operating frequency of 1 GHz, whereas a drain efficiency of 82% can be achieved with a 0.12-μm GaN HEMT device.[33]

5.6 Effect of nonlinear shunt capacitance

At high operating frequencies close to the maximum switching frequency $f_{\max}$, the shunt capacitance C required for an ideal switchmode Class-E operation will be fully represented by the output capacitance of the active device. However, the intrinsic output transistor capacitance (collector capacitance of a bipolar device or drain-source capacitance of a field-effect transistor) is generally nonlinear. If its contribution to the overall shunt capacitance is significant, it is necessary to consider the nonlinear nature of this capacitance. Fig. 5.17 shows the equivalent Class-E load network with a nonlinear shunt capacitor C.

The nonlinear capacitance can be represented as a junction capacitance by

$$C(v) = \frac{C_0}{\left(1 + \dfrac{v}{V_{\mathrm{bi}}}\right)^{\gamma}} \tag{5.70}$$

where v is the reverse voltage over the diode junction, V_{bi} is the built-in potential, γ is the junction sensitivity or grading coefficient ($\gamma = 1/3$ for gradient junction and $\gamma = 1/2$ for abrupt junction), and $C_0 = C(0)$ is the collector capacitance at $v = 0$, which can be defined through the supply voltage V_{cc} as

$$C(0) = C(V_{\mathrm{cc}})\left(1 + \frac{V_{\mathrm{cc}}}{V_{\mathrm{bi}}}\right)^{\gamma} \tag{5.71}$$

The nonlinear capacitance has an effect only during the time period when the transistor is turned off. Therefore the collector current during the time period when the transistor is turned on can be

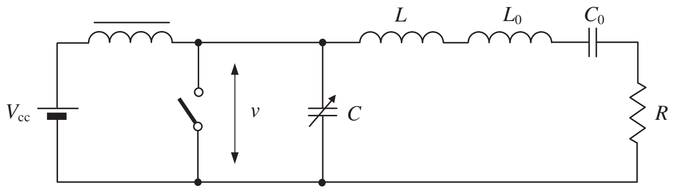

FIG. 5.17

Equivalent Class-E load network with nonlinear shunt capacitor.

determined by Eq. (5.23). Then, the collector voltage because of the current flowing through the nonlinear capacitance

$$i_C(\omega t) = \omega C(v)\frac{dv(\omega t)}{d\omega t} \tag{5.72}$$

can be calculated by substituting Eqs. (5.70) and (5.16) into Eq. (5.72) and integrating of its both parts as

$$\int_0^v \frac{C_0}{\left(1+\frac{v}{V_{bi}}\right)^\gamma} dv = \frac{1}{\omega}\int_\pi^{\omega t} i_C(\omega t)d\omega t \tag{5.73}$$

As a result,

$$\frac{V_{bi}}{1-\gamma}\left[\left(1+\frac{v}{V_{bi}}\right)^{1-\gamma} - 1\right] = \frac{I_0}{\omega C_0}\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{5.74}$$

or

$$v = V_{bi}\left\{\left[\frac{I_0}{\omega C_0}\frac{1-\gamma}{V_{bi}}\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) + 1\right]^{\frac{1}{1-\gamma}} - 1\right\} \tag{5.75}$$

Because the optimum load phase angle, DC current, and output voltage are not affected by the capacitance nonlinearity, Eq. (5.74) can be rewritten using Eq. (5.35) as

$$\frac{V_{bi}}{1-\gamma}\left[1 + \frac{v}{V_{bi}} - \left(1+\frac{v}{V_{bi}}\right)^\gamma\right] = V_{cc}\pi\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{5.76}$$

which represents a nonlinear algebraic equation with respect to the collector voltage $v(\omega t)$ for any type of the device junction.[34] For abrupt diode junction with $\gamma = 0.5$, it can be simplified to the quadratic equation and solved analytically. The optimum small-signal value of the shunt capacitance C_0 can then be calculated from Eq. (5.70) by considering Eqs. (5.32) and (5.33).

Fig. 5.18 shows the difference between the collector voltage waveforms corresponding to the circuits with nonlinear capacitance (curve 1) and linear capacitance (curve 3). The nonlinear nature of this capacitance must be considered when specifying the breakdown voltage of the transistor. For example, the collector voltage waveform will rise in the case of the shunt capacitance described by abrupt diode junction in comparison with the linear capacitance, and its maximum voltage can be greater by about 20% for a 50% duty ratio.[13, 34] However, a stronger nonlinearity of the shunt capacitance causes the

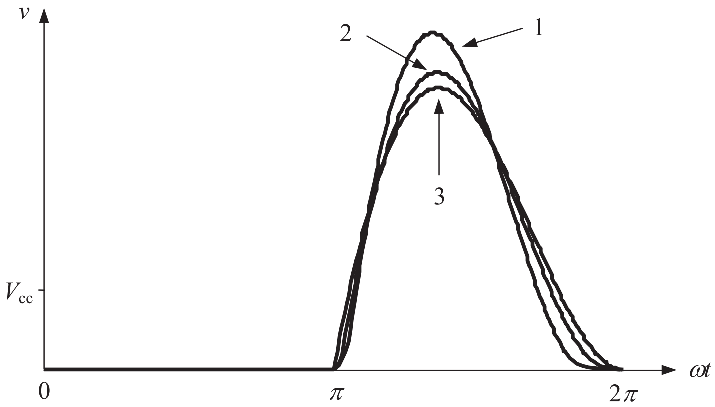

FIG. 5.18

Collector voltage waveforms due to nonlinear shunt capacitance.

peak voltages to be higher.[35] At the same time, the deviations of the optimum load network parameters are insignificant, less than 5% in a wide range of supply voltages. Because the nonlinear capacitance is largest at zero voltage, the collector waveform will rise more slowly than in the linear case. As the collector voltage increases, the capacitance will decrease, and hence the voltage should begin to rise more quickly than in the linear case. If the shunt capacitance consists of both nonlinear and linear capacitances, the collector voltage waveform is intermediate (curve 2) and located between the two extreme cases of entirely nonlinear or entirely linear capacitance.[36] In some cases, when the manufacturer provides the device intrinsic capacitances at specified bias values, the output capacitance can be considered as an equivalent linear shunt capacitance specified at the operating bias point and expressed as a function of the supply voltage.[37, 38] It was found that the Class-E power amplifier with nonlinear shunt capacitance does not achieve zero-voltage-switching operation when the supply voltage is lower than the value designed for an idealized optimum Class-E operation mode, thus resulting in switching power loss and lower power efficiency.[39] The highest power efficiency can be obtained at a lower DC supply voltage than the designed DC supply voltage, even though the circuit was designed to achieve idealized optimum Class-E operation at the designed DC supply voltage.[40]

5.7 Optimum, nominal, and off-nominal Class-E operation

A more detailed theoretical analysis of the time-dependent behavior of the collector voltage and current waveforms shows that, for a finite value of the saturation resistance r_{sat}, the optimum conditions for an idealized Class-E operation mode given by Eqs. (5.9) and (5.10) no longer correspond to the minimum dissipated power losses, and there are optimum nonzero values of the collector voltage and its derivative at switching time instant corresponding to minimum overall power losses.[1, 41] For example, even for small losses with the normalized loss parameter $\omega C r_{\mathrm{sat}} = 0.1$ for a duty ratio of 50%, the optimum series inductance L is almost two times greater, and the optimum shunt capacitance C is about 20% greater than those obtained under optimum conditions given by Eqs. (5.9) and (5.10). However, for collector efficiencies of 90% and greater, both optimum inductance and optimum capacitance differ by less than 20% from their optimum values for $r_{sat} = 0$.[28] It should be noted that, if the first condition is satisfied, then the power losses close to minimum can be achieved with zero second condition because the positive voltage derivative results in a positive current jump, which requires greater driving amplitude, while the negative voltage derivative with a negative current jump demonstrates a reduction in power loss by only 3%.[42] Thus generally, the switching conditions given by Eqs. (5.9) and (5.10) can be considered optimum only for an idealized case of the Class-E load network with zero saturation resistance, providing the switchmode transistor operation when it is operated in only pinch-off and saturation regions. However, they can be considered as a sufficiently accurate initial assumption for further design and optimization of the practical high-efficiency power amplifier circuits.

The term "optimum" for the Class-E conditions given by Eqs. (5.9) and (5.10) means that the voltage across the switch should be equal to zero, and there are no current jumps across the capacitor C (capacitor must be discharged) at the moments when the switch is turned on with further instant transitions from off-state to on-state modes, thus resulting in a maximum achievable collector efficiency. Otherwise, if the current starting to flow through the switch at this moment is not equal to zero, the device cannot be considered an ideal switch because of the appearance of the active operation mode of the device between its pinch-off and saturation modes. In this case, the collector current and voltage waveforms overlap each other, reducing the collector efficiency because of the power dissipation in the device. Therefore it is more proper to call the *optimum conditions* given by Eqs. (5.9) and (5.10) for a lossless operation mode with ideal switch as the *nominal (or idealized optimum) conditions*.

Optimum electrical operation is defined as the operating condition that gives the highest possible drain or collector efficiency at a specified output power and peak switch voltage for a given set of parasitic parameters such as the transistor saturation resistance, turn-off and turn-on switching transition times, and finite quality factors of the load-network inductors and capacitors. In this case, each set of components results in a specific "optimum" off-nominal design. The smaller are the parasitic series resistances, the larger are the parasitic parallel resistances, and the closer is the optimum switch voltage waveform to the nominal waveform. The designer can trade-off among the power dissipations to minimize the total power dissipation at the specified output power and peak switch voltage.

Typically, manual or automatic optimization of the Class-E load-network parameters can reduce the power dissipation of a nominal design by about 30%. As an example, Fig. 5.19 shows the switch (A) voltage and (B) current waveforms for a nominal 13.56-MHz 101-W switchmode Class-E design, providing a drain efficiency of 82.1%. At the same time, Fig. 5.20 shows the switch (A) voltage and (B) current waveforms for an optimized version of that design, achieving a drain efficiency of 86.6% at 102-W output. In that example, the 23-W power dissipation of the nominal design was reduced by 6.4 W (to 16.6 W) in the optimized design. As a result, the 6.4-W reduction of dissipated power represents 28% of the 23-W power dissipated in the nominal design. In this optimized design, as seen from Fig. 5.20A, the drain voltage waveform at the switch turn-on time is slightly positive.

In a nominal (or idealized optimum) Class-E operation, the load network discharges the device output capacitance prior to turn on of the device, producing ideally 100% efficiency. Below the maximum frequency, at which the shunt susceptance required for optimum operation is provided by only the device output capacitance, it is generally possible to adjust the series load reactance to achieve almost 100% efficiency. For example, an optimum operation can be achieved by adding external shunt capacitance to the device output. However, above the maximum frequency, it is impossible to achieve an ideal 100% efficiency by varying the series load network parameters. As the frequency increases,

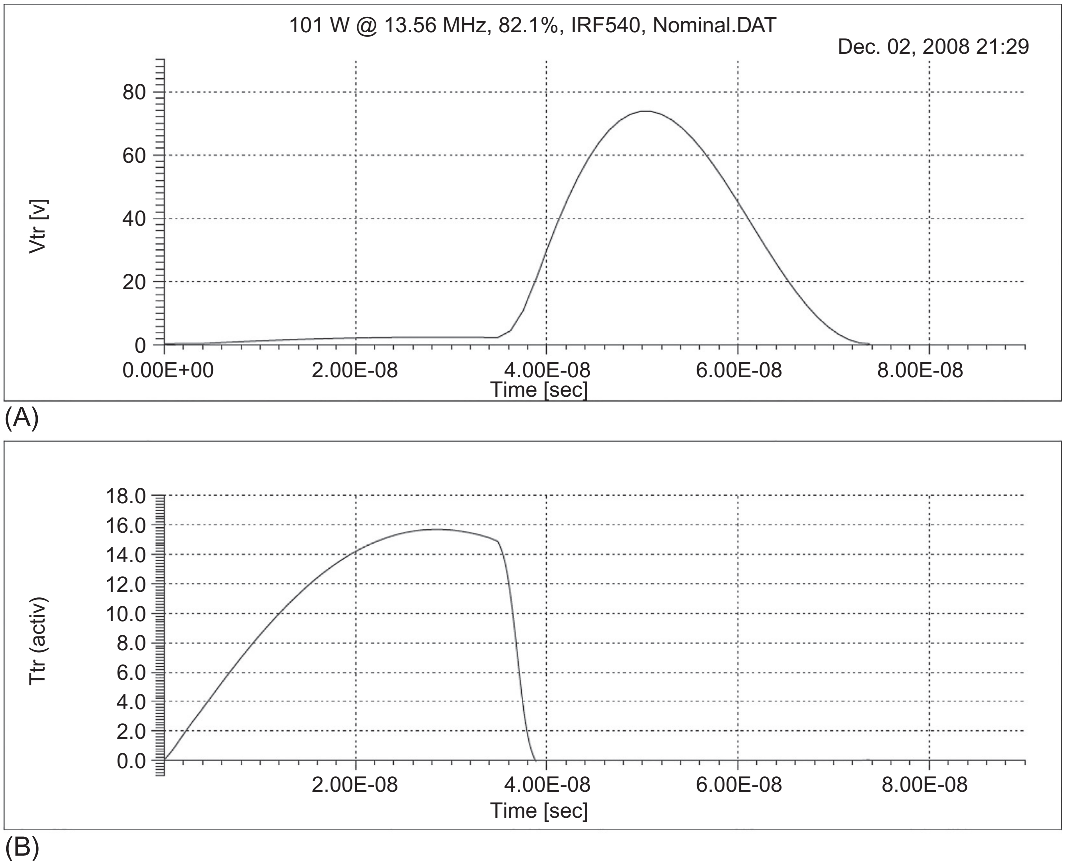

FIG. 5.19

Switching voltage and current waveforms for nominal Class-E operation.

the collector voltage waveform approaches the ramp produced by DC charging of the shunt capacitor. Consequently, the maximum achievable collector (or drain) efficiency decreases as the frequency of operation is increased above the maximum frequency. The maximum possible efficiency $\eta_{\max}$ and the normalized circuit parameter $\omega L/R$ required to produce it, along with the normalized peak voltage $V_{\max}/V_{cc}$ for a fixed supply voltage V_{cc}, are shown in Table 5.3.[43]

From Table 5.3 it follows that, above the maximum frequency, the efficiency can be maximized by a proper selection of the series inductance and load resistance when it looks reasonable. For example, at an operating frequency $f = 2.512 f_{\max}$, the collector efficiency of an ideal Class-E mode remains still high, being even higher than that for a Class-F mode with the control of three collector voltage and three collector current harmonic components. The collector efficiency of an ideal Class-E power amplifier drops at $f = 3.162 f_{\max}$ to 77.87%, which approximately corresponds to the maximum collector efficiency of an ideal Class-B power amplifier of 78.5%.

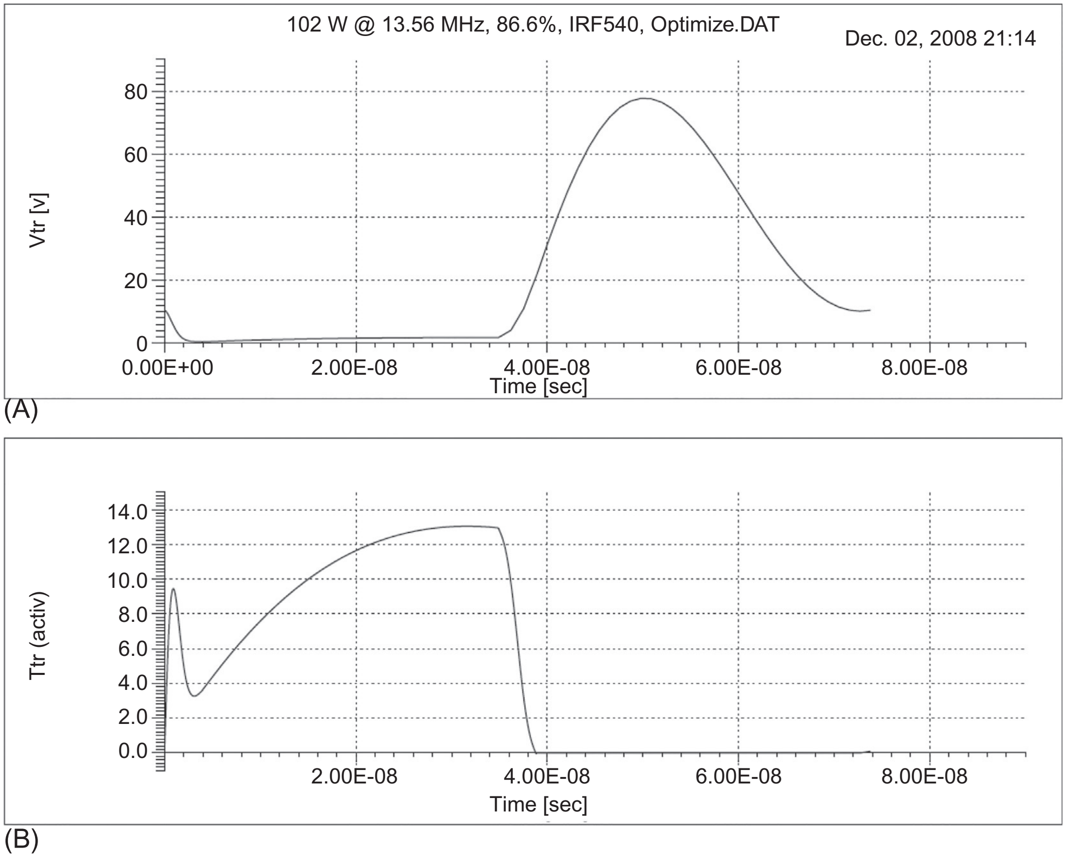

FIG. 5.20

Switching voltage and current waveforms for optimized Class-E operation.

For off-nominal Class-E operation when only zero-voltage switching condition is satisfied, the designer can use a higher shunt capacitance than for nominal operation at the same switching frequency and load resistance.[44] In this case, both peak voltage and current values are higher for off-nominal operation that occurs within $-0.5\pi < \varphi < 0$ for phase angles $\varphi > \varphi_{\text{opt}}$, where φ_{opt} is the optimum phase angle determined by Eq. (5.18) for a nominal Class-E mode at 50% duty ratio. Generally, the peak switch voltage and current values vary with the turn-on switch voltage slope and the duty ratio.[45]

A small load variation has no significant effect on the efficiency of an ideal Class-E power amplifier operated in nominal switching conditions. For example, the efficiency varies gradually, remaining at 95% or more for variations in the load resistance R of +55% to −37% relative to its nominal value.[46] Generally, the minimum efficiency for a given output voltage standing wave ratio (*VSWR*) decreases almost linearly, as shown in Table 5.4.[47] For the usual design requirement of operation with $VSWR \leq 2$, the efficiency is no lower than 89%. However, for some load impedance of any specified *VSWR*, it is possible to achieve the maximum collector efficiency of 100%, which is realized at phase angles of the

Table 5.3 Suboptimum operation above the maximum frequency.

$f/f_{\max}$	$\omega L/R$	$V_{\max}/V_{cc}$	$\eta_{\max}$ (%)
1.000	1.152	3.562	100
1.259	1.330	3.198	99.59
1.585	1.053	2.981	96.96
1.995	0.852	2.789	92.16
2.512	0.691	2.632	85.62
3.162	0.561	2.519	77.87

Table 5.4 Minimum efficiency for different values of *VSWR*.

VSWR	$V_{\max}/V_{cc}$	$\eta_{\max}$ (%)
1.0	3.5621	100
1.5	3.0133	96.00
2.0	2.6814	88.88
2.5	2.4449	81.63
3.0	2.2615	74.99

complex reflection coefficient Γ equal to +65 degrees and −115 degrees. Consequently, the contour of $\eta = 100\%$ on a Smith chart is a straight line. The contours for lower values of efficiency are curved but symmetrical about the contour of $\eta = 100\%$. These results are very helpful in practical implementation. Because 100% efficiency can be achieved along a line that goes through the center of the Smith chart, a single tuning element is generally sufficient to transform any specified load impedance into an impedance on the line corresponding to $\eta = 100\%$. The specified output power can then be obtained by adjusting the DC supply voltage V_{cc} but not exceeding the safe V_{cc}.

5.8 Push-pull operation mode

The push-pull power amplifier configuration offers a possibility of combining powers from two linear power amplifiers to obtain a larger overall output power. The switchmode power amplifiers can also be configured to operate in a push-pull mode. The simplest way is to use a push-pull power amplifier with resistive load by adding either a series or a parallel *LC* circuit. In a push-pull power amplifier shown in Fig. 5.21A, the rectangular pulses of voltage $V_{cc} \pm V_{cc}$ drive the series resonant *LC* circuit, resulting in a switchmode power amplifier with switching voltage. In a push-pull power amplifier shown in Fig. 5.21B, the rectangular pulses of current $I_0 \pm I_0$ drive the parallel resonant *LC* circuit, resulting in a switchmode power amplifier with switching current.

With high-Q_L resonant circuits tuned to the fundamental frequency, these power amplifiers operate as the switchmode Class-D power amplifiers with a sinusoidal load current. However, when low-Q_L resonant *LC* circuit shown in Fig. 5.21B is mistuned to the frequency of about $1.5f_0$, where f_0 is the fundamental frequency, the collector voltage waveform will represent the typical Class-E collector

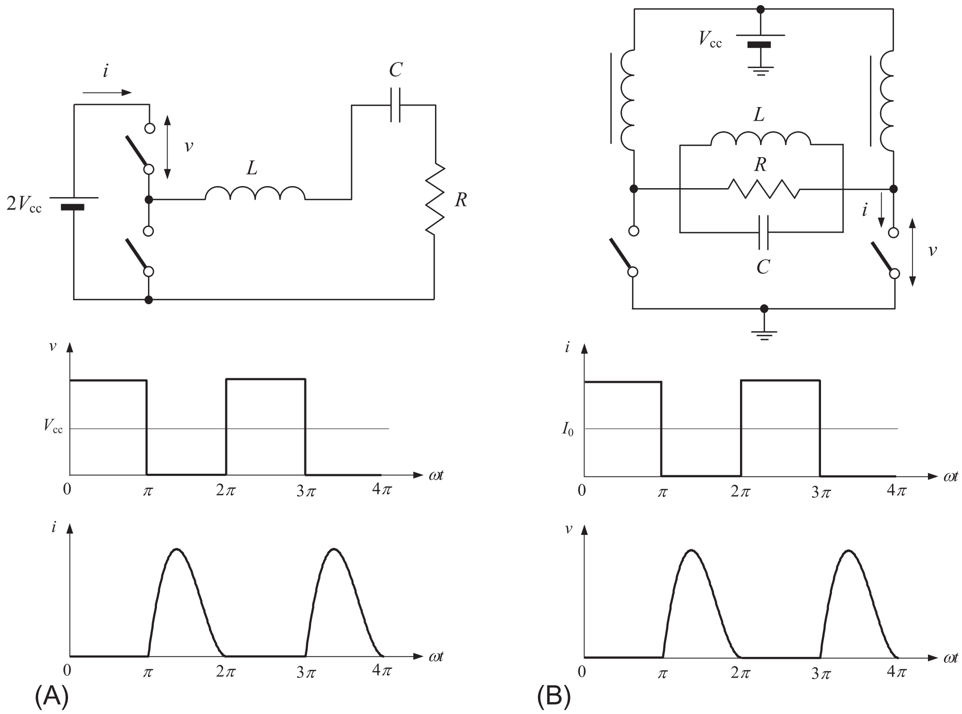

FIG. 5.21

Basic circuits of push-pull switchmode power amplifiers.

waveform with zero-voltage and zero-voltage-derivative nominal conditions.[28] In this case, the load current will not contain the even harmonics of the fundamental frequency. However, to provide a purely sinusoidal load current, the remaining third- and higher-order harmonic components can be eliminated by using an additional high-Q_L filter tuned to the fundamental frequency.

Fig. 5.22 shows the push-pull configuration of an optimally tuned Class-E power amplifier with a series-resonant filter representing an open-circuit for harmonic components of the fundamental frequency, where the input transformer provides the device driving signals with opposite phases.[17, 48] Each device, however, operates as if it were a single-ended Class-E power amplifier. When a given transistor is driven on, it provides a ground connection on the primary winding of the output transformer, causing the DC current and transformed sinusoidal output current to charge the capacitor shunting the other transistor. The DC power is supplied to the switching devices through the center tap of the primary winding of the output transformer. The voltage appearing on the secondary winding of the output transformer contains both positive and negative Class-E collector voltage waveforms. Consequently, it has a fundamental-frequency component that has twice the amplitude of the fundamental-frequency component of either collector waveform. The resulting impedance seen by either half of the power amplifier looking into primary winding of the output transformer depends on the squared ratio between the number of turns of the primary winding and the secondary winding. The sinusoidal load voltage will be shifted relative to the collector voltage by the same phase as for the case of a single-ended Class-E power amplifier.

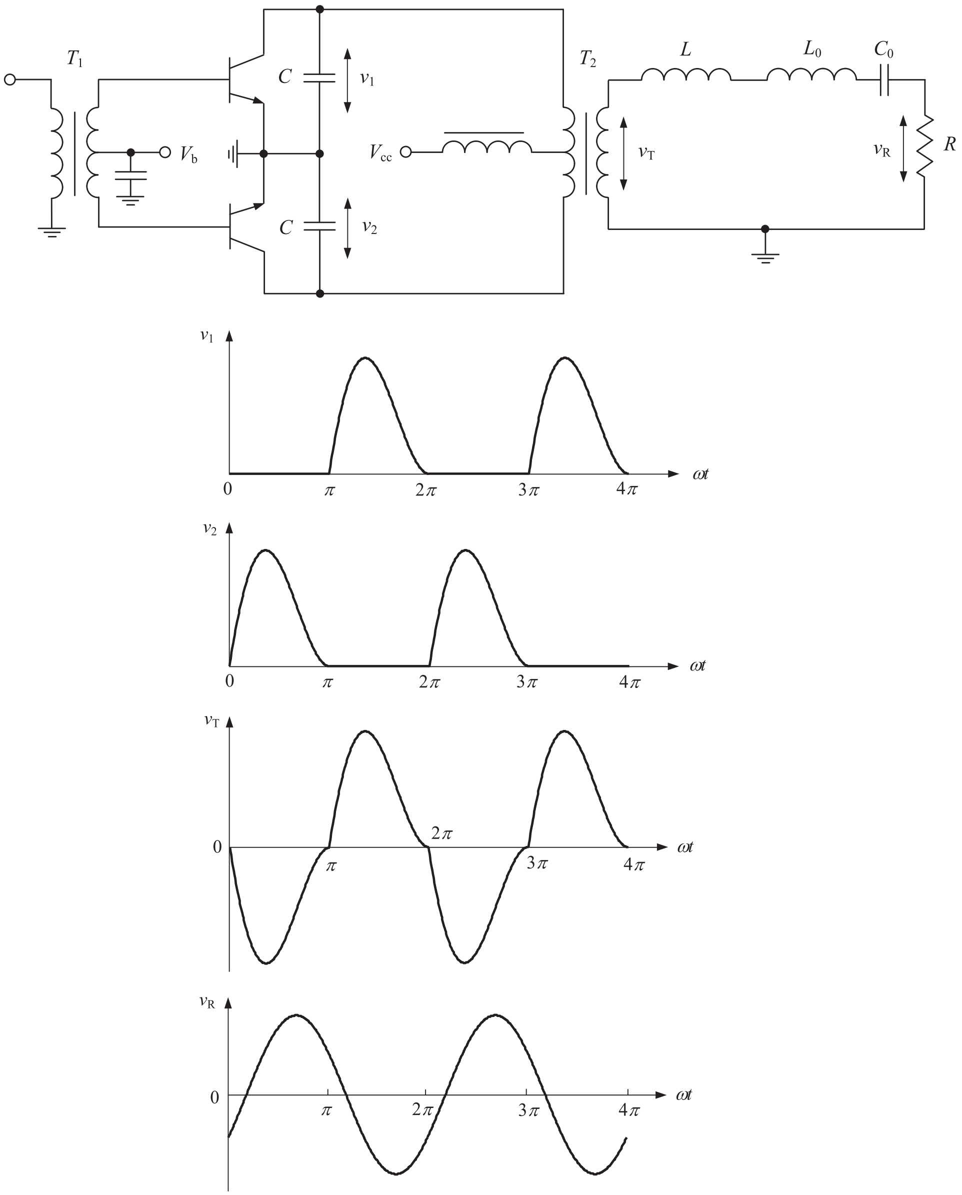
T_1
V_b
C
v_1
C
v_2
V_{cc}
T_2
L
L_0
C_0
v_T
v_R
R
v_1
v_2
v_T
v_R
0
π
2π
3π
4π
ωt

FIG. 5.22

Basic concept of transformer-coupled Class-E push-pull operation.

The push-pull Class-E power amplifier can be designed based on a balanced circuit topology with symmetrical Class-E load networks with shunt capacitances, connected to a common load. Fig. 5.23A shows the bipolar push-pull Class-E power amplifier with a series load resistor.[49] Here, both bipolar transistors operate as switches with opposite 180 degrees phases to each other when the even harmonics can be significantly suppressed in the load resistor. To provide the transition from a balanced load to an unbalanced load, an additional transformer or balanced to unbalanced (balun) can be used. Being designed to operate at a carrier frequency of 100 kHz with a 50% duty ratio, such a push-pull bipolar Class-E power amplifier achieved a *PAE* of 82.2% with an output power of 1.89 W at a supply voltage of 5 V.

A symmetrically driven push-pull Class-E power amplifier using high-power MOSFET devices is shown in Fig. 5.23B.[50] In this circuit, the load resistor is connected in parallel to the series capacitor. For a symmetrically driven Class-E power amplifier, the switches are driven on and off within each of the half-operating period. The duty ratio of the switches is adjusted to realize zero-voltage and zero-voltage-derivative nominal conditions. However, the nominal Class-E operation mode can be maintained only for relatively low loaded quality factors below 2, which is a design constraint for this symmetrically driven push-pull Class-E power amplifier. Although the use of low Q_L-factors has an advantage of low component stress, the harmonic content of the output signal may be significant. As a result, the measured drain efficiency of about 85% with a Q_L-factor of 1.9 was achieved within the ranges of output power from 30 to 150 W and supply voltages from 15 to 32 V at a switching frequency of about 1 MHz. Note that, in view of nonzero device saturation voltage, the zero-voltage and zero-voltage-derivative conditions are no longer optimum to provide maximum operating efficiency.

At microwave frequencies, push-pull Class-E power amplifiers can be designed by using transmission-line power dividers and combiners. Fig. 5.24A shows the circuit schematic of a monolithic *X*-band push-pull pHEMT power amplifier, including an input power divider and an output power combiner based on slotlines and coplanar waveguides.[51] The input balun separates the input signal into two differential signals that are 180 degrees out-of-phase, while the output balun is reverse-oriented to the input one. The input and output matching circuits consist of the series coplanar waveguides providing inductive impedances and shunt coplanar waveguides providing capacitive reactances at the fundamental frequency. The Class-E load network, which is followed by the output matching circuit, includes the internal device shunt capacitance and part of the series coplanar waveguide. The input transmission-line balun shown in Fig. 5.24B provides first the balanced-to-unbalanced signal transformation by transition from the waveguide coplanar with left open-circuit end to slotline, then followed by the slotline T-junction, and finally connected to two differential paths based on the coplanar waveguides with open-circuit terminations at each of their ends. An *X*-band power amplifier based on these baluns with broadband performance and compact size and pHEMT transistors with gate geometry of 0.3 μm × 600 μm can achieve a *PAE* close to 60% in a frequency band of 9–10 GHz with output powers of several hundred milliwatts.

5.9 Load networks with transmission lines

At ultrahigh and microwave frequencies, different types of transmission lines are often preferred over lumped inductors because of the convenience of their practical implementation, more predictable performance, less insertion loss, and less effect of the parasitic elements. For example, the matching circuit

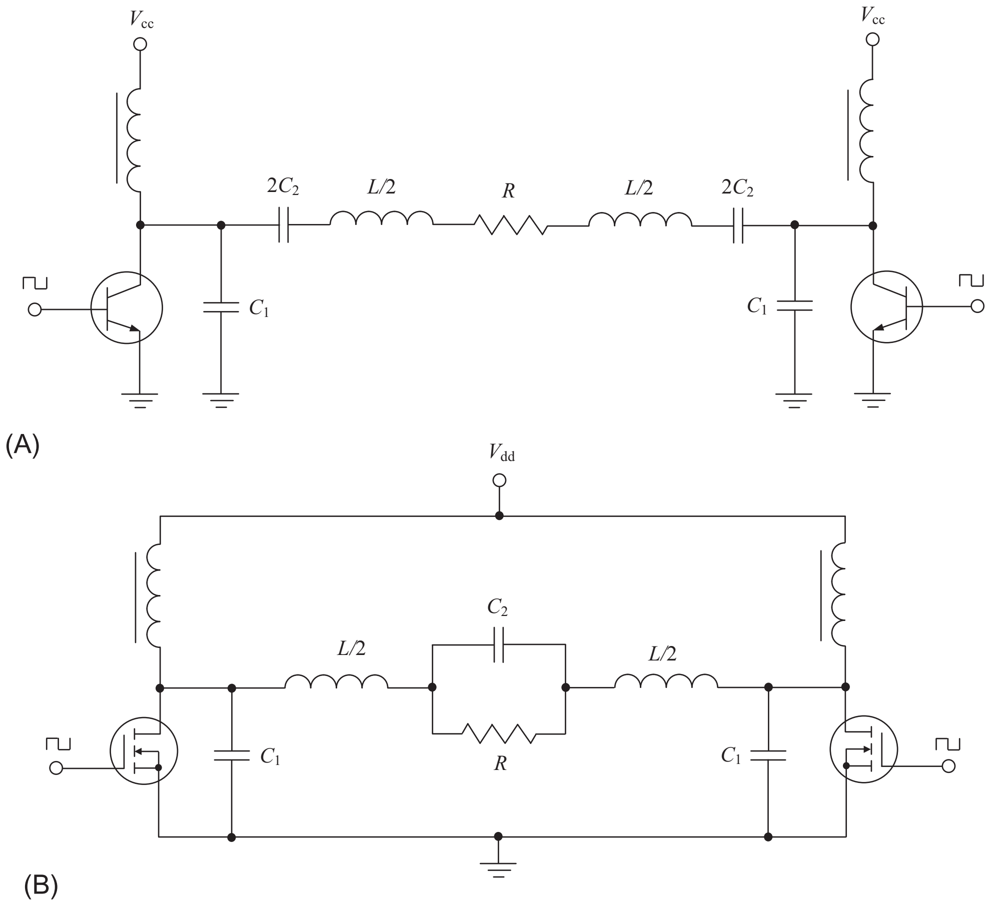

FIG. 5.23

Symmetrically driven push-pull Class-E power amplifiers.

can be composed with any types of transmission lines, including open-circuit or short-circuit stubs to provide the required matching and harmonic suppression conditions. In this case, to approximate the idealized Class-E operation mode of the microwave power amplifier, it is necessary to design the transmission-line load network satisfying the required idealized optimum impedances at the fundamental-frequency and harmonic components. Generally, the device output capacitance can represent the required shunt capacitance, the nominal (or idealized optimum) Class-E value of which is defined by Eq. (5.32). Consequently, the main challenge is to satisfy simultaneously the idealized optimum requirements at the fundamental-frequency impedance $Z_L(\omega_0)$ shown in Fig. 5.25A and harmonic component impedances $Z_L(n\omega_0)$ shown in Fig. 5.25B, which are expressed by using Eq. (5.31) at the fundamental frequency f_0 as

$$Z_L(\omega_0) = R + j\omega L = R\left(1 + j\frac{\omega L}{R}\right) = R\,(1 + j\tan 49.052^\circ) \tag{5.77}$$

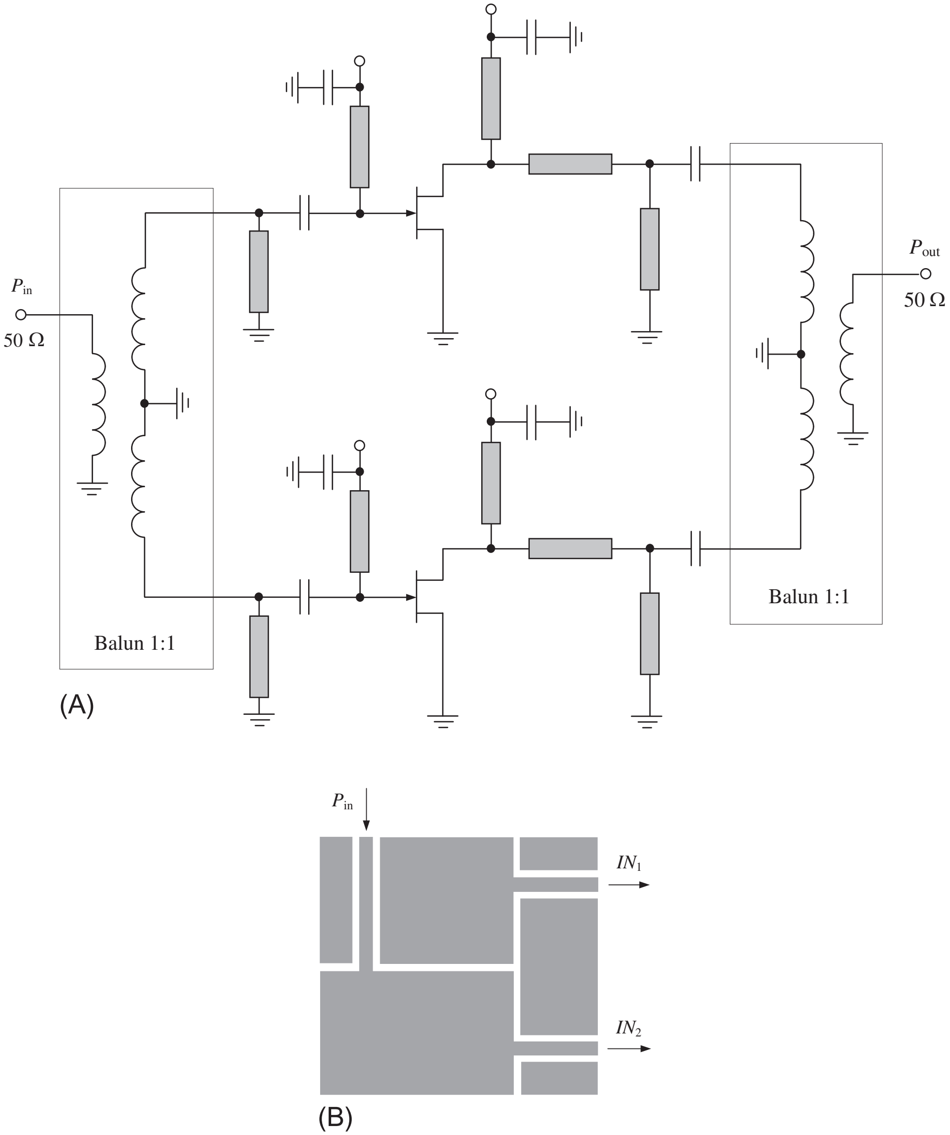
P_{in}
50 Ω
Balun 1:1
(A)
P_{out}
50 Ω
Balun 1:1
P_{in}
IN_1
IN_2
(B)

FIG. 5.24

Microwave push-pull Class-E power amplifier.

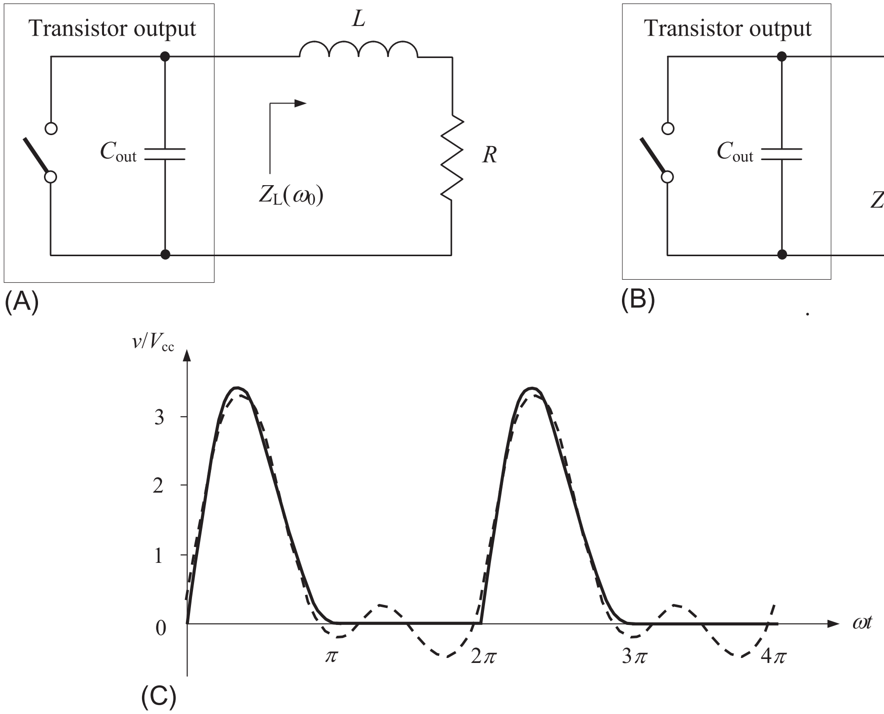

FIG. 5.25

Optimum load impedance and two-harmonic Class-E voltage waveform.

and at the harmonic components nf_0, where $n = 2, 3, \ldots, \infty$, as

$$Z_L(n\omega_0) = \infty \tag{5.78}$$

Generally, it is practically impossible to realize these conditions for an infinite number of harmonic components by using only transmission lines. However, as it turned out from the Fourier series analysis, a good approximation to Class-E mode may be obtained with the DC, fundamental-frequency, and second-harmonic components of the voltage waveform across the switch.[52, 53] In this case, the drain efficiency will be the same as in a maximum-efficiency Class-F mode with second-harmonic control.[54] Fig. 5.25C shows the collector (or drain) voltage waveform containing these two harmonic components (dashed line) plotted along with an ideal voltage waveform (solid line). In practical implementation, the two-harmonic Class-E load network designed for microwave applications will include a series microstrip line l_1 and an open-circuit stub l_2, as shown in Fig. 5.26A. The electrical lengths of microstrip lines l_1 and l_2 are chosen to be of about 45 degrees at the fundamental frequency to provide an open-circuit condition seen by the device output at the second harmonic, according to Eq. (5.78). Their characteristic impedances are calculated to satisfy the required inductive-impedance condition at the fundamental frequency given by Eq. (5.77). In the case of a packaged active device, its output bondwire and lead inductance can be accounted for by shortening the length l_1.

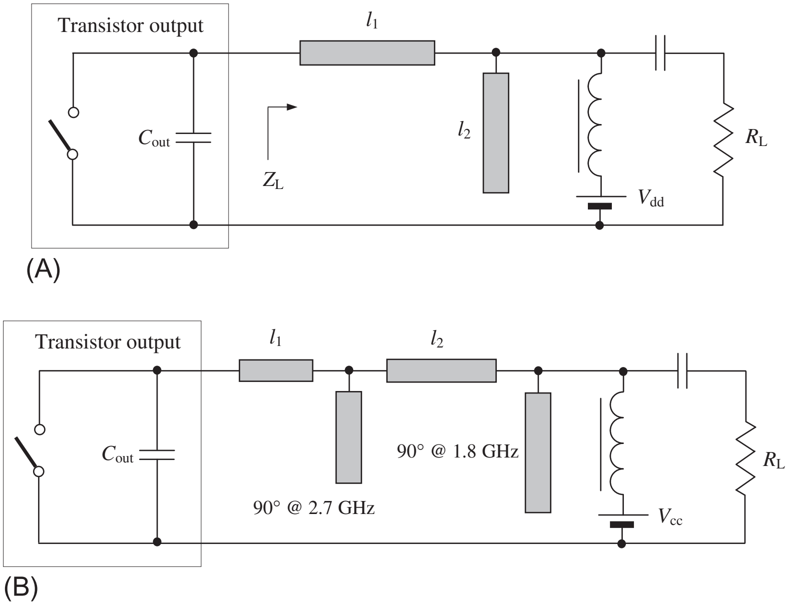

FIG. 5.26

Equivalent circuits of Class-E power amplifiers with transmission lines.

In some cases, a value of the device output capacitance exceeds the required nominal value for a Class-E mode with shunt capacitance. In this situation, it is possible to approximate Class-E mode with high efficiency by setting a properly optimized load at the fundamental frequency and strongly reactive load at the second-harmonic and third-harmonic components.[55] Such a harmonic control network consists of open-circuit quarterwave stubs at the second- and third-harmonic components separately, as shown in Fig. 5.26B, where the third-harmonic quarterwave stub is located before the second-harmonic quarterwave stub. As a result, a very high collector efficiency can be achieved even with values of the device output capacitance higher than it is conventionally required, but at the expense of lower output power, keeping the load at the second and third harmonics strictly inductive. Maximum collector efficiency over 90% with an output power of 1.5 W for the test power amplifier using a commercial bipolar transistor MRF557 was measured at a carrier frequency of 900 MHz. The second-harmonic open-circuit stub can be replaced by a $\lambda/4$-long shortened (by the decoupling capacitor) stub, which is a half-wave long at $2f_0$, used to bias the transistor.[56]

An analysis of a nominal Class-E mode in the frequency domain shows that the combined effect of the saturation resistance r_{sat} and second-harmonic loading is characterized by a shift of the idealized optimum-load fundamental-frequency impedance.[57] Besides, parasitic effects due to packaging and microstrip junction discontinuities may upset the transmission-line open-circuit requirement. Therefore it is practically important to predict the power amplifier performance due to nonideal harmonic terminations. For example, the voltage peak factor increases when the second-harmonic load varies from capacitive to inductive, and excessive current flow can be realized under capacitive load reactance. In this case, to achieve an optimum switchmode Class-E operation mode, the maximum collector efficiency with lower output power is obtained for negative collector voltage-derivative condition.[58] Generally, higher efficiency is achieved for open-circuit terminations of the second- through fifth-harmonic components, with up to 5% efficiency degradation when the loading configurations for odd harmonics are modified from open-circuit to short-circuit termination across 9–11 GHz.[59] The variation of the second-harmonic load reflection coefficient by 10% in magnitude from 1 to 0.9 and ±20 degrees in phase angle results in an insignificant efficiency variation of only 1%.

The resultant transmission-line topology of the Class-E load network, including the matching properties as well, can be designed based on a lumped circuit prototype.[60] The design procedure includes the following steps:

1. Calculation of the optimum Class-E load network parameters (shunt capacitance C, series inductance L, and load resistance R) based on the specified supply voltage V_{cc} and power delivered to the load P_{L}.
2. Design of the lumped-element circuit to match the nominal (or optimized) load resistance R with standard load resistance of 50 Ω at the fundamental frequency, with corresponding harmonic suppression.
3. Transformation of the lumped-element circuit into its transmission-line circuit equivalent, carefully observing the impedances at the higher harmonics.
4. Circuit simulation to validate its operation and component parameters to obtain Class-E approximation.
5. Transformation of the transmission-line equivalent circuit into a distributed microstrip layout.

Fig. 5.27A shows the lumped-element Class-E load network with impedance transformation for a 1-GHz power amplifier delivering 1 W into a 50-Ω load. It is assumed that the MESFET device has a saturation resistance of 1 Ω and output shunt capacitance of around 2 pF. Considering the drain breakdown voltage of 15 V, the maximum supply voltage would be limited to $V_{\max} = 15/3.562 = 4.2\,\mathrm{V}$, according to Eq. (5.27). In this case, to achieve an output power of 1 W, an ideal value of $R = 0.5768 \times (4.2)^2 = 10\,\Omega$ is required, according to Eq. (5.33). The inductive reactance $X = \omega L = 11.5\,\Omega$ is chosen to provide a load phase angle of 49.052 degrees.[17] The required load-network shunt capacitance is $C = 0.1836/(2\pi \times 10) = 2.92\,\mathrm{pF}$, according to Eq. (5.32). To achieve the required impedance transformation from 10 to 50 Ω and to provide a sufficient harmonic suppression in the load, a two-stage cascaded low-pass L-type transformer was chosen, where the first L-section transforms from 10 to 22 Ω and the second L-section transforms from 22 to 50 Ω.

The conversion of the lumped-element circuit involves replacing the series inductors and shunt capacitors with equivalent transmission-line elements. The series inductors can be realized by high-impedance transmission-line short sections with electrical length of $\theta \le \lambda/8$, calculated from equivalent equation $\omega L = Z_0 \tan\theta$, where Z_0 is the characteristic impedance of the line, while shunt capacitances are replaced by low-impedance open-circuit stubs with electrical length of $\theta \le \lambda/8$, calculated from equivalent equation $\omega C = \tan\theta / Z_0$.[23] The electrical parameters of the capacitive stubs (characteristic impedance and electrical length) can be optimized to provide simultaneously the correct reactance at the fundamental frequency f_0 and enhanced suppression of harmonics, reaching the load by arranging the stub lengths to have low input impedance at selected harmonics, that is, short-circuiting these harmonics to ground. This is achieved by choosing the stub length such that its electrical length is exactly 90 degrees at the particular harmonic component that one would like to suppress. The characteristic impedance of the stub is then chosen to provide the desired capacitive reactance at the fundamental frequency.

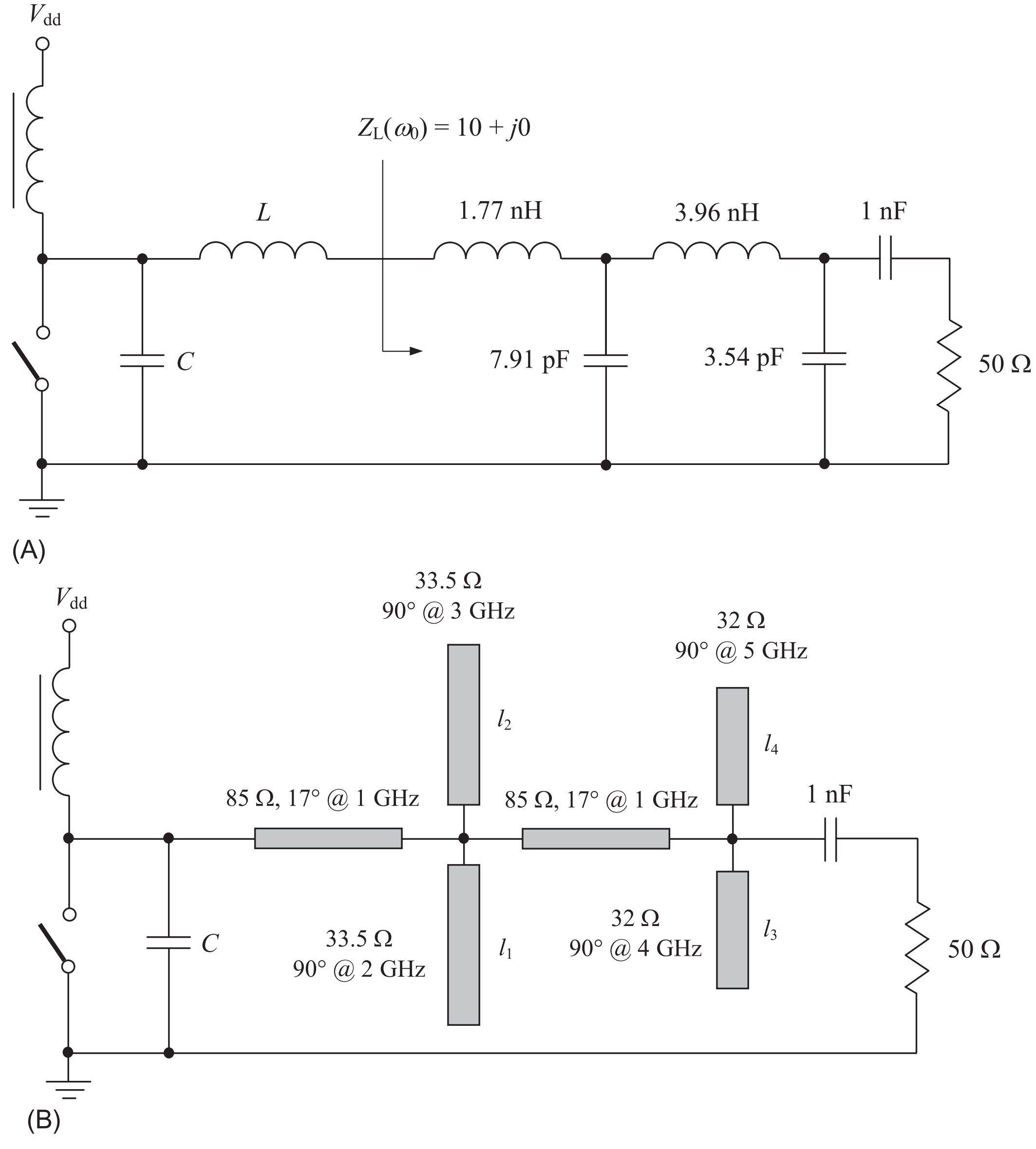
V_{dd}
$Z_L(\omega_0) = 10 + j0$
L
1.77 nH
3.96 nH
1 nF
C
7.91 pF
3.54 pF
50 Ω
(A)
V_{dd}
33.5 Ω
90° @ 3 GHz
32 Ω
90° @ 5 GHz
l_2
l_4
85 Ω, 17° @ 1 GHz
85 Ω, 17° @ 1 GHz
1 nF
C
33.5 Ω
90° @ 2 GHz
l_1
32 Ω
90° @ 4 GHz
l_3
50 Ω
(B)

FIG. 5.27

Equivalent circuits of (A) lumped-element and (B) transmission-line Class-E load networks.

Fig. 5.27B shows the resultant transmission-line topology of a 1-GHz Class-E power amplifier where each shunt capacitor is replaced by two parallel open-circuit stubs, providing the harmonic suppression at four frequencies.[60] The capacitive stubs were chosen to have an electrical length of 90 degrees at frequencies $2f_0$, $3f_0$, $4f_0$, and $5f_0$. Table 5.5 lists the first three frequencies suppressed by each of the four harmonic stubs. By using the printed circuit board (PCB) with a relative dielectric permittivity of 2.2, a loss tangent of 0.009 at 10 GHz, and substrate thickness of 0.381 mm for microstrip realization of this Class-E load network, a drain efficiency of 72% at 950 MHz with an output power of 458 mW and a harmonic suppression of greater than 40 dB at a drain supply voltage of 3.53 V were achieved. The equivalent output capacitance of the used MESFET device ATF8140 was approximately 2.5 pF, which is 0.6 pF less than the required switch capacitance of 3.1 pF. An additional 0.6 pF capacitance was made up of two short capacitive stubs attached at the point where the device drain is connected to the load network. To simplify the overall design procedure of a highly efficient MMIC power amplifier at *K*-band, the load network may contain only two capacitive stubs to provide the reactance required for the fundamental load transformation and low impedances at selected second and third harmonics by making the electrical lengths of these stubs exactly one quarter wavelength at a particular harmonic.[61]

For a packaged high-power transistor with large output capacitance, additionally, a series capacitor can be used to compensate for the package parasitic inductance followed by the shunt short-circuited transmission line, which is required to compensate for excessive device output capacitance.[62] In this case, a *PAE* of 73.6% and a power gain of 14.8 dB were measured at an output power of 39.1 dBm for a 1-GHz LDMOSFET Class-E power amplifier using MRF282 device biased with a gate voltage of 3.2 V and a drain voltage of 21.4 V. The peak *PAE* of 79.2% and drain efficiency of 80.4% with a power gain of 18.1 dB are achieved at an output power of more than 41.1 dBm for a 1-GHz GaN HEMT Class-E power amplifier using a compensating circuit with series capacitor and shunt inductor followed by a harmonic-control network with quarterwave open-circuit stubs for the second to fifth harmonics.[63]

Fig. 5.28 shows the circuit schematic of a 25-V GaN HEMT Class-E power amplifier designed for WCDMA applications at 2.14 GHz.[64] Here, the series capacitor C_c and shunt inductor L_c are used to compensate for parasitic components of bonding inductance L_{out} and output capacitance C_{out}. The harmonic-control load network suppresses all harmonic power levels below −60 dBc for the whole output power range. As a result, the peak *PAE* of 70% with a power gain of 13 dB was achieved at an output power of 43 dBm. The broadband performance with a power gain over 12 dB and a *PAE* over 60% is maintained through 200 MHz. Using the LDMOSFET device in this Class-E design results in a *PAE* of 62.5% with a power gain of 13.8 dB at an output power of 39.8 dBm.[65]

The transmission-line Class-E load network shown in Fig. 5.26B can be modified in order to obtain simple analytical equations to explicitly define the transmission-line parameters.[66] Such a modified transmission-line Class-E load network is shown in Fig. 5.29, where the combined series quarterwave

Table 5.5 First three frequencies suppressed by each of the four harmonic stubs.

Harmonic stub	Suppressed frequency		
l_1	$2f_0$	$6f_0$	$10f_0$
l_2	$3f_0$	$9f_0$	$15f_0$
l_3	$4f_0$	$12f_0$	$20f_0$
l_4	$5f_0$	$15f_0$	$25f_0$

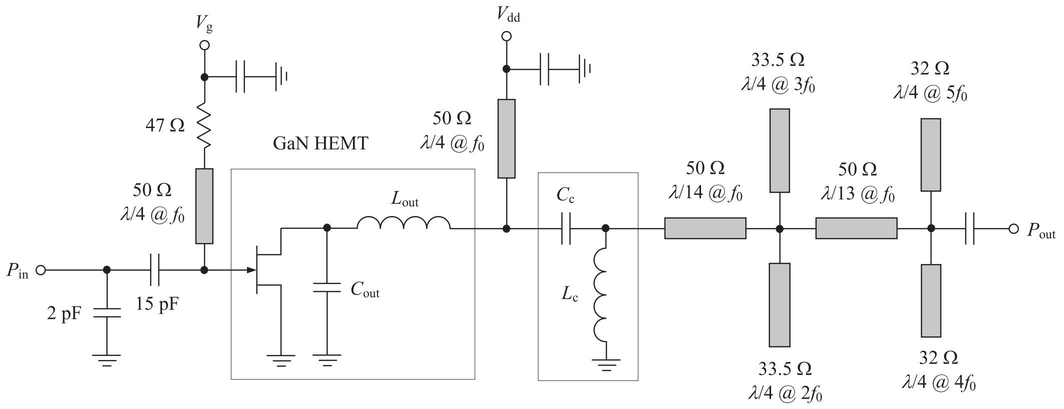
V_g
V_{dd}
47 Ω
50 Ω
λ/4 @ f_0
GaN HEMT
50 Ω
λ/4 @ f_0
L_{out}
C_c
50 Ω
λ/14 @ f_0
33.5 Ω
λ/4 @ 3f_0
50 Ω
λ/13 @ f_0
32 Ω
λ/4 @ 5f_0
P_{out}
P_{in}
2 pF
15 pF
C_{out}
L_c
33.5 Ω
λ/4 @ 2f_0
32 Ω
λ/4 @ 4f_0

FIG. 5.28

Circuit schematic of high-efficiency Class-E GaN HEMT power amplifier for WCDMA applications.

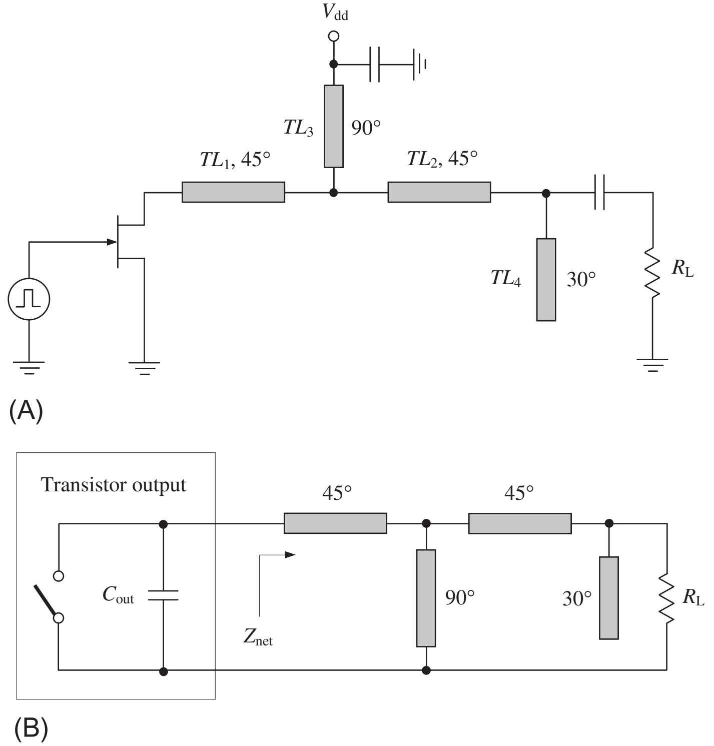
V_{dd}
TL_3
90°
TL_1, 45°
TL_2, 45°
TL_4
30°
R_L
(A)
Transistor output
45°
45°
C_{out}
Z_{net}
90°
30°
R_L
(B)

FIG. 5.29

Modified transmission-line Class-E power amplifier.

transmission line provides an impedance transformation at the fundamental frequency, and the RF grounded quarterwave line and open-circuit stub with an electrical length of 30 degrees create the open-circuit conditions seen from the device output at the second and third harmonics, respectively.

Fig. 5.30A shows the load network seen from the transistor output at the fundamental frequency. Here, the combined quarter-wavelength series transmission line $TL_1 + TL_2$, together with an open-circuit capacitive stub TL_4 having an electrical length of 30 degrees, provides simultaneously the required inductive reactance and impedance transformation of the nominal or optimized Class-E load resistance R to the standard load resistance R_L by proper choice of the transmission-line characteristic impedances Z_1 and Z_2.

The capacitive load impedance Z_L provided by the load resistance R_L and capacitive stub TL_4 can be written at the fundamental frequency as

$$Z_L = \frac{Z_2 R_L}{Z_2 + jR_L \tan 30^\circ} \tag{5.79}$$

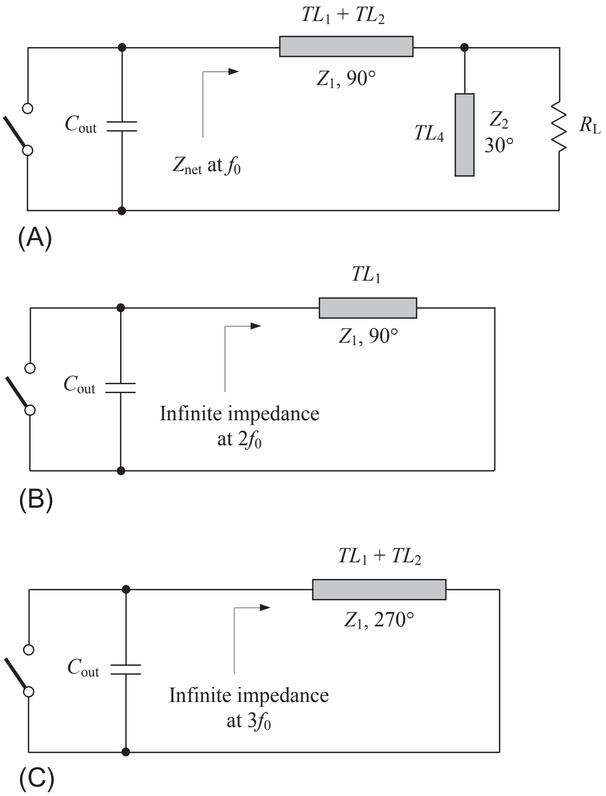
$TL_1 + TL_2$
Z_1, 90°
C_{out}
Z_{net} at f_0
TL_4
Z_2
30°
R_L
(A)
TL_1
Z_1, 90°
C_{out}
Infinite impedance
at $2f_0$
(B)
$TL_1 + TL_2$
Z_1, 270°
C_{out}
Infinite impedance
at $3f_0$
(C)

FIG. 5.30

Load networks seen by the device output at harmonics.

where Z_2 is the characteristic impedance of a 30-degrees open-circuit stub. Generally, the input impedance of the loaded transmission line can be written as

$$Z_{\mathrm{net}} = Z_1 \frac{Z_{\mathrm{L}} + jZ_1 \tan\theta}{Z_1 + jZ_{\mathrm{L}} \tan\theta} \tag{5.80}$$

where θ is the electrical length of the transmission line. Then, substituting Eq. (5.79) into Eq. (5.80) for $\theta = 90$ degrees results in an inductive input impedance

$$Z_{\mathrm{net}} = \frac{Z_1^2}{Z_{\mathrm{L}}} = \frac{Z_1^2}{Z_2 R_{\mathrm{L}}}(Z_2 + jR_{\mathrm{L}} \tan 30^{\mathrm{o}}) \tag{5.81}$$

when the required nominal or optimized Class-E resistance can be provided by proper choice of the characteristic impedance Z_1, while the required optimum Class-E inductive reactance can be achieved with the corresponding value of the characteristic impedance Z_2.

Separating Eq. (5.81) into real and imaginary parts results in the following system of two equations with two unknown parameters:

$$\mathrm{Re}Z_{\mathrm{net}} = \frac{Z_1^2}{R_{\mathrm{L}}} \tag{5.82}$$

$$\mathrm{Im}Z_{\mathrm{net}} = \frac{Z_1^2}{\sqrt{3}Z_2} \tag{5.83}$$

which allow direct calculation of the characteristic impedances Z_1 and Z_2. As a result, by using Eq. (5.77),

$$Z_1 = \sqrt{R_{\mathrm{L}} R} \tag{5.84}$$

$$Z_2 = 0.5R_{\mathrm{L}} \tag{5.85}$$

where $R_{\mathrm{L}} = 50\,\Omega$ and R is calculated from Eq. (5.33).

The transmission-line Class-E load network seen from the device output at the second harmonic is shown in Fig. 5.30B, considering the shorting effect of the quarterwave short-circuit stub TL_3, where the transmission line TL_1 provides an open-circuit condition for the second harmonic. At the third harmonic, the transmission-line Class-E load network can similarly be represented, as shown in Fig. 5.30C, because of an open-circuit effect of the short-circuited quarterwave line TL_3 and a short-circuit effect of the open-circuited harmonic stub TL_4 at the third harmonic. In this case, the combined transmission line $TL_1 + TL_2$ provides an open-circuit condition for the third harmonic at the device output, being shorted at its right-hand side.

However, in a common case, it is necessary to take into account the transistor output parasitic series bondwire and lead inductance L_{out} shown in Fig. 5.31, which provides an additional inductive reactance at the fundamental frequency and does not affect the open-circuit conditions at the second and third harmonics. The inductive effect at the input of the series quarter-wavelength transmission line can be reduced by proper changing of the characteristic impedance Z_2. In this case, Eq. (5.83) can be rewritten as

$$\mathrm{Im}Z_{\mathrm{net}} = \frac{Z_1^2}{\sqrt{3}Z_2} + \omega_0 L_{\mathrm{out}} \tag{5.86}$$

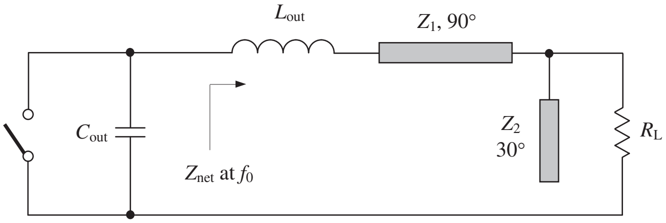

FIG. 5.31

Load network with series inductance at fundamental.

Hence, by using Eqs. (5.77) and (5.84), the characteristic impedance Z_2 can now be calculated from

$$Z_2 = \frac{R_L}{2} \frac{1}{1 - \dfrac{\omega_0 L_{out}}{1.1586R}} \tag{5.87}$$

resulting in a higher characteristic impedance of the open-circuit stub for greater values of the series inductance L_{out}.

Fig. 5.32 shows the simulated circuit schematic of a transmission-line Class-E power amplifier based on a commercial 28-V 5-W GaN HEMT power transistor NPTB00004 in a plastic package.[66] The input matching circuit with an open-circuit stub and a series transmission line provides a complex-conjugate matching with the standard 50-Ω source. The load network represents the optimized transmission-line Class-E load network shown in Fig. 5.28A. By using a 30-mil RO4350 substrate, an output power of 37 dBm, a drain efficiency of 73%, and a *PAE* of 71% at an operating frequency of 2.14 GHz are achieved with a power gain of 14 dB (linear gain of 19 dB) and a supply voltage of 25 V.

5.10 Practical Class-E power amplifiers and applications

A high level of output power with a very high operation efficiency can be easily achieved in a Class-E mode by using high-voltage power MOSFET devices at sufficiently low frequencies. Fig. 5.33A shows the circuit schematic of a 13.56-MHz 400-W Class-E power amplifier providing a drain efficiency of 82% with an input sinusoidal drive of 12 W at a supply voltage of 120 V.[67] The series inductor L_s and capacitor C_s form the resonant network that produces the rising and falling voltage waveform required for a Class-E operation. The series tank circuit at the load composed of a capacitor C_1 and an inductor L_1 is a trap for the second-harmonic component, which contributes to the overall level of harmonic suppression of greater than 40 dB below the carrier. Because at the fundamental frequency this second-harmonic resonant circuit represents a capacitive reactance, it transforms together with a part of the series inductance L_s the standard load of 50 Ω to around 13 Ω required for a nominal Class-E mode. The impedance of the gate is small with a real part of about 3 Ω and an inductive reactance of about 4 Ω. The input transformer with a voltage transformation ratio of 6:1 is used to step up from the input gate impedance to the driving source impedance of 50 Ω. This transformer also sets the DC gate bias to zero volts and ensures the transistor is turned off when it is not driven, as this is far below

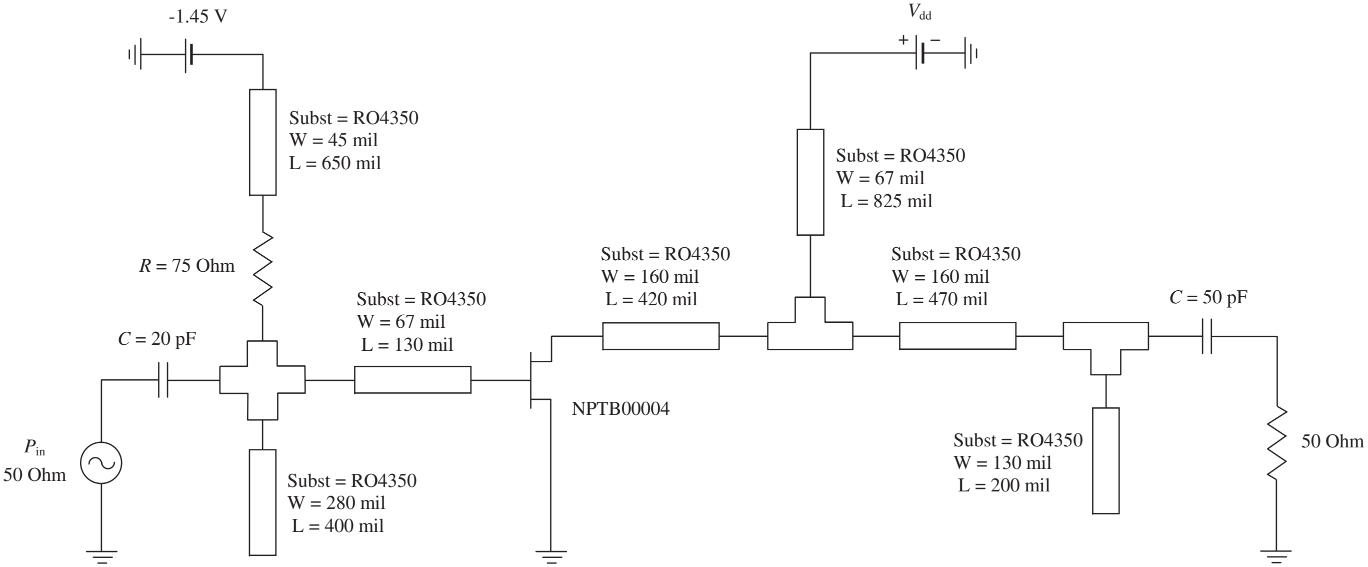
-1.45 V
Subst = RO4350
W = 45 mil
L = 650 mil
R = 75 Ohm
C = 20 pF
Subst = RO4350
W = 67 mil
L = 130 mil
Pin
50 Ohm
Subst = RO4350
W = 280 mil
L = 400 mil
NPTB00004
Subst = RO4350
W = 160 mil
L = 420 mil
Vdd
+
−
Subst = RO4350
W = 67 mil
L = 825 mil
Subst = RO4350
W = 160 mil
L = 470 mil
C = 50 pF
Subst = RO4350
W = 130 mil
L = 200 mil
50 Ohm

FIG. 5.32

Circuit schematic of a transmission-line Class-E GaN HEMT power amplifier.

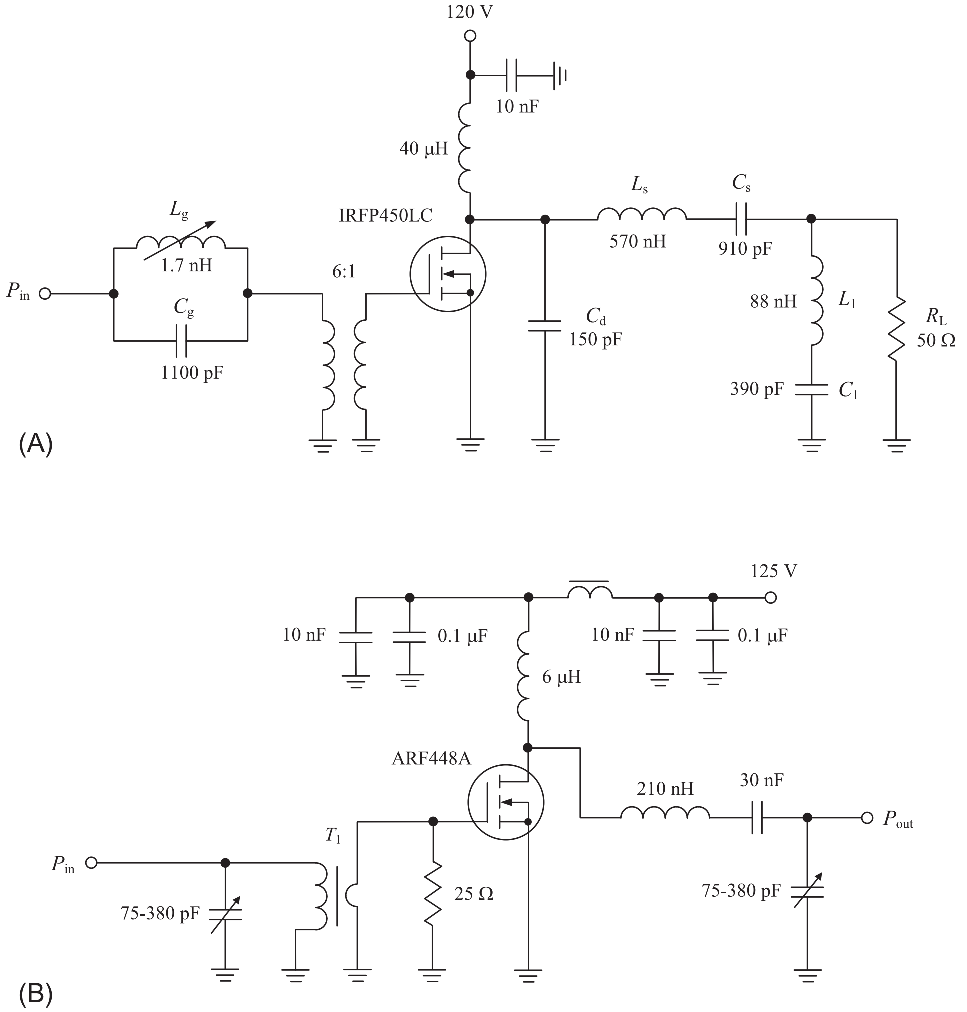
120 V
10 nF
40 μH
IRFP450LC
L_g
1.7 nH
P_{in}
C_g
1100 pF
6:1
L_s
570 nH
C_s
910 pF
C_d
150 pF
88 nH
L_1
390 pF
C_1
R_L
50 Ω
(A)
125 V
10 nF
0.1 μF
6 μH
10 nF
0.1 μF
ARF448A
210 nH
30 nF
P_{out}
T_1
P_{in}
75-380 pF
25 Ω
75-380 pF
(B)

FIG. 5.33

High-power high-frequency Class-E MOSFET power amplifiers.

the threshold voltage of 4 V. The capacitor C_g with the variable inductor L_g is used to compensate for the input inductive reactance of the transistor providing the input *VSWR* of 1.6:1.

Fig. 5.33B shows the circuit schematic of a 27.12-MHz 500-W Class-E MOSFET power amplifier with a drain efficiency of 83% at a supply voltage of 125 V.[68] The input ferrite transformer provides the 2:1 transformation voltage ratio to match the gate impedance, which is represented by the parallel equivalent circuit with a capacitance of 2200 pF and a resistance of 210 Ω. Use of the external parallel resistor of 25 Ω simplifies the matching procedure and improves the amplifier stability conditions.

The transformer secondary winding provides an inductance of 19 nH, which is required to compensate for the device input capacitance at the operating frequency. High-quality passive components are necessary to use in the low-pass L-type output network, where the quality factor of the bare copper wire inductor was equal to 375. The series blocking capacitor consists of three parallel disk ceramic capacitors. To realize a Class-E operation with shunt capacitance, it is sufficient to be limited to only the output device capacitance with a value of 125 pF. This is just slightly larger than that required to obtain the idealized optimum drain voltage and current Class-E waveforms.

Silicon LDMOSFET devices made it possible in Class-E operation to achieve a high output power level with a sufficiently high efficiency at higher frequencies. Fig. 5.34A shows the simplified circuit schematic of a high-power VHF LDMOSFET Class-E power amplifier achieving a drain efficiency of 70% for maximum output power of 54 W at an operating frequency of 144 MHz with an input drive of 5 W.[69] The drain efficiency can be increased to 88% if the output power level is reduced to 14 W by an appropriate increase of the series inductance in the load network. The input device impedance is

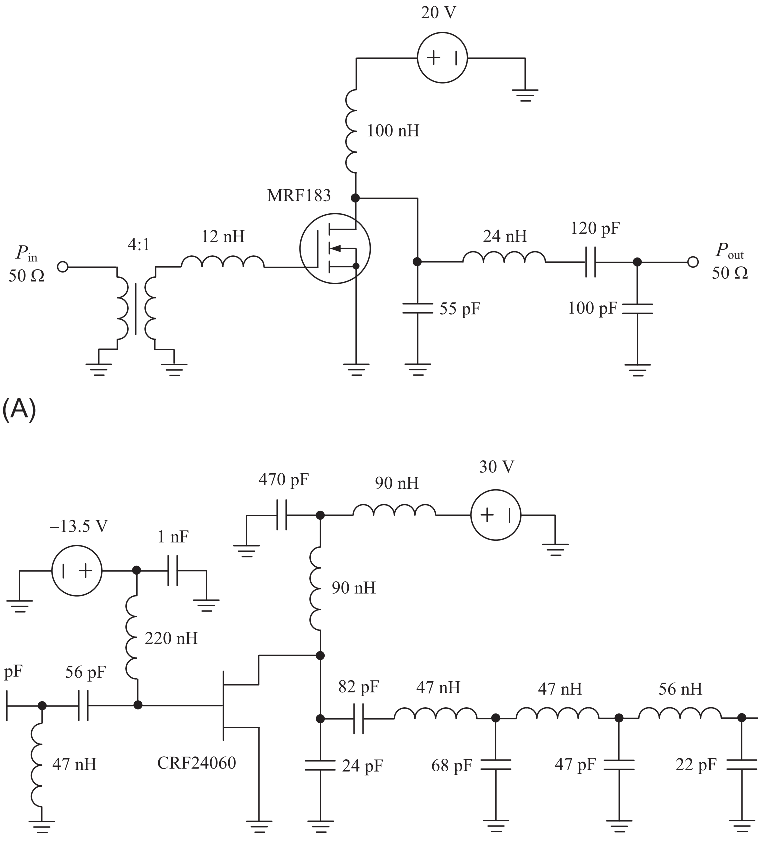
20 V
100 nH
MRF183
P_{in}
50 Ω
4:1
12 nH
24 nH
120 pF
P_{out}
50 Ω
55 pF
100 pF
(A)
470 pF
90 nH
30 V
−13.5 V
1 nF
90 nH
220 nH
12 pF
56 pF
P_{in}
50 Ω
82 pF
47 nH
47 nH
56 nH
P_{out}
50 Ω
47 nH
CRF24060
24 pF
68 pF
47 pF
22 pF
(B)

FIG. 5.34

High-power VHF Class-E power amplifier.

sufficiently low; therefore a ferrite transformer and a series inductor are used at the input. At the output, the standard load impedance of 50 Ω is transformed to the load resistance of 1.5 Ω, required for an idealized optimum Class-E mode by a lumped L-transformer with a series inductor whose value is included with the inductance of 24 nH and a shunt 100-pF capacitor. The required value of a shunt switching capacitance is provided by the values of the intrinsic device output capacitance of 38 pF and external capacitance of 55 pF. The loaded quality factor of the resonant circuit was chosen at a sufficiently low value of 5 that allows some frequency bandwidth operation to be provided and sensitivity of amplifier performance to the resonant-circuit parameters to be reduced. To decrease the loss in the load network, the inductor was fabricated by using a 5-mm-wide copper ribbon that provides the inductor quality factor of 150–250, depending on the distance to the ground plane. By inserting a spacer between the ribbon and the ground plane, the inductance can be tuned at least a factor of two.

Fig. 5.34B shows the simplified circuit schematic of a silicon carbide (SiC) MESFET Class-E power amplifier that provides a maximum drain efficiency of 86.8% at an output power of 20.5 W at 145 MHz reached at a drain voltage of 30 V, with an input drive power level of 27 dBm.[70] The output nominal Class-E impedance of approximately 18 Ω was matched to a 50-Ω load with a low-pass three-section L-type matching network to suppress harmonics by at least 60 dB below the carrier. The input of the active device was matched to 50-Ω source by means of a high-pass filter network to prevent the attenuation of the high-frequency harmonic components of the drive signal. Because this power amplifier was designed to provide linear amplification by restoring the input signal envelope with drain amplitude modulation, the drain bias network was built with a low-pass filter that allows drain modulating frequencies of up to a few megahertz to pass through it with minimum attenuation while at the same time achieving acceptable isolation at the carrier frequency and its harmonics.

The modified Class-E power amplifier with a tuned series-parallel resonance load network is shown in Fig. 5.35, which is characterized by higher maximum operating frequency and maximum drain peak voltage compared to the conventional Class-E power amplifier with shunt capacitance.[71] With a high-power LDMOSFET device, a drain efficiency of 81.77%, a *PAE* of 79.58%, and an output power of

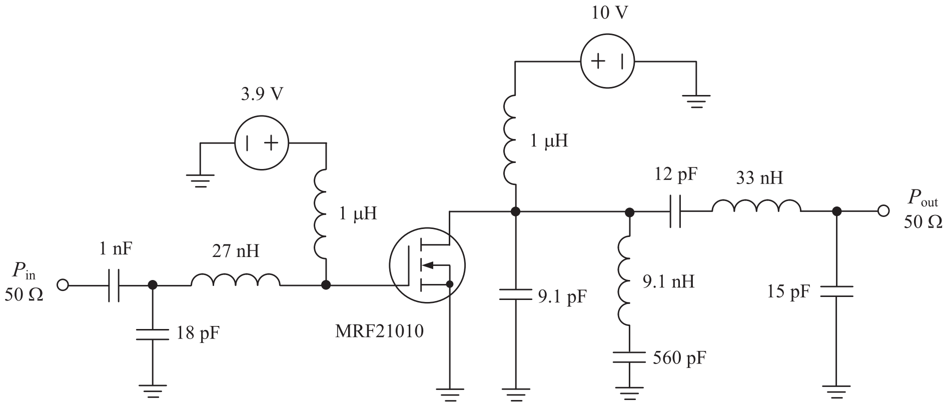

FIG. 5.35

Schematic of a VHF LDMOSFET Class-E power amplifier with series-parallel network.

32.71 dBm at 250 MHz were measured. This power amplifier can retain its high efficiency over 78% and output power over 32.7 dBm within approximately 21% relative bandwidth from 240 to 290 MHz.

The transmission-line Class-E power amplifier topology is shown in Fig. 5.36A, where the electrical lengths of microstrip lines l_3 and l_4 in the load network must be close to 45 degrees so that an approximate open circuit at the second harmonic will be presented to the switch shunt capacitor, which is an equivalent output device capacitance. Microstrip lines with a characteristic impedance of 50 Ω each were fabricated using a substrate with thickness of 2.54 mm and effective dielectric permittivity $\varepsilon_r = 10.5$. For a MESFET device having a drain-source capacitance $C_{ds} = 2.4$ pF, a *PAE* of 80% was achieved at 0.5 GHz with an output power of 0.55 W.[53] In this case, the electrical lengths of microstrip lines are $l_1 = 73$ degrees, $l_2 = 79$ degrees, $l_3 = 58$ degrees, and $l_4 = 46$ degrees. The *PAE* remains above 75% over a 10% bandwidth and above 50% over a 26% bandwidth. Moreover, a *PAE* of 73% can be realized at 1.0 GHz with an output power of 0.94 W. By using a MESFET device with a sufficiently

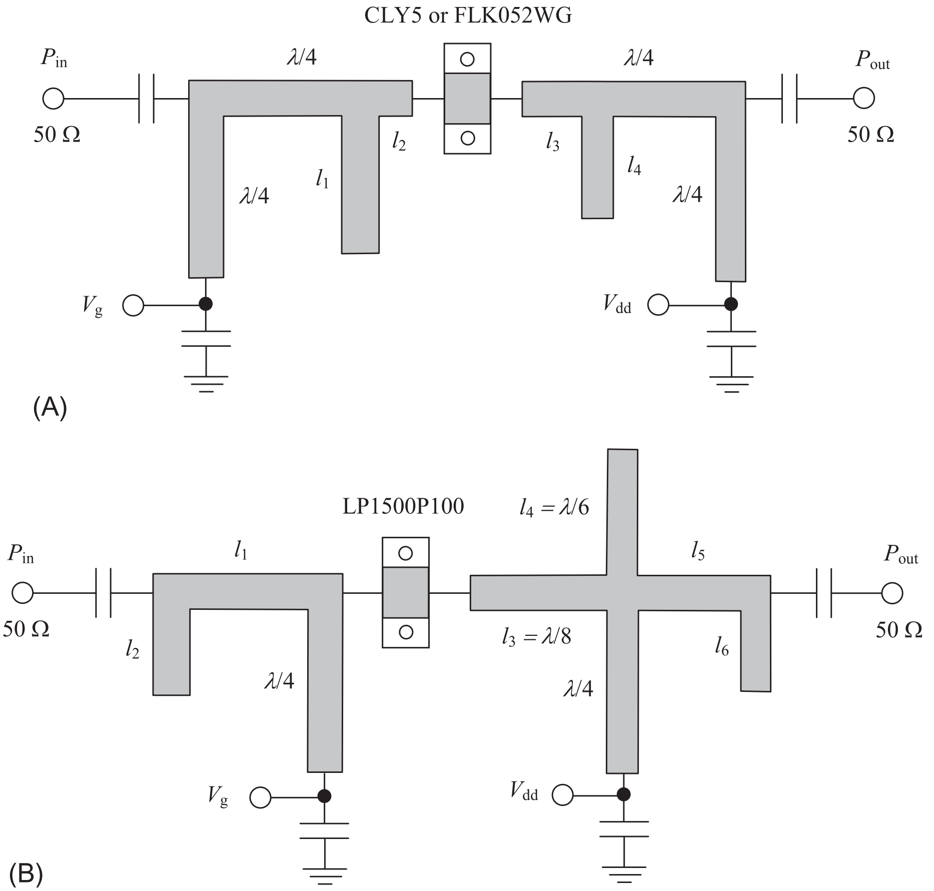
CLY5 or FLK052WG
P_{in}
50 Ω
$\lambda/4$
$\lambda/4$
l_1
l_2
l_3
l_4
$\lambda/4$
$\lambda/4$
P_{out}
50 Ω
V_g
V_{dd}
(A)
LP1500P100
$l_4 = \lambda/6$
P_{in}
50 Ω
l_1
l_2
$\lambda/4$
l_5
$l_3 = \lambda/8$
l_6
$\lambda/4$
P_{out}
50 Ω
V_g
V_{dd}
(B)

FIG. 5.36

Schematic diagram of a 1.8-GHz pHEMT Class-E power amplifier.

higher transition frequency f_T in such a microstrip Class-E power amplifier, an output power of 0.61 W, a 1-dB compressed power gain of 7.6 dB, a drain efficiency of 81%, and a *PAE* of 72% were achieved at 5 GHz.[19] The power amplifier was fabricated on a substrate with a thickness of 0.508 mm and $\varepsilon_r = 2.2$. As a result, the lengths of 50-Ω microstrip lines (1.6 mm wide) are 9 mm for l_1, 1.8 mm for l_2, 5.3 mm for l_3, and 6.2 mm for l_4. The *PAE* is greater than 70% over a 5% bandwidth and greater than 60% over a 10% bandwidth. A similar design approach can be used to design a monolithic Class-E power amplifier in *X*-band. As a result, the measured performance of a monolithic power amplifier that employs a pHEMT device with a geometry of 0.3 μm × 600 μm showed a peak *PAE* of 63% at 10.6 GHz and a constant output power of greater than 24 dBm together with a power gain of 10 dB over a frequency bandwidth of 9–11 GHz.[72]

Fig. 5.36B shows the schematic diagram of a 1.8-GHz transmission-line Class-E power amplifier using a commercially available pHEMT device that can offer a power gain over 12 dB for up to 15 GHz at a supply voltage of 3 V.[57] The gate and drain biasing are accomplished through the quarterwave stubs printed on a substrate with thickness of 0.79 mm and $\varepsilon_r = 2.33$. In this case, the input quarterwave stub provides a short-circuit termination of the second harmonic at the device input. The load impedance at the second harmonic is made close to an open circuit by using microstrip line l_3 having an electrical wavelength of 45 degrees at the fundamental frequency. Fundamental input and output matching are achieved through the microstrip lines l_1, l_2, l_4, l_5, and l_6, which were made adjustable by using high-quality copper foil. Initially, the device output capacitance C_{out} of 0.3–0.5 pF and saturation resistance r_{sat} of 1–2 Ω were assumed, and l_4 was set to 60 degrees. The transistor was biased near pinch-off with a quiescent current of 5 mA, which is about 5% of the maximum DC drain current of about 100 mA. The amplifier exhibited a maximum saturated power of 22 dBm, a maximum drain efficiency of 93%, and a maximum *PAE* of 88%.

Significant progress in CMOS technology has shown a promising future for CMOS RF power amplification. Much progress has been achieved at the research level, and the obvious possibility to minimize cost and size of the integrated circuits for RF handset transmitters, especially power amplifier MMICs, makes CMOS technology very feasible and brings considerable economic benefits. However, realizing high-efficiency operation of power amplifiers is limited by technology issues such as high value of the device saturation resistance, low value of breakdown voltage, and lossy silicon substrate. Therefore it is vital to apply high-efficiency techniques in the design of CMOS power amplifiers. Fig. 5.37A shows the design structure of a two-stage CMOS Class-E power amplifier, where biasing inductors are used to perform the function of DC-level shifting because the device threshold voltage is positive for the nMOS devices.[73] Note that these inductors should have extremely low parasitic resistance to reduce the metal power loss. To further reduce the power loss in passive components, bondwire inductors can be used instead of low-*Q* on-chip inductors, which especially makes sense under high-current conditions. A square driving waveform can be realized by using a high-pass interstage matching section, employing a high-frequency filter to minimize the second harmonic of the driving signal, or by overdriving the final stage with a large driving signal, provided there is a sufficient power gain.

While most of the Class-E power amplifiers use a single-ended topology because of practical implementation issues and available power devices, a differential counterpart, which exhibits smaller harmonic distortion since even harmonics cancel each other in a purely symmetrical structure, can be easily implemented using a CMOS technology with nMOS and pMOS devices. The simplified topology of a Class-E complementary CMOS power amplifier is shown in Fig. 5.37B.[74] To minimize the saturation resistance of the devices, it is necessary to use transistors with a large gate width, resulting in

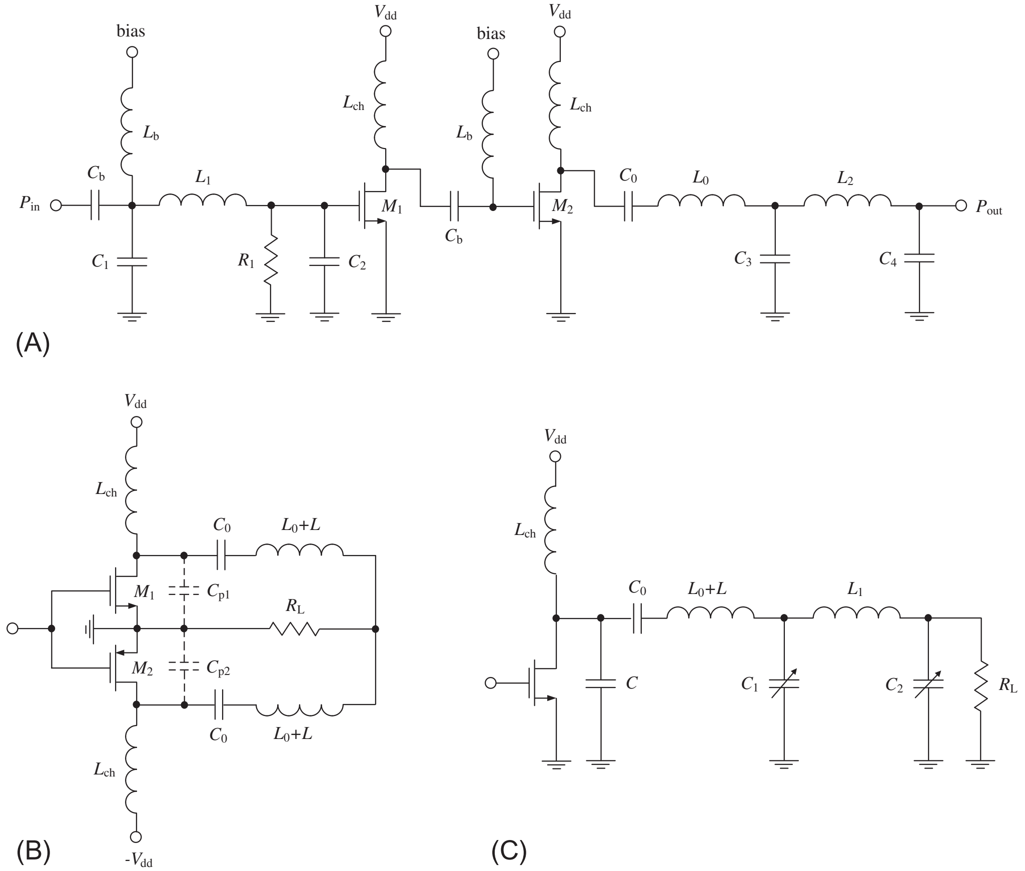

FIG. 5.37

Schematics of CMOS Class-E power amplifiers.

large parasitic output capacitances. In some cases, the device output parasitic capacitances C_{p1} and C_{p2} can fully represent the shunt capacitances required for a nominal Class-E operation mode. The identical series resonant circuits are each composed of a high-Q_L series L_0C_0 filter and an optimum Class-E inductance L. As a result, the ideal Class-E switching conditions are provided for MOS devices, while the current flowing into the load R_L is free from the even harmonics.

Modern wireless communication systems require the power amplifier to amplify linearly an input signal whose RF amplitude varies with time. In this case, there is a tradeoff between power amplifier efficiency and linearity, with improvement in one coming at the expense of the other. In addition, the power amplifiers in communications systems, such as GSM/EDGE, WCDMA/LTE, or CDMA2000, are required to cover linearly a dynamic range of the transmitter output power up to 80 dB. As a result, being designed for the highest power level with maximum available efficiency, the power amplifier tends to operate less efficiently at lower power levels, which leads to shortening the battery life and talk time reduction. In this case, to maximize the efficiency of the power amplifier operation, the load resistance for different output power levels should be different to provide a collector voltage amplitude close to the value of the supply voltage. Despite the fact that the shunt capacitance stays constant under different load conditions, resulting in a nonoptimum Class-E operation, the efficiency at a lower output power level can be significantly increased. Fig. 5.37C shows the architecture of the power-controllable Class-E power amplifier whose matching network consists of two electrically tunable shunt capacitors and a series inductor.[75] This Π-type matching circuit can transform the standard load of 50 Ω into different loads whose resistance values are greater than the optimum Class-E load.

Another possibility to improve the efficiency of the power amplifier for RF signals with nonconstant envelope is to use the traditional analog envelope elimination and restoration (EER) approach combined with a digital signal processing (DSP) system, whose polar architecture is shown in Fig. 5.38. Here, the two separate signals, one with amplitude (envelope) information and the other with phase information only, are generated by DSP. The phase signal, in which the amplitude variations are canceled, modulates the phase of the phase-locked loop (PLL). Then, the output signal of the PLL is amplified by the highly efficient Class-E power amplifier. The amplitude signal is fed to the Class-S modulator to effectively vary the supply voltage according to the envelope amplitude. A Class-S modulator is a high-efficiency low-frequency power amplifier based on pulse-width modulation (PWM), and its output is a baseband envelope signal, including a DC component. To minimize misalignment between phase and amplitude, a delay line is required. Adding the output phase feedback circuit allows the intermodulation distortion to be reduced. The measured results from a prototype test chip operating at 835 MHz indicate that phase correcting feedback reduces the 30 degrees phase distortion of the Class-E power amplifier down to 4 degrees when it delivers an output power of 443 mW to the load at a supply voltage of 2.4 V, and the total power efficiency of the linearized Class-E power amplifier reaches 65%.[73]

Generally, the dependence of the output voltage on the DC supply voltage is linear enough that amplitude modulation can be achieved by linearly varying the supply voltage, both for bipolar and MESFET devices.[76, 77] Variations from perfect linearity can be caused by variations in the transistor

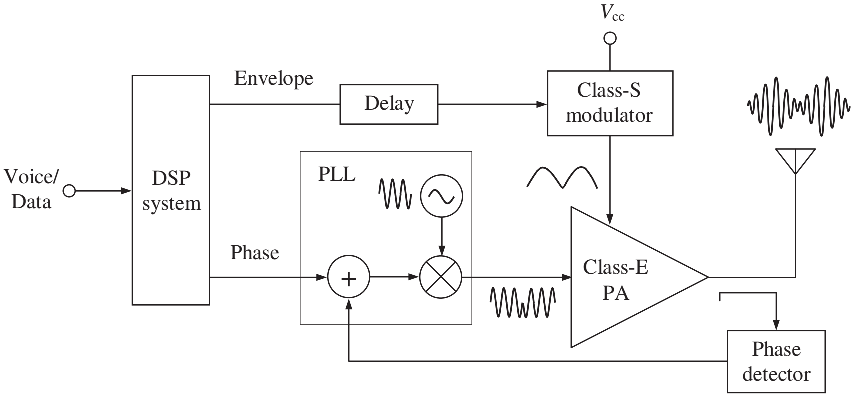

FIG. 5.38

Polar transmitter architecture.

saturation voltage being a function of the supply voltage, input-to-output feedthrough of the driving signal through the feedback capacitance, and voltage-variable output capacitance of the transistor. Because efficiency degrades at a low DC supply voltage, it can be improved with simultaneous extension of dynamic range by reducing the on-duty ratio by adaptive gate bias voltage optimization.[78] In this case, the maximum operating frequency $f_{\max}$ of the Class-E power amplifier derived under nominal zero-voltage and zero-voltage-derivative conditions for fixed values of the shunt capacitance, supply voltage, and output power is approximately 10 times higher at 25% duty ratio than that of at 50% duty ratio.[79]

In addition, the size of a Class-S modulator can be too large for MMIC implementation, and the modulator can be inefficient at high frequencies. Note that, for such a polar architecture, a high degree of amplitude and phase tracking is required to achieve a high depth of modulation. For instance, a combination of 0.2-dB amplitude and 3 degrees of phase tracking error will result in a maximum modulation dynamic range of only 20 dB. There should be a tradeoff between the switching frequency in a Class-S modulator and the order of a low-pass filter to minimize the intermodulation distortion. An experimental improved 3.9-MHz EER system with a peak envelope power (PEP) of 26 W and level of the third-order intermodulation distortion lower than −40 dBc achieved the overall drain efficiency of 90% (95% in the Class-E power amplifier and 95% in the 1-MHz DC-DC converter that supplied the time-varying collector supply voltage to the RF power amplifier).[80] The harmonic level in the RF output was −60 dBc or lower.

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CHAPTER

6

Class-E with finite DC-feed inductance

In this chapter, the switchmode second-order Class-E configurations with one capacitor and one inductor and generalized load network including the finite DC-feed inductance, shunt capacitance, and series reactance are discussed and analyzed. The results of the Fourier analysis and derivation of the equations governing the operation in an idealized operation mode are presented. Based on these equations, the required voltage and current waveforms and load-network parameters are determined for both general case and particular circuits, corresponding to the subharmonic Class-E, parallel-circuit Class-E, and even-harmonic Class-E modes. The effect of the device output bondwire inductance on the optimum circuit parameters is demonstrated. To minimize an effect of the load variation on efficiency, a Class-E with inductive impedance inverter is analyzed. The possibilities to realizing a parallel-circuit Class-E approximation with transmission lines are shown and discussed. The operating power gain achieved with a parallel-circuit Class-E power amplifier is evaluated and compared with the operating power gain of a conventional Class-B power amplifier. The circuit design examples and practical implementations of the Class-E power amplifiers with finite DC-feed inductance using a CMOS technology are given.

6.1 Class-E with one capacitor and one inductor

The Class-E load network with shunt capacitor and series inductor represents the simplest load network used for a switchmode operation because it can be analytically described by a first-order differential equation resulting in exact values for the load-network parameters. However, a switchmode tuned Class-E power amplifier can also be realized with only one inductor and one capacitor connected in parallel in the load network.[1–4] In this case, the load-network topology is the same as in the classical current-source Class-C power amplifier, but the operation of these two circuits is entirely different. In a Class-C power amplifier, the tank circuit provides sinusoidal voltage on the device collector, being tuned to the fundamental frequency. In a Class-E power amplifier, this circuit is tuned between the fundamental frequency and second-harmonic component, providing a nonsinusoidal collector voltage waveform to minimize overlapping between the collector current and voltage waveforms, thus reducing the power losses on the device and increasing the collector efficiency.

The basic circuit of a switchmode Class-E power amplifier with a parallel *LC* circuit is shown in Fig. 6.1A. In this case, the load network consists of a parallel inductor *L*, a parallel capacitor *C*, a DC-blocking capacitor C_0, and a load *R*. In a common case, the parallel capacitance *C* can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The active device is considered an ideal switch that is driven to provide the device switching between

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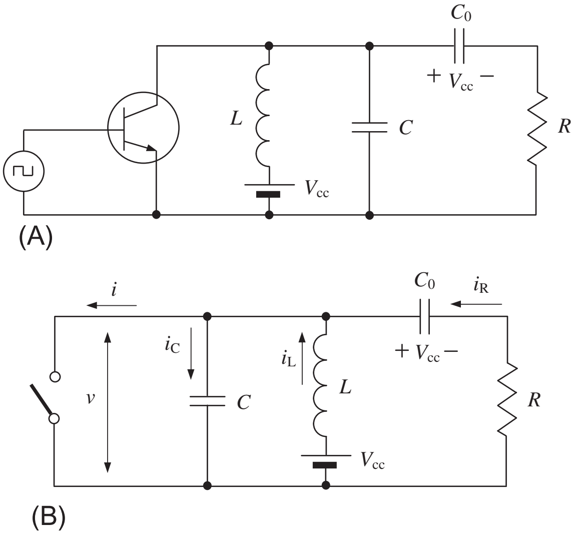


FIG. 6.1

Basic circuits of Class-E power amplifier with one capacitor and one inductor.

its on-state and off-state operation modes. As a result, the collector voltage waveform is determined by the transient response of the load network when the switch is turned off.

To simplify an analysis of a Class-E power amplifier with one capacitor and one inductor, which can be represented by an equivalent circuit shown in Fig. 6.1B, consider the same idealized assumptions as for the Class-E power amplifier with shunt capacitance:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-state resistance, and its switching action is instantaneous and lossless.
- The total parallel capacitance is independent of the collector-emitter voltage and is assumed linear.
- There are no losses in the circuit except only into the load R.
- For an optimum operation mode, a 50% duty ratio is used (other values can also be used if desired, as part of a trade-off among several performance parameters).

For an idealized theoretical analysis, an active device is replaced by the ideal switch, as shown in Fig. 6.1B. The moment of switch-on is $\omega t = 0$ and switch-off is $\omega t = \pi$ with period of repeatability of $\omega T = 2\pi$ determined by the drive input to the power amplifier. For lossless operation mode, it is necessary to provide the following idealized optimum (or nominal) conditions for voltage across the switch just prior to the start of switch-on at the moment $\omega t = 2\pi$, when the transistor is voltage-saturated:

$$v(\omega t)|_{\omega t = 2\pi} = 0, \tag{6.1}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} = 0, \tag{6.2}$$

where $v(\omega t)$ is the voltage across the switch.

When the switch is turned on for $0 \leq \omega t < \pi$, the voltage $v(\omega t)$ across the switch and the current $i_{\mathrm{C}}(\omega t)$ flowing through the capacitance C are equal to zero,

$$v(\omega t) = V_{\mathrm{cc}} - v_{\mathrm{L}}(\omega t) = 0, \tag{6.3}$$

$$i_{\mathrm{C}}(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = 0. \tag{6.4}$$

The current i_{R} flowing into the load R can generally be determined by

$$i_{\mathrm{R}}(\omega t) = \frac{V_{\mathrm{cc}}}{R} \exp\left(-\frac{\omega t}{\omega \tau}\right), \tag{6.5}$$

where $\tau = RC_0$. However, for $\tau \to \infty$, when the series capacitor C_0 serves as a DC-blocking capacitor with a large value of $C \to \infty$, the current i_{R} can be simply rewritten as $i_{\mathrm{R}}(\omega t) = V_{\mathrm{cc}}/R$. Then, to describe the circuit operation in the time domain, the following system of equations can be obtained:

$$V_{\mathrm{cc}} = \omega L \frac{di_{\mathrm{L}}(\omega t)}{d\omega t}, \tag{6.6}$$

$$i = i_{\mathrm{L}} + i_{\mathrm{R}}. \tag{6.7}$$

Assuming $i(0) = 0$ and

$$i_{\mathrm{L}}(\omega t) = \frac{1}{\omega L} \int_0^{\omega t} v_{\mathrm{L}}(\omega t) d\omega t + i_{\mathrm{L}}(0), \tag{6.8}$$

where $v_{\mathrm{L}} = V_{\mathrm{cc}}$ and $i_{\mathrm{L}}(0) = -V_{\mathrm{cc}}/R$, the current $i(\omega t)$ flowing through the switch can be defined as

$$i(\omega t) = \frac{V_{\mathrm{cc}}}{\omega L} \omega t. \tag{6.9}$$

When the switch is turned off for $\pi \leq \omega t < 2\pi$, the following system of equations can be written:

$$V_{\mathrm{cc}} = \omega L \frac{di_{\mathrm{L}}(\omega t)}{d\omega t}, \tag{6.10}$$

$$i_{\mathrm{C}} = i_{\mathrm{L}} + i_{\mathrm{R}}, \tag{6.11}$$

where the current $i_{\mathrm{C}}(\omega t) = i_{\mathrm{L}}(\omega t) + i_{\mathrm{R}}(\omega t)$ flowing through the capacitance C can be rewritten as

$$\omega C \frac{dv(\omega t)}{d\omega t} = \frac{1}{\omega L} \int_{\pi}^{\omega t} [V_{\mathrm{cc}} - v(\omega t)] d\omega t + i_{\mathrm{L}}(\pi) + \frac{V_{\mathrm{cc}} - v(\omega t)}{R}, \tag{6.12}$$

under the initial off-state conditions $v(\pi) = 0$ and

$$\omega C \left. \frac{dv}{d\omega t} \right|_{\omega t = \pi} = i(\pi) = \frac{V_{\mathrm{cc}} \pi}{\omega L}.$$

The solution of the integro-differential equation given by Eq. (6.12) is obtained by applying the Laplace transform method.[2] However, another approach is to apply the methods of solving the differential equations directly. As a result, Eq. (6.12) can be represented in the form of the linear nonhomogeneous second-order differential equation given by

$$\omega^2 LC\frac{d^2 v(\omega t)}{d(\omega t)^2} + \frac{\omega L}{R}\frac{dv(\omega t)}{d\omega t} + v(\omega t) = V_{\mathrm{cc}}, \tag{6.13}$$

the general solution of which can be obtained in the form

$$v(\omega t) = \exp(a\omega t)[C_1\cos(b\omega t) + C_2\sin(b\omega t)] + V_{\mathrm{cc}}, \tag{6.14}$$

where

$$a = -\frac{1}{2Q} \qquad b = \frac{1}{2Q}\sqrt{(2Qq)^2 - 1},$$

$$q = \frac{1}{\omega\sqrt{LC}} \qquad Q = \omega RC.$$

The coefficients C_1 and C_2 are determined from the initial off-state conditions as

$$C_1 = -V_{\mathrm{cc}}\exp(-a\pi)\left[\cos b\pi + \frac{\pi q^2 + a}{b}\sin b\pi\right], \tag{6.15}$$

$$C_2 = -V_{\mathrm{cc}}\exp(-a\pi)\left[\sin b\pi - \frac{\pi q^2 + a}{b}\cos b\pi\right]. \tag{6.16}$$

To solve Eq. (6.14) with regard to two unknown parameters q and Q, it is necessary to apply two idealized optimum conditions given by Eqs. (6.1) and (6.2). Let us consider the oscillatory case $2Qq > 1$ for the second-order differential equation. As a result, the numerical solution gives the following values:

$$q = 1.542, \tag{6.17}$$

$$Q = 1.025. \tag{6.18}$$

Thus, the idealized optimum values of a parallel inductance and a parallel capacitance corresponding to the switchmode Class-E load network with only one inductor and one capacitor can be calculated from

$$L = 0.41\frac{R}{\omega}, \tag{6.19}$$

$$C = \frac{1.025}{\omega R}, \tag{6.20}$$

which are similar to those obtained in Refs. 2, 3.

The optimum load R and initial phase shift φ for the fundamental-frequency component can be determined using the load-network impedance at the fundamental seen by the switch, whose phase angle ϕ can be represented as a function of the load-network parameters by

$$\phi = \tan^{-1}\left(\frac{R}{\omega L} - \omega RC\right) = \tan^{-1}\left[Q\left(q^2 - 1\right)\right] = 54.729°. \tag{6.21}$$

However, the fundamental-frequency current $i_1(\omega t)$ flowing through the switch consists of two quadrature components, active i_{R1} and reactive i_{X1}, whose amplitudes can be found using Fourier formulas and Eq. (6.9) by

$$I_{\rm R1} = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)\sin(\omega t+\varphi)d\omega t = \frac{V_{\rm cc}}{\pi\omega L}(\pi\cos\varphi - 2\sin\varphi), \tag{6.22}$$

$$I_{\rm X1} = -\frac{1}{\pi}\int_0^{2\pi} i(\omega t)\cos(\omega t+\varphi)d\omega t = \frac{V_{\rm cc}}{\pi\omega L}(\pi\sin\varphi + 2\cos\varphi), \tag{6.23}$$

where φ is the initial phase shift of the fundamental-frequency current.

Hence,

$$\tan\phi = \frac{I_{\rm X1}}{I_{\rm R1}} = \frac{\pi\sin\varphi + 2\cos\varphi}{\pi\cos\varphi - 2\sin\varphi}, \tag{6.24}$$

and the phase shift φ can be finally calculated as

$$\varphi = \tan^{-1}\left(\frac{\pi\tan\phi - 2}{2\tan\phi + \pi}\right) = 22.25°. \tag{6.25}$$

The DC supply current I_0 can be obtained using Fourier formula from Eq. (6.9) as

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)d\omega t = \frac{\pi V_{\rm cc}}{4\omega L}. \tag{6.26}$$

Using Eq. (6.22), the optimum load resistance R for the specified values of supply voltage $V_{\rm cc}$ and output power P_1 at the fundamental frequency can be written as

$$R = \frac{2P_1}{I_{\rm R1}^2} = 2\left(\frac{\pi\omega L}{V_{\rm cc}}\right)^2 \frac{P_1}{(\pi\cos\varphi - 2\sin\varphi)^2}. \tag{6.27}$$

Then, Eqs. (6.19) and (6.25), Eq. (6.27) can be simplified to

$$R = 1.394\frac{V_{\rm cc}^2}{P_1}. \tag{6.28}$$

Fig. 6.2 shows the normalized (A) fundamental-frequency load current (not including the harmonic components); (B) collector voltage; and (C) collector current waveforms for an idealized optimum Class-E mode with one capacitor and one inductor. From the collector voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch, and the current $i(\omega t)$, consisting of the total load current and inductor current, flows through the switch. However, when the transistor is turned off, this current flows through the shunt capacitor. As a result, there is no nonzero voltage and current simultaneously, which indicates a lack of the power losses and gives an idealized collector efficiency of 100%. The normalized currents flowing through the (A) shunt capacitor C; (B) parallel inductor L; and (C) load resistor R for an idealized optimum Class-E operation mode are given in Fig. 6.3.

The peak collector current $I_{\rm max}$ can be directly determined from Eq. (6.9) using Eq. (6.26), while the peak collector voltage $V_{\rm max}$ is calculated numerically from Eq. (6.14), resulting in

$$I_{\rm max} = 4.000 I_0, \tag{6.29}$$

$$V_{\rm max} = 3.849\, V_{\rm cc}. \tag{6.30}$$

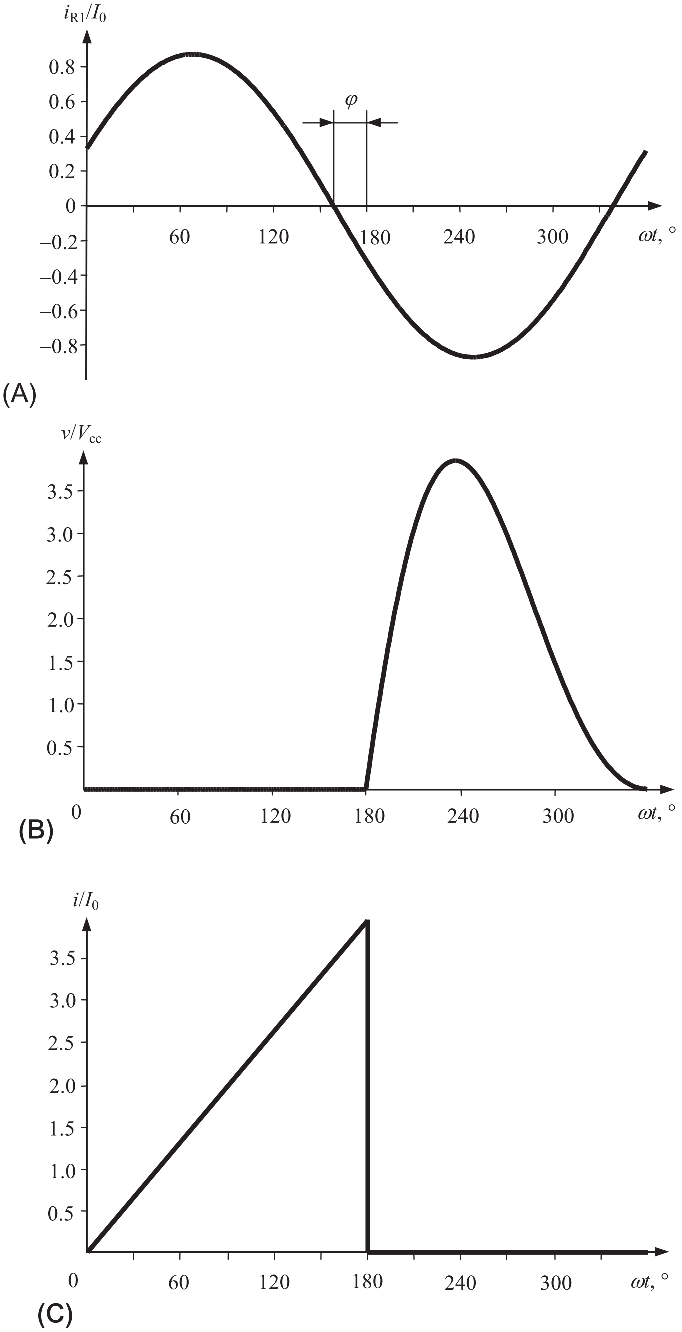


FIG. 6.2

Normalized (A) load current and collector (B) voltage and (C) current waveforms for idealized optimum Class-E with one capacitor and one inductor.

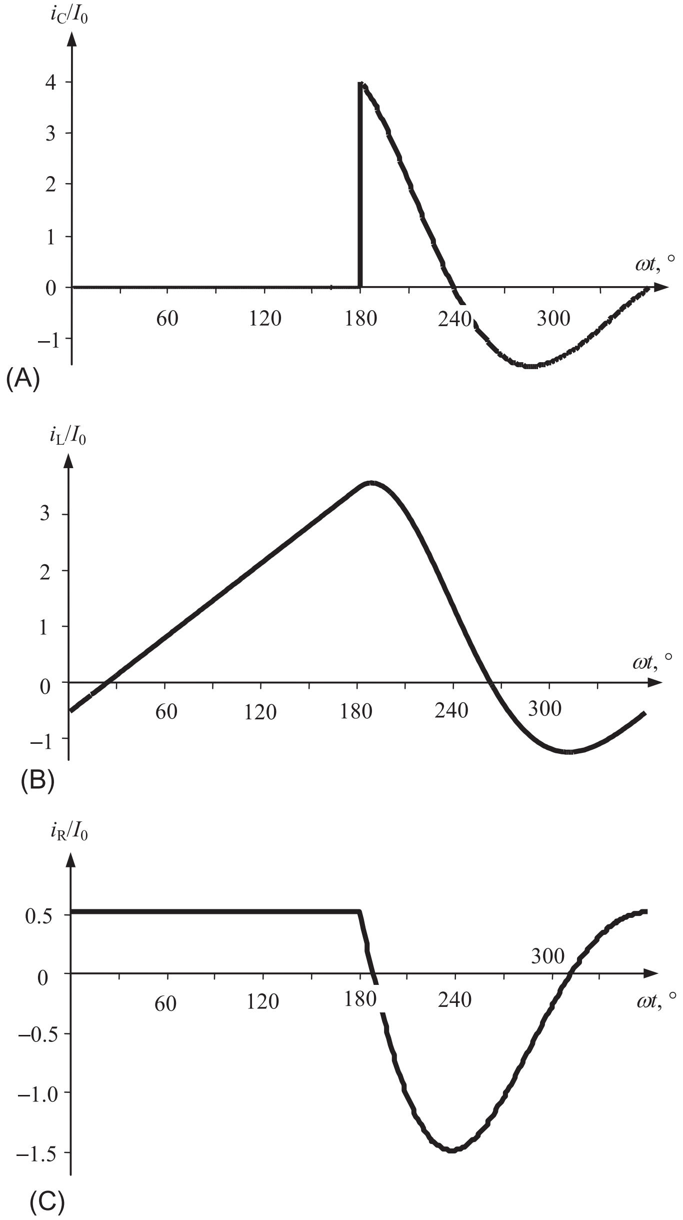


FIG. 6.3

Normalized currents flowing through (A) shunt capacitor; (B) parallel inductor; and (C) load resistor.

The numerical calculation shows that the harmonic level of the output signal spectrum is significant. The ratio of the fundamental-frequency output power P_1, second-harmonic output power P_2, and third-harmonic output power P_3 is

$$P_1/P_2/P_3 = 1/0.3156/0.0405, \tag{6.31}$$

which shows that the levels of the second and third harmonics relative to the fundamental-frequency component in the output power spectrum are approximately -5 dBc and -14 dBc, respectively.[2] Note that the harmonic level in the output power spectrum in the Class-E power amplifier with shunt capacitor and series inductor of Fig. 5.2 is lower than that in the Class-E power amplifier with one capacitor and one inductor of Fig. 6.1, being less than 10% of the fundamental-frequency power.[5, 6] Therefore, this version of the Class-E load network is suitable for applications in which the power delivered to the load R has been allowed to have a fairly large harmonic content and phase-modulation noise because of the absence of any additional filtering. However, this circuit can be effectively used as a test bench for extracting the parameters of a simple active device output port model such as saturation resistance and output capacitance.[7] This approach can provide designers with a quick way to find out if the transistor will be useful in a Class-E operation and with what maximum operating frequency.

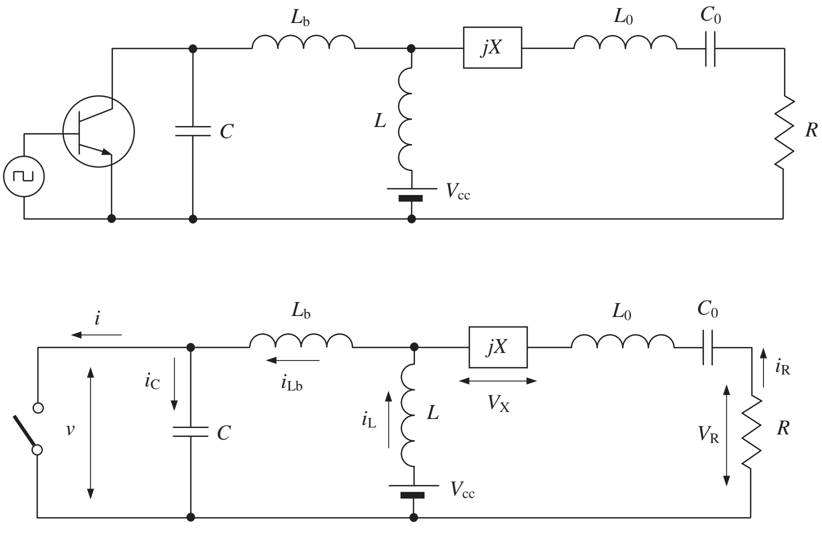
6.2 Generalized Class-E load network with finite DC-feed inductance

In practice, it is impossible to realize radio-frequency (RF) choke with infinite impedance at the fundamental frequency and other harmonic components. Moreover, using a finite DC-feed inductance has an advantage of minimizing size, cost, and complexity of the overall circuit. The detailed approach for analyzing the effect of a finite DC-feed inductance on the idealized Class-E mode with shunt capacitance and series filter was first described in Ref. 8. An analysis was based on the Laplace-transform technique to solve a second-order differential equation describing the behavior of a Class-E load network with finite DC-feed inductance. Later this approach was extended to the load network with finite Q_L-factor of the series filter and finite device saturation resistance.[9, 10] The obtained results can be summarized as follows[10]:

- For a smaller DC-feed inductance, the smaller detuning of a series-tuned circuit is necessary, which is very attractive for radio-transmitter applications, where the amplitudes of two sidebands should not be substantially different.
- Using a small DC-feed inductance is attractive when both the DC voltage and load resistance are specified and higher output power is needed.
- Q_L-factor of a series filter affects the power amplifier performance less when the DC-feed inductance is small.
- Maximum output power increases as the DC-feed inductance decreases for large values of Q_L-factor and behaves oppositely for small values of Q_L-factors.
- Device saturation resistance r_{sat} should be considered, especially when its value is larger than $0.1R$, where R is an optimum Class-E load resistance.

However, because the results of excessive analytical and numerical calculations are given only for a few particular cases, it is difficult to define the basic behavior of the load-network elements and derive simple equations for their parameters. Generally, based on the composing of the circuit equations in the form of a system of the first-order differential equations for currents and voltages and setting the design specifications, the optimum Class-E load-network parameters can be numerically calculated considering the finite DC-feed inductance, drain current fall time, finite Q_L-factor, nonzero device saturation resistance, and nonlinear operation of any passive element simultaneously.[11] More physical insight into Class-E load-network specifics was given when Class-E load network with finite DC-feed inductance was analyzed for a duty ratio of 50% based on the idealized optimum Class-E conditions.[12] It was analytically shown that the series excessive reactance can be either inductive or capacitive depending on the values of the DC-feed inductance and shunt capacitance. In a similar detailed analytical derivation procedure with particular examples, the finite device saturation resistance is taken into account to predict the power losses on the active device.[13] Based on a certain number of cases, a Lagrange polynomial interpolation was used to obtain explicit and directly usable design equations for an idealized Class-E mode with small DC-feed inductance and series inductive reactance.[14]

Now let us consider a general case of the Class-E load network with finite DC-feed inductance. The main goal is to demonstrate an analytical design procedure in a clear mathematical form and to represent the design equations in a simple explicit analytical or graphical form with special highlighting of the specific particular cases. The generalized second-order load network of a switchmode Class-E power amplifier with finite DC-feed inductance is shown in Fig. 6.4A.[15] The load network consists of a shunt capacitor C, a series inductor L_b, a parallel inductor L, a series reactance X, a series resonant L_0C_0 circuit tuned to the fundamental frequency, and a load resistor R. In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network; a series inductance L_b can be considered as the bondwire and lead inductance; a parallel inductance L represents the finite DC-feed inductance; and a series reactance X can be positive



b).

FIG. 6.4

Equivalent circuits of the Class-E power amplifiers with generalized load network.

(inductance), negative (capacitance), or zero, depending on the particular Class-E mode. The active device is considered an ideal switch that is driven to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the transient response of the load network when the switch is off.

To simplify an analysis of the general-circuit Class-E power amplifier, a simplified equivalent circuit of which is shown in Fig. 6.4B, it makes sense to introduce the preliminary assumptions similar to those for the Class-E power amplifier with shunt capacitance. The moment of switch-on is $\omega t = 0$ and switch-off is $\omega t = \pi$, with a period of repeatability of the input driving signal $\omega T = 2\pi$ determined by the input drive to the power amplifier. Assume the *losses in the reactive circuit* elements are negligible and the loaded quality factor of the series L_0C_0 circuit is sufficiently high. For a lossless operation, it is necessary to provide the optimum zero-voltage and zero voltage-derivative conditions for voltage $v(\omega t)$ across the switch just prior to the start of switch-on at the moment $\omega t = 2\pi$, when the transistor is saturated, given by Eqs. (6.1) and (6.2).

The output current flowing through the load is written as sinusoidal by

$$i_{\mathrm{R}}(\omega t) = I_{\mathrm{R}} \sin(\omega t + \varphi), \tag{6.32}$$

where I_{R} is the load current amplitude and φ is the initial phase shift.

When the switch is turned on for $0 \le \omega t < \pi$, the voltage on the switch is

$$v(\omega t) = V_{\mathrm{cc}} - v_{\mathrm{L_b}}(\omega t) - v_{\mathrm{L}}(\omega t) = 0, \tag{6.33}$$

where

$$v_{\mathrm{L_b}}(\omega t) = \omega L_{\mathrm{b}} \frac{di(\omega t)}{d\omega t}, \tag{6.34}$$

$$v_{\mathrm{L}}(\omega t) = \omega L \frac{di_{\mathrm{L}}(\omega t)}{d\omega t}. \tag{6.35}$$

Since the current flowing through the capacitance C is

$$i_{\mathrm{C}}(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = 0, \tag{6.36}$$

the current flowing through the switch can be written using Eqs. (6.32), (6.33), and (6.35) as

$$i(\omega t) = i_{\mathrm{L}}(\omega t) + i_{\mathrm{R}}(\omega t) = \frac{1}{\omega L}\int_0^{\omega t} [V_{\mathrm{cc}} - v_{\mathrm{L_b}}(\omega t)]d\omega t + i_{\mathrm{L}}(0) + I_{\mathrm{R}} \sin(\omega t + \varphi). \tag{6.37}$$

Substituting Eq. (6.34) into Eq. (6.37) results in

$$i(\omega t) = \frac{V_{\mathrm{cc}}}{\omega(L + L_{\mathrm{b}})}\omega t + \frac{\omega L}{\omega(L + L_{\mathrm{b}})}[i_{\mathrm{L}}(0) + I_{\mathrm{R}} \sin(\omega t + \varphi)]. \tag{6.38}$$

Since $i(0) = 0$, the initial value for the current $i_{\mathrm{L}}(\omega t)$ flowing through the DC-feed inductance L at $\omega t = 0$ can be found using Eq. (6.32) by

$$i_{\mathrm{L}}(0) = i(0) - i_{\mathrm{R}}(0) = -I_{\mathrm{R}} \sin\varphi. \tag{6.39}$$

As a result,

$$i(\omega t) = \frac{V_{\mathrm{cc}}}{\omega(L + L_{\mathrm{b}})}\omega t + \frac{\omega L I_{\mathrm{R}}}{\omega(L + L_{\mathrm{b}})}[\sin(\omega t + \varphi) - \sin\varphi]. \tag{6.40}$$

When the switch is turned off for $\pi \leq \omega t < 2\pi$, the current $i(\omega t) = 0$ and the voltage across the parallel inductance $v_L(\omega t) = V_{cc} - v(\omega t) - v_{L_b}(\omega t)$. Consequently, the current $i_C(\omega t) = i_L(\omega t) + i_R(\omega t)$ flowing through the capacitance C can be rewritten as

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = \frac{1}{\omega L} \int_{\pi}^{\omega t} [V_{cc} - v(\omega t) - v_{L_b}(\omega t)] d\omega t + i_L(\pi) + I_R \sin(\omega t + \varphi), \tag{6.41}$$

under the initial off-state conditions $v(\pi) = 0$ and

$$\omega C \frac{dv(\omega t)}{d\omega t}\bigg|_{\omega t = \pi} = \frac{V_{cc}\pi - 2\omega L I_R \sin\varphi}{\omega(L + L_b)}.$$

Since the voltage $v_{L_b}(\omega t)$ across the inductor L_b can be obtained from

$$v_{L_b}(\omega t) = \omega L_b \frac{di_C(\omega t)}{d\omega t} = \omega^2 L_b C \frac{d^2 v(\omega t)}{d(\omega t)^2}. \tag{6.42}$$

Eq. (6.41) can be rewritten in the form

$$\omega C \frac{dv(\omega t)}{d\omega t} = \frac{1}{\omega L} \int_{\pi}^{\omega t} \left[V_{cc} - v(\omega t) - \omega^2 L_b C \frac{d^2 v(\omega t)}{d(\omega t)^2} \right] d\omega t + i_L(\pi) + I_R \sin(\omega t + \varphi). \tag{6.43}$$

As a result, by differentiating both sides of Eq. (6.43) and combining similar terms, it can be represented in the form of the linear nonhomogeneous second-order differential equation

$$\omega^2 (L + L_b) C \frac{d^2 v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{cc} - \omega L I_R \cos(\omega t + \varphi) = 0, \tag{6.44}$$

the general solution of which can be obtained in the normalized form

$$\frac{v(\omega t)}{V_{cc}} = C_1 \cos(q\omega t) + C_2 \sin(q\omega t) + 1 - \frac{q^2 p}{1 - q^2} \cos(\omega t + \varphi), \tag{6.45}$$

where

$$q = \frac{1}{\omega \sqrt{C(L + L_b)}}, \tag{6.46}$$

$$p = \frac{\omega L I_R}{V_{cc}}, \tag{6.47}$$

and the coefficients C_1 and C_2 are determined from the initial off-state conditions by

$$\begin{aligned} C_1 = &-(\cos q\pi + q\pi \sin q\pi) \\ &- \frac{qp}{1 - q^2} \left[q \cos\varphi \cos q\pi - \left(1 - 2q^2\right) \sin\varphi \sin q\pi \right], \end{aligned} \tag{6.48}$$

$$\begin{aligned} C_2 = &(q\pi \cos q\pi - \sin q\pi) \\ &- \frac{qp}{1 - q^2} \left[q \cos\varphi \sin q\pi + \left(1 - 2q^2\right) \sin\varphi \cos q\pi \right]. \end{aligned} \tag{6.49}$$

The DC-supply current I_0 can be found using Fourier formula and Eq. (6.40) by

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)d\omega t = \frac{I_R}{2\pi}\left(\frac{\pi^2}{2p} + 2\cos\varphi - \pi\sin\varphi\right)\Big/\left(1 + \frac{L_b}{L}\right). \tag{6.50}$$

In an idealized Class-E operation mode, there is no nonzero voltage and current simultaneously, which indicates a lack of the power losses and gives an idealized collector efficiency of 100%. This implies that the DC power and the fundamental output power are equal,

$$I_0 V_{cc} = \frac{V_R^2}{2R}, \tag{6.51}$$

where $V_R = I_R R$ is the fundamental voltage amplitude across the load resistance R.

As a result, using Eqs. (6.50) and (6.51) and considering the fact that $R = V_R^2/2P_{out}$, the optimum load resistance R for the specified values of a supply voltage V_{cc} and a fundamental output power P_{out} can be obtained by

$$R = \frac{1}{2}\left(\frac{V_R}{V_{cc}}\right)^2 \frac{V_{cc}^2}{P_{out}}, \tag{6.52}$$

where

$$\frac{V_R}{V_{cc}} = \frac{1}{\pi}\left(\frac{\pi^2}{2p} + 2\cos\varphi - \pi\sin\varphi\right)\Big/\left(1 + \frac{L_b}{L}\right). \tag{6.53}$$

The normalized load-network inductance L and capacitance C as a function of the ratio L_b/L can be appropriately defined using Eqs. (6.46), (6.47), and (6.50) by

$$\frac{\omega L}{R} = p\left(1 + \frac{L_b}{L}\right)\Big/\left(\frac{\pi}{2p} + \frac{2}{\pi}\cos\varphi - \sin\varphi\right), \tag{6.54}$$

$$\omega CR = \frac{1}{q^2\left(1 + \dfrac{L_b}{L}\right)\dfrac{\omega L}{R}}. \tag{6.55}$$

The series reactance X, which may have an inductive, capacitive, or zero reactance in special cases depending on the load-network parameters, can be generally calculated using two quadrature fundamental-frequency voltage Fourier components

$$V_R = -\frac{1}{\pi}\int_0^{2\pi} [v(\omega t) + v_{L_b}(\omega t)]\sin(\omega t + \varphi)d\omega t, \tag{6.56}$$

$$V_X = -\frac{1}{\pi}\int_0^{2\pi} [v(\omega t) + v_{L_b}(\omega t)]\cos(\omega t + \varphi)d\omega t. \tag{6.57}$$

Generally, Eq. (6.45) for normalized collector voltage contains three unknown parameters, q, p, and φ, which must be determined. In a common case, the parameter q can be considered a variable, and the other two parameters, p and φ, are determined from a system of two equations resulting from applying two optimum zero-voltage and zero voltage-derivative conditions given by Eqs. (6.1) and (6.2) to Eq. (6.45). Fig. 6.5 shows the dependencies of the optimum parameters p and φ versus q for Class-E with finite DC-feed inductance when $L_b = 0$.

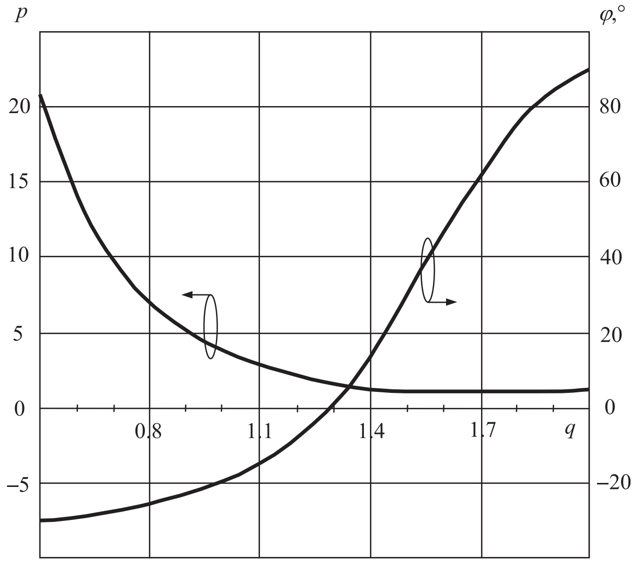


FIG. 6.5

Optimum Class-E parameters p and φ versus q.

However, there is a specific point of $q=1$ in Eq. (6.45) when the denominator of its last term becomes zero. Therefore, it is necessary to define the optimum parameters corresponding to this special point separately. Such a case when $q=1$ means that the parallel circuit comprising a DC-feed inductor L and a shunt capacitor C is tuned to the fundamental frequency. This implies in turn that the imaginary fundamental-frequency collector current component is equal to zero. Generally, the fundamental-frequency current flowing through the switch consists of two quadrature components, the amplitudes of which can be found using Fourier formulas and Eq. (6.40) by

$$\begin{aligned} I_{\mathrm{R}} &= \frac{1}{\pi}\int_0^{2\pi} i(\omega t)\sin(\omega t+\varphi)d\omega t \\ &= \frac{I_{\mathrm{R}}}{\pi}\left[\frac{\pi\cos\varphi - 2\sin\varphi}{p} + \frac{\pi}{2} - \sin 2\varphi\right], \end{aligned} \tag{6.58}$$

$$\begin{aligned} I_{\mathrm{X}} &= -\frac{1}{\pi}\int_0^{2\pi} i(\omega t)\cos(\omega t+\varphi)d\omega t \\ &= \frac{I_{\mathrm{R}}}{\pi}\left[\frac{\pi\sin\varphi + 2\cos\varphi}{p} - 2\sin^2\varphi\right] = 0. \end{aligned} \tag{6.59}$$

Hence, the optimum parameters p and φ can be calculated as

$$p = -\frac{4}{\pi\sin\varphi} = 3.84, \tag{6.60}$$

$$\varphi = \tan^{-1}\left(-\frac{2\pi}{\pi^2+8}\right) = -19.4°. \tag{6.61}$$

Based on the calculated optimum parameters p and φ as functions of q, the optimum load-network parameters of the Class-E load network with finite DC-feed inductance can be determined using Eqs. (6.52)–(6.55). The series reactance X can be calculated through the ratio of two quadrature fundamental-frequency voltage Fourier components given in Eqs. (6.56) and (6.57) as

$$\frac{X}{R}=\frac{V_\mathrm{X}}{V_\mathrm{R}}. \tag{6.62}$$

The dependences of the normalized optimum DC-feed inductance $\omega L/R$ and series reactance X/R are shown in Fig. 6.6A, while the dependences of the normalized optimum shunt capacitance ωCR and load resistance $RP_\mathrm{out}/V_\mathrm{cc}^2$ are plotted in Fig. 6.6B. Here, we can see that the subharmonic case of $q=0.5$ is very close to Class-E with shunt capacitance since the value of the normalized inductance $\omega L/R$ is sufficiently high and the variations of normalized values of ωCR and $RP_\mathrm{out}/V_\mathrm{cc}^2$ are insignificant. The value of the series reactance X changes its sign from positive to negative, which indicates that inductive reactance is followed by capacitive reactance. As a result, there is a special case of the load network with a parallel circuit and a load resistor only when $X=0$ at $q=1.412$. In this case, the maximum value of the optimum load resistance R can be provided for the same supply voltage and output power, thus simplifying the matching with the standard load of 50 Ω. In addition, the values of a DC-feed inductance L become sufficiently small, making Class-E very attractive for monolithic applications. The maximum operation frequency f_max is realized at $q=1.468$, where the normalized optimum shunt capacitance ωCR reaches its maximum.

The graphical solutions for the optimum load-network parameters can be replaced by the analytical design equations represented in terms of the simple second-order and third-order polynomial functions given by Tables 6.1–6.3 for different ranges of the parameter q from 0.6 to 1.9.[16] The maximum difference between the polynomial approximations and exact numerical solutions given in the graphic form is about 2%.

Now let us consider the particular cases of the Class-E operation mode such as a subharmonic Class-E with $q=0.5$, a parallel-circuit Class-E with $X=0$, and an even-harmonic Class-E with $q=2n$ assuming $L_\mathrm{b}=0$, which can be easily and explicitly described analytically. Then, the effect of a bondwire inductor L_b on the parameters of a Class-E load network will be described based on the example of a parallel-circuit Class-E.

6.3 Subharmonic Class-E

The basic circuit of a switchmode subharmonic Class-E power amplifier is shown in Fig. 6.7. The load network consists of a parallel inductor L, a shunt capacitor C, a series L_0C_0 resonant circuit tuned to the fundamental frequency, and a load R. The condition of a subharmonic tuning implies that the inductance L resonates with the capacitance C at half the fundamental frequency f_0. In this case, to provide an inductive reactance at the fundamental frequency seen by the device collector, it is necessary to include a series inductance L_X. Hence, the first unknown parameter q can be set to

$$q=0.5. \tag{6.63}$$

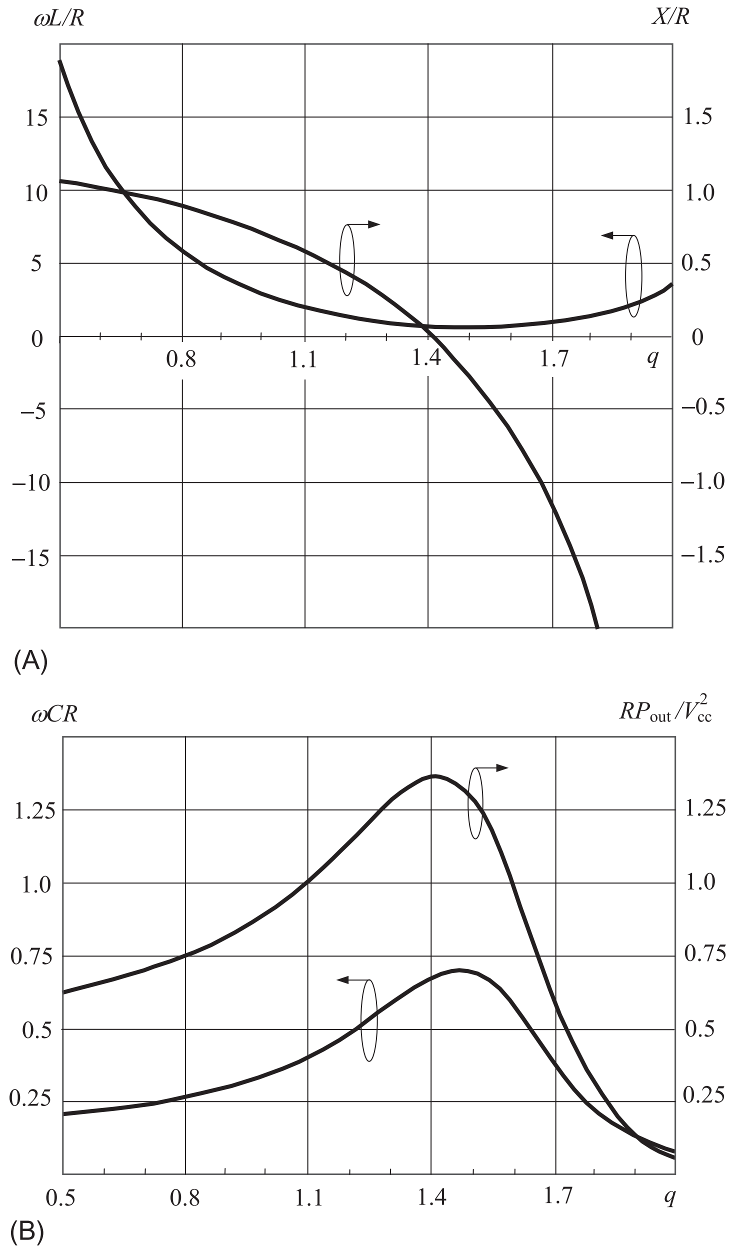


FIG. 6.6

Normalized optimum Class-E load-network parameters.

Table 6.1 Load-network parameters for $0.6 < q < 1.0$.

Parameter	Design equation
$\frac{\omega L}{R}$	$44.93q^2 - 94.32q + 52.46$
ωCR	$0.426q^2 - 0.379q + 0.3$
$\frac{P_{\text{out}}R}{V_{\text{cc}}^2}$	$-0.73q^2 + 0.411q + 1.03$
$\frac{X}{R}$	$0.74q^2 - 0.6q + 0.76$

Table 6.2 Load-network parameters for $1.0 < q < 1.65$.

Parameter	Design equation
$\frac{\omega L}{R}$	$8.085q^2 - 24.53q + 19.23$
ωCR	$-6.97q^3 + 25.93q^2 - 31.071q + 12.48$
$\frac{P_{\text{out}}R}{V_{\text{cc}}^2}$	$-2.9q^3 + 8.8q^2 - 10.2q + 5.02$
$\frac{X}{R}$	$-11.9q^3 + 42.753q^2 - 49.63q + 19.7$

Table 6.3 Load-network parameters for $1.65 < q < 1.9$.

Parameter	Design equation
$\frac{\omega L}{R}$	$16.17q^2 - 52.26q + 42.94$
ωCR	$2.55q^2 - 10.53q + 10.92$
$\frac{P_{\text{out}}R}{V_{\text{cc}}^2}$	$6.25q^2 - 24.73q + 24.56$
$\frac{X}{R}$	$-16.84q^2 + 51.38q - 39.83$

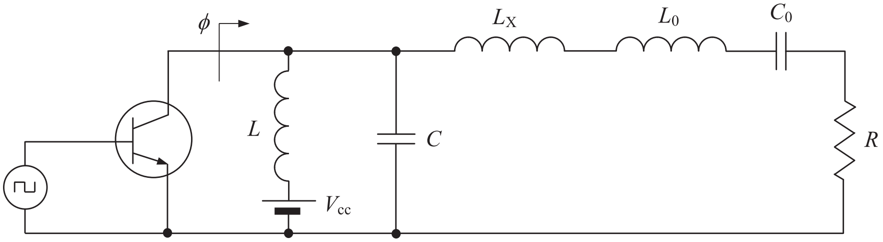


FIG. 6.7

Equivalent circuit of subharmonic Class-E power amplifier.

The coefficients C_1 and C_2 are determined from

$$C_1 = -\frac{\pi}{2} + \frac{p}{3}\sin\,\varphi, \tag{6.64}$$

$$C_2 = -1 - \frac{p}{3}\cos\varphi. \tag{6.65}$$

Then, the other two parameters φ and p can be found by applying the optimum Class-E condition given by Eqs. (6.1) and (6.2) to Eq. (6.45) and using Eqs. (6.64) and (6.65) as

$$\varphi = \tan^{-1}\left(-\frac{\pi+4}{2\pi+6}\right) = -30.2°, \tag{6.66}$$

$$p = \frac{3\pi+9}{\cos\varphi} = 21.3. \tag{6.67}$$

Fig. 6.8 shows the normalized collector (A) voltage and (B) current waveforms for idealized optimum subharmonic Class-E mode. From collector voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch, and current $i(\omega t)$ consisting of the load sinusoidal and inductive current flows through the device. The collector voltage and current waveforms are very similar to those of a Class-E with shunt capacitance.

As a result, the optimum load resistance R, finite DC-feed inductance L, and shunt capacitance C for a subharmonic Class-E mode can be obtained using Eqs. (6.52)–(6.55) by

$$R = 0.635\frac{V_{\rm cc}^2}{P_{\rm out}}, \tag{6.68}$$

$$L = 18.9\frac{R}{\omega}, \tag{6.69}$$

$$C = \frac{0.212}{\omega R}. \tag{6.70}$$

To define the phase-shifting series inductance $L_{\rm X}$, it is necessary to solve Eq. (6.57) for an imaginary component of the fundamental-frequency voltage amplitude $V_{\rm X}$, which can be simplified to

$$\frac{V_{\rm X}}{V_{\rm cc}} = \frac{4}{3\pi}\left[(C_1 - C_2)\sin\varphi + 0.5(C_1 + C_2)\cos\varphi\right] - \frac{2\sin\varphi}{\pi} + \frac{p}{6}. \tag{6.71}$$

Thus, using Eqs. (6.53), (6.64), and (6.65) yields

$$L_{\rm X} = \frac{V_{\rm X}}{V_{\rm R}}\frac{R}{\omega} = 1.058\frac{R}{\omega}. \tag{6.72}$$

The peak collector current $I_{\max}$ and peak collector voltage $V_{\max}$ can be determined from Eqs. (6.40) and (6.45) using Eq. (6.50) as

$$I_{\max} = 2.843 I_0, \tag{6.73}$$

$$V_{\max} = 3.571 V_{\rm cc}. \tag{6.74}$$

From Eqs. (6.68), (6.70), and (6.72) it follows that reducing a value of the DC-feed inductance to the case when it resonates with the shunt capacitance at half the fundamental frequency contributes to small variations of the optimum load-network parameters C, $L_{\rm X}$, and R derived for a Class-E with shunt capacitance, within approximately 10% only.

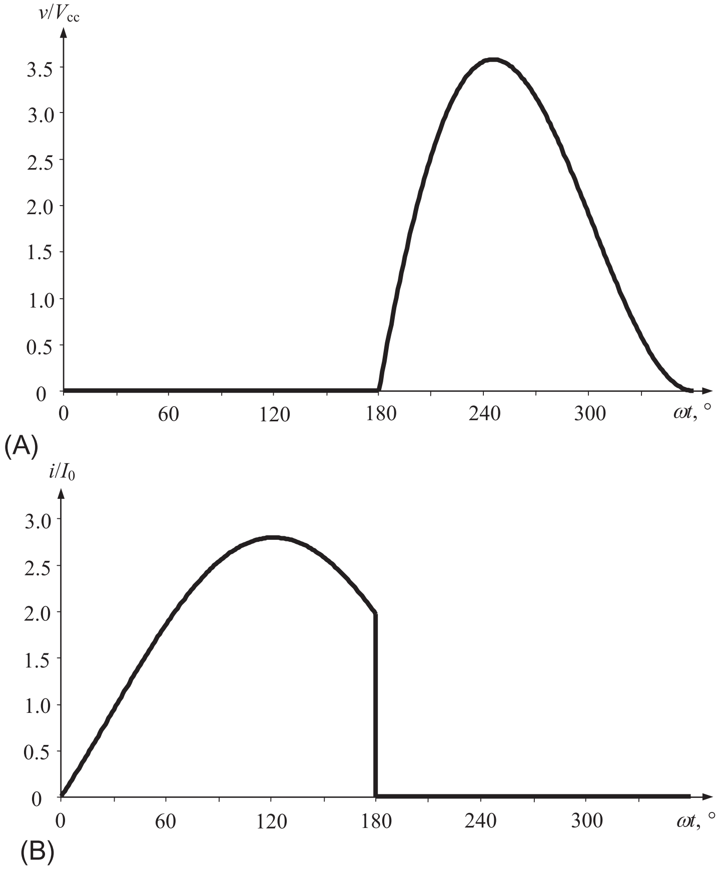


FIG. 6.8

Normalized collector (A) voltage and (B) current waveforms for idealized optimum subharmonic Class-E.

6.4 Parallel-circuit Class-E

The theoretical analysis of a switchmode parallel-circuit Class-E power amplifier using a series filter with calculation of the voltage and current waveforms and some graphical results was first published by Kozyrev.[17, 18] Let us analyze the parallel-circuit Class-E mode in more detail. The basic circuit of a switchmode parallel-circuit Class-E power amplifier is shown in Fig. 6.9A. The load network consists of a finite DC-feed inductor L, a shunt capacitor C, a series L_0C_0 resonant circuit tuned to the fundamental frequency, and a load resistor R. In this case, the switch sees a parallel connection of the load resistor R and parallel LC circuit at the fundamental frequency, as shown in Fig. 6.9B, where the real and imaginary collector fundamental-frequency current components I_X and I_R and the real collector fundamental-frequency voltage component V_R are also indicated.

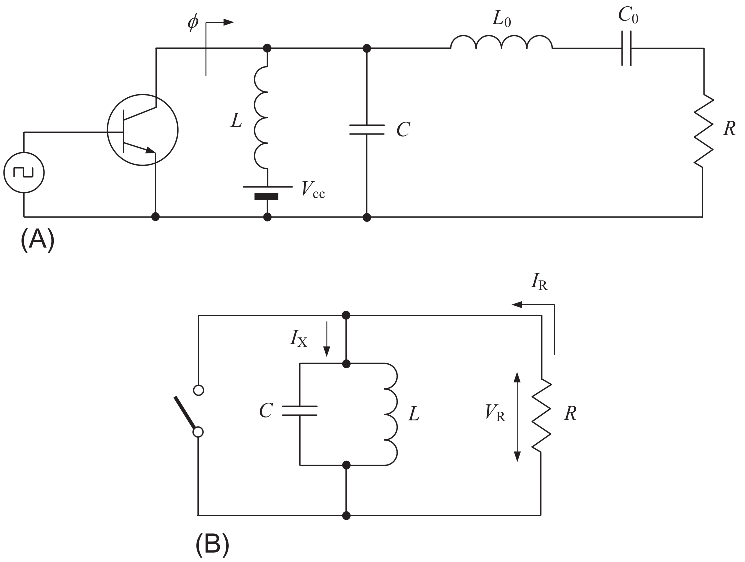


FIG. 6.9

Equivalent circuits of parallel-circuit Class-E power amplifier.

For a subharmonic Class-E mode, to compensate for the resulting phase shift provided by the finite DC-feed inductance and shunt capacitance tuned to half the fundamental frequency, it is required to include an additional series phase-shifting inductance L_X. In the case of a parallel-circuit Class-E load network without series phase-shifting reactance, because the parameter q is initially unknown, generally it is necessary to solve a system of three equations to define the three unknown parameters, q, p, and φ. In this case, first two equations are the result of applying two optimum zero-voltage and zero voltage-derivative Class-E conditions given by Eqs. (6.1) and (6.2) to Eq. (6.45). Since the fundamental-frequency collector voltage is fully applied to the load, this means that its reactive part must have zero value, resulting in an additional equation

$$V_X = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t + \varphi)d\omega t = 0. \tag{6.75}$$

Solving the system of three equations with three unknown parameters numerically gives the following values[19, 20]:

$$q = 1.412, \tag{6.76}$$

$$p = 1.210, \tag{6.77}$$

$$\varphi = 15.155°. \tag{6.78}$$

Fig. 6.10 shows the normalized (A) load current; (B) collector voltage; and (C) collector current waveforms for an idealized optimum parallel-circuit Class-E operation. From collector voltage and current waveforms, it follows that, similar to other Class-E subclasses, there is no nonzero voltage and current simultaneously. When this happens, no power loss occurs and an idealized collector efficiency of 100%

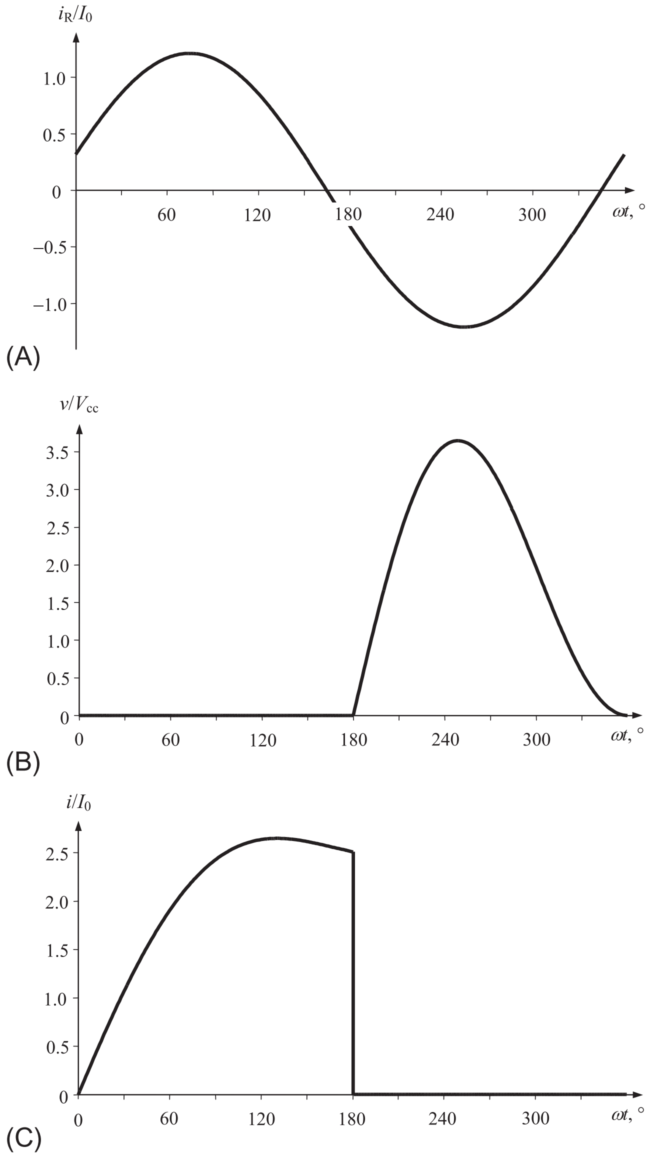


FIG. 6.10

Normalized (A) load current and collector (B) voltage and (C) current waveforms for idealized optimum parallel-circuit Class-E.

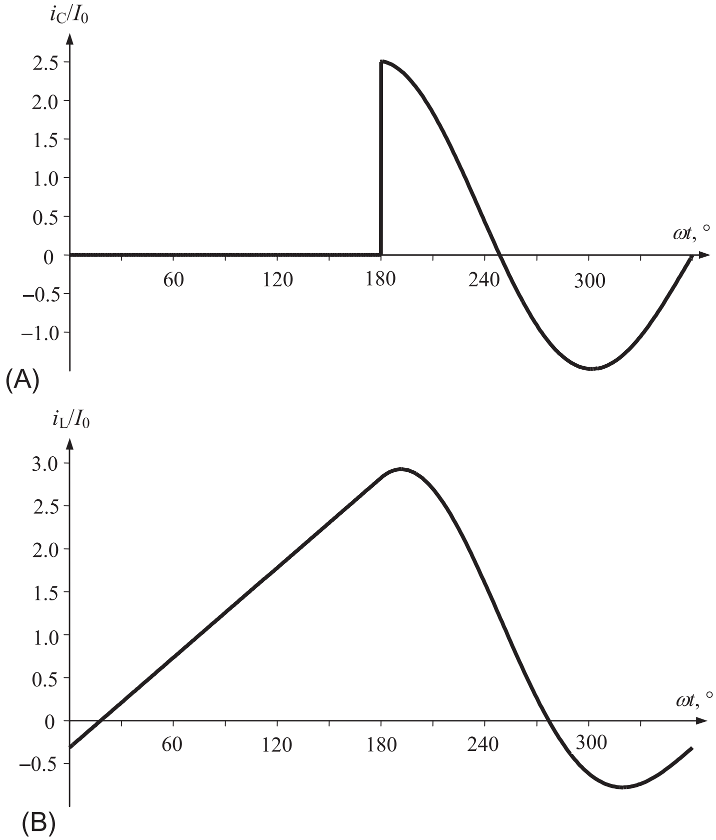


FIG. 6.11

Normalized currents flowing through load network parallel (A) capacitance and (B) inductance for idealized optimum parallel-circuit Class-E.

is achieved. The normalized currents flowing through the load-network (A) shunt capacitance C and (B) finite DC-feed inductance L for an idealized optimum parallel-circuit Class-E operation mode are given in Fig. 6.11.

Using Eqs. (6.52)–(6.55), the idealized optimum (or nominal) load resistance R, parallel inductance L, and shunt capacitance C can be appropriately obtained by

$$R = 1.365\frac{V_{cc}^2}{P_{out}}, \tag{6.79}$$

$$L = 0.732\frac{R}{\omega}, \tag{6.80}$$

$$C = \frac{0.685}{\omega R}. \tag{6.81}$$

The DC supply current I_0 can be calculated from Eq. (6.50) as

$$I_0 = 0.826 I_R. \tag{6.82}$$

The phase angle ϕ seen from the device collector at the fundamental frequency can be represented either through the ratio of two quadrature fundamental-frequency current Fourier components I_X and I_R or as a function of the load-network parameters by

$$\phi = \tan^{-1}\left(\frac{R}{\omega L} - \omega RC\right) = 34.244°. \tag{6.83}$$

If the calculated value of the optimum Class-E load resistance R is too small or differs significantly from the standard load impedance R_L (usually equal to 50 Ω), it is necessary to use an additional matching circuit to deliver maximum output power to the load. It should be noted that, among a family of the Class-E load networks, a parallel-circuit Class-E load network offers the largest value of R, thus simplifying the final matching design procedure. In this case, the first series element of such matching circuits should be the inductor to provide high impedance conditions for harmonics, as shown in Fig. 6.12.

The peak collector current $I_{\max}$ and peak collector voltage $V_{\max}$ can be determined from Eqs. (6.40) and (6.45) using Eq. (6.82) as follows

$$I_{\max} = 2.647 I_0, \tag{6.84}$$

$$V_{\max} = 3.647 V_{cc}. \tag{6.85}$$

When realizing the optimum Class-E operation mode, it is important to know the maximum operation frequency $f_{\max}$, at which such an efficient operation mode can be achieved. In this case, it needs to establish a relationship between the maximum frequency $f_{\max}$, device output capacitance C_{out}, and supply voltage V_{cc}. The device output capacitance C_{out} is the main limitation of the maximum operation frequency, as it is an intrinsic device parameter and cannot be reduced for a given active device. As a result, using Eqs. (6.79) and (6.81) when $C = C_{out}$ gives the value of the maximum operation frequency of

$$f_{\max} = 0.0798 \frac{P_{out}}{C_{out} V_{cc}^2}, \tag{6.86}$$

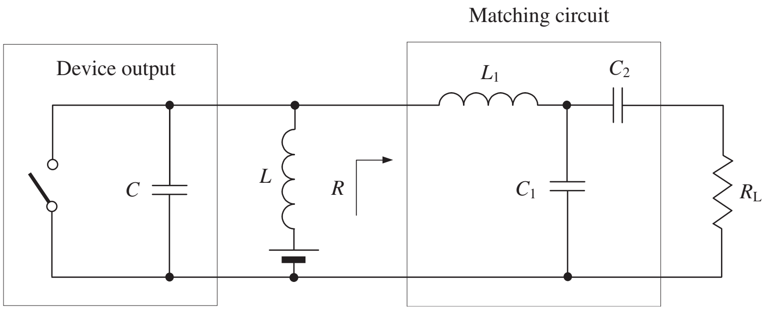


FIG. 6.12

Parallel-circuit Class-E power amplifier with lumped matching circuit.

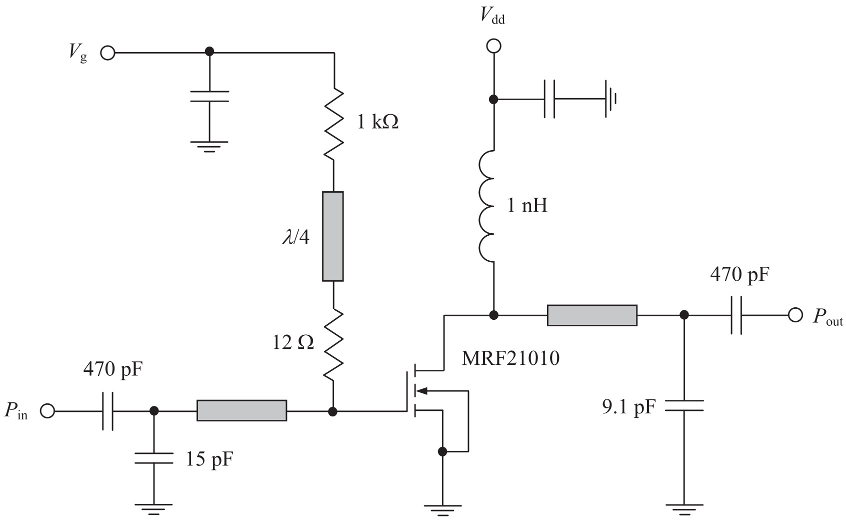


FIG. 6.13

Schematic of Class-E power amplifier with transmission-line matching.

which is 1.57 times higher than the maximum operation frequency for an optimum Class-E mode with shunt capacitance.[21] As a result, the parallel-circuit Class-E power amplifiers characterized by higher load resistance, higher maximum operating frequency, and lower DC-feed inductance are better suited to the envelope elimination and restoration (EER) transmitters, and provide much wider modulation bandwidth, better modulation linearity, and ease in practical implementation, having the same transistors.[22]

Fig. 6.13 shows the circuit schematic of a 1-GHz LDMOSFET parallel-circuit Class-E power amplifier achieving a drain efficiency of 70.4% and an output power of greater than 38 dBm at a supply voltage of 12 V.[23] In this case, the series *LC* resonant circuit is replaced by a low-pass L-type output matching circuit with a series transmission line to match the low-value optimum Class-E resistance of 3.4 Ω to a 50-Ω load, having almost zero series excessive reactance *X*. The quarterwave transmission line in the gate bias circuit provides RF isolation from the DC-voltage supply, and the 12-Ω gate resistor is required for stability.

6.5 Even-harmonic Class-E

The well-defined analytic solution based on an assumption of the even-harmonic resonant conditions when the finite DC-feed inductance and parallel capacitance are tuned to any even-harmonic component was given in Ref. 24. The load network of an even-harmonic Class-E is shown in Fig. 6.14, where the series capacitor C_X is needed to compensate for the excessive inductive reactance caused by the preliminary choice of particular load-network parameters. The value of this capacitance can be found from the consideration of two fundamental-frequency voltage quadrature components across the switch given by Eqs. (6.56) and (6.57).

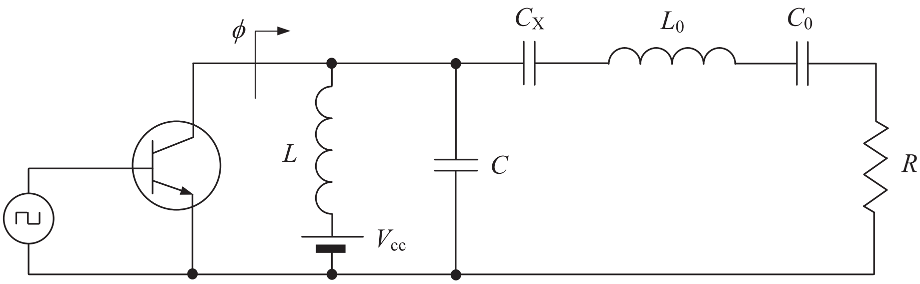


FIG. 6.14

Equivalent circuit of the even-harmonic Class-E power amplifier.

Since, for an even-harmonic Class-E operation mode, the DC-feed inductance is restricted to values that satisfy an even-harmonic resonance condition and it is assumed that the fundamental-frequency voltage across the switch and output voltage across the load have a phase difference of $\pi/2$, the two unknown parameters can be set in this particular case as

$$q = 2n, \tag{6.87}$$

$$\varphi = -90°, \tag{6.88}$$

where $n = 1, 2, 3, \ldots$.

The third parameter p can be found using an idealized optimum zero voltage-derivative condition given by Eq. (6.2) as

$$p = \frac{4n^2 - 1}{8n^2}\pi. \tag{6.89}$$

The DC supply current I_0 can be found from Eq. (6.50) when $L_b = 0$ by

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)d\omega t = \frac{1}{2(4n^2 - 1)}I_R. \tag{6.90}$$

As a result, the normalized steady-state collector voltage waveform for $\pi \le \omega t < 2\pi$ and current waveform for period of $0 \le \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{cc}} = 1 - \frac{\pi}{2}\sin\omega t + \frac{\pi}{4n}\sin(2n\omega t) - \cos(2n\omega t), \tag{6.91}$$

$$\frac{i(\omega t)}{I_0} = 2\left[\frac{8n^2}{\pi}\omega t - 4n^2 + 1 + \left(4n^2 - 1\right)\cos\omega t\right]. \tag{6.92}$$

Fig. 6.15 shows the normalized (A) load current; (B) collector voltage; and (C) collector current waveforms for an idealized optimum even-harmonic Class-E mode. If the collector voltage waveform corresponding to even-harmonic Class-E is very similar to the collector voltage waveform corresponding to Class-E with shunt capacitance, then the behavior of the collector current waveform is substantially different. So, for even-harmonic Class-E configuration, the collector current reaches its peak value, which is four times as high as the DC current, at the end of the conduction interval. Consequently,

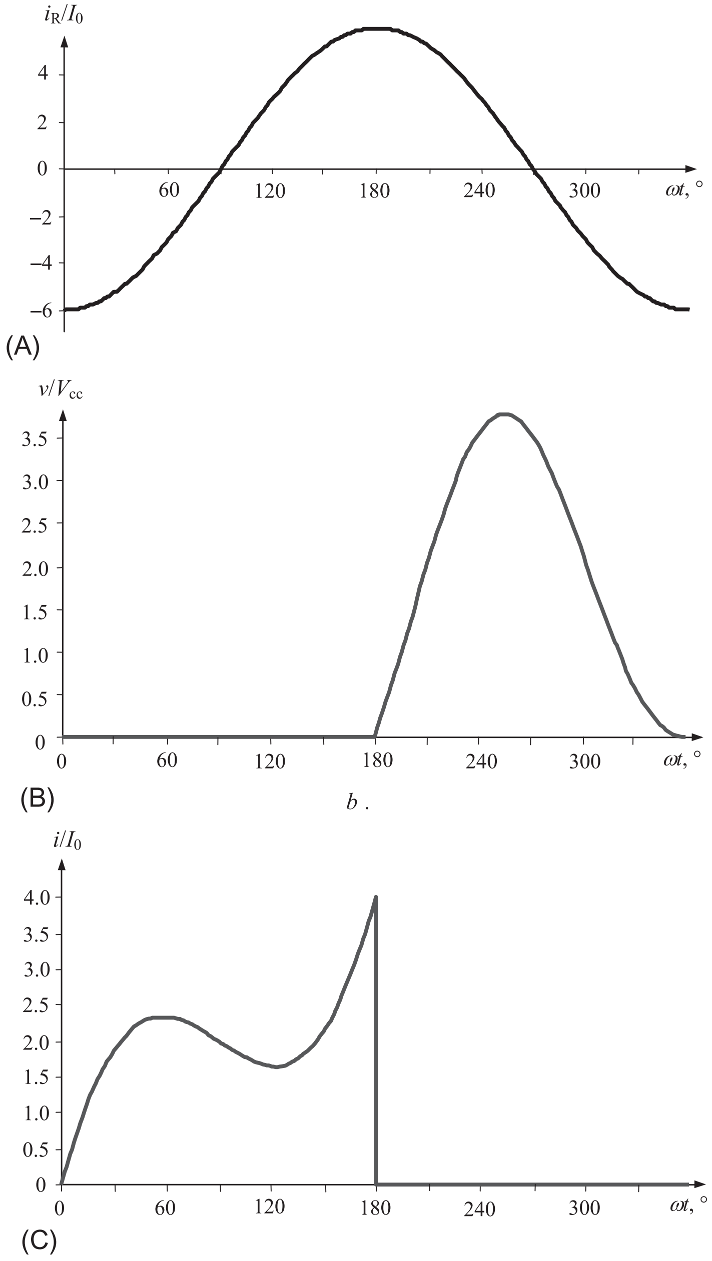


FIG. 6.15

Normalized (A) load current and collector; (B) voltage; and (C) current waveforms for idealized optimum even-harmonic Class-E.

in the case of a sinusoidal driving signal, it is impossible to provide close to the maximum collector current when the input base current is smoothly reducing to zero.

The optimum load-network parameters for the most practical case when $n = 1$ can be calculated from

$$R = \frac{1}{18}\frac{V_{\rm cc}^2}{P_{\rm out}} = 0.056\frac{V_{\rm cc}^2}{P_{\rm out}}, \tag{6.93}$$

$$L = \frac{9\pi}{8}\frac{R}{\omega} = 3.534\frac{R}{\omega}, \tag{6.94}$$

$$C = \frac{2}{9\pi}\frac{1}{\omega R} = 0.071\frac{1}{\omega R}, \tag{6.95}$$

$$C_{\rm X} = \frac{4\pi}{32 + 3\pi^2}\frac{1}{\omega R} = 0.204\frac{1}{\omega R}. \tag{6.96}$$

The main problem of an even-harmonic Class-E operation mode is a substantially small value of the load resistance R, which is over an order of magnitude smaller than that for a Class-E with shunt capacitance and much smaller than that for a parallel-circuit Class-E.

The phase angle ϕ between the fundamental-frequency voltage and current components seen by switch is equal to

$$\phi = \tan^{-1}\left[\frac{3}{4}\frac{R}{\omega L}\frac{1 + (\omega C_{\rm X}R)^2}{(\omega C_{\rm X}R)^2} - \frac{1}{\omega C_{\rm X}R}\right] = 22.302°, \tag{6.97}$$

while the maximum frequency $f_{\rm max}$, up to which an idealized optimum even-harmonic Class-E mode can be realized, is calculated from

$$f_{\rm max} = \frac{2}{\pi^2}\frac{P_{\rm out}}{C_{\rm out}V_{\rm cc}^2} = 0.203\frac{P_{\rm out}}{C_{\rm out}V_{\rm cc}^2}, \tag{6.98}$$

where $C_{\rm out}$ is the device output capacitance.

6.6 Effect of bondwire inductance

At higher frequencies when the packaged power transistors are used in hybrid power amplifier integrated circuits, it is necessary to consider the device output bondwire and lead inductance. Its influence may be significant, especially in particular cases of high output power level or low supply voltage. For instance, the effect of a bondwire inductance for even-harmonic Class-E configuration may result in unrealistically small values for the optimum load resistance and DC-feed inductance when typical values for the bondwire inductance of about 1 nH constitute most, if not all, of the required DC-feed inductance, even at ultra-high frequencies.[25]

The exact values for the idealized optimum load-network parameters are easily obtained from Eqs. (6.52)–(6.55), which were derived analytically for a generalized Class-E load network. Fig. 6.16 shows the dependences of the normalized parallel inductance $l = \omega L/R$, shunt capacitance $c = \omega CR$, and load resistance $r = RP_{\rm out}/V_{\rm cc}^2$ for a parallel-circuit Class-E mode as functions of the normalized bondwire inductance $L_{\rm b}/L$. From Fig. 6.16 it follows that an increasing effect of the bondwire

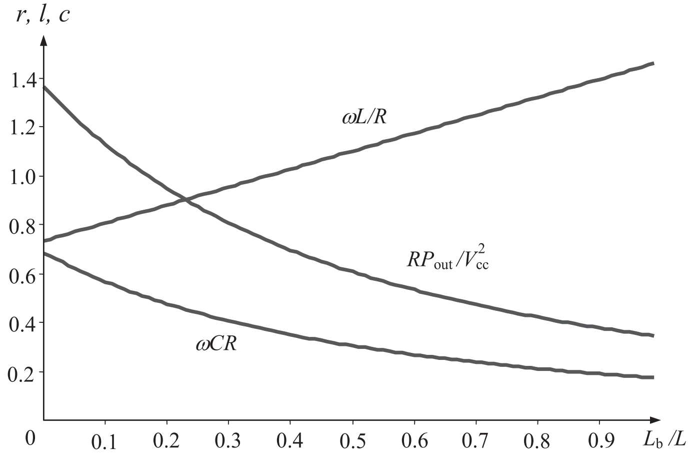


FIG. 6.16

Normalized optimum load-network parameters versus normalized bondwire inductance L_b/L for parallel-circuit Class-E.

inductance L_b leads to the significantly reduced Class-E optimum values for the load resistance R and shunt capacitance C and increased optimum value for the finite DC-feed inductance L.

6.7 Class-E with inductive impedance inverter

In many applications such as high-efficiency DC/DC power converters, electronic ballasts for fluorescent lighting, power sources for high-frequency electric process heating, or wireless power transfer for electric vehicle charging, it is necessary to provide high efficiency over a wide range of the load variation when zero-voltage switching conditions should be maintained. For an optimum resistance $R = R_{opt}$ defined for Class-E with shunt capacitance by Eq. (5.33) in Chapter 5, the switch voltage is zero; the slope of the switch voltage is zero; and the switch current does not have a step change when the switch is turned on, which corresponds to an optimum Class-E operation. For $0 < R < R_{opt}$, when the switch is turned on, the switch voltage is zero, whereas the slope of the switch voltage is negative when the switch current has a negative step change, which is referred to as suboptimum Class-E operation.[26] In both cases, the switch is turned on at zero voltage, thus resulting in zero turn-on switching loss and thereby high efficiency. In contrast, for $R > R_{opt}$, the switch voltage has a step change at turn-on, resulting in turn-on switching loss, and the switch current has a spike at turn-on that may destroy the transistor. To overcome this impedance limitation, the Class-E power amplifier can be improved by adding an inductive impedance inverter to keep the load resistance less than R_{opt}.[27]

Fig. 6.17A shows the simplified schematic of a Class-E power amplifier with inductive impedance inverter, where L_1 is an RF choke having an infinite inductance, although a finite DC-feed inductance can also be used. The load network consists of a shunt capacitor C_1, a series capacitor C_2, a series inductor L_2, and an inductor L_3 connected in parallel with the load resistance R_L and operated as an

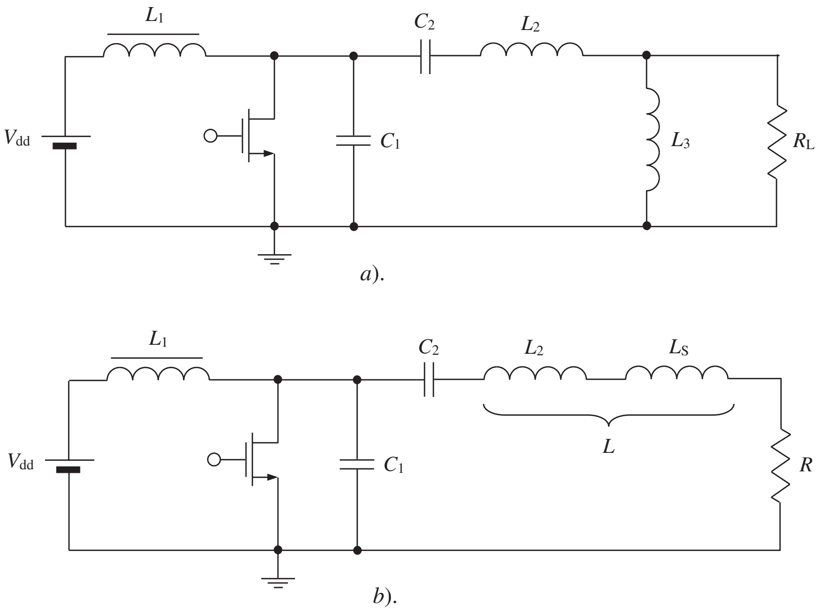


FIG. 6.17

Basic circuits of Class-E power amplifier with inductive impedance inverter.

impedance inverter. To characterize this inverter, the parallel L_3R_L circuit should be transformed into its equivalent series L_SR circuit shown in Fig. 6.17B, resulting in

$$q_B = \frac{R_L}{X_{L3}} = \frac{X_{LS}}{R}, \tag{6.99}$$

$$R = \frac{R_L}{1 + \left(\frac{R_L}{X_{L3}}\right)^2} = \frac{R_L}{1 + q_B^2}, \tag{6.100}$$

$$X_{LS} = \frac{X_{L3}}{1 + \left(\frac{X_{L3}}{R}\right)^2} = \frac{q_B^2 X_{L3}}{1 + q_B^2}, \tag{6.101}$$

where $X_{L3} = \omega L_3$ and $X_{LS} = \omega L_S$.

Fig. 6.18 shows the characteristics of the impedance inverter given by Eqs. (6.100) and (6.101). In Fig. 6.18A, as the load resistance R_L increases from zero to infinity, the resistance R first increases from zero to its maximum value $R_{max} = X_{L3}/2$ (that occurs at $R_L = X_{L3}$) and then decreases to zero, according to Eq. (6.100). From Eqs. (6.100) and (6.101), it follows that for $q_B^2 \gg 1$ (or $R_L^2 \gg X_{L3}^2$), $R \approx X_{L3}^2/R_L$ and $X_{LS} \approx X_{L3}$. Since R is inversely proportional to R_L for $q_B^2 \gg 1$, the circuit acts as an impedance inverter. According to Fig. 6.18B, the equivalent series reactance $X_{LS} = \omega L_S$ increases from zero to $X_{L3} = \omega L_3$ (or L_S increases from zero to L_3) as the load resistance R_L increases. Therefore, the overall inductance of the series-resonant circuit $L = L_2 + L_S$ increases with R_L, while the resonant frequency of the

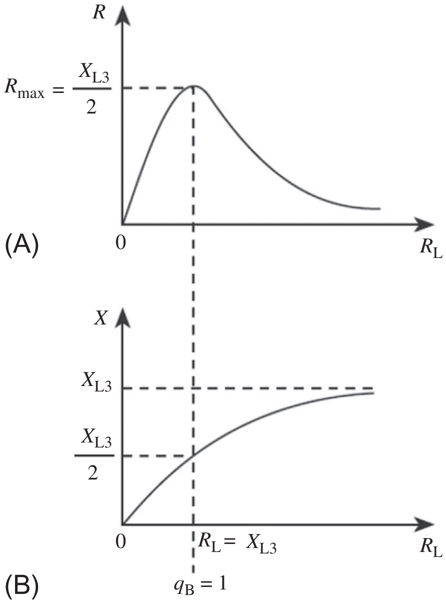


FIG. 6.18

Impedance characteristics of inductive impedance inverter.

series-resonant circuit $f_1 = 1/2\pi\sqrt{C_2(L_2 + L_S)}$ decreases with R_L. As a result, zero-voltage switching conditions can be satisfied over a wide range of the load resistance R_L at a fixed frequency.

Generally, if $R_{opt} = R_{max}$, zero-voltage switching can be obtained at any value of the load resistance R_L, because $R \leq R_{max}$ for $0 \leq R_L \leq \infty$, according to Fig. 6.18A. However, if $R_{opt} < R_{max}$, zero-voltage switching can be obtained for two ranges of R_L: $0 \leq R_L \leq R_{Lmax}$ and $R_{Lmin} \leq R_L \leq \infty$ when in both these ranges $R_L \leq R_{opt}$, as shown in Fig. 6.19. At the same time, for $R_{Lmax} \leq R_L \leq R_{Lmin}$, the switch is turned on at nonzero voltage because $R > R_{opt}$, which results in a turn-on loss, reducing efficiency.

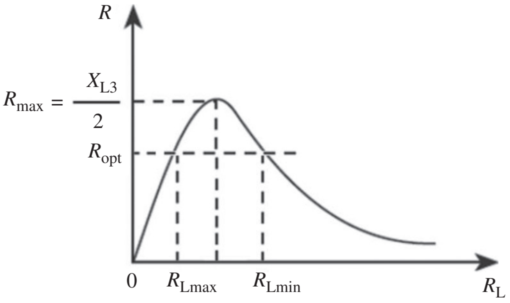


FIG. 6.19

Three impedance ranges of load impedance R_L when $R_{opt} < R_{max}$.

The optimum load-network parameters of the Class-E power amplifier with shunt capacitance shown in Fig. 6.17B for any values of the loaded quality factor Q_L can be calculated according to

$$R_{opt} = \frac{bV_{dd}^2}{P_{out}}, \tag{6.102}$$

$$C_1 = \frac{c}{\omega R_{opt}}, \tag{6.103}$$

$$C_2 = \frac{d}{\omega R_{opt}}, \tag{6.104}$$

$$L = \frac{eR_{opt}}{\omega}, \tag{6.105}$$

where the values of the normalized coefficients b, c, d, and e are given in Table 6.4.[28] In this case, the normalized drain peak voltage varies in the range of 3.732 for zero Q_L to 3.56 for infinite Q_L.

To obtain the corresponding load-network parameters of a Class-E power amplifier with inductive impedance inverter shown in Fig. 6.17A, from Eq. (6.100) it follows that

$$q_{Bmin} = \sqrt{\frac{R_{Lmin}}{R_{opt}} - 1}. \tag{6.106}$$

Then, using Eq. (6.99),

$$X_{L3} = \frac{R_{Lmin}}{q_{Bmin}}, \tag{6.107}$$

resulting in

$$L_3 = \frac{X_{L3}}{\omega}. \tag{6.108}$$

Table 6.4 Load-network parameters of Class-E power amplifier with inductive impedance inverter versus loaded quality factor Q_L.

Q_L	$b = \frac{P_{out}R}{V_{dd}^2}$	$c = \omega RC_1$	$d = \omega RC_2$	$e = \frac{\omega L}{R}$
0	0.3587	0.2177	∞	1.788
1	0.4008	0.2204	2.104	2.104
2	0.4570	0.2190	0.7124	2.850
3	0.4916	0.2150	0.4166	3.750
5	0.5249	0.2067	0.2269	5.673
7	0.5401	0.2017	0.1560	7.642
10	0.5514	0.1971	0.1062	10.62
20	0.5644	0.1909	0.05149	20.60
100	0.5744	0.1851	0.01006	100.58
∞	0.5768	0.1836	0	∞

From Eqs. (6.99) and (6.101),

$$X_{\mathrm{LSmin}} = q_{\mathrm{Bmin}} R_{\mathrm{opt}} = \frac{X_{\mathrm{L3}} q_{\mathrm{Bmin}}^2}{1 + q_{\mathrm{Bmin}}^2}, \tag{6.109}$$

$$L_{\mathrm{Smin}} = \frac{X_{\mathrm{LSmin}}}{\omega}. \tag{6.110}$$

Consequently,

$$L_2 = L - L_{\mathrm{Smin}}. \tag{6.111}$$

To achieve zero-voltage switching at any value of R_{L}, one can assume $q_{\mathrm{B}} = 1$ at R_{Lopt}. In this case, Eqs. (6.99)–(6.106), (6.110), and (6.111) remain the same. At the same time, from Eqs. (6.106), (6.107), and (6.109), it follows that

$$X_{\mathrm{L3}} = R_{\mathrm{Lopt}} = 2R_{\mathrm{opt}}, \tag{6.112}$$

$$X_{\mathrm{LSmin}} = \frac{X_{\mathrm{L3}}}{2} = R_{\mathrm{opt}}. \tag{6.113}$$

The fabricated Class-E power amplifier with inductive impedance inverter, whose simplified circuit schematic is shown in Fig. 6.17A, was designed to operate at 1 MHz based on an IRF620 MOSFET with the following optimum load-network parameters for $Q_{\mathrm{L}} = 5$: $L_1 = 100\,\mu\mathrm{H}$, $C_1 = 1.35\,\mathrm{nF}$, $C_2 = 1.8\,\mathrm{nH}$, $L_2 = 15\,\mu\mathrm{H}$, and $L_3 = 6.45\,\mu\mathrm{H}$. Fig. 6.20A shows the measured output power P_{o} as a function of the load resistance R_{L}, which is reduced with increasing R_{L}, with a maximum efficiency of 96% at $R_{\mathrm{Lopt}} = 40\,\Omega$ for $V_{\mathrm{dd}} = 28\,\mathrm{V}$.[27] The peak values of the switch voltage V_{SM} and the switch current I_{SM} are reduced with increasing load resistance R_{L}, being almost independent of R_{L} for $R_{\mathrm{L}} > 3R_{\mathrm{Lopt}} = 120\,\Omega$, as shown in Fig. 6.20B.

The circuit schematic of a Class-E power amplifier with inductive impedance inverter designed for practical implementation using a 30-W GaN high-electron-mobility transistor CGH35030F device is shown in Fig. 6.21A, with the corresponding test board shown in Fig. 6.21B.[29, 30] Here, the RF choke is replaced by a finite DC-feed inductance to improve bandwidth performance, and the 12.5-nH coil self-resonates between the second and third harmonics, providing high impedance conditions for both to maximize efficiency over a wide range of load impedances. Fig. 6.22A shows the efficiency variation over a wide range of R_{L} from 15 to 400 Ω when the drain efficiencies of 76% and 70% were measured at power backoffs as high as 9.6 and 10 dB, respectively. At the same time, the drain efficiency and power-added efficiency (*PAE*) remain above 75% across the frequency ranges of 150 and 130 MHz, respectively. The drain efficiency achieves a maximum value of 85% at 750 MHz with an output power of 41.4 dBm. Using a Class-E/F$_2$ mode when a second-harmonic parallel *LC* circuit is connected in series to the drain, the output power control range for which the drain efficiency exceeds 70% is enhanced by 2.7 dB.[31]

6.8 Load network with transmission lines

At ultra-high and microwave frequencies, generally all inductances in the load-network circuits of power amplifiers are normally replaced by transmission lines to minimize power losses and effects of parasitic capacitances. The load-network circuit can be composed with any types of transmission

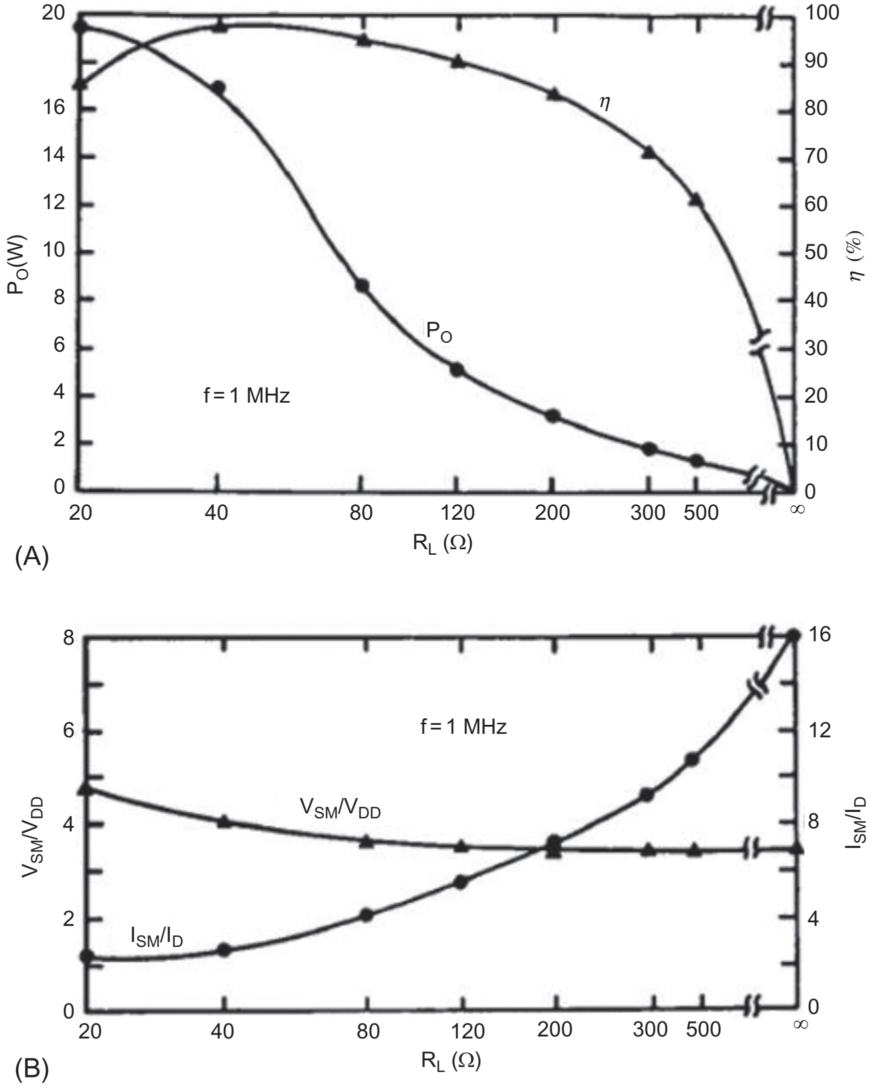


FIG. 6.20

Measured (A) output power and efficiency and (B) normalized switch voltage and current versus load resistance R_L.[27]

lines, including open-circuit or short-circuit stubs to provide the required impedance-matching and harmonic-termination conditions. In some cases, for example, for compact small-size power amplifier modules designed for handset wireless transmitters, the series microstrip lines and shunt chip capacitors are usually used in the external output matching circuits. In this case, a lumped-distributed Class-E

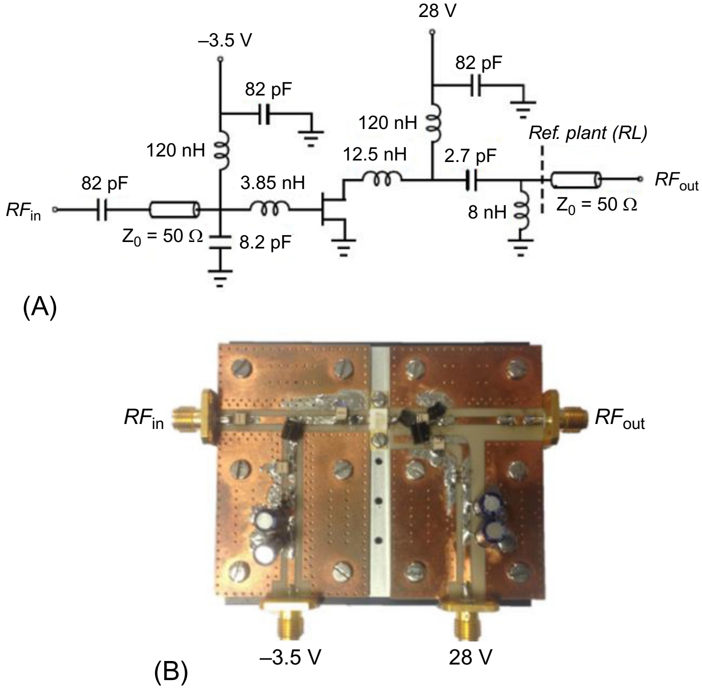


FIG. 6.21

Circuit schematic and test board of Class-E power amplifier with grounded inductance.[29]

load-network structure with short-length transmission lines can be very effective and helpful to increase the efficiency of a microwave power amplifier.[32] Generally, the transmission-line modeling (TLM) technique in the time domain can be used to simulate the Class-E power amplifier when the load-network elements can be modeled by open-circuit and short-circuit stubs.[33] However, the TLM technique cannot be used to evaluate the required optimum parameter values directly to obtain the desired performance, and optimum conditions cannot be ensured. In the frequency domain, idealized calculation of collector voltage and current waveforms required for an optimum Class-E mode implies the availability of an infinite number of harmonics with their optimum amplitudes and phases in the output spectrum.

First, consider the contribution of any harmonic component to the collector waveforms corresponding to a parallel-circuit Class-E mode similar to that for a Class-E with shunt capacitance. The Fourier-series expansion of the collector voltage $v(\omega t)$ is defined as

$$v(\omega t) = V_{cc} + \sum_{k=1}^{\infty} [V_{Rk} \sin k(\omega t + \varphi) + V_{Xk} \cos k(\omega t + \varphi)], \tag{6.114}$$

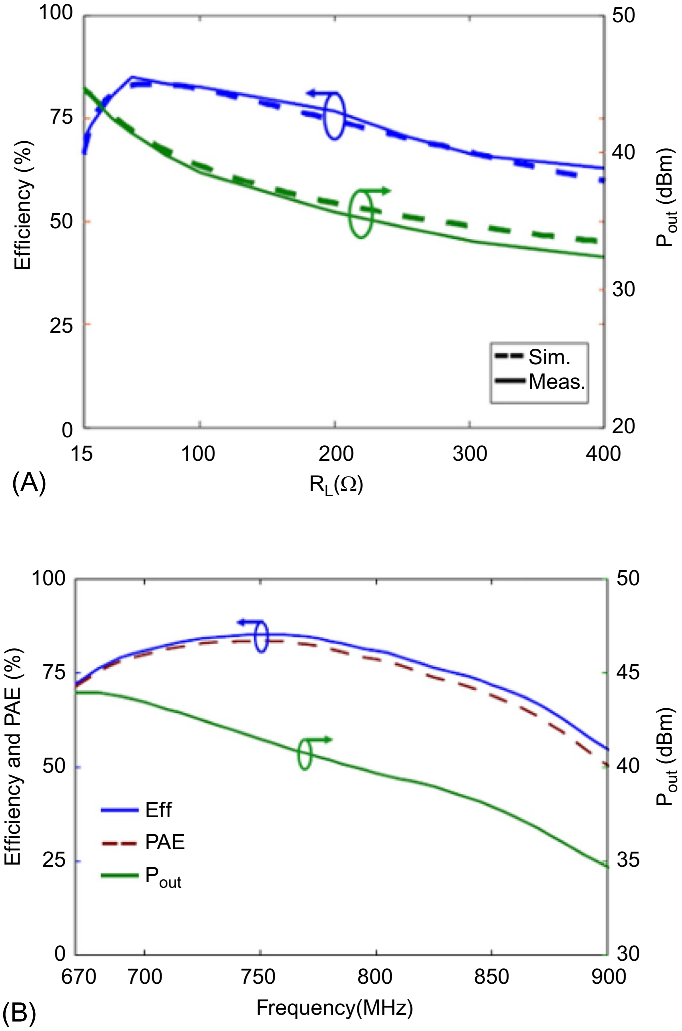


FIG. 6.22

Measured efficiency and output power versus (A) load resistance and (B) frequency.[29]

where the DC supply voltage V_{cc} and the real and imaginary harmonic components V_{Rk} and V_{Xk} are obtained, respectively, from

$$V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)d\omega t, \tag{6.115}$$

$$V_{Rk} = \frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin k(\omega t + \varphi)d\omega t, \tag{6.116}$$

$$V_{Xk} = \frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos k(\omega t + \varphi)d\omega t. \tag{6.117}$$

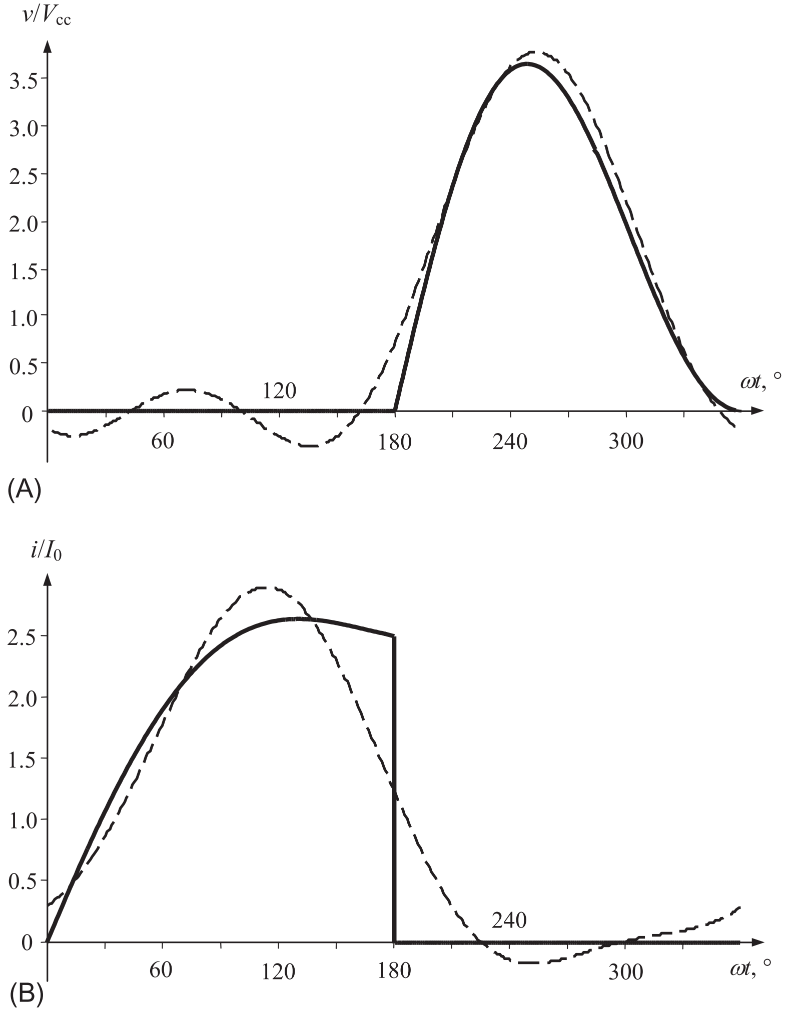


FIG. 6.23

Two-harmonic approximation to parallel-circuit Class-E mode.

The same Fourier analysis can be applied to the collector current $i(\omega t)$. Fig. 6.23 shows the normalized ideal collector (A) voltage and (B) current waveforms plotted by solid lines, where I_0 is the DC current. In this case, as clearly seen from Fig. 6.23, a good approximation to parallel-circuit Class-E mode can be obtained with only the fundamental-frequency and second-harmonic components, fully determining the collector voltage and current waveforms, which are indicated by dashed lines. The same conclusion, which is very important for practical design of microwave Class-E power amplifiers, was obtained for a Class-E mode with shunt capacitance.[34] Consequently, the high-efficiency parallel-circuit Class-E power amplifier circuit can also be effectively used in monolithic microwave integrated

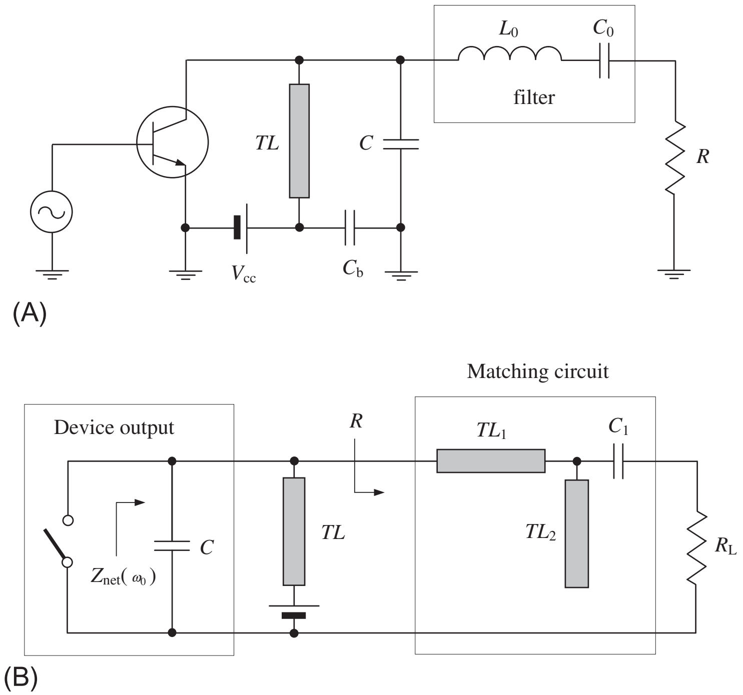


FIG. 6.24

Equivalent circuits of transmission-line parallel-circuit Class-E power amplifier.

circuit (MMIC) design, provided the optimum Class-E conditions at the fundamental frequency and second harmonic are fulfilled.

In the first step, the parallel inductance L at microwaves should be replaced by a short-length short-circuited transmission line TL shown in Fig. 6.24A according to

$$Z_0 \tan\theta = \omega L, \tag{6.118}$$

where Z_0 and θ are the characteristic impedance and electrical length of the transmission line TL, respectively.[35] To approximate the idealized optimum parallel-circuit Class-E operation conditions for a microwave power amplifier, it is necessary to design the load network satisfying the required idealized optimum input impedance of the load network at the fundamental frequency according to

$$Z_{net}(\omega_0) = \frac{R}{1 - j\tan 34.244^\circ}, \tag{6.119}$$

which can be obtained from Eqs. (6.80), (6.81), and (6.83).

Using Eq. (6.80), defining the idealized optimum (or nominal) parallel inductance L for a parallel-circuit Class-E mode, Eq. (6.118) can be rewritten as

$$\tan\theta = 0.732\frac{R}{Z_0}. \tag{6.120}$$

In practical circuits, when the impedance transformation between the optimum Class-E load resistance R and standard load resistance of 50 Ω is required, the series L_0C_0 filter should be replaced by the output matching circuit, the input impedance of which needs to be sufficiently high at the second- and higher-order harmonics. For example, the series L_0C_0 filter can be replaced by a lumped T-transformer containing a series inductor and two (shunt and series) capacitors. For a transmission-line realization, the output matching circuit can be composed with any types of the transmission lines, including open-circuit or short-circuit stubs to provide the required matching and harmonic-termination conditions. However, to maintain the optimum switching conditions at the fundamental frequency, such an output matching circuit should contain the series transmission line as the first element, as shown in Fig. 6.24B.

Fig. 6.25A shows an example of the transmission-line Class-E load network of a two-stage 1.75-GHz GaAs HBT power amplifier with an output power of 33 dBm, which was designed to use in a cellular handset transmitter and includes the series microstrip line with two shunt chip capacitors.[19, 36] However, because of the finite electrical lengths of the transmission lines, it is impossible to simultaneously realize the required inductive impedance at the fundamental frequency with the purely capacitive reactances at higher-order harmonics. For example, at the second harmonic, the real part of the load-network impedance $Z_{net}(2\omega_0)$ is sufficiently high, as shown in Fig. 6.25B. Nevertheless, even such an approximation provides a good proximity to the parallel-circuit Class-E operation mode, resulting in a high operating efficiency of the power amplifier. In this case, there is no need to use an additional RF choke for DC-supply current, because its function can be performed by the same short-length parallel microstrip line, which is necessary to provide an optimum inductive impedance at the fundamental frequency.

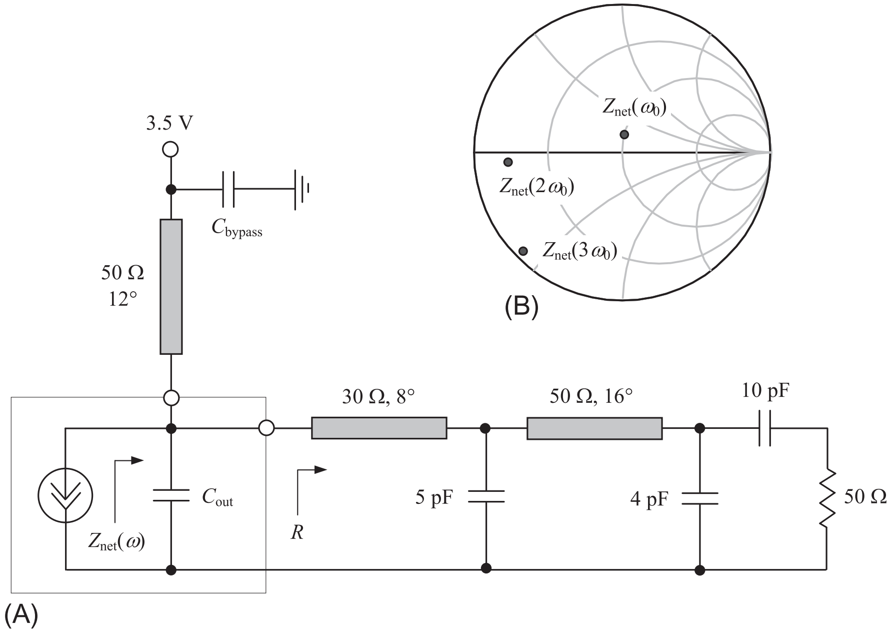


FIG. 6.25

Transmission-line load network of parallel-circuit Class-E power amplifier for handset application.

Comparison of the different Class-E load network topologies in terms of their parameters shows a clear preference of the parallel-circuit Class-E mode, especially for low supply voltage application with high level of circuit integration. For such a load network, the DC-feed inductance L is sufficiently low, which can be provided by a short-length transmission line, and an optimum load resistance R (for the same output power and supply voltage) is greater by approximately 2.4 times and 24 times compared to the Class-E with shunt capacitance and even-harmonic Class-E, respectively. In addition, the parallel-circuit Class-E configuration can be easily implemented in a high-efficiency broadband high-power or low-voltage power amplifier design. In this case, it is only necessary to satisfy the required phase angle seen by the device collector at the fundamental frequency and to choose the proper low-Q_L-factor of the series resonant L_0C_0 circuit.[37, 38]

Fig. 6.26A shows the circuit schematic and module structure of a 500-MHz single-stage parallel-circuit Class-E LDMOSFET power amplifier with a supply voltage of 28 V, an output power of 42 dBm, a linear power gain of 15 dB, and a *PAE* of 67%.[19] The input and output matching circuits represent T-type transformers with series 50-Ω microstrip lines fabricated using a laminate substrate with a dielectric permittivity of 4.7 and a thickness of 0.4 mm. The required fundamental-frequency load-network phase angle is provided with the device output capacitance and parallel 50-Ω microstrip line with an electrical length of 25 degrees. The overall size of a hybrid module is $45 \times 20\,\text{mm}^2$, including a eutectic-attached 1.25-μm LDMOSFET die with a total gate width of 28×1.44 mm, which is characterized by a small-signal transconductance $g_m = 0.6$ A/V and a transition frequency $f_T = 4.5$ GHz. The die is connected to the input microstrip line by four bondwires and to the output microstrip line by five bondwires, each having a length of 1.5 mm.

The circuit schematic of a two-stage InGaP/GaAs HBT power amplifier intended to operate in the handset WCDMA transmitters is shown in Fig. 6.26B.[37] The MMIC part of this power amplifier contains the transistors with emitter areas of the first and second stages as large as 540 and 3600 μm^2, respectively, input and interstage matching circuits, and bias circuits on a die with a total area of $<1\,\text{mm}^2$. Without any tuning of the output matching circuit, a saturated output power >30 dBm and a PAE greater than 50% were obtained. Using high-Q capacitors in output matching circuit can improve the power-added efficiency by about 8%. At the same time, this power amplifier without any additional tuning could achieve high-linearity performance for WCDMA band (1920–1980 MHz) at a 3.5-dB backoff output power of 27 dBm with a power gain of 22.6 dB and a sufficiently high efficiency. The measured PAE reached a value of 38.3% at center bandwidth frequency of 1.95 GHz with an adjacent channel leakage power ratio (*ACLR*) of −37 dBc at a 5-MHz offset.

As an example of close proximity to the idealized optimum parallel-circuit Class-E mode, the simulated collector (A) voltage and (B) current waveforms shown in Fig. 6.27 and collector efficiency of about 90% were achieved for a 1.75-GHz InGaP/GaAs HBT power amplifier at a supply voltage of 5 V.[20] During off-state operation mode, only the current flowing through the device collector capacitance determines the total collector current. The collector voltage waveform is very similar to the ideal one, with a peak factor of about 3. The main reason for efficiency degradation from an ideal 100% is a high value of the saturation voltage of about 0.5–0.8 V, which can result in 15%–20% collector efficiency reduction for a supply voltage of 3.5 V. Generally, further decrease in collector efficiency in a real circuit can be explained by violation of the required optimum impedance conditions because of transmission-line effect at second- and higher-order harmonics, device finite switching time and parasitics, and power losses in the load network.

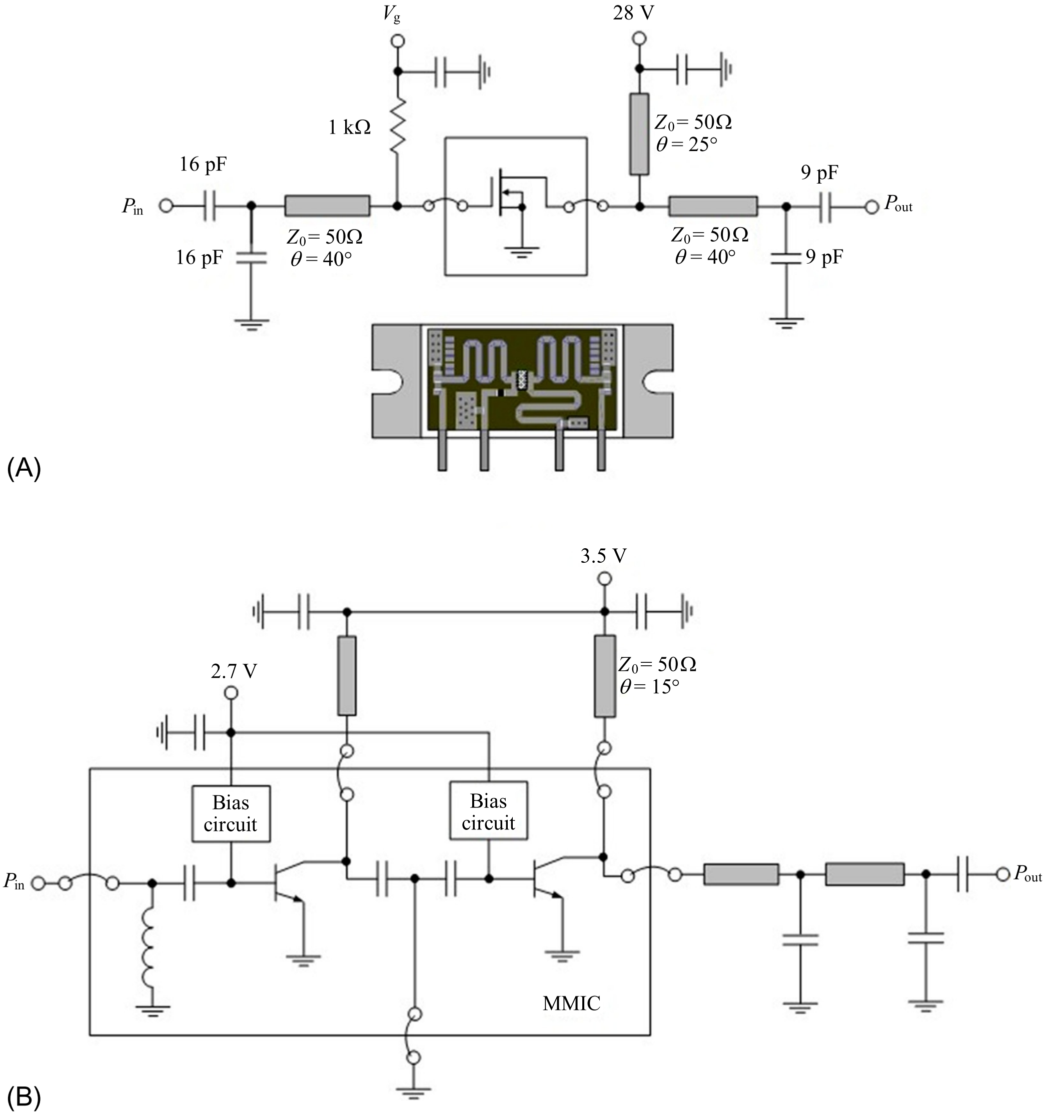

V_g
28 V
1 kΩ
$Z_0 = 50\Omega$
$\theta = 25°$
16 pF
9 pF
P_{in}
P_{out}
$Z_0 = 50\Omega$
$\theta = 40°$
16 pF
$Z_0 = 50\Omega$
$\theta = 40°$
9 pF
(A)
3.5 V
2.7 V
$Z_0 = 50\Omega$
$\theta = 15°$
Bias circuit
Bias circuit
P_{in}
P_{out}
MMIC
(B)

FIG. 6.26

Circuit schematics and module design of parallel-circuit Class-E high-voltage LDMOSFET and low-voltage GaAs HBT power amplifiers.

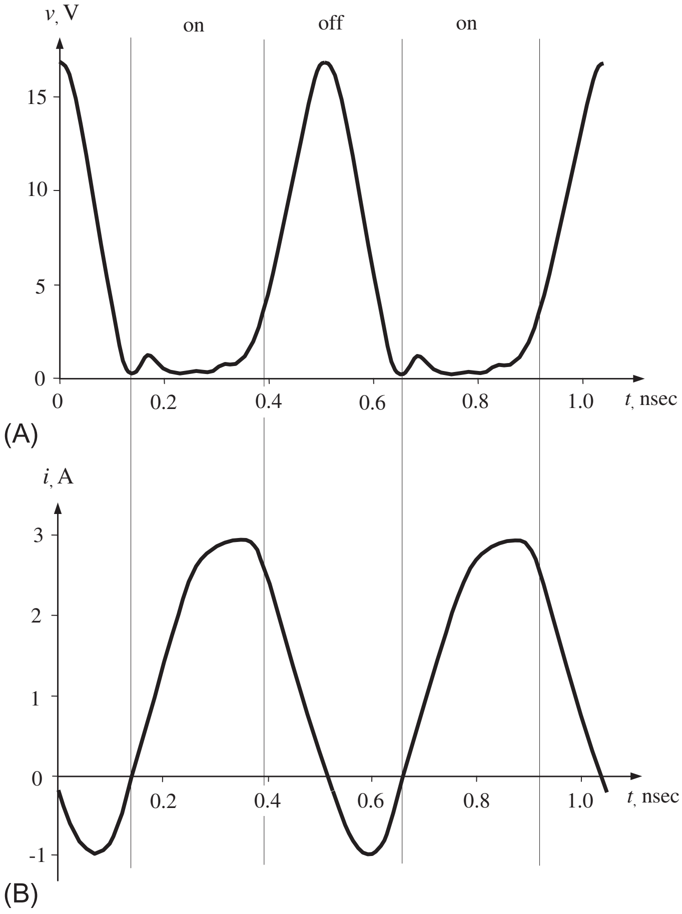


FIG. 6.27

Simulated collector (A) voltage and (B) current waveforms of transmission-line parallel-circuit Class-E low-voltage InGaP/GaAs HBT power amplifier.

The suboptimum Class-E design techniques can also be applied to millimeter-wave power amplifiers implemented using a silicon-based technology when a high-power gain can be achieved using a cascode configuration. Fig. 6.28 shows the circuit schematic of a *W*-band cascode power amplifier using a parallel-circuit Class-E approximation, which is implemented in a 0.13-μm SiGe Bi CMOS process with SiGe HBT with f_T and f_{max} of 300 and 500 GHz, respectively.[39] The cascode configuration allows to protect devices from breakdown for the increased voltage swing corresponding to Class-E mode. In this case, the optimum parallel-circuit Class-E capacitance is determined entirely by the parasitic output capacitance of the common-base stage representing a sum of the collector-substrate and collector-base capacitances, with RF shorted substrate and base nodes. The Class-E load network with a low-pass response consists of a short series microstrip line of 10 degrees and an RF shorted parallel microstrip line of 60 degrees to provide the required inductive impedance at the fundamental and the

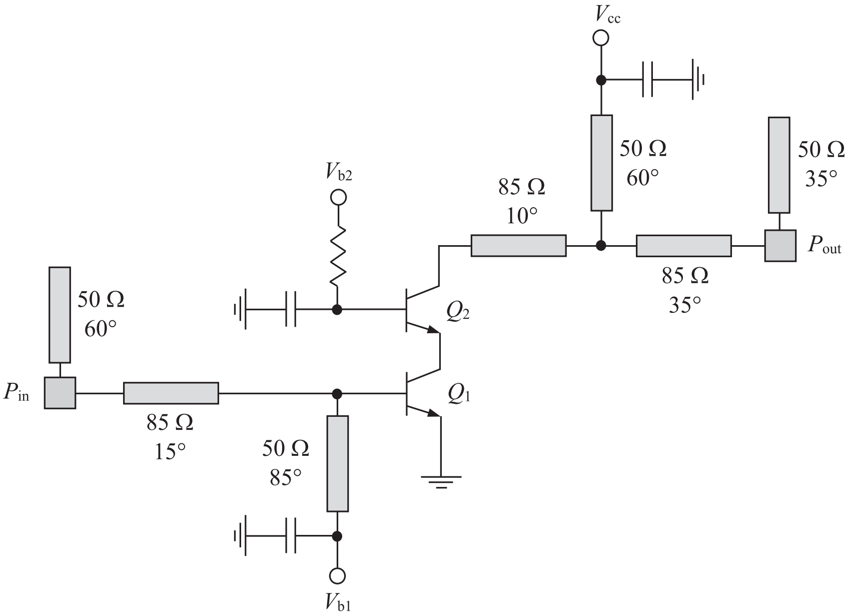


FIG. 6.28

Circuit schematic of *W*-band cascode Class-E SiGe HBT power amplifier.

output L-type matching section consisting of a series microstrip line of 35 degrees and an open-circuit microstrip stub of 35 degrees to compensate for the parasitic capacitance of the output RF pad and to provide the output impedance matching with a standard 50-Ω load. As a result, a peak *PAE* of 40.4% and a saturated output power of 17.7 dBm were achieved at 93 GHz with a DC-supply voltage of 4 V. With the bias increased to 5.2 V, the peak *PAE* and saturated output power at 93 GHz were measured to be 37.6% and 19.3 dBm, respectively.

6.9 Operation beyond maximum Class-E frequency

To obtain an optimum Class-E mode beyond its maximum operation frequency when the shunt capacitance becomes excessive, the value of the parallel DC-feed inductor has to be chosen so as to compensate for the negative effect of this excessive capacitance not only at the fundamental frequency, but also at the higher-order harmonic components. Fig. 6.29A shows the circuit schematic of a parallel-circuit Class-E power amplifier, where C is the nominal Class-E capacitance, C_{ex} is the excess capacitance, and L_{new} is the required frequency-varying DC-feed inductance.[40] Adding the susceptances of C_{ex} and L_{new} should result in the inductive admittance of an optimum Class-E DC-feed inductance L according to

$$\frac{1}{j\omega L} = j\omega C_{ex} + \frac{1}{j\omega L_{new}}, \tag{6.121}$$

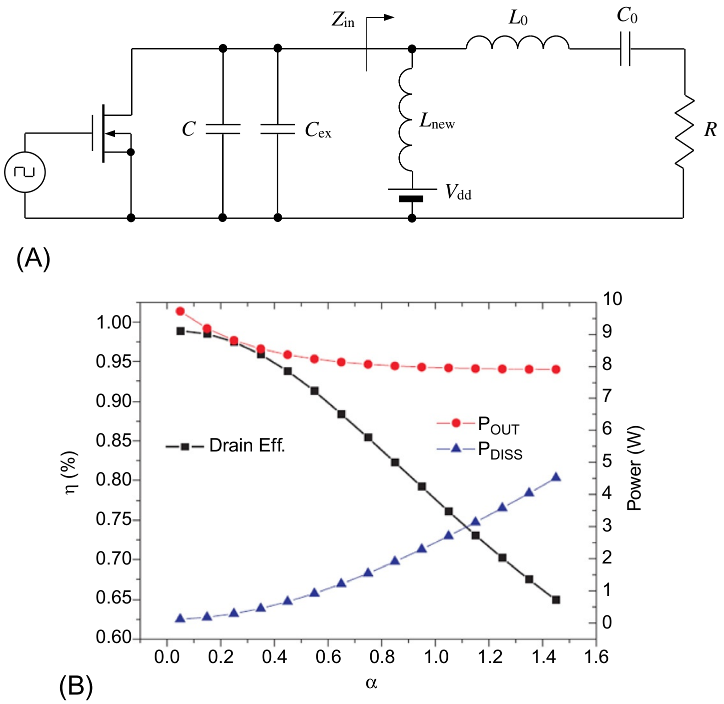


FIG. 6.29

Parallel-circuit Class-E power amplifier with excess capacitance.

from which it follows that

$$L_{\rm new} = \frac{L}{1 + \left(\dfrac{\omega}{\omega_{\rm ex}}\right)^2}, \tag{6.122}$$

where $\omega_{\rm ex} = 1/\sqrt{LC_{\rm ex}}$. In this case, an inductor $L_{\rm new}$ becomes a frequency-dependent element, whose value is different for the corresponding harmonic component and which can be realized using an appropriate arrangement of lumped components. The number of lumped components depends on the accuracy of the approximation to the optimum parallel-circuit Class-E mode.

Considering the fact that the output series resonant circuit tuned to the fundamental frequency ω_0 is characterized by a high $Q_{\rm L}$-factor, the input impedance $Z_{\rm in}(\omega_0)$ can be written as

$$Z_{\rm in}(\omega_0) = \frac{j\omega_0 L_{\rm new} R}{R + j\omega_0 L_{\rm new}} = \frac{j\omega_0 R \dfrac{L}{1 + (\omega_0/\omega_{\rm ex})^2}}{R + j\omega_0 \dfrac{L}{1 + (\omega_0/\omega_{\rm ex})^2}}. \tag{6.123}$$

Introducing the excess factor $\alpha = C_{\mathrm{ex}}/C$ and using Eqs. (6.80) and (6.81), we can write

$$\omega_{\mathrm{ex}} = \omega_0 \sqrt{\frac{2}{\alpha}}. \tag{6.124}$$

As a result, Eq. (6.123) as a function of the excess factor α can be simplified using Eq. (6.80) for an optimum Class-E inductance L at the fundamental frequency to

$$Z_{\mathrm{in}}(\omega_0) = R\frac{1 + j1.366(1+0.5\alpha)}{1 + 1.866(1+0.5\alpha)^2}, \tag{6.125}$$

and at the second- and higher-order harmonics ($n \geq 2$) to

$$Z_{\mathrm{in}}(n\omega_0) = j\frac{n\omega_0 L}{1 + 0.5\alpha n^2}. \tag{6.126}$$

In order to predict the effect of an excess capacitance C_{ex} on the parallel-circuit Class-E power amplifier performance, the drain efficiency η, output power P_{out}, and power dissipation P_{diss} shown in Fig. 6.29B have been obtained by varying the excess factor α, while keeping constant the rest of the circuit components.[40]

Fig. 6.30A shows the single-resonator topology of a parallel-circuit Class-E power amplifier, which can compensate for the excess capacitance at the second harmonic. The same network was used to approximate the three-harmonic impedance conditions of a Class-F power amplifier.[41] The equations relating the values of the load-network parameters to the excess factor α can be obtained by equating the impedance of the $L_1L_2C_2$ network to the impedance in Eq. (6.126) for $n=1$ and $n=2$, respectively, as

$$\omega_0 L_1 + \frac{\omega_0 L_2}{1 - \omega_0^2 L_2 C_2} = \frac{\omega_0 L}{1 + 0.5\alpha}, \tag{6.127}$$

$$2\omega_0 L_1 + \frac{2\omega_0 L_2}{1 - 4\omega_0^2 L_2 C_2} = \frac{2\omega_0 L}{1 + 2\alpha}, \tag{6.128}$$

where the resonant frequency ω_2 of the L_2C_2 resonator is located within $\omega_0 < \omega_2 < 2\omega_0$.

By introducing a new parameter γ determining the ratio between ω_0 and ω_2,

$$\gamma = \left(\frac{\omega_0}{\omega_2}\right)^2. \tag{6.129}$$

Eqs. (6.127) and (6.128) can now be rewritten as

$$\omega_0 L_1 + \frac{\omega_0 L_2}{1-\gamma} = \frac{\omega_0 L}{1 + 0.5\alpha}, \tag{6.130}$$

$$2\omega_0 L_1 + \frac{2\omega_0 L_2}{1-4\gamma} = \frac{2\omega_0 L}{1 + 2\alpha}, \tag{6.131}$$

resulting finally in three separate equations for the load-network parameters given by

$$L_1 = \frac{L(2\gamma + \alpha)}{\gamma(2\alpha^2 + 5\alpha + 2)}, \tag{6.132}$$

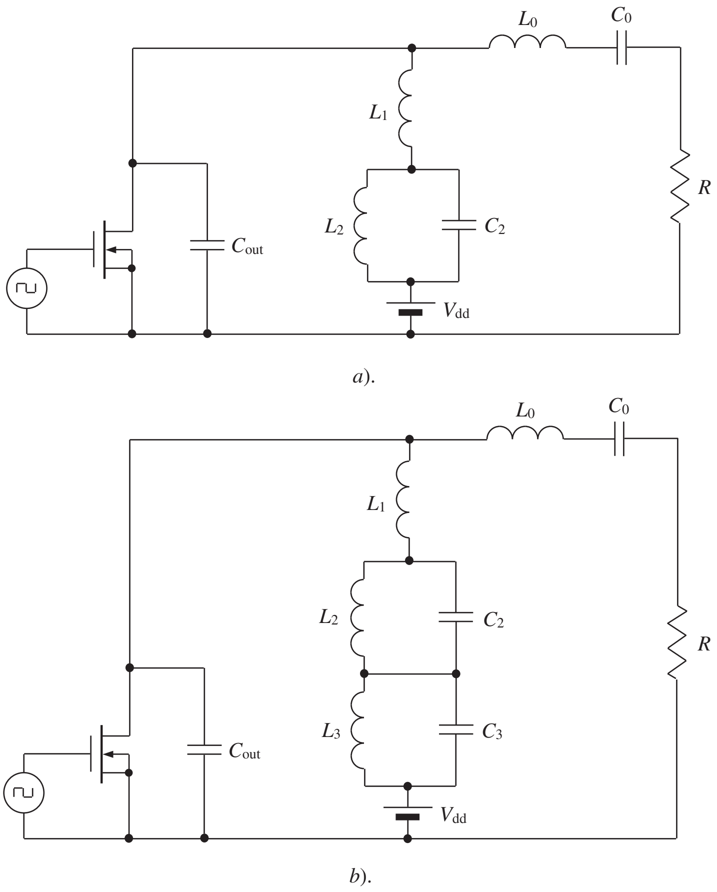


FIG. 6.30

Single- and double-resonator topologies of parallel-circuit Class-E power amplifier.

$$L_2 = -\frac{\alpha L(4\gamma^2 - 5\gamma + 1)}{\gamma(2\alpha^2 + 5\alpha + 2)}, \tag{6.133}$$

$$C_2 = \frac{\gamma}{\omega_0^2 L_2}. \tag{6.134}$$

Fig. 6.23B shows the double-resonator topology of a parallel-circuit Class-E power amplifier, which can compensate for the excess capacitance at the second and third harmonics. In this case, the lumped load network comprises a series inductor and two parallel *LC* resonators. The resonance frequency ω_2 of the L_2C_2 resonator is located between ω_0 and $2\omega_0$, whereas the resonant frequency ω_3 of the L_3C_3 resonator is located between $2\omega_0$ and $3\omega_0$.[40] Fixing the value of these resonances and selecting appropriate values for L_1, L_2, and L_3 allows the right value of harmonic reactances to be obtained.

The equations for the parameters of the $L_1L_2C_2L_3C_3$ network can be written as

$$L_1 = \frac{L[\alpha^2 + 2\alpha(\gamma_2 + \gamma_3) + 4\gamma_2\gamma_3]}{\gamma_2\gamma_3(18\alpha^3 + 49\alpha^2 + 28\alpha + 4)}, \tag{6.135}$$

$$L_2 = \frac{\alpha L(\alpha + 2\gamma_3)\left(-36\gamma_2^3 + 49\gamma_2^2 - 14\gamma_2 + 1\right)}{\gamma_2(\gamma_2 - \gamma_3)(18\alpha^3 + 49\alpha^2 + 28\alpha + 4)}, \tag{6.136}$$

$$L_3 = \frac{\alpha L\,(\alpha + 2\gamma_2)\left(36\gamma_3^3 - 49\gamma_3^2 + 14\gamma_3 - 1\right)}{\gamma_3(\gamma_2 - \gamma_3)(18\alpha^3 + 49\alpha^2 + 28\alpha + 4)}, \tag{6.137}$$

$$C_2 = \frac{\gamma_2}{\omega_0^2 L_2}, \tag{6.138}$$

$$C_3 = \frac{\gamma_3}{\omega_0^2 L_3}, \tag{6.139}$$

where L represents an optimum inductance in the classical parallel-circuit Class-E load network obtained by Eq. (6.80) and

$$\gamma_2 = \left(\frac{\omega_0}{\omega_2}\right)^2 \quad \text{where } \frac{1}{4} < \gamma_2 < 1, \tag{6.140}$$

$$\gamma_3 = \left(\frac{\omega_0}{\omega_3}\right)^2 \quad \text{where } \frac{1}{9} < \gamma_3 < \frac{1}{4}. \tag{6.141}$$

The simulated voltage and current drain waveforms obtained for $\alpha = 1.174$ with an ideal switch demonstrate that, if the switch current exhibits a small negative peak during turn-on for a single-resonator topology, as shown in Fig. 6.31A, this peak disappears for a double-resonator topology, as shown in Fig. 6.31B, thus clearly approximating the ideal optimum Class-E switching conditions. The component values of the series L_0C_0 resonant circuit were obtained by selecting $Q_L = 8$ and by setting the resonance frequency equal to 434 MHz.

6.10 Power gain

To realize the idealized switching conditions, the load network corresponding to any type of a Class-E mode must be tuned to provide inductive or capacitive impedance at the fundamental frequency, thus violating the conjugate-matching conditions required for conventional Class-B operation to provide maximum power delivery to the load. This means that generally the output voltage and current waves consist of both incident and reflected components. Besides, the power gain in a switchmode operation is normally lower than that in a conventional mode, because it requires higher driving voltage to realize the device voltage saturation mode. In this case, the ratio of the power gain in a Class-E power amplifier to that in a Class-B power amplifier for the same output power is inversely proportional to a squared ratio of their voltage peak factors.[42] For a Class-E with one inductor and one capacitor, a maximum operating power gain $G_{\mathrm{P(E)max}}$ of a single-stage bipolar power amplifier can be estimated by

$$G_{\mathrm{P(E)}}\mathrm{max} \approx \frac{\pi f_{\mathrm{T}}}{2f_0}\frac{V_{\mathrm{cc}}}{V_{\mathrm{th}}}, \tag{6.142}$$

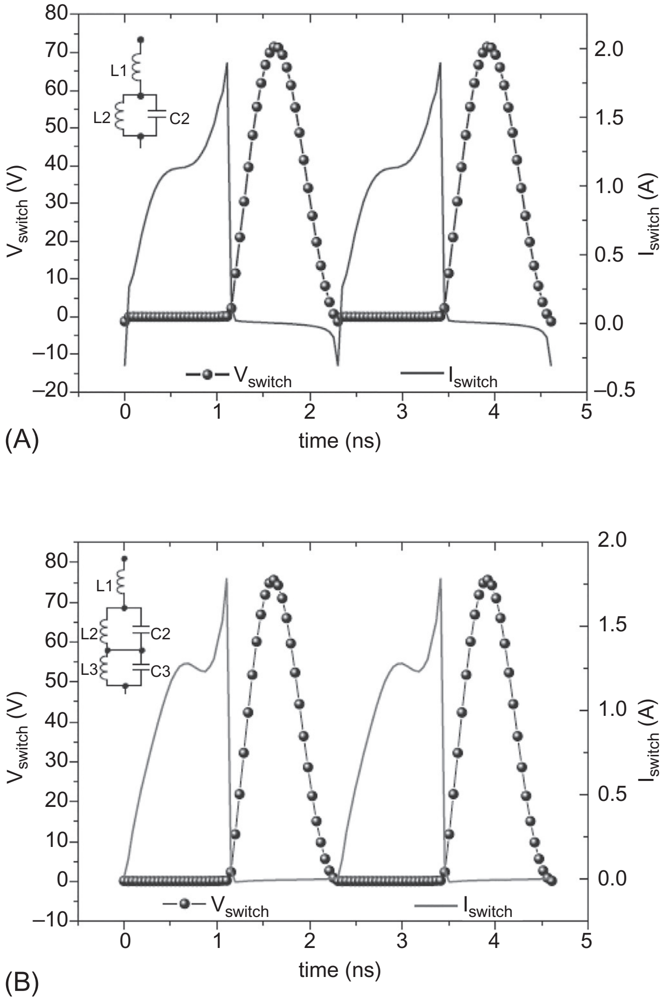


FIG. 6.31

Simulated waveforms using lumped Class-E load networks with excess capacitance.

where f_0 is the operating frequency, V_{th} is the threshold voltage, and it is assumed that the effect of a nonzero fall time is negligible.[43]

However, it is very important to qualitatively compare the power gains of the Class-B and Class-E power amplifiers as functions of the device and load-network parameters. In this case, a parallel-circuit Class-E mode looks very attractive since it provides the highest value of load resistance compared with other Class-E alternatives. The operating power gain G_{P}, expressed through the active-device Y-parameters and load admittance Y_{L}, can be obtained by

$$G_{\mathrm{P}} = \frac{|Y_{21}|^2}{\mathrm{Re}Y_{\mathrm{in}}} \frac{G}{|Y_{22} + Y_{\mathrm{L}}|^2}, \tag{6.143}$$

where Y_{21} and Y_{22} are the device transfer and driving-point output admittances, Y_{in} is the input admittance of the loaded device, and $Y_{\text{L}} = G + jB$.[44] Because the power amplifier is operated in a nonlinear mode, the admittance Y-parameters of the active device are considered linearized at the fundamental frequency. For example, for a power amplifier operating at the same conduction angle over various bias and drive conditions, these Y-parameters remain constant, and operating power gain becomes the function of load admittance only.

Eq. (6.143) can be rewritten as

$$G_{\text{P}} = \frac{|Y_{21}|^2}{\text{Re}Y_{\text{in}}} \frac{R}{\left(1 + \dfrac{G_{22}}{G}\right)^2 + \left(\dfrac{B_{22} + B}{G}\right)^2}, \tag{6.144}$$

where $G_{22} = \text{Re}Y_{22}$, $B_{22} = \text{Im}Y_{22}$, and $R = 1/G$ is the load resistance. Without significant loss of accuracy, the output conjugate-matching condition between imaginary parts of the device output admittance and the load admittance can be replaced by a simple condition of $B_{22} + B = 0$, which indicates a resonance tuning of the load network including the device output susceptance B_{22}. Besides, normally the device output conductance G_{22} is significantly smaller than the load conductance G for both MOSFET and bipolar transistors, especially at frequencies well below the device transition frequency f_{T}.

Consequently, the simplified ratio between the operating power gain $G_{\text{P(E)}}$ of a parallel-circuit Class-E power amplifier and the operating power gain $G_{\text{P(B)}}$ of a conventional Class-B power amplifier with conjugate-matched load can be written as

$$\frac{G_{\text{P(E)}}}{G_{\text{P(B)}}} = \frac{1}{1 + (B_{22} + B)^2 R_{(\text{E})}^2} \frac{R_{(\text{E})}}{R_{(\text{B})}}, \tag{6.145}$$

where $R_{(\text{E})}$ is the load resistance of a Class-E power amplifier and $R_{(\text{B})}$ is the load resistance of a Class-B power amplifier.

For a nominal parallel-circuit Class-E operation mode with 100% collector efficiency, from Eq. (6.53) for $L_{\text{b}} = 0$ it follows that

$$V_{\text{R(E)}} = 1.652 V_{\text{cc}}. \tag{6.146}$$

For the same output power P_{out} and considering the fact that $V_{\text{R(B)}} = V_{\text{cc}}$ in a conventional Class-B mode with zero saturation voltage, we can write

$$\frac{R_{(\text{E})}}{R_{(\text{B})}} = \frac{V_{\text{R(E)}}^2}{V_{\text{R(B)}}^2} = 2.729, \tag{6.147}$$

which shows a significantly higher value for the load resistance in a nominal parallel-circuit Class-E operation mode.

As a result, the power gain ratio given by Eq. (6.145) can be rewritten in the form

$$\frac{G_{\text{P(E)}}}{G_{\text{P(B)}}} = \frac{2.729}{1 + \tan^2 \phi} = 1.865, \tag{6.148}$$

where $\phi = 34.244°$ is the phase angle between the fundamental-frequency voltage and current components at the device output required for the nominal parallel-circuit Class-E mode.

The result given by Eq. (6.148) indicates that ideally the operating power gain for an idealized optimum parallel-circuit Class-E mode compared to a conventional Class-B mode is almost the same and even slightly greater, despite the detuning of the load network. This can be explained by the larger value of load resistance required for the nominal parallel-circuit Class-E load network. For example, for a Class-E mode with shunt capacitance, the operating power gain is smaller compared to a Class-B power amplifier because its nominal Class-E load resistance is about 2.4 times smaller than that of a parallel-circuit Class-E mode.[45] The idealized conditions for a switchmode operation can be achieved with instant on/off active device switching, which requires a rectangular input driving signal as compared to a sinusoidal driving signal for a conventional Class-B mode. However, the power losses due to nonzero switching time are sufficiently small and, for example, they are only about 1% for switching time of $\tau_s = 0.35$ or 20 degrees.[18, 20] Consequently, a slight overdrive of the active device is needed when the input power should be increased by 1–2 dB to minimize the switching time and maximize the collector efficiency of a switchmode parallel-circuit Class-E power amplifier. As a result, its resulting operating power gain becomes approximately equal to the operating power gain of a conventional Class-B power amplifier.

6.11 CMOS Class-E power amplifiers

Recent significant progress in CMOS technology with possibility to use high-resistivity silicon substrates and silicon-on-insulator (SOI) technology has shown its promising future for high-efficiency power applications at microwave- and millimeter-wave frequencies. Therefore, it is very vital to apply a corresponding high-efficiency technique into the design of CMOS power amplifiers. For example, a 900-MHz power amplifier based on a 0.25-μm CMOS technology with active die area of $2 \times 2\,\text{mm}^2$ could provide an output power of 0.9 W and a PAE of 41% using a Class-E load network with shunt capacitance and finite DC-feed inductance, the circuit schematic of which is shown in Fig. 6.32A.[46]

In this case, to minimize the voltage stress on the switching transistor and to maximize the allowable supply voltage, the cascode connection of two n-type metal-oxide-semiconductor (nMOS) devices is used, which allows the supply voltage to be as high as 1.8 V. Because a cascode switch has higher on-resistance per unit channel width than a single common-source switch during on-state mode, wider devices of 15-mm gate widths are used. The interstage bondwire inductor of 2 nH and external capacitor are used to resonate out the gate capacitance of the cascode device. Since the quality factor of the on-chip spiral inductors in a typical CMOS technology is low, because of a large loss in the silicon substrate and thin metal layers, the bondwires can be successfully used instead, having less than 5% of inductance variation and less than 6% of Q-factor change as a result of machine-bonding process. As a result, the complete power amplifier load network consists of two aluminum bondwire inductors and one on-chip (37 pF) and two off-chip (20 and 14 pF) capacitors. The implemented power amplifier is differential, and baluns are used at both input and output to combine two single-ended paths.

In order to further increase the efficiency of the CMOS power amplifier, a high-Q integrated passive device (IPD) based on a high-resistivity substrate to implement an output matching network can be used, which also makes the power amplifier module easier to manufacture. As a result, for an input power of 0 dBm, an output power of 34.5 dBm with a *PAE* of 55% was achieved in a low-frequency band of 824–915 MHz, whereas an output power of 32.5 dBm with a *PAE* of 52% was measured in a high-frequency band of 1.71–1.98 GHz at a 3.4-V power supply.[47]

The circuit schematic of a 30-dBm Class-E power amplifier with a self-biasing technique implemented in a 65-nm CMOS technology is shown in Fig. 6.32B.[48] Here, the final cascode stage is formed

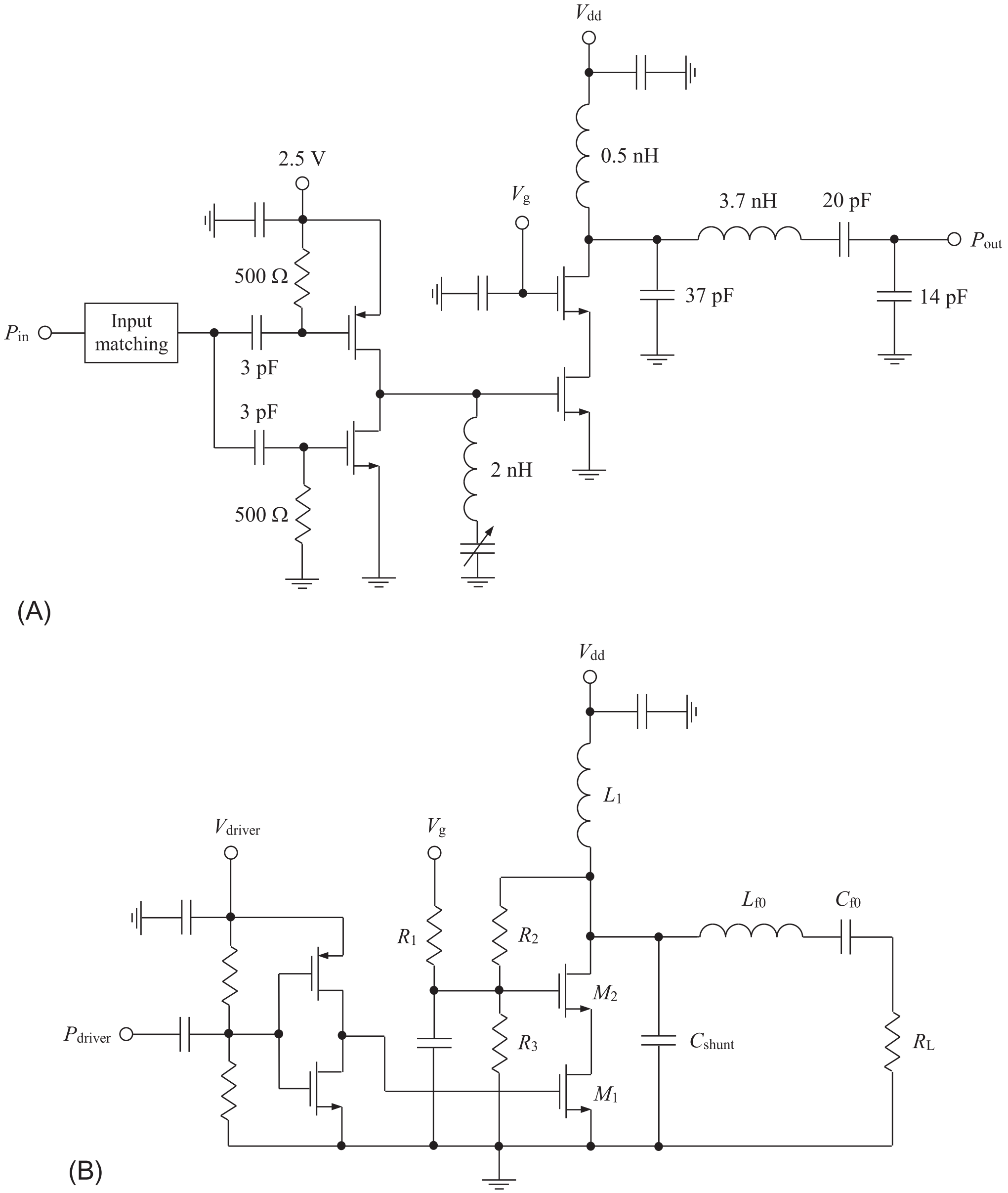

V_{dd}
0.5 nH
2.5 V
V_g
3.7 nH
20 pF
P_{out}
500 Ω
37 pF
14 pF
P_{in}
Input matching
3 pF
3 pF
2 nH
500 Ω
(A)
V_{dd}
L_1
V_{driver}
V_g
L_{f0}
C_{f0}
R_1
R_2
M_2
P_{driver}
R_3
C_{shunt}
R_L
M_1
(B)

FIG. 6.32

Cascode CMOS Class-E power amplifiers with finite DC-feed inductance.

by a standard thin-oxide (18 Å) device and a dedicated high-voltage extended-drain thick-oxide (50 Å) device, which has an offset breakdown voltage of 15 V and operates safely up to at least 10 V in the on-state. The measured f_T and f_{max} of the device exceed 30 and 50 GHz, respectively, enabling its usage at microwave frequencies up to 5 GHz. Thus, such a cascode topology combines the fast switching capability of the thin-oxide device M_1 in a common-source configuration and the high voltage sustainability of the thick-gate M_2 device in a common-gate configuration. Additionally, the device M_1 provides a high-gain capability and presents lower values of parasitic capacitances at the input of the device M_2, and proper choice of its width results in a better matching of its output impedance to the input impedance of the common-gate device. The self-biased cascode configuration was introduced to optimally divide the voltage swing across the common-gate and common-source devices so as to optimize the efficiency and output power within the breakdown limits of the device. Because the linearity and efficiency degrade as the device M_2 is turned off at lower supply voltages V_{dd}, which is required for envelope tracking, the resulting poor performance can be restored by DC-biasing the gate of the cascode device M_2 independently with a fixed gate supply voltage V_g and optimum values of the bias resistors R_1, R_2, and R_3, so that the transistor is always turned on. To operate the cascode stage as a switch optimally, an inverter-based driver using two thin-oxide devices with a sufficient driving capability and an input impedance of 50 Ω to minimize the return loss was used. Using an active load-pull measurement system for power amplifier characterization, a *PAE* over 60% when delivering a 30-dBm output power was achieved in a frequency range of 800 MHz to 2 GHz at $V_{dd} = 5$ V.

Fig. 6.33 shows the circuit schematic of a parallel-circuit Class-E power amplifier with a 1:*n* output transformer implemented in a 0.18-μm CMOS technology, where *n* is the turns ratio, *M* is the mutual inductance between the primary and secondary windings, and Z_T is the impedance looking into the transformer.[49] In this case, the real and imaginary parts of the impedance Z_T must be equal to *R* and ωL_0, respectively, where *R* is the optimum Class-E load resistance and L_0 is the series inductance tuned to the fundamental frequency together with a series capacitance C_0. The optimum Class-E shunt

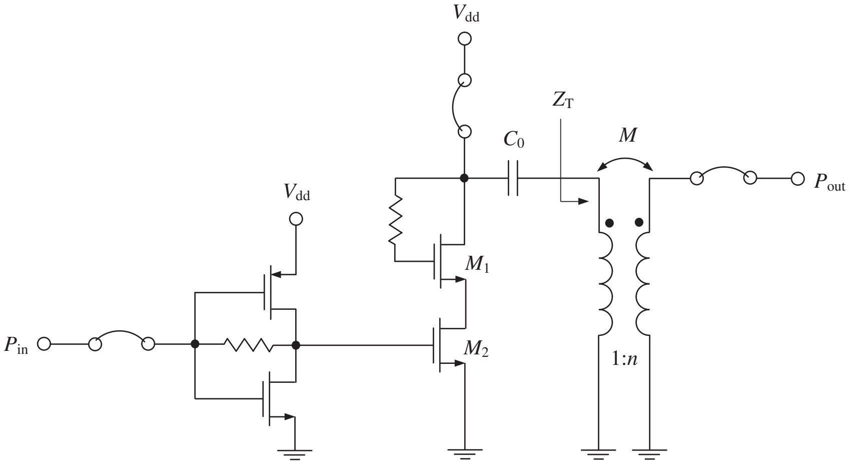


FIG. 6.33

Cascode Class-E power amplifier with output transformer.

capacitance C is fully represented by the output CMOS capacitance, and the bondwire inductance connected to the DC supply represents the optimum Class-E DC-feed inductance. A complete three-stage fully integrated CMOS power amplifier consists of the two push-pull parallel-circuit Class-E power amplifiers in a final stage with a 2 × 1:2 on-chip output transformer, where a two-turn secondary winding was selected to provide the necessary impedance transformation ratio to achieve 2 W of output power. As a result, a compressed power gain of around 19.5 dB and a *PAE* of 31% were achieved in single-ended 50-Ω input and output conditions at the operating frequency of 1.8 GHz, with overall die size of $1.8 \times 1.65\,\text{mm}^2$.

In a cascode configuration, the voltage across each transistor reduces by two times with the same current, thus resulting in a higher overall saturation resistance and power loss. To overcome this problem, a common-gate Class-E power amplifier, the equivalent circuit of which is shown in Fig. 6.34, can be used.[50] Here, the input signal is directly applied to the device source, and power losses can be reduced for the same voltage across the device by choosing an inductor with a high Q-factor. Since CMOS monolithic inductors are known for their low-quality factors due to high substrate losses and high parasitics, a bondwire inductor can be used to maximize the inductor quality factor. However, these bondwire inductors must be modeled very accurately for a particular design since their geometry is difficult to predetermine. For a two-stage power amplifier, it is very important to minimize the power consumption of the driving stage to minimize its effect of reducing the overall efficiency. In this case, the driver stage can include a positive feedback to operate as an injection-locked oscillator to maximize a power gain. When using a differential structure of a CMOS Class-E power amplifier, a driver stage can be designed by utilizing a cross-coupled differential pair to form a positive feedback. As a result, such a two-stage differential 2.45-GHz Class-E power amplifier with finite DC-feed inductance, implemented in a 0.25-μm standard CMOS process with chip area of $0.8 \times 0.9\,\text{mm}^2$, achieved a *PAE* of

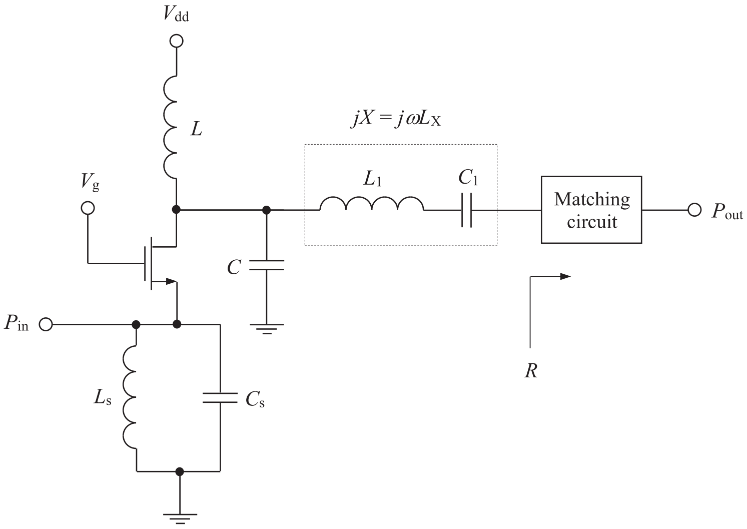


FIG. 6.34

Common-gate Class-E power amplifier.

34.5% and an output power of 18 dBm (63 mW) at a supply voltage of 1 V. The power-added efficiency was at least 33% over the frequency range of 2.40–2.48 GHz.

For a given geometry of a CMOS device, there is an optimum output power which provides the maximum power-added efficiency. Maximizing the output power by lowering an optimum load resistance will result in a higher current flowing through the saturation resistance, increasing the power dissipation. However, lowering the output power by increasing the optimum load resistance will decrease the power-added efficiency because of a reduced power gain. Besides, there is an optimum device size that provides the maximum power-added efficiency. A larger transistor size will lower the saturation resistance but will require more power from the driver stage and consumes more silicon area. In this case, it is more difficult to provide input matching due to increasing gate-source capacitance and lower gate resistance with a sufficiently small DC-feed inductance, thus resulting in implementation difficulties.[51] For example, for a simulated 1-GHz CMOS Class-E power amplifier fabricated using a 0.35-μm standard CMOS technology, a maximum *PAE* of about 62% is achieved for device gate widths of 6000–8000 μm with an output power of about 900 mW, a DC-feed inductance of 2 nH, and a load resistance of 2 Ω.[52]

Fig. 6.35 shows the circuit schematic of a two-stage fully differential Class-E power amplifier designed using a 0.18-μm standard CMOS technology.[53] The driver stage is used to convert the sinusoidal input signal into its square-wave approximation to drive the output stage. In some cases, the

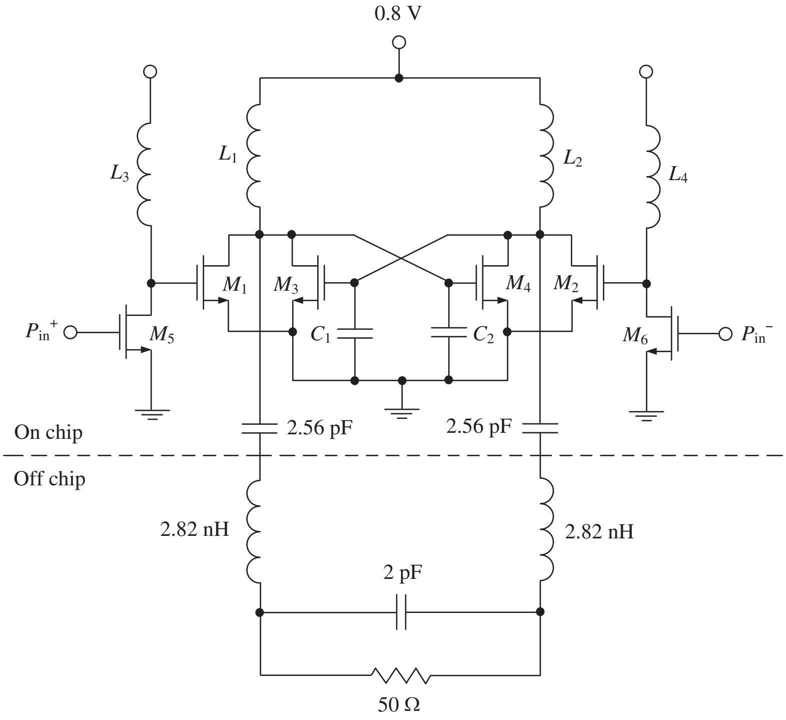


FIG. 6.35

Two-stage fully differential Class-E power amplifier.

interstage circuit can contain parallel-tank circuits tuned to the fundamental-frequency and third-harmonic components, realizing a Class-F mode of the driving stage and making the driving voltage waveform closer to a square wave, thus minimizing the power loss due to nonzero switching time.[54, 55] To obtain high operating efficiency, bondwires are used to implement the inductors L_1 and L_2, while the on-chip spiral inductors L_3 and L_4 are used in the driver stage for a better matching. The nMOS transistors M_3 and M_4 in the output stage are cross-coupled to assist the operation of the nMOS transistors M_1 and M_2, respectively, thus resulting in a significant reduction of the input-driving requirement due to injection-locking operating mode. The sizes of the nMOS devices were optimized to compromise the efficiency and output power. The shunt capacitors C_1 and C_2 can be used if the values of the gate-source capacitances are not enough to get self-oscillations at the operating frequency to realize an injection-locking mode. As a result of an accurate simulation and optimization design procedure, such a two-stage Class-E power amplifier was able to deliver an output power of 84.8 mW with a drain efficiency of 69.1% at an operating frequency of 2.4 GHz. The results of practical implementation of a two-stage injection-locked differential CMOS power amplifier in a 0.25-μm standard CMOS technology demonstrated the possibility to achieve an output power of 26 dBm with a *PAE* of 62% at a carrier frequency of 1 GHz, using a DC power supply of 1 V.[56]

Fig. 6.36A shows the circuit schematic of a modified cascode Class-E CMOS power amplifier that achieves higher output power and occupies smaller area than a conventional cascode Class-E power amplifier.[57] Here, the extra power is taken from the common-source device directly, considering no phase shift between the drain voltages at M_1 and M_2 operating as switches. The capacitors C_2 and C_3 couple and combine the output powers from both drains and then deliver the total power to the load through the output matching section composed of a series inductor L_2 and a shunt capacitor C_4. The drain inductance L_1 in parallel to the output capacitance of the cascode configuration provides the required inductive reactance at the fundamental required for a parallel-circuit Class-E operation mode. Being implemented in a fully differential dual cascode structure with an on-chip 1:2 combining transformer using a 0.18-μm RFSOI CMOS technology, a peak *PAE* of 51% with a saturated output power of 29.6 dBm at 1.8 GHz was measured with a DC-supply voltage of 2.5 V. The quality factors of the primary and secondary winding of the combining transformer were as high as 15 and 14, respectively, with the coupling factor of 0.8. The total area of the power amplifier including all test pads was $1.5 \times 1.0\,\text{mm}^2$.

The availability of deeply scaled CMOS technologies with $f_T > 300\,\text{GHz}$ has opened a possibility of implementing highly integrated millimeter-wave systems including silicon-based power amplifiers. In this case, employing the relevant high-efficiency technique for power amplifier to reduce its power consumption is of great importance. Fig. 6.36B shows the circuit schematic of a single-ended millimeter-wave Class-E power amplifier implemented in a 32-nm SOI CMOS process.[58] Here, the input matching circuit is composed of a 183-μm series microstrip line and a 100-μm shunt RF grounded microstrip stub, whereas the load network comprises a 490-μm RF grounded microstrip line connected in parallel to the shunt capacitance C_C required to provide an overall inductive reactance in a parallel-circuit Class-E approximation and an output matching section consisting of a 105-μm series microstrip line and a 120-μm open-circuit microstrip stub. As a result, a peak *PAE* of 27%, a power gain of 8 dB, and a saturated output power greater than 9 dBm were measured at 60 GHz with a DC-supply voltage of 0.9 V.

To provide much more reliable operation of the CMOS devices caused by the high peak drain voltage, especially using high DC-supply voltages, a multi-stacked configuration of the CMOS devices with adaptive bias conditions can be used. Fig. 6.37A shows the circuit schematic of a triple-stacked Class-E power amplifier with dynamic biasing network implemented in a standard 0.18-μm CMOS process, where L_1, L_{in}, and L_{ck} are off-chip inductors with high quality factors and L_{p} is on-chip spiral

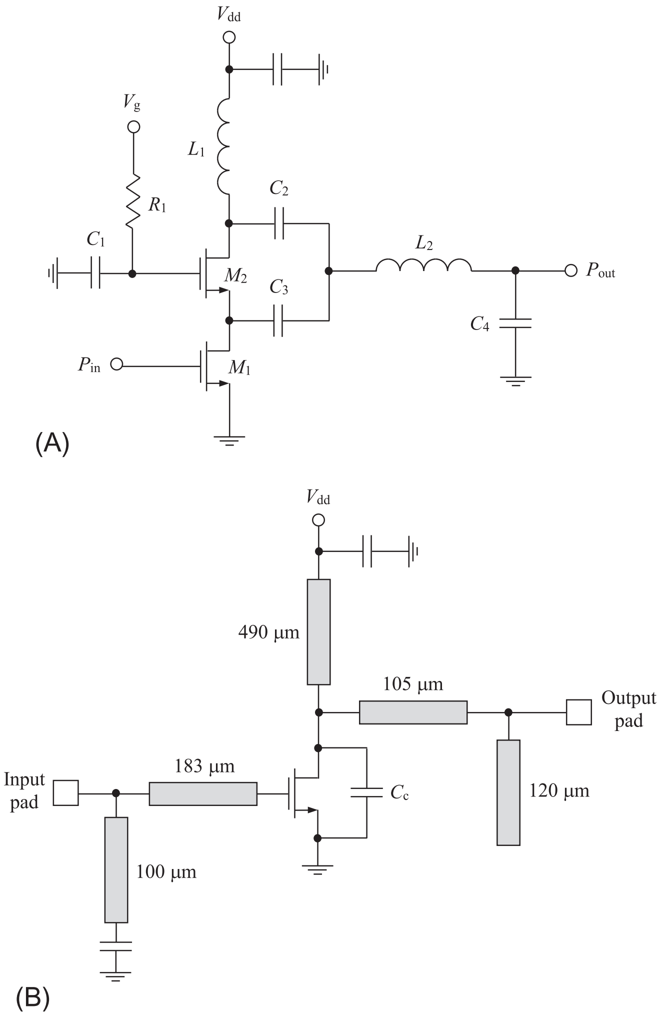


FIG. 6.36

Circuit schematics of (A) cascode dual-drain and (B) single-ended millimeter-wave Class-E power amplifiers.

inductor.[59] Because the transistors in a stacked configuration should have larger size to minimize losses due to finite on-resistance, the parallel inductor L_p is necessary to compensate for the excess parasitic capacitance for the required Class-E approximation. By dynamically biasing the gate of the device M_3 and fixed-biasing the gate of the device M_2, the voltage stress is distributed equally among three devices, thus improving power amplifier reliability. Simulation results show that the drain efficiency of 53.7%, *PAE* of 49.5%, and peak output power of 22.3 dBm can be achieved at 5 GHz with a DC-supply voltage of 2.5 V. Fig. 6.37B shows the simulated voltage and current waveforms at the drain of the top device M_3. Here, the drain voltage is close to zero when M_3 is turned on, and the current is almost zero when M_3 is turned off, resulting in lower power dissipation and increased efficiency.

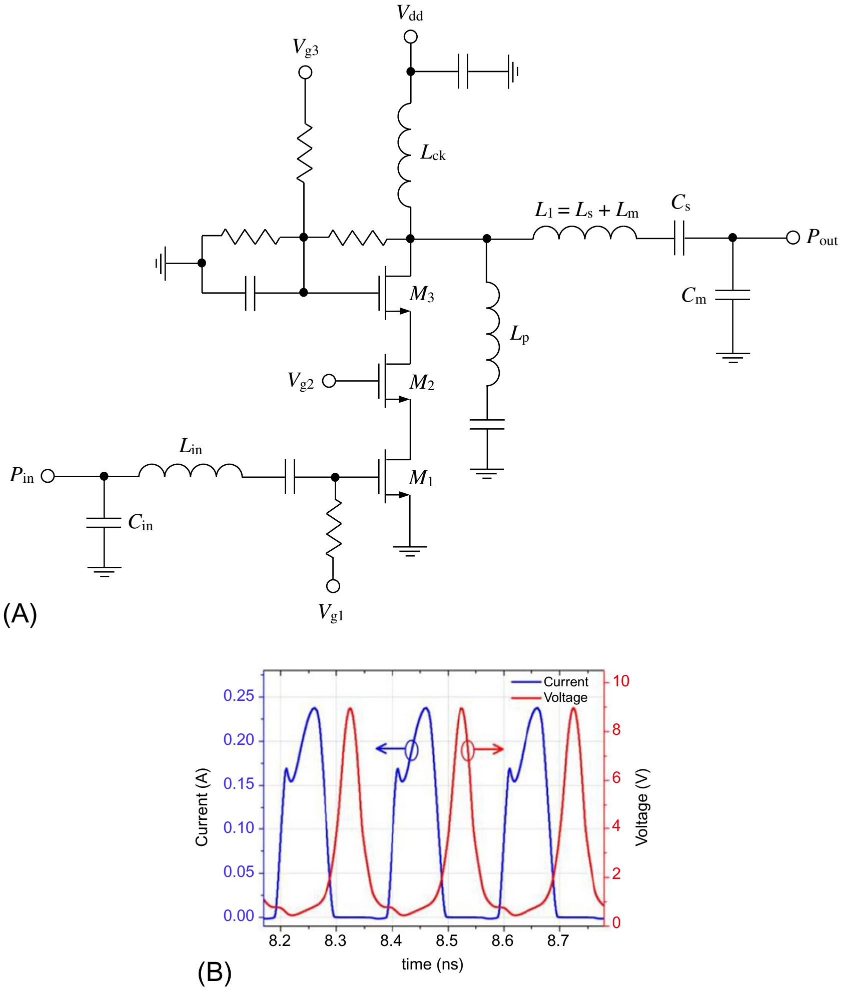

V_{dd}
V_{g3}
L_{ck}
$L_1 = L_s + L_m$
C_s
P_{out}
C_m
M_3
L_p
V_{g2}
M_2
L_{in}
P_{in}
M_1
C_{in}
(A)
V_{g1}
Current
Voltage
0.25
0.20
0.15
0.10
0.05
0.00
Current (A)
10
8
6
4
2
0
Voltage (V)
8.2
8.3
8.4
8.5
8.6
8.7
time (ns)
(B)

FIG. 6.37

Circuit schematic of triple-stacked power amplifier and drain voltage and current waveforms of M_3 device.[59]

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CHAPTER

7

Class-E with quarterwave transmission line

This chapter presents the results of exact time-domain analysis of the switchmode Class-E power amplifiers with a quarterwave transmission line. The load network parameters are derived analytically. The ideal collector voltage and current waveforms demonstrate a possibility of 100% efficiency without overlapping each other. The load network implementation including the output matching circuit at radio-frequency (RF) and microwave frequencies using lumped and transmission-line elements is considered with accurate derivation of the matching circuit parameters. The switchmode Class-E power amplifiers with a quarterwave transmission line offer a new possibility for RF and microwave power amplification to provide the high-efficiency and harmonic-suppression operation conditions simultaneously.

7.1 Load network with parallel quarterwave line

The ideal Class-F load network with a quarterwave transmission line and a series L_0C_0 filter tuned to the fundamental frequency provides a collector efficiency of 100% when the open-circuit conditions for odd-harmonic components and short-circuit conditions for even-harmonic components are realized. However, in practice, the idealized collector rectangular voltage and half-sinusoidal current waveforms corresponding to a Class-F operation mode provided by using a quarterwave transmission line in the load network can be realized at sufficiently low frequencies when an effect of the device output capacitance shown in Fig. 7.1 is negligibly small. Generally the effect of the device output capacitance contributes to a finite switching time, thus resulting in time periods when the collector voltage and collector current exist simultaneously. As a result, such a load network with a quarterwave transmission line and a shunt capacitor cannot provide the switchmode operation with an instantaneous transition from the device pinch-off mode to the saturation mode. Hence, during a finite time interval, the active device operates in an active region as a current source with reverse-biased collector-base junction, and the collector current is provided by this current source. In this case the required optimum conditions can be provided only for the fundamental frequency and several higher-order harmonic components. Moreover, it is necessary to consider at higher frequencies the effects of the bondwire inductor connecting physically the device die with the off-chip board. In a packaged device, it is also important to consider the effect of the external lead inductance. Therefore a special case is a load network with a quarterwave transmission line when the lossless transformation of a DC power to a fundamental-frequency output power can be provided. Fortunately, as it will be further demonstrated, the collector efficiency can be increased and the effect of the collector capacitance can be compensated with an inclusion of a series inductor between the shunt capacitor and the quarterwave transmission line realizing the switching

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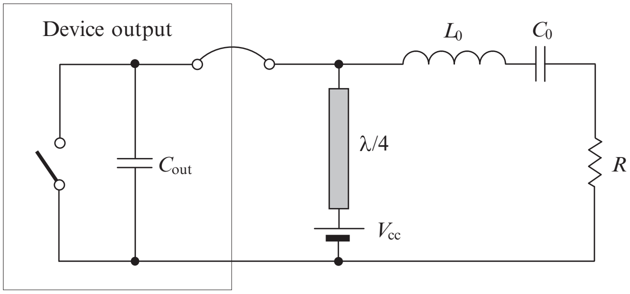


FIG. 7.1

Class-F load network with parasitic shunt capacitance and bondwire inductance.

Class-E operation conditions. The clear advantage of such a load network is a combination of the high operating efficiency corresponding to a Class-E mode and an even-harmonic suppression due to a quarterwave transmission line used in a Class-F mode.

The possibility to include a quarterwave transmission line into the Class-E load network with a shunt capacitance instead of an RF choke was first considered in 1975.[1] However, such a location for a quarterwave transmission line with a straight connection to the device collector violates the required capacitive reactance conditions at even harmonics by providing simply their short-circuiting. As a result, an optimum Class-E operation mode cannot be realized when the shapes of the collector current and voltage waveforms provide a condition at which the high current and high voltage do not overlap simultaneously. Moreover, the larger value of the shunt capacitance, smaller collector efficiency can be achieved.

Fig. 7.2 shows the Class-E load network consisting of a shunt capacitor C, a series inductor L, a quarterwave transmission line TL, a series reactance X, a series resonant L_0C_0 circuit tuned to the

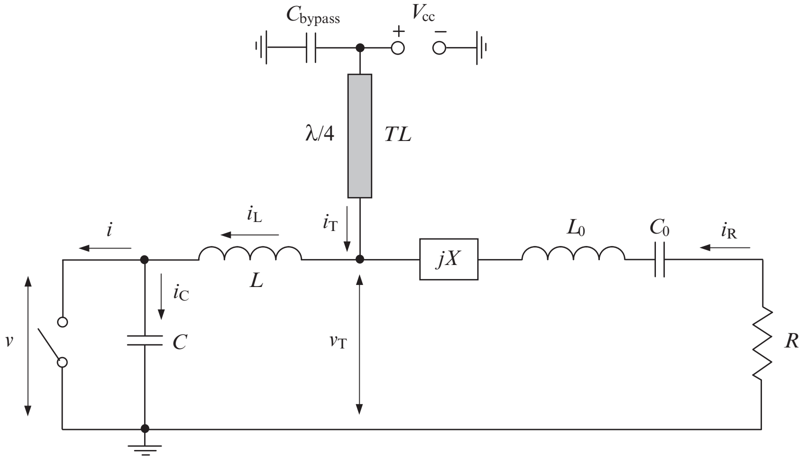


FIG. 7.2

Equivalent circuit of Class-E power amplifier with quarterwave transmission line.

fundamental frequency, and a load resistor R. The bottom end of the quarterwave transmission line is connected between the series inductor L and the series reactance X, whereas its top end is connected to the DC power supply which is RF grounded through the bypass capacitor. In a common case, a shunt capacitance C represents the intrinsic device output capacitance and external circuit capacitance added by the load network. The series reactance X generally can be positive (inductance), negative (capacitance), or zero depending on the values of the shunt capacitance C and the series inductance L. The active device is considered an ideal switch that is driven so as to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the switch when it is turned on and by the transient response of the load network when the switch is turned off.

To simplify an analysis of a Class-E power amplifier with a quarterwave transmission line, the following assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.
- The total shunt capacitance is independent of the collector and is assumed linear.
- The loaded quality factor $Q_L = \omega L_0/R = 1/\omega C_0 R$ of the series-resonant L_0C_0 circuit tuned to the fundamental frequency is high enough that the output current is sinusoidal at the switching frequency.
- There are no losses in the circuit except in the load R.
- For an optimum switching operation mode, a 50% duty cycle is used.

Let the output current flowing into the load be sinusoidal,

$$i_R(\omega t) = I_R \sin(\omega t + \varphi), \tag{7.1}$$

where φ is the initial phase shift due to the shunt capacitance and series inductance.

For lossless operation, it is necessary to provide the following optimum conditions for voltage across the switch at the turn-on instant of $\omega t = 2\pi$, when the transistor is voltage saturated:

$$v(\omega t)|_{\omega t = 2\pi} = 0, \tag{7.2}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} = 0, \tag{7.3}$$

where v is the voltage across the switch.

When the switch is turned on for $0 \le \omega t \le \pi$, the current flowing through the shunt capacitance $i_C(\omega t) = 0$ and, consequently,

$$i(\omega t) = i_L(\omega t) = i_T(\omega t) + i_R(\omega t). \tag{7.4}$$

When the switch is turned off for $\pi \le \omega t \le 2\pi$, there is no current flowing through the switch when $i(\omega t + \pi) = 0$, and the current flowing through the shunt capacitance C is

$$i_C(\omega t + \pi) = i_L(\omega t + \pi) = i_T(\omega t + \pi) + i_R(\omega t + \pi). \tag{7.5}$$

To correlate both Eqs. (7.4) and (7.5), each corresponding to one-half period, it is necessary to use a basic equation for the current flowing into the quarterwave transmission line given by Eq. (3.70) as

$$i_T(\omega t) = i_T(\omega t + \pi), \tag{7.6}$$

which means that the period of a signal flowing into the quarterwave transmission line is equal to π because it contains only even harmonics.

Then,

$$i_L(\omega t) = i_T(\omega t+\pi) + i_R(\omega t) = i_L(\omega t+\pi) + i_R(\omega t) - i_R(\omega t+\pi), \tag{7.7}$$

resulting in

$$i_L(\omega t) - i_L(\omega t+\pi) = 2 i_R(\omega t). \tag{7.8}$$

The current $i_L(\omega t+\pi) = i_C(\omega t+\pi)$ can be expressed through the voltages $v_T(\omega t+\pi)$ and

$$v_L(\omega t+\pi) = \omega L \frac{di_L(\omega t+\pi)}{d\omega t}, \tag{7.9}$$

as

$$\begin{aligned} i_L(\omega t+\pi) &= \omega C \frac{dv(\omega t+\pi)}{d\omega t} \\ &= \omega C \frac{d}{d\omega t}\left[v_T(\omega t+\pi) - \omega L \frac{di_L(\omega t+\pi)}{d\omega t}\right]. \end{aligned} \tag{7.10}$$

Now, we can use the equation for a voltage at the input of the quarterwave transmission line corresponding to each of a period given by Eq. (3.69) as

$$v_T(\omega t) = 2V_{cc} - v_T(\omega t+\pi). \tag{7.11}$$

Hence, when the switch is turned on resulting in $v_T(\omega t) = v_L(\omega t)$,

$$v_T(\omega t+\pi) = 2V_{cc} - \omega L \frac{di_L(\omega t)}{d(\omega t)}. \tag{7.12}$$

Substituting Eq. (7.12) in Eq. (7.10) and using Eqs. (7.1) and (7.8) yield a second-order nonhomogeneous differential equation, corresponding to half a period of $\pi \le \omega t < 2\pi$ when $i_L(\omega t+\pi) = i_C(\omega t+\pi)$, in the form

$$\frac{d^2 i_C(\omega t+\pi)}{d(\omega t)^2} + \frac{q^2}{2} i_C(\omega t+\pi) - I_R \sin(\omega t+\varphi) = 0 \tag{7.13}$$

or

$$\frac{d^2 i_C(\omega t)}{d(\omega t)^2} + \frac{q^2}{2} i_C(\omega t) + I_R \sin(\omega t+\varphi) = 0, \tag{7.14}$$

where

$$q = \frac{1}{\omega\sqrt{LC}}. \tag{7.15}$$

The general solution of Eq. (7.14) in the normalized form can be written as

$$\frac{i_C(\omega t)}{I_R} = C_1 \cos\left(\frac{q\omega t}{\sqrt{2}}\right) + C_2 \sin\left(\frac{q\omega t}{\sqrt{2}}\right) + \frac{2}{2-q^2} \sin(\omega t+\varphi), \tag{7.16}$$

where the coefficients C_1 and C_2 are determined from the initial off-state conditions.

The first initial condition is obtained from Eq. (7.8) as

$$i_C(\omega t)|_{\omega t=\pi} = 2i_R(\pi), \tag{7.17}$$

assuming that $i_L(\pi) = i_C(\pi)$ and $i_L(2\pi) = i_C(2\pi) = 0$.

To obtain the second initial condition, let us substitute Eq. (7.9) in Eq. (7.12) and use Eq. (7.8). As a result, we have

$$\begin{aligned}\omega L\frac{di_L(\omega t+\pi)}{d\omega t} &= 2V_{cc} - \omega L\frac{di_L(\omega t)}{d\omega t}\\ &= 2V_{cc} - \omega L\frac{di_L(\omega t+\pi)}{d\omega t} - 2\omega L\frac{di_R(\omega t)}{d\omega t}.\end{aligned} \tag{7.18}$$

Then, by assuming that $i_L(\pi) = i_C(\pi)$, we can write

$$\left.\frac{di_C(\omega t)}{d\omega t}\right|_{\omega t=\pi} = \frac{V_{cc}}{\omega L} - I_R\cos\varphi. \tag{7.19}$$

As a result, applying the initial conditions given by Eqs. (7.17) and (7.19) to Eq. (7.16) yields

$$\begin{aligned}C_1 = &-\frac{\sqrt{2}}{qp}\sin\left(\frac{q\pi}{\sqrt{2}}\right) - \frac{q\sqrt{2}}{2-q^2}\sin\left(\frac{q\pi}{\sqrt{2}}\right)\cos\varphi\\ &-2\frac{1-q^2}{2-q^2}\cos\left(\frac{q\pi}{\sqrt{2}}\right)\sin\varphi,\end{aligned} \tag{7.20}$$

$$\begin{aligned}C_2 = &\frac{\sqrt{2}}{qp}\cos\left(\frac{q\pi}{\sqrt{2}}\right) + \frac{q\sqrt{2}}{2-q^2}\cos\left(\frac{q\pi}{\sqrt{2}}\right)\cos\varphi\\ &-2\frac{1-q^2}{2-q^2}\sin\left(\frac{q\pi}{\sqrt{2}}\right)\sin\varphi,\end{aligned} \tag{7.21}$$

where

$$p = \frac{\omega L I_R}{V_{cc}}. \tag{7.22}$$

The DC supply current I_0 can be written using the Fourier formula and Eqs. (7.5) and (7.6) as

$$\begin{aligned}I_0 &= \frac{1}{2\pi}\int_0^{2\pi} i_T(\omega t)d\omega t = \frac{1}{\pi}\int_0^{\pi} i_T(\omega t+\pi)d\omega t\\ &= \frac{1}{\pi}\int_0^{\pi}[i_C(\omega t+\pi) - i_R(\omega t+\pi)]d\omega t.\end{aligned} \tag{7.23}$$

Then, substituting Eqs. (7.1) and (7.16) in Eq. (7.23) results in

$$\begin{aligned}I_0 = \frac{I_R}{\pi}\Bigg\{&C_1\frac{\sqrt{2}}{q}\left[\sin\left(q\pi\sqrt{2}\right) - \sin\left(\frac{q\pi}{\sqrt{2}}\right)\right]\\ &-C_2\frac{\sqrt{2}}{q}\left[\cos\left(q\pi\sqrt{2}\right) - \cos\left(\frac{q\pi}{\sqrt{2}}\right)\right] - \frac{2q^2}{2-q^2}\cos\varphi\Bigg\}.\end{aligned} \tag{7.24}$$

The voltage $v(\omega t)$ across the switch is produced by charging of the shunt capacitor C by the current given by Eq. (7.16) according to

$$v(\omega t) = \frac{1}{\omega C}\int_{\pi}^{\omega t} i_{\mathrm{C}}(\omega t)d\omega t = \frac{I_{\mathrm{R}}\sqrt{2}}{q\omega C}\left\{C_1\left[\sin\left(\frac{q\omega t}{\sqrt{2}}\right) - \sin\left(\frac{q\pi}{\sqrt{2}}\right)\right]\right.$$
$$\left. -C_2\left[\cos\left(\frac{q\omega t}{\sqrt{2}}\right) - \cos\left(\frac{q\pi}{\sqrt{2}}\right)\right] - \frac{q\sqrt{2}}{2-q^2}\left[\cos(\omega t+\varphi)+\cos\varphi\right]\right\}. \tag{7.25}$$

Generally, Eq. (7.25) for the collector voltage contains the three unknown parameters q, p, and φ, which must be determined. In a common case, the parameter q can be considered a variable, and the other two parameters p and φ are determined from a system of the two equations resulting from applying the two optimum zero-voltage and zero-voltage-derivative conditions given by Eqs. (7.2) and (7.3) to Eq. (7.25). Fig. 7.3 shows the dependences of the optimum parameters p and φ versus q for Class-E with a parallel quarterwave transmission line.

For the boundary cases when $q = 1/\sqrt{2}$ and $q = 3/\sqrt{2}$, the optimum parameters p and φ are defined analytically, the exact values of which are

$$\varphi = \tan^{-1}\left(-\frac{2}{3}\right) = -33.69°, \tag{7.26}$$

$$p = -\frac{6}{\sin\varphi} = 10.82, \tag{7.27}$$

for $q = 1/\sqrt{2} = 0.707$ and

$$\varphi = \tan^{-1}\left(-\frac{6}{5}\right) = -50.2°, \tag{7.28}$$

$$p = -\frac{10}{27\sin\varphi} = 0.482, \tag{7.29}$$

for $q = 3/\sqrt{2} = 2.12$.

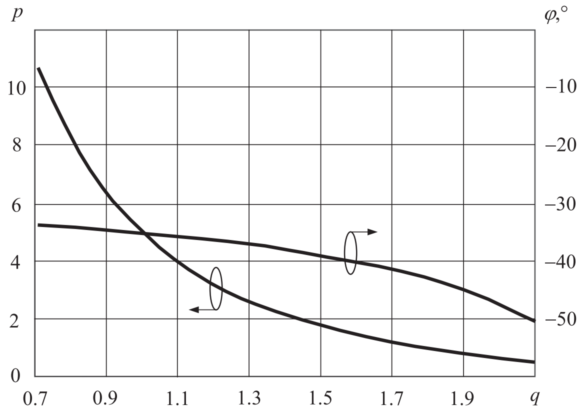


FIG. 7.3

Optimum quarterwave-line Class-E parameters p and φ versus q.

The current $i(\omega t) = i_L(\omega t)$ flowing through the inductor L and when the switch is turned on for $0 \le \omega t \le \pi$, the expression for the current can be written using Eqs. (7.4)–(7.6) and (7.16) in a normalized form as

$$\frac{i(\omega t)}{I_R} = C_1 \cos\left[\frac{q}{\sqrt{2}}(\omega t + \pi)\right] + C_2 \sin\left[\frac{q}{\sqrt{2}}(\omega t + \pi)\right] + 2\,\frac{1 - q^2}{2 - q^2}\sin(\omega t + \varphi). \tag{7.30}$$

Then the normalized voltage $v_T(\omega t)$ during this period can be obtained by

$$\begin{aligned} \frac{v_T(\omega t)}{V_{cc}} = \frac{\omega L I_R}{V_{cc}}\frac{di_L(\omega t)}{d\omega t} = p\Bigg\{ &-C_1 \frac{q}{\sqrt{2}} \sin\left[\frac{q}{\sqrt{2}}(\omega t + \pi)\right] \\ &+ C_2 \frac{q}{\sqrt{2}} \cos\left[\frac{q}{\sqrt{2}}(\omega t + \pi)\right] + 2\,\frac{1 - q^2}{2 - q^2}\cos(\omega t + \varphi)\Bigg\}. \end{aligned} \tag{7.31}$$

However, when the switch is turned off for $\pi \le \omega t \le 2\pi$, it can be calculated from Eq. (7.11).

7.2 Optimum load-network parameters

To calculate the optimum load-network parameters for a Class-E power amplifier with a parallel quarterwave transmission line, first it is necessary to define the reactive quadrature fundamental-frequency Fourier component of the voltage $v_T(\omega t)$ according to

$$\begin{aligned} V_X = &-\frac{1}{\pi}\int_0^{\pi} v_T(\omega t)\cos(\omega t + \varphi)\,d\omega t \\ &-\frac{1}{\pi}\int_{\pi}^{2\pi} [2V_{cc} - v_T(\omega t - \pi)]\cos(\omega t + \varphi)\,d\omega t. \end{aligned} \tag{7.32}$$

Then the two real and imaginary quadrature fundamental-frequency Fourier components of the collector voltage $v(\omega t)$ are defined from

$$V_R = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin(\omega t + \varphi)\,d\omega t, \tag{7.33}$$

$$V_{L+X} = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t + \varphi)\,d\omega t. \tag{7.34}$$

Finally, as it follows from Fig. 7.4, the optimum normalized series reactance X, series inductance L, and shunt capacitance C can be calculated from

$$\frac{X}{R} = \frac{V_X}{V_R}, \tag{7.35}$$

$$\frac{\omega L}{R} = \frac{V_{L+X}}{V_R} - \frac{X}{R}, \tag{7.36}$$

$$\omega C R = \frac{1}{q^2 \dfrac{\omega L}{R}}. \tag{7.37}$$

By assuming that $R = V_R^2/2P_{out}$, the optimum load resistance R for the specified values of a supply voltage V_{cc} and an output power P_{out} delivered to the load can be obtained by

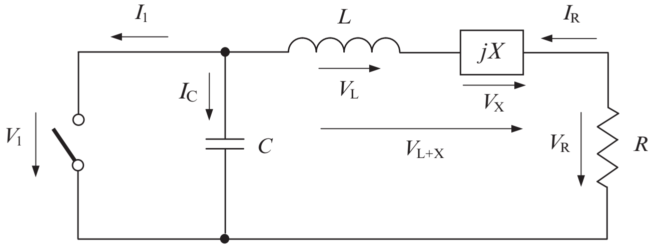


FIG. 7.4

Equivalent quarterwave-line Class-E load network at fundamental frequency.

$$R = \frac{1}{2}\left(\frac{V_R}{V_{cc}}\right)^2 \frac{V_{cc}^2}{P_{out}} \tag{7.38}$$

or, using Eq. (7.22), by

$$R = \frac{1}{2}\left(\frac{p}{l}\right)^2 \frac{V_{cc}^2}{P_{out}}, \tag{7.39}$$

where $l = \omega L/R$.

The dependences of the normalized optimum series inductance $\omega L/R$ and series reactance X/R are shown in Fig. 7.5A, while the dependences of the normalized optimum shunt capacitance ωCR and load resistance RP_{out}/V_{cc}^2 are plotted in Fig. 7.5B. Here, it is clearly seen that greater value of the normalized series inductance $\omega L/R$ corresponds to a lower value of q. To compensate for such an increased inductive value, the reactance X should have a negative capacitive value. Generally, the value of the series reactance X changes its sign from negative to positive, which means that the capacitive reactance is followed by the inductive reactance, and it is required to add an additional inductance at higher values of q. As a result, there is a special case of a load network with $X = 0$ when there is no need for additional phase compensation. The variations of the normalized values of ωCR and RP_{out}/V_{cc}^2 versus q are not so significant.

Fig. 7.6 shows the circuit schematics of the Class-E power amplifiers with a parallel quarterwave transmission line corresponding to different values of the optimum parameter q. The inclusion of a series capacitance C_X is necessary to compensate for the excess inductive reactance at the fundamental frequency when the series reactance X is negative, as shown in Fig. 7.6A. However, when the series reactance X is positive, an additional series inductance L_X shown in Fig. 7.6C is necessary to increase the total series inductance at the fundamental frequency. The special case is a zero series reactance X corresponding to the circuit schematic shown in Fig. 7.6B, which is discussed in detail later.

7.3 Load network with zero series reactance

In this case, the Class-E load network consists of a shunt capacitor C, a series inductor L, a parallel quarterwave transmission line connected to the DC voltage supply, a series L_0C_0 resonant circuit tuned to the fundamental frequency, and a load resistor R. As the parameter q corresponding to a zero reactance X is unknown a priori, generally it is necessary to solve a system of three equations to define the

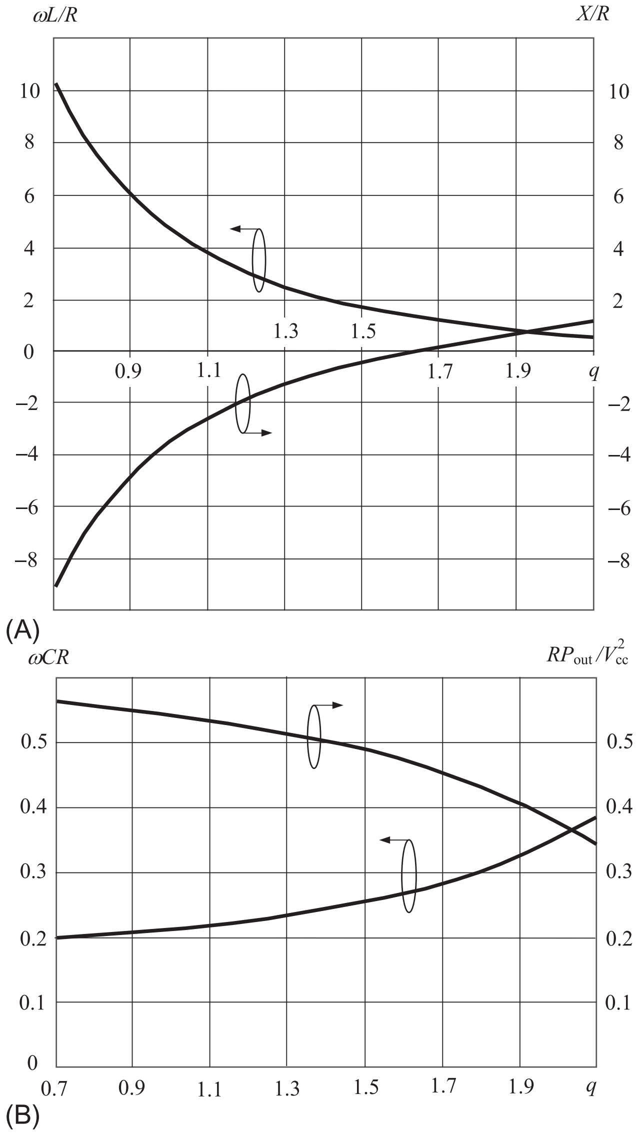


FIG. 7.5

Normalized optimum quarterwave-line Class-E load network parameters.

three unknown parameters q, p, and φ. Two equations are the result of applying the two optimum zero-voltage and zero voltage-derivative conditions given by Eqs. (7.2) and (7.3) to Eq. (7.25). Since the fundamental component of the voltage $v_T(\omega t)$ is fully applied to the load, this means that its reactive part must have zero value, resulting in an additional equation

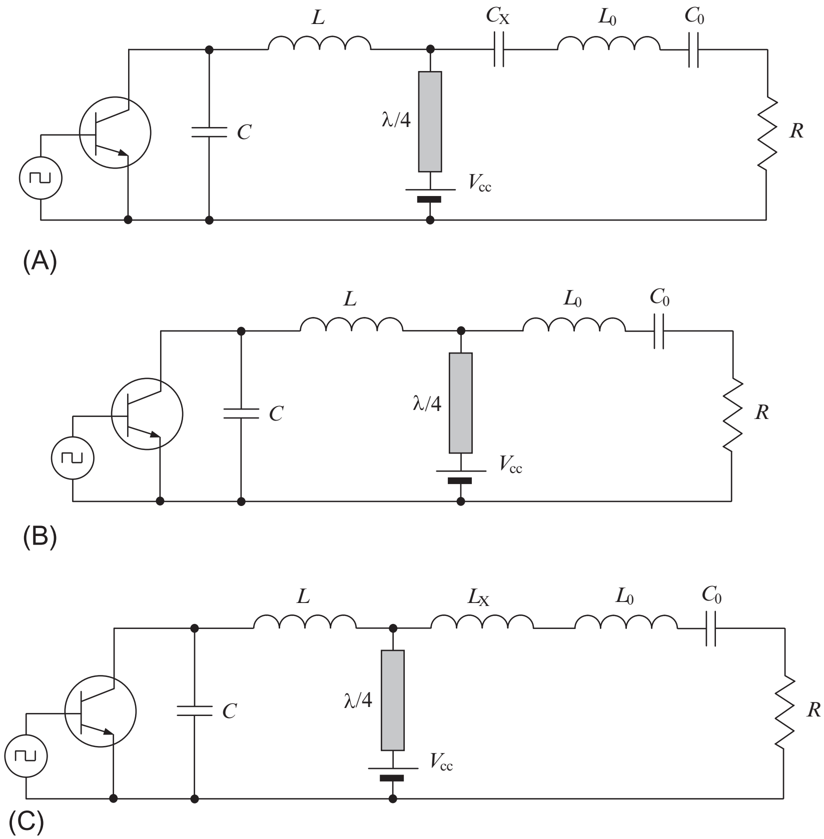


FIG. 7.6

Schematic of Class-E power amplifiers with quarterwave line.

$$\begin{aligned} V_X = & -\frac{1}{\pi}\int_0^{\pi} v_T(\omega t)\cos(\omega t+\varphi)d\omega t \\ & -\frac{1}{\pi}\int_{\pi}^{2\pi}[2V_{cc}-v_T(\omega t-\pi)]\cos(\omega t+\varphi)d\omega t = 0. \end{aligned} \tag{7.40}$$

As a result, the following exact values can be obtained numerically for the unknown parameters[2, 3]:

$$q = 1.649, \tag{7.41}$$

$$p = 1.302, \tag{7.42}$$

$$\varphi = -40.8°. \tag{7.43}$$

Fig. 7.7 shows the normalized (A) load current, (B) collector voltage, and (C) current waveforms for idealized optimum (or nominal) Class-E mode with a parallel quarterwave transmission line. From the collector voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch, and the collector current consisting of the load sinusoidal current shown in

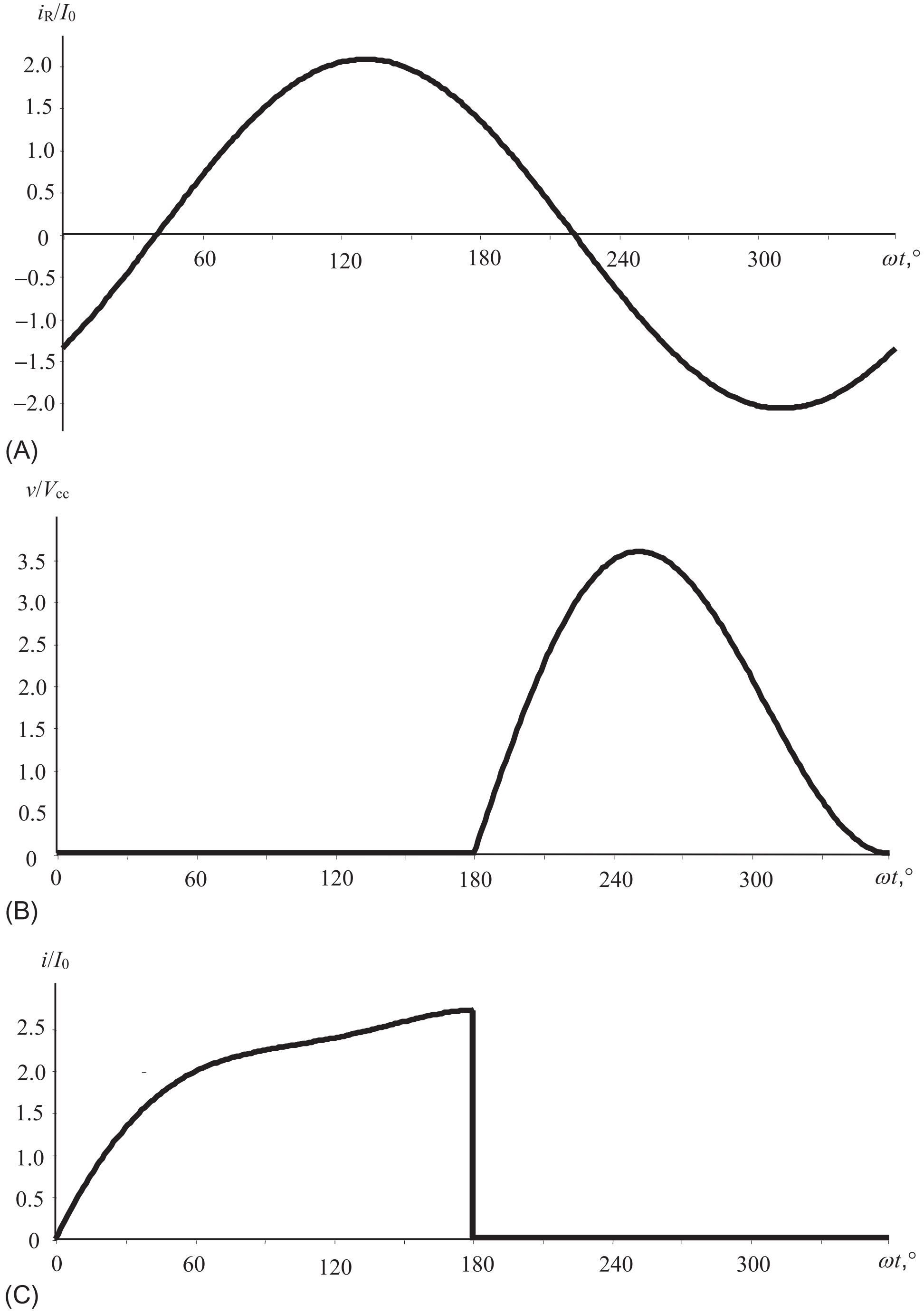


FIG. 7.7

Voltage and current waveforms of quarterwave-line Class-E power amplifier.

Fig. 7.7A and transmission-line current shown in Fig. 7.8A flows through the switch. However, when the transistor is turned off, this current with the waveform shown in Fig. 7.8B now flows through the shunt capacitor C, charging process of which produces the collector voltage.

In an idealized Class-E operation mode, there is no nonzero voltage and current simultaneously that means a lack of power losses and gives an idealized collector efficiency of 100%. This implies that the DC power and the fundamental output power are equal,

$$I_0 V_{\rm cc} = \frac{I_{\rm R} V_{\rm R}}{2}, \tag{7.44}$$

where $V_{\rm R} = I_{\rm R} R$ is the fundamental voltage amplitude across the load resistor R.

By using Eqs. (7.22) and (7.44), the normalized inductance can be defined as

$$\frac{\omega L}{R} = \frac{p}{2} \left(\frac{I_0}{I_{\rm R}} \right)^{-1}. \tag{7.45}$$

As a result, the exact values of the optimum series inductance L, shunt capacitance C, and load resistance R can be calculated by using Eqs. (7.24), (7.37), and (7.39) from

$$L = 1.349 \frac{R}{\omega}, \tag{7.46}$$

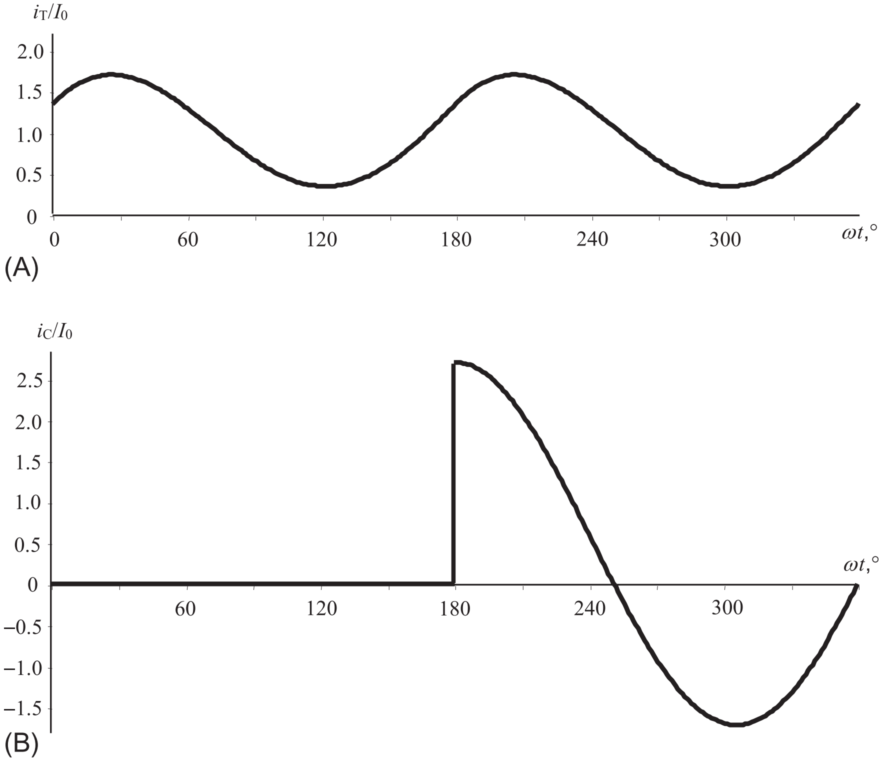


FIG. 7.8

Current waveforms of quarterwave-line Class-E power amplifier.

$$C = \frac{0.2725}{\omega R}, \tag{7.47}$$

$$R = 0.465 \frac{V_{cc}^2}{P_{out}}. \tag{7.48}$$

The peak collector current I_{max} and peak collector voltage V_{max} can be determined directly from Eqs. (7.25) and (7.30) using Eq. (7.24) from numerical calculations that gives

$$I_{max} = 2.714 I_0, \tag{7.49}$$

$$V_{max} = 3.589 V_{cc}. \tag{7.50}$$

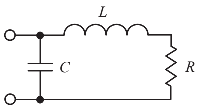
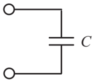
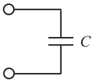
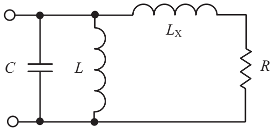
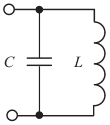
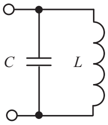
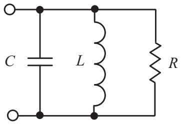
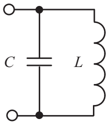
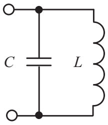
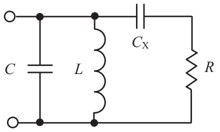
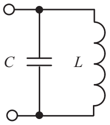
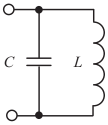
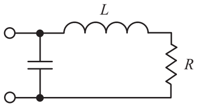
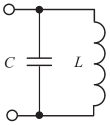
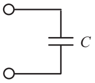
Using Eqs. (7.47) and (7.48) when $C = C_{out}$, where C_{out} is the device output capacitance, gives the value of a maximum operation frequency f_{max} determined by

$$f_{max} = 0.093 \frac{P_{out}}{C_{out} V_{cc}^2}, \tag{7.51}$$

which is 1.63 times as high as the maximum operation frequency for an optimum Class-E mode with shunt capacitance.[4]

In Table 7.1, the optimum impedances seen by the device collector at the fundamental-frequency and higher-order harmonic components are illustrated by the appropriate circuit configurations. It can

Table 7.1 Optimum impedances at fundamental and harmonics for different Class-E load networks.

Class-E load network	**f_0 (fundamental)**	**$2nf_0$ (even harmonics)**	**$(2n+1)f_0$ (odd harmonics)**
Class-E with shunt capacitance			
Subharmonic Class-E			
Parallel-circuit Class-E			
Even-harmonic Class-E			
Class-E with quarterwave transmission line			

be seen that a Class-E mode with quarterwave transmission line shows different impedance properties at even and odd harmonics. At odd harmonics, the optimum impedances can be established by the shunt capacitance that is required for all harmonic components in a Class-E with shunt capacitance. At even harmonics, the optimum impedances are realized by using a parallel LC circuit that is required for all harmonic components in a Class-E with finite DC-feed inductance. Thus the frequency properties of a grounded parallel quarterwave transmission line with its open-circuit conditions at odd harmonics and short-circuit conditions at even harmonics enable a Class-E with quarterwave transmission line to combine simultaneously the harmonic impedance conditions typical for both Class-E with shunt capacitance and Class-E with finite DC-feed inductance.

7.4 Matching circuit with lumped elements

The theoretical results obtained for the Class-E power amplifier with a quarterwave transmission line show that it is enough to use a very simple load network to realize the optimum impedance conditions even for four harmonics. From Fig. 7.8A, the current flowing into the quarterwave transmission line is very close to the sinusoidal second-harmonic current, which means that the level of fourth- and higher-order harmonic components is negligible because of the significant shunting effect of the capacitance C. In this case, as the shunt capacitor C and series inductor L provide optimum inductive impedance at the fundamental frequency and the quarterwave transmission line realizes the shorting of even harmonics, it is only required to provide an open-circuit condition at the third harmonic component. Consequently, when the ideal series L_0C_0 circuit is replaced by the output matching circuit, the optimum impedance conditions for Class-E load network with a quarterwave transmission line can be practically fully realized by simply providing an open-circuit condition at the third harmonic component.

Fig. 7.9 shows the circuit schematic of a lumped Class-E power amplifier with a parallel quarterwave transmission line, where the parallel resonant L_1C_1 circuit tuned to the third harmonic component

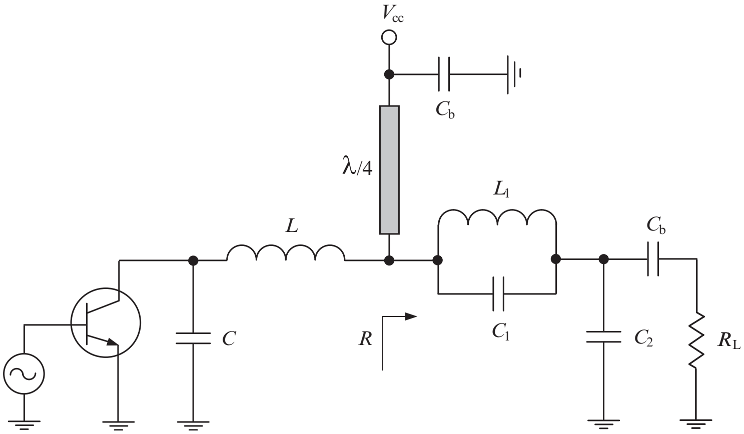


FIG. 7.9

Schematic of quarterwave-line Class-E power amplifier with lumped matching circuit.

is used and C_b represents the blocking or bypass capacitor. Because the reactance of the parallel third-harmonic tank circuit is inductive at the fundamental, it is enough to use the shunt capacitance C_2 composing the L-type low-pass matching circuit to provide the required impedance matching of the nominal Class-E load resistance R with the standard load impedance of $R_L = 50\,\Omega$. In this case, it is assumed that $R < R_L$, which is normally the case for high-power or low-voltage power amplifiers.

To calculate the parameters of the matching-circuit elements, consider the loaded quality factor $Q_L = \omega C_2 R_L$, which also can be expressed through the resistances R and R_L as[3, 5]

$$Q_L = \sqrt{\frac{R_L}{R} - 1}. \tag{7.52}$$

As a result, the matching-circuit parameters can be calculated at the fundamental frequency $f_0 = \omega_0 / 2\pi$ from

$$C_2 = \frac{Q_L}{\omega_0 R_L}, \tag{7.53}$$

$$L_1 = \frac{8}{9} \frac{Q_L R}{\omega_0}, \tag{7.54}$$

$$C_1 = \frac{1}{9 \omega_0^2 L_1}. \tag{7.55}$$

7.5 Matching circuit with transmission lines

At ultra-high frequencies and microwaves, the output lumped matching circuit is replaced by the transmission-line load network where the transmission lines are used instead of lumped inductors. In this case, the optimum Class-E inductance L can be composed of the internal package bondwire inductance, external inductance of the device package lead, and inductance of the short-length transmission line required to properly connecting the transistor package to the transmission-line load-network fabricated on printed-circuit board (PCB). At the same time, the shunt capacitance C represents a fully internal active-device output capacitance. Fig. 7.10 shows the basic circuit schematic of a transmission-line Class-E power amplifier with a parallel quarterwave transmission line. The output matching circuit represents an L-type low-pass matching circuit consisting of a series transmission line with electrical length θ_X, which is required for optimum Class-E mode to provide a positive reactance X (can be replaced by a series capacitor if negative reactance X is required), a series transmission line with electrical length θ_1, which provides a required inductive reactance, and a shunt open-circuit stub with an electrical length θ_2 of less than 90 degrees, which provides a capacitive reactance.

Usually the characteristic impedance Z_1 of a transmission line (often equal to $50\,\Omega$) is much higher than the required optimum Class-E load network resistance R for high-power or low-voltage applications. Consequently, the input impedance Z_{in} of the loaded series transmission line with the characteristic impedance Z_0 and electrical length θ_X under the condition

$$\frac{R \tan \theta_X}{Z_0} \ll 1, \tag{7.56}$$

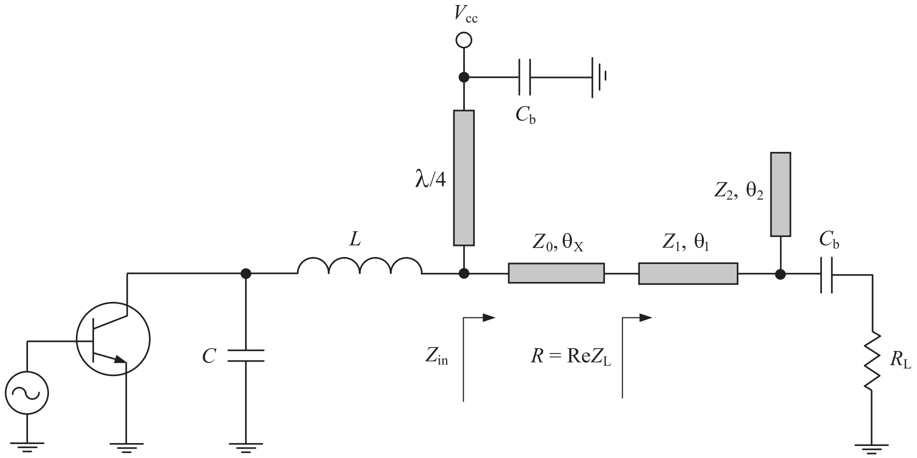


FIG. 7.10

Schematic of transmission-line Class-E power amplifier.

when the electrical length of a sufficiently short transmission line is much less than 45 degrees, is determined by

$$Z_{in} = Z_0 \frac{R + jZ_0 \tan\theta_X}{Z_0 + jR\tan\theta_X} = Z_0 \frac{\frac{R}{Z_0} + j\tan\theta_X}{1 + j\frac{R}{Z_0}\tan\theta_X} \approx R + jZ_0 \tan\theta_X. \tag{7.57}$$

As a result, the required optimum value of the electrical length θ_X for nominal Class-E mode with a quarterwave transmission line and series reactance using Eq. (7.57) can be obtained from $X = Z_0 \tan\theta_X$ as

$$\theta_X = \tan^{-1}\left(\frac{X}{Z_0}\right), \tag{7.58}$$

where an electrical length θ_X can be positive or negative depending on the inductive or capacitive reactance X, respectively.

The output matching circuit is necessary to match the required nominal Class-E resistance R calculated in accordance with Eq. (7.39) in a general case or Eq. (7.48) in a particular case with zero series reactance to the standard load resistance of 50 Ω. In addition, it is required to provide an open-circuit condition at the third-harmonic component. This can be easily done using the output matching topology in the form of an L-type low-pass transformer with the series transmission line and open-circuit stub.[3, 6] In this case, the electrical length of the total series transmission line with combined electrical length $\theta_X + \theta_1$ should be chosen to provide an open circuit at its input at the third harmonic, and the electrical length of the open-circuit stub with electrical length θ_2 should be chosen to be 30 degrees. If both transmission lines have the same characteristic impedance, their total electrical length $\theta_X + \theta_1$ should be equal to 30 degrees at the fundamental. However, the stepped-impedance transmission line can change the position of poles of its input impedance which depends on the characteristic impedance ratio and position of their sections.[7] The load impedance Z_L can be written by

$$Z_L = Z_1 \frac{R_L(Z_2 - Z_1 \tan\theta_1 \tan\theta_2) + jZ_1 Z_2 \tan\theta_1}{Z_1 Z_2 + jR_L(Z_1 \tan\theta_2 + Z_2 \tan\theta_1)}, \tag{7.59}$$

where Z_1 and θ_1 are the characteristic impedance and electrical length of the series transmission line, and Z_2 and θ_2 are the characteristic impedance and electrical length of the open-circuit stub.

Hence the complex-conjugate matching with the load at the fundamental can be provided by proper choice of the characteristic impedances Z_1 and Z_2. Separating Eq. (7.59) into real and imaginary parts and taking into account that $\mathrm{Re}Z_L = R$ and $\mathrm{Im}Z_L = 0$, the following system of two equations with two unknown parameters can be obtained as

$$R\left[R_L\left(1 + \tan^2\theta_1\right) - R\right] - Z_1^2 \tan^2\theta_1 = 0, \tag{7.60}$$

$$\left(Z_1^2 - R^2\right) Z_2 \tan\theta_1 - \left(R^2 + Z_1^2 \tan^2\theta_1\right) Z_1 \tan\theta_2 = 0, \tag{7.61}$$

which enables the characteristic impedances Z_1 and Z_2 to be properly calculated.

This system of two equations can be explicitly solved as a function of the parameter $r = R_L/R$ and electrical length θ_1 when $\theta_2 = 30°$, resulting in

$$\frac{Z_1}{R_L} = \frac{\sqrt{r(1 + \tan^2\theta_1) - 1}}{r \tan\theta_1}, \tag{7.62}$$

$$\frac{Z_1}{Z_2} = \frac{\sqrt{3}}{\tan\theta_1} \frac{r - 1}{r}, \tag{7.63}$$

where the electrical length θ_1 generally affects the electrical length θ_X. In a simple case of zero series reactance X when $\theta_X = 0$ and $\theta_1 = 30°$, Eqs. (7.62) and (7.63) can be rewritten as

$$\frac{Z_1}{R_L} = \frac{\sqrt{4r - 3}}{r}, \tag{7.64}$$

$$\frac{Z_1}{Z_2} = 3\left(\frac{r - 1}{r}\right). \tag{7.65}$$

Consequently, for the specified value of the parameter r with the required Class-E optimum load resistance R and standard load $R_L = 50\,\Omega$, the characteristic impedance Z_1 is calculated from Eq. (7.64), and then the characteristic impedance Z_2 is calculated from Eq. (7.65). For example, if the required load resistance R is equal to $12.5\,\Omega$ resulting in $r = 4$, the characteristic impedance of the series transmission line Z_1 is equal to $45\,\Omega$ and the characteristic impedance of the shunt open-circuit stub Z_2 is equal to $20\,\Omega$.

Unlike the transmission-line Class-E load-network approximations with two-harmonic control[8] and with three-harmonic control,[9] the Class-E load network with a quarterwave transmission line, which can provide the optimum impedance conditions for at least four harmonic components, is very simple in terms of circuit implementation and does not require an additional lumped RF choke element. In addition, there is no need to use the special computer simulation tools required to calculate the parameters of the existing Class-E transmission-line load-network topologies,[9–11] since all parameters of the Class-E load network with a quarterwave transmission line and the output matching-circuit parameters are easily calculated explicitly from simple analytical equations. Besides, such a Class-E load network with a quarterwave transmission line is very useful in practical design providing simultaneously significant higher-order harmonic suppression.

7.6 Load network with series quarterwave line and shunt filter

Fig. 7.11 shows an alternative configuration for the Class-E power amplifier with a series quarterwave transmission line, consisting of a shunt capacitor C, a series inductor L, a series quarterwave transmission line, a parallel-resonant L_0C_0 circuit tuned to the fundamental frequency, a shunt susceptance B, and a load resistor R. In a common case, the shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The shunt susceptance B generally can be positive (capacitance), negative (inductance), or zero depending on the value of the optimum load network parameter q. The RF choke is necessary to isolate the DC power supply from the RF circuit, while the blocking capacitor C_b is necessary to separate the DC supply circuit from the load.

The operation principle of such a Class-E load network with a series quarterwave line is similar to the Class-E load network with a parallel quarterwave line, assuming that the parallel L_0C_0 filter is ideal, having infinite impedance at the fundamental frequency and zero impedances at the second- and higher-order harmonic components. In this case, the short circuit on the load side of the quarterwave transmission line produces a short circuit at its input for even harmonics and open circuit at its input for odd harmonics, with resistive load at the fundamental frequency.

However, unlike the parallel quarterwave transmission line, a series quarterwave transmission line can also serve as an impedance transformer at the fundamental frequency. As a result, there is no need for an additional output matching circuit as required for the Class-E power amplifier with a parallel quarterwave transmission line. The impedance Z_{in} at the input of the loaded quarterwave transmission line with the characteristic impedance Z_0 and electrical length θ at the fundamental frequency can be written as

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan\theta}{Z_0 + jZ_L \tan\theta}\bigg|_{\theta=90^\circ} = \frac{Z_0^2}{Z_L}, \tag{7.66}$$

where

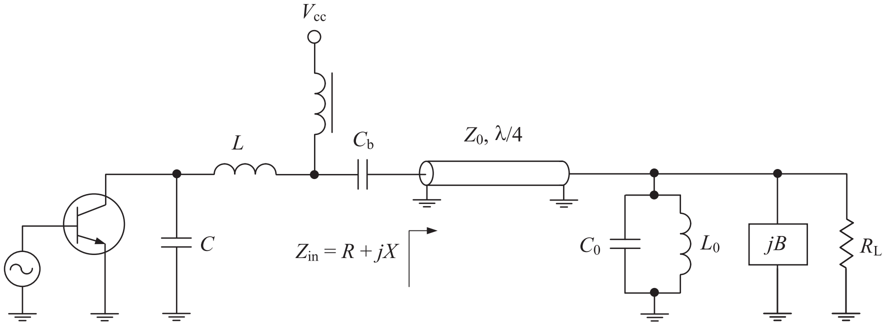


FIG. 7.11

Class-E power amplifier with series quarterwave transmission line and shunt filter.

$$Z_L = \frac{R_L}{1 + jBR_L}. \tag{7.67}$$

Substituting Eq. (7.67) in Eq. (7.66) yields

$$R + jX = Z_0^2 \frac{1 + jBR_L}{R_L}. \tag{7.68}$$

Then, separating Eq. (7.68) into real and imaginary parts enables the standard load resistance R_L and shunt susceptance B to be expressed through the optimum load resistance R and series reactance X corresponding to the Class-E with a parallel quarterwave line as

$$R_L = \frac{Z_0^2}{R}, \tag{7.69}$$

$$B = \frac{X}{Z_0^2}. \tag{7.70}$$

To calculate the optimum parameters of a Class-E load network with series quarterwave transmission line and shunt filter, it is necessary to use Eqs. (7.35)–(7.39) for a Class-E load network with parallel quarterwave transmission line defining the optimum shunt capacitance C, series inductance L, series reactance X, and a load resistance R in a common case or Eqs. (7.46)–(7.48) in a particular case when $X = 0$.

7.7 Design example: 10-W 2.14-GHz Class-E GaN HEMT power amplifier with parallel quarterwave transmission line

As an example, our objective is to design a high-efficiency single-stage hybrid Class-E GaN high-electron-mobility transistor (HEMT) power amplifier with a parallel quarterwave transmission line, operating at 2.14 GHz with an output fundamental-frequency power $P_{out} = 40$ dBm (10 W) at a supply voltage $V_{dd} = 28$ V. Using a GaN HEMT device can provide higher efficiency compared to other types of active devices and it is easier to apply a switchmode Class-E technique because of a sufficiently low output capacitance inherent to these devices. This kind of a power amplifier requires an operation in saturation mode resulting in a poor linearity, and therefore is not suitable to directly replace linear power amplifiers in conventional WCDMA/LTE or CDMA2000 communication transmitters with nonconstant envelope signal. However, to obtain both high efficiency and good linearity, a nonlinear high-efficiency power amplifier operating in a Class-E mode can be used in advanced transmitter architectures such as Doherty, linear amplification using nonlinear components (LINC), or envelope tracking (ET) with digital predistortion.[12–14]

Assuming the drain efficiency of the Class-E power amplifier of 80%, the DC power is equal to $P_0 = 10\,\text{W}/0.8 = 12.5\,\text{W}$ with the DC supply current $I_0 = P_0/V_{dd} = 12.5\,\text{W}/28\,\text{V} \approx 450\,\text{mA}$. The DC output current-voltage characteristics I_{drain} (V_{dd}) of a selected Cree CGH40010 GaN HEMT transistor for different gate bias voltage V_{gate} varying from -3.0 to -0.5 V with a voltage step of 0.25 V are shown in Fig. 7.12.[15] In this case, it is sufficient to evaluate the peak drain current for a Class-E mode with quarterwave transmission line and zero series reactance according to Eq. (7.49) with some margin, resulting in $I_{max} = 2.8I_0 \approx 1.25$ A. The idealized Class-E load line (with instant transition between pinch-off and

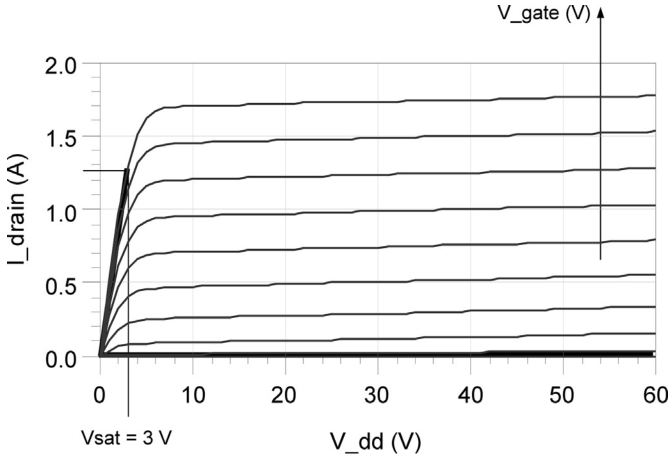


FIG. 7.12

Device output current-voltage characteristics and load line.

saturation regions) is shown as a broken heavy line. It can be seen that the operating point moves along the horizontal V_{dd} axis (pinch-off region) and then along the drain current saturated line (voltage saturation region) until $I_{drain} = I_{max} = 1.25\,A$. At this final point, the saturation voltage can be found as equal to $V_{sat} \approx 3\,V$, which means that the power loss due to the finite device saturation resistance can be calculated as $P_{sat} = I_0 V_{sat} = 1.35\,W$ with degradation in the drain efficiency of $P_{sat}/P_0 \approx 0.11$ or 11%.

In view of the device saturation voltage, the calculated parameters of the Class-E load network cannot generally be considered optimum unlike the ideal case of zero saturation voltage. However, they can be considered as a sufficiently accurate initial guess for final design and optimization when efficiency is sufficiently high. The drain-source capacitance $C_{ds} = 1.3\,pF$ is considered an output capacitance, while the series inductance is composed of the internal bondwire inductance and external package lead inductance, which can be estimated as approximately equal to 1 nH. To improve accuracy of simulation results, the device leads can be modeled as a strip line in air substrate with 45-mil width and 60-mil length. For $q = 2.1$, the optimum parameters of a Class-E load network with a quarterwave transmission line can be approximately estimated using corresponding plots in Fig. 7.5A and B in view of the saturation voltage V_{sat} as

$$R = 0.38/\omega C = 0.34(V_{dd} - V_{sat})^2/P_{out} \approx 20\Omega,$$

$$X = 1.2R = 24\Omega,$$

$$L = 0.7R/\omega \approx 1\,nH.$$

In this case, the electrical length θ_X can be estimated for $Z_0 = 50\,\Omega$ as

$$\theta_X = \tan^{-1}(X/Z_0) \approx 25°,$$

which is sufficiently long compared with a total 30 degrees. However, for $Z_0 = 100\ \Omega$,

$$\theta_X = \tan^{-1}(X/Z_0) \approx 15°.$$

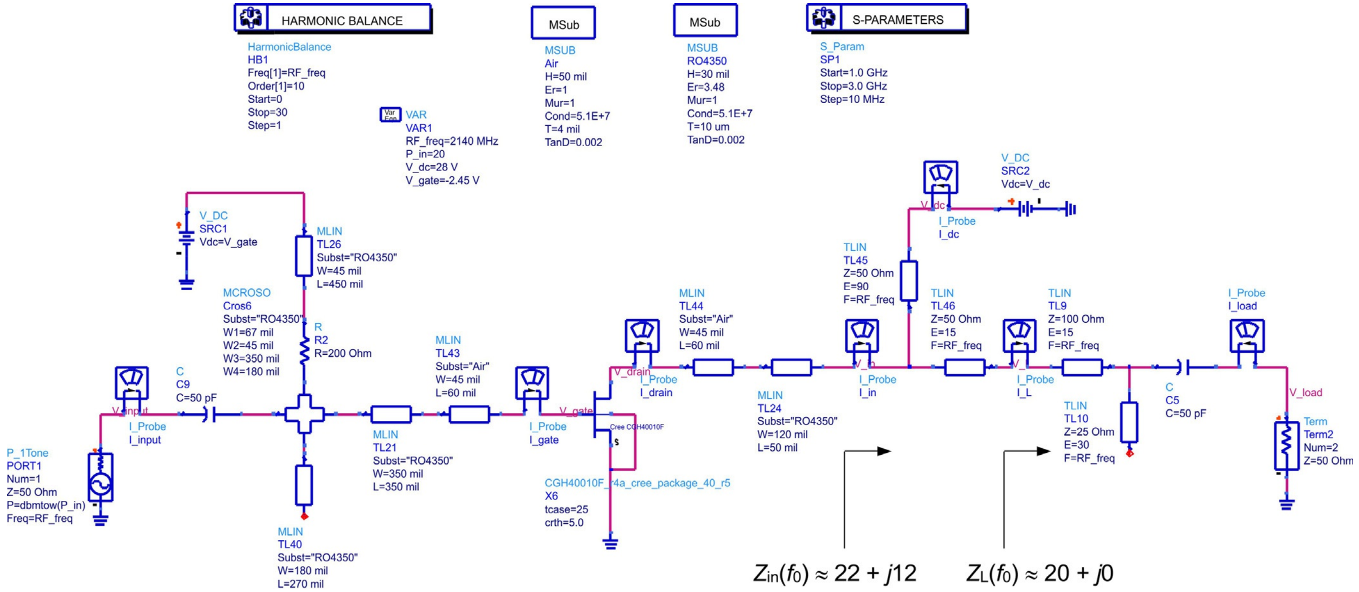
As a result, if the required optimum Class-E load resistance R is equal to $20\,\Omega$ and standard load $R_L = 50\,\Omega$ resulting in $r = R_L/R = 2.5$, the characteristic impedance of the series transmission line Z_1 calculated from Eq. (7.62) is equal to approximately $100\,\Omega$ and the characteristic impedance of the open-circuit stub Z_2 calculated from Eq. (7.63) is equal to $25\,\Omega$ for electrical length $\theta_1 = 15°$.

Fig. 7.13 shows the simulated circuit schematic which approximates a 2.14-GHz transmission-line Class-E power amplifier based on a 28-V 10-W Cree GaN HEMT power transistor CGH40010F and ideal transmission-line load network with the second- and third-harmonic tuning. The input matching circuit provides a complex-conjugate matching of the device input gate-source impedance $Z_{gs} \approx 5 + j2$ with the standard 50-Ω source. In this case, the input matching topology can simply be designed in the form of an L-type transformer with a series transmission line and an open-circuit stub.[3, 6] The device output stripline lead is connected to a short-length wide metal pad of 50 mil × 120 mil on the substrate. In this case, the device input and output leads are modeled by the stripline of 45 mil × 60 mil each in air substrate. It should be noted that approximated equivalent network of device output parasitics for a packaged 10-W GaN Cree device model includes not only the shunt capacitance C_{ds} and series bondwire inductance but also two low-pass LC sections corresponding to the internal package model.[16] Therefore the parameters of the ideal transmission lines in the load network can be optimized to achieve maximum efficiency since effect on the second- and third-harmonic impedance can be slightly different when considering a simplified model of the device output circuit with one shunt capacitance and one series inductance only.

Fig. 7.14 shows the simulated results of a transmission-line Class-E GaN HEMT power amplifier with ideal transmission lines in the load network. The maximum output power of 40.5 dBm, power gain of 12.7 dB (linear gain over 18 dB), drain efficiency of 85.5%, and *PAE* of 81% are achieved at an operating frequency of 2.14 GHz with a supply voltage of 28 V and a quiescent current of 50 mA. The maximum drain efficiency was achieved at a gain compression point of about 5 dB.

Fig. 7.15 shows the drain (A) voltage and (B) current waveforms corresponding to the transmission-line Class-E approximation. The drain voltage waveform is very similar to idealized one shown in Fig. 7.7B, with a peak factor of about 2.4 which is sufficiently small taking into account the device drain-source breakdown voltage of 120 V. The current flowing through the device output capacitance during off-state operation mode contributes to the total drain current waveform shown in Fig. 7.15B, since it is measured at the output device terminal outside of the device package. In this case, the main contributor to efficiency degradation is the saturation resistance r_{sat} reducing efficiency by 11%, whereas the finite fall time of the driving switching signal degrades efficiency by a few percent only. At the same time, to maximize drain efficiency, it is very important to choose the PCB board with a low-loss substrate such as RO4350.

Fig. 7.16 shows the simulated circuit schematic of a 2.14-GHz transmission-line Class-E power amplifier, which is based on the nonlinear model for a 28-V 10-W GaN HEMT power transistor CGH40010F and technical parameters for a 30-mil RO4350 substrate. The load network is slightly modified by optimizing the parameters of the series microstrip lines and open-circuit stub because the series microstrip line with very high characteristic impedance results in excessive insertion losses. The physical parameters of the microstrip lines using a RO4350 substrate can easily be determined by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HarmonicBalance
HB1
Freq[1]=RF_freq
Order[1]=10
Start=0
Stop=30
Step=1
VAR
VAR1
RF_freq=2140 MHz
P_in=20
V_dc=28 V
V_gate=-2.45 V
MSub
MSUB
Air
H=50 mil
Er=1
Mur=1
Cond=5.1E+7
T=4 mil
TanD=0.002
MSub
MSUB
RO4350
H=30 mil
Er=3.48
Mur=1
Cond=5.1E+7
T=10 um
TanD=0.002
S-PARAMETERS
S_Param
SP1
Start=1.0 GHz
Stop=3.0 GHz
Step=10 MHz
V_DC
SRC1
Vdc=V_gate
MLIN
TL26
Subst="RO4350"
W=45 mil
L=450 mil
MCROSO
Cros6
Subst="RO4350"
W1=67 mil
W2=45 mil
W3=350 mil
W4=180 mil
R
R2
R=200 Ohm
C
C9
C=50 pF
V_input
I_Probe
I_input
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(P_in)
Freq=RF_freq
MLIN
TL40
Subst="RO4350"
W=180 mil
L=270 mil
MLIN
TL21
Subst="RO4350"
W=350 mil
L=350 mil
MLIN
TL43
Subst="Air"
W=45 mil
L=60 mil
I_Probe
I_gate
V_gate
V_drain
I_Probe
I_drain
Cree CGH40010F
S
CGH40010F_r4a_cree_package_40_r5
X6
tcase=25
crth=5.0
MLIN
TL44
Subst="Air"
W=45 mil
L=60 mil
MLIN
TL24
Subst="RO4350"
W=120 mil
L=50 mil
V_in
I_Probe
I_in
TLIN
TL45
Z=50 Ohm
E=90
F=RF_freq
V_dc
I_Probe
I_dc
V_DC
SRC2
Vdc=V_dc
TLIN
TL46
Z=50 Ohm
E=15
F=RF_freq
V_L
I_Probe
I_L
TLIN
TL9
Z=100 Ohm
E=15
F=RF_freq
TLIN
TL10
Z=25 Ohm
E=30
F=RF_freq
C
C5
C=50 pF
I_Probe
I_load
V_load
Term
Term2
Num=2
Z=50 Ohm
$Z_{in}(f_0) \approx 22 + j12$
$Z_L(f_0) \approx 20 + j0$

FIG. 7.13

Simulation setup for Class-E power amplifier with ideal transmission lines in load network.

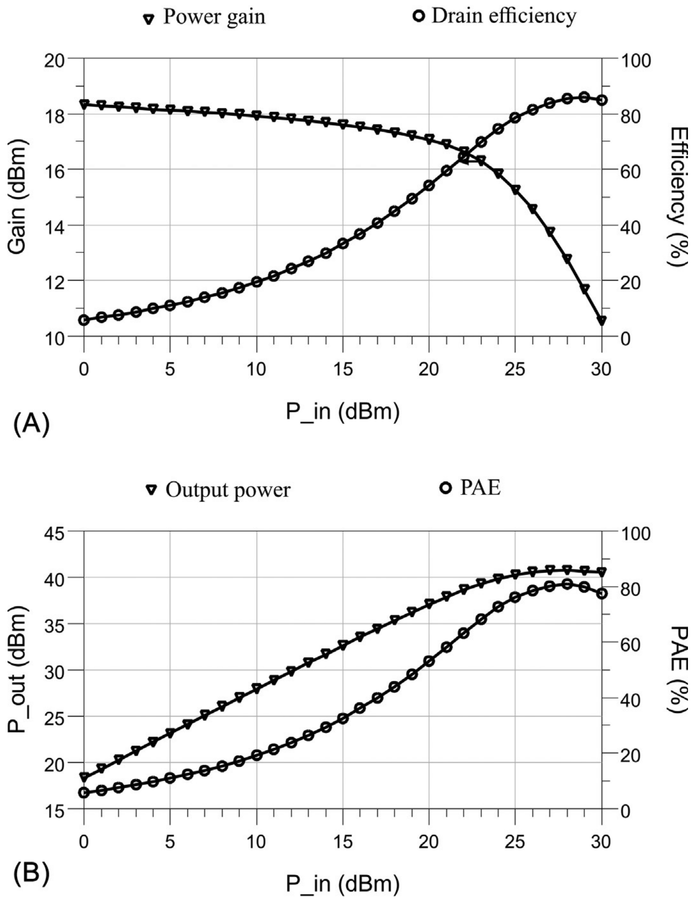


FIG. 7.14

Simulated results of Class-E power amplifier with ideal transmission lines.

using an ADS transmission-line calculator LineCalc, which can be found in Tools displayed by Project menu. The input matching circuit remains the same as for an idealized version of the Class-E power amplifier with a quarterwave transmission line shown in Fig. 7.13.

Fig. 7.17 shows the simulated results of a transmission-line Class-E GaN HEMT power amplifier implemented on a 30-mil RO4350 substrate. In this case, the maximum output power of 40.0 dBm, power gain of 12.0 dB (linear gain close to 20 dB), drain efficiency of 83.8%, and *PAE* of 79.5% are achieved at an operating frequency of 2.14 GHz with a supply voltage of 28 V.

Because of the shorting effect for the second harmonic of the grounded quarterwave microstrip line and high-impedance condition provided by the open-circuit stub and series microstrip line with a quarterwave length for the third harmonic, the second- and third-harmonic suppression is achieved at the level of approximately 40 dB, as shown in Fig. 7.18.

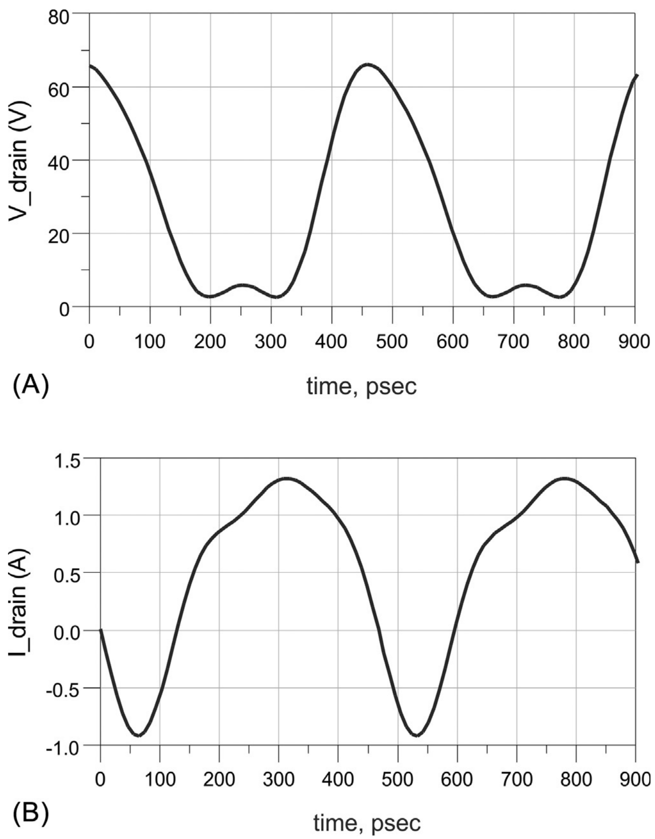
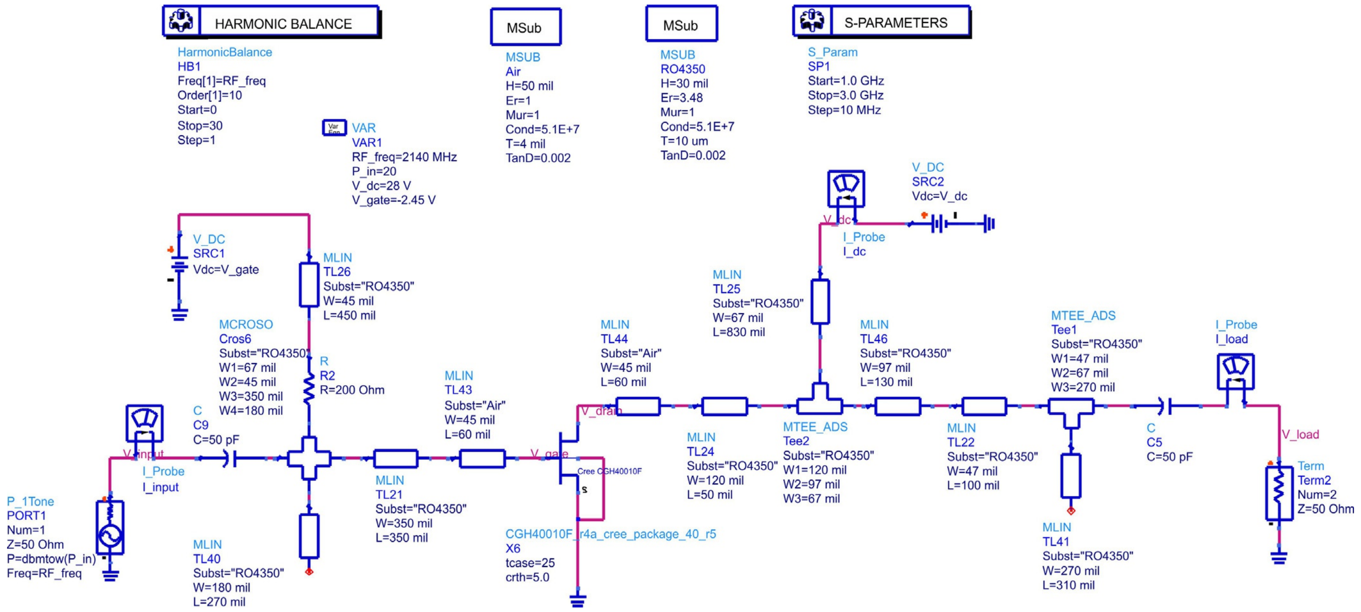


FIG. 7.15

Drain voltage and current waveforms.

7.8 Design example: 10-W 2.14-GHz Class-E GaN HEMT power amplifier with transmission-line filter

As an alternative, the quarterwave line can be conductively connected into the load network providing a parallel connection of the shunt open- and short-circuit stubs, which provides more compact design and also can add the broader capability of such a Class-E power amplifier with transmission-line filter.[17] Let us analyze these two transmission-line circuits, one representing by a grounded quarterwave line, as shown in Fig. 7.19A, and the other representing by a parallel connection of the shunt open- and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HarmonicBalance
HB1
Freq[1]=RF_freq
Order[1]=10
Start=0
Stop=30
Step=1
MSub
MSUB
Air
H=50 mil
Er=1
Mur=1
Cond=5.1E+7
T=4 mil
TanD=0.002
MSub
MSUB
RO4350
H=30 mil
Er=3.48
Mur=1
Cond=5.1E+7
T=10 um
TanD=0.002
S-PARAMETERS
S_Param
SP1
Start=1.0 GHz
Stop=3.0 GHz
Step=10 MHz
VAR
VAR1
RF_freq=2140 MHz
P_in=20
V_dc=28 V
V_gate=-2.45 V
V_DC
SRC1
Vdc=V_gate
MLIN
TL26
Subst="RO4350"
W=45 mil
L=450 mil
MCROSO
Cros6
Subst="RO4350"
W1=67 mil
W2=45 mil
W3=350 mil
W4=180 mil
R
R2
R=200 Ohm
C
C9
C=50 pF
V_input
I_Probe
I_input
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(P_in)
Freq=RF_freq
MLIN
TL40
Subst="RO4350"
W=180 mil
L=270 mil
MLIN
TL21
Subst="RO4350"
W=350 mil
L=350 mil
MLIN
TL43
Subst="Air"
W=45 mil
L=60 mil
V_gate
Cree CGH40010F
s
CGH40010F_r4a_cree_package_40_r5
X6
tcase=25
crth=5.0
V_drain
MLIN
TL44
Subst="Air"
W=45 mil
L=60 mil
MLIN
TL24
Subst="RO4350"
W=120 mil
L=50 mil
V_dc
I_Probe
I_dc
V_DC
SRC2
Vdc=V_dc
MLIN
TL25
Subst="RO4350"
W=67 mil
L=830 mil
MTEE_ADS
Tee2
Subst="RO4350"
W1=120 mil
W2=97 mil
W3=67 mil
MLIN
TL46
Subst="RO4350"
W=97 mil
L=130 mil
MLIN
TL22
Subst="RO4350"
W=47 mil
L=100 mil
MTEE_ADS
Tee1
Subst="RO4350"
W1=47 mil
W2=67 mil
W3=270 mil
MLIN
TL41
Subst="RO4350"
W=270 mil
L=310 mil
C
C5
C=50 pF
I_Probe
I_load
V_load
Term
Term2
Num=2
Z=50 Ohm

FIG. 7.16

Simulation setup for Class-E power amplifier with microstrip lines.

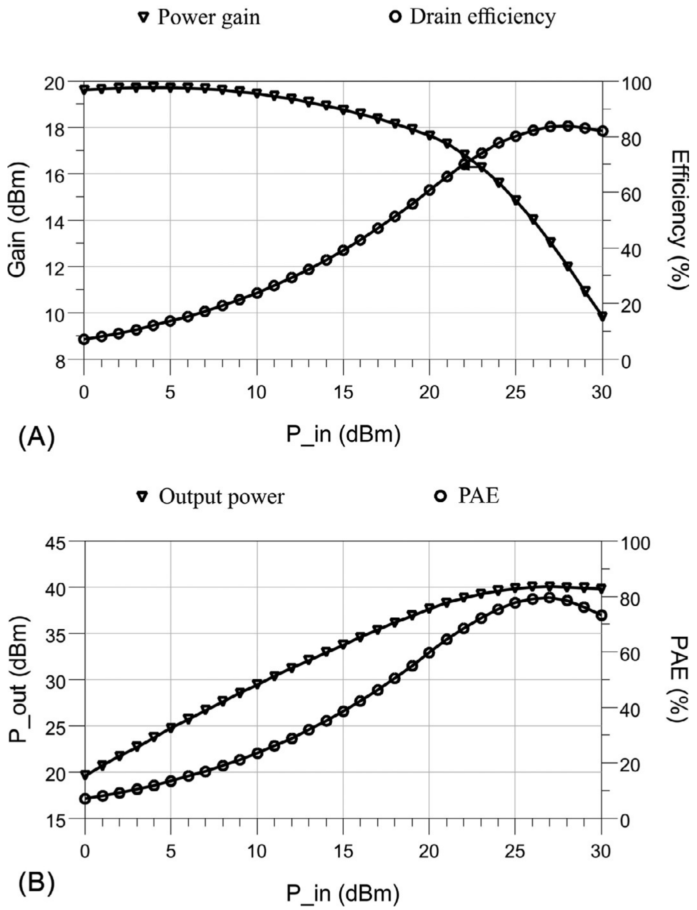


FIG. 7.17

Simulated results of Class-E power amplifier with microstrip lines.

short-circuit stubs, as shown in Fig. 7.19B. The input impedance Z_{net} for the grounded quarterwave line with the characteristic impedance Z_0 and electrical length θ is written as

$$Z_{\text{net}} = jZ_0 \tan\theta, \tag{7.71}$$

whereas the input impedance Z_{net} for the parallel connection of a shunt open-circuit stub with the characteristic impedance Z_1 and electrical length $k\theta$ and a shunt short-circuit stub with the characteristic impedance Z_1 and electrical length $(1-k)\theta$, where k is the connecting factor, are obtained by

$$Z_{\text{net}} = \frac{Z_{\text{net1}} Z_{\text{net2}}}{Z_{\text{net1}} + Z_{\text{net2}}} = jZ_1 \frac{\tan k\theta}{1 - \tan k\theta \tan(1-k)\theta}, \tag{7.72}$$

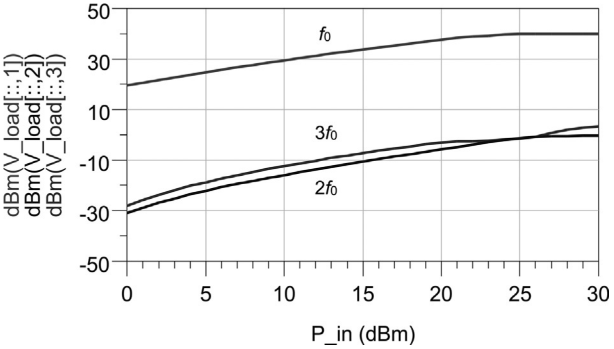


FIG. 7.18

Simulated results of second- and third-harmonic suppression.

where

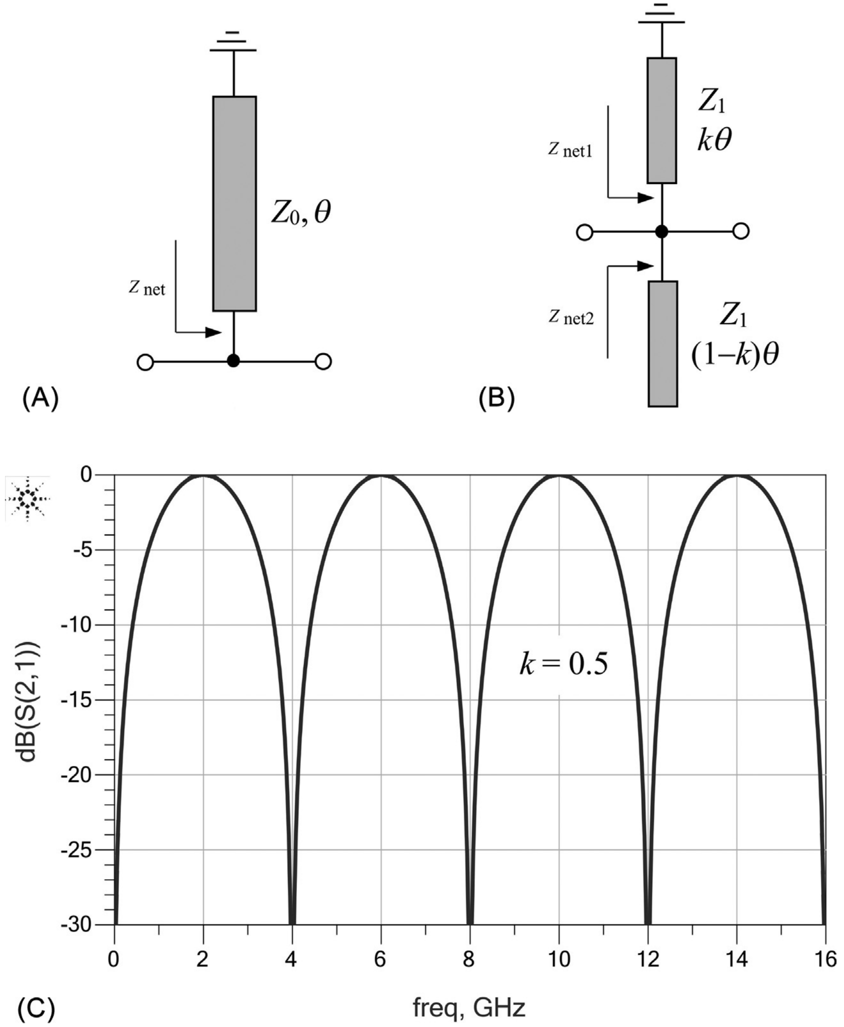
$$Z_{\text{net1}} = jZ_1 \tan k\theta, \tag{7.73}$$

$$Z_{\text{net2}} = \frac{Z_1}{j\tan(1-k)\theta}. \tag{7.74}$$

Comparing of Eqs. (7.71) and (7.72) for identical frequency behavior of the input impedance Z_{net} for both transmission-line circuits results in $k = 0.5$ and $Z_1 = 2Z_0$. This means that, for example, at an operating frequency of 2 GHz, infinite impedance at the fundamental and odd harmonics and zero impedance at even harmonics will be provided both for the circuit with shunt quarterwave line ($\theta = 90°$) and for the circuit with shunt short- and open-circuit stubs having an electrical length $\theta = 45°$ and a characteristic impedance of $2Z_0$ each, as shown in Fig. 7.19C.

Fig. 7.20 shows the circuit schematic of a high-efficiency Class-E power amplifier with transmission-line filter and output matching circuit, where the nominal Class-E load resistance $R = \text{Re}Z_{\text{net}}(\omega_0)$ is matched to the standard load impedance $R_L = 50\,\Omega$ at the fundamental frequency using an output transmission-line L-type impedance transformer. Here the equivalent of a quarterwave line is composed of 45 degrees short- and open-circuit stubs to create short-circuit conditions at even harmonics. To create an open-circuit condition at the third harmonic at the input of the output matching circuit, the corresponding series and shunt open-circuit stubs are used, each having an electrical length of 30 degrees.

First, consider separately the transmission-line filter consisting of the open- and short-circuit microstrip stubs and an L-type microstrip-line output matching circuit shown in Fig. 7.21A. Because the output drain-source capacitance of a 28-V 10-W Cree GaN HEMT power transistor CGH40010F is equal to 1.3 pF which is almost two times greater than that required for nominal Class-E mode according to Eq. (7.47), therefore the load resistance Z_{load} was intentionally lowered to 12 Ω, as shown in Fig. 7.21B by hodograph for $Z_{\text{load}}(\omega_0)$ at the Smith chart within the bandwidth of 2.1–2.2 GHz, to further approximate the required Class-E inductive impedance at the fundamental frequency seen by the device multiharmonic current source operating as a nonideal switch. Here, hodograph for the



Z_0, θ
Z net
(A)
Z_1
$k\theta$
Z net1
Z net2
Z_1
$(1-k)\theta$
(B)
0
-5
-10
-15
-20
-25
-30
dB(S(2,1))
$k = 0.5$
0
2
4
6
8
10
12
14
16
freq, GHz
(C)

FIG. 7.19

Conductive connection of quarterwave line and frequency response.

second-harmonic $Z_{\text{load}}(2\omega_0)$ demonstrates near-zero impedance conditions within the bandwidth of 4.2–4.4 GHz, whereas hodograph for the third-harmonic Z_{load} $(3\omega_0)$ shows the high-impedance conditions within the bandwidth of 6.3–6.6 GHz.

The entire Class-E load network with transmission-line filter with a 30 degrees series microstrip-line stub and a 30 degrees shunt open-circuit microstrip-line stub, both having a characteristic impedance of 50 Ω, and L-type transmission-line output matching circuit implemented in a 30-mil RO4350 substrate is shown in Fig. 7.22A, with the device output shunt capacitance and series bondwire

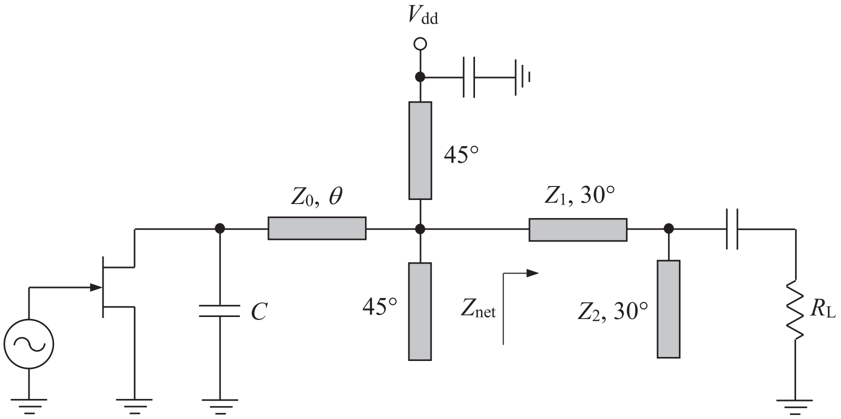


FIG. 7.20

Schematic of Class-E power amplifiers with transmission-line load network.

inductance. Here the device output shunt capacitance and series inductance with an additional series microstrip line provides the required Class-E inductive impedance at the fundamental frequency and approximate the capacitive reactances at the second and third harmonics, respectively. The hodographs corresponding to the inductive fundamental impedance Z_{load} (ω_0) and to the second-harmonic reactance Z_{load} $(2\omega_0)$ and third-harmonic reactance Z_{load} $(3\omega_0)$ for the entire load network of a 10-W GaN HEMT power amplifier shown in Fig. 7.22B demonstrates their close proximity to those of the idealized Class-E load network with a series filter.[17] This means that if even the required output device parameters do not properly match the nominal Class-E load-network parameters, the high efficiency can nonetheless be achieved by optimizing the external load-network parameters to provide close approximation of the required impedances for the fundamental, second, and third harmonics.

Fig. 7.23 shows the simulated circuit schematic, which approximates the Class-E power amplifier with transmission-line filter, based on a 28-V 10-W Cree GaN HEMT power transistor CGH40010F and a transmission-line load network shown in Fig. 7.22A. Here the input matching circuit provides a complex-conjugate matching with the standard 50-Ω source with acceptable accuracy and stability of operation. The load network was slightly modified by optimizing the parameters of the series and shunt transmission lines because the device output capacitance C_{out} and series inductance L_{out} formed by drain bondwires and package lead do not properly match the required values of the shunt capacitance C and series inductance L for a nominal Class-E mode with transmission-line filter. To maximize the level of harmonic suppression, the lengths of both open- and short-circuit stubs were slightly increased.

For the GaN HEMT Class-E power amplifier with transmission-line filter using a 30-mil RO4350 substrate, the simulated drain efficiency of 85.2% and power gain of 15 dB resulting in a *PAE* of 82.5% at an output power of 40.8 dBm with a quiescent current of 18 mA are achieved at an operating frequency of 2.14 GHz with a DC supply voltage of 28 V, as shown in Fig. 7.24.[17] The second and third harmonics were suppressed by more than 34 dB.

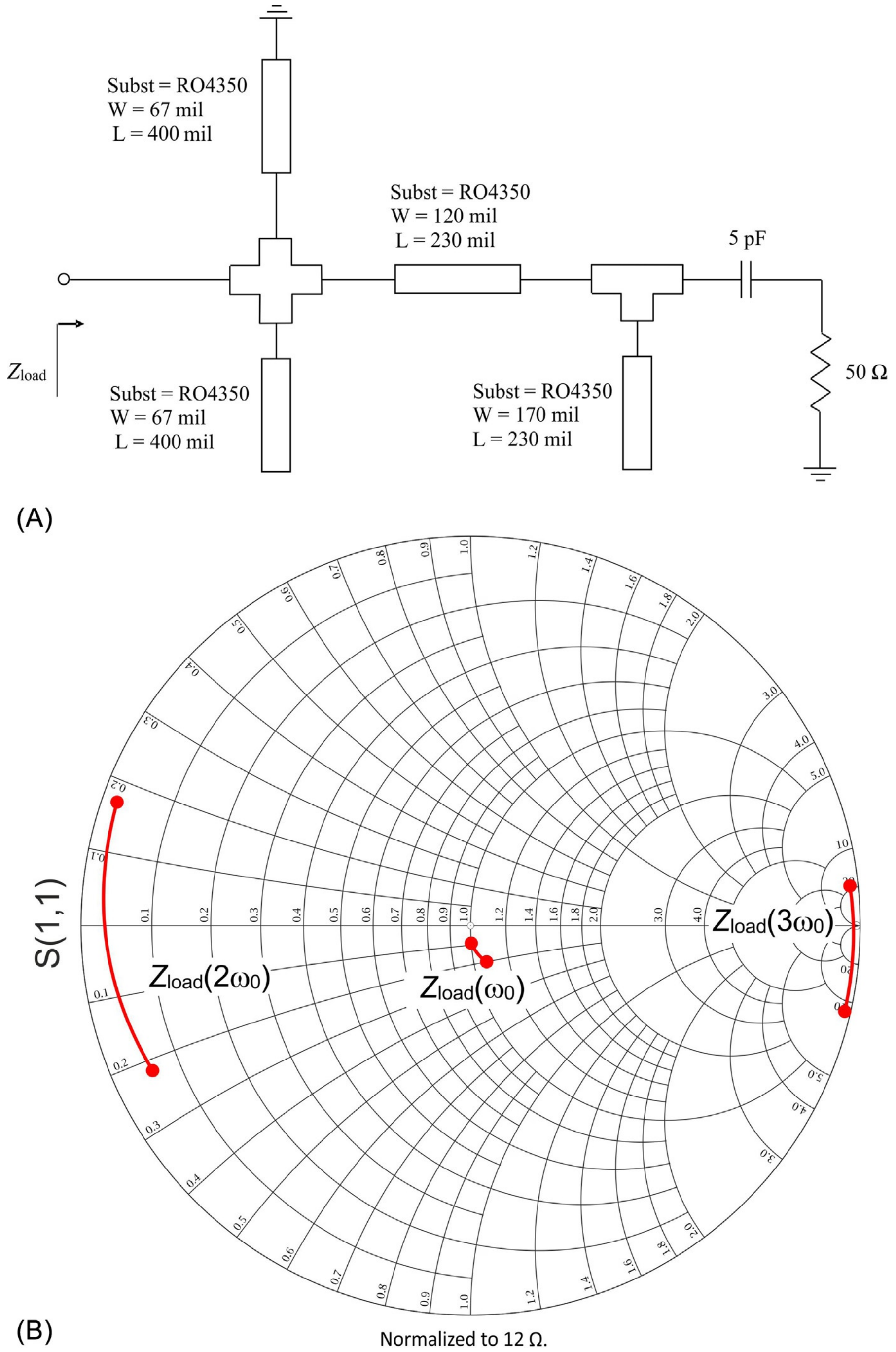

Subst = RO4350
W = 67 mil
L = 400 mil
Subst = RO4350
W = 120 mil
L = 230 mil
5 pF
Z_{load}
50 Ω
Subst = RO4350
W = 67 mil
L = 400 mil
Subst = RO4350
W = 170 mil
L = 230 mil
(A)
S(1,1)
$Z_{load}(2\omega_0)$
$Z_{load}(\omega_0)$
$Z_{load}(3\omega_0)$
(B)
Normalized to 12 Ω.

FIG. 7.21

Transmission-line load network and harmonic impedances.

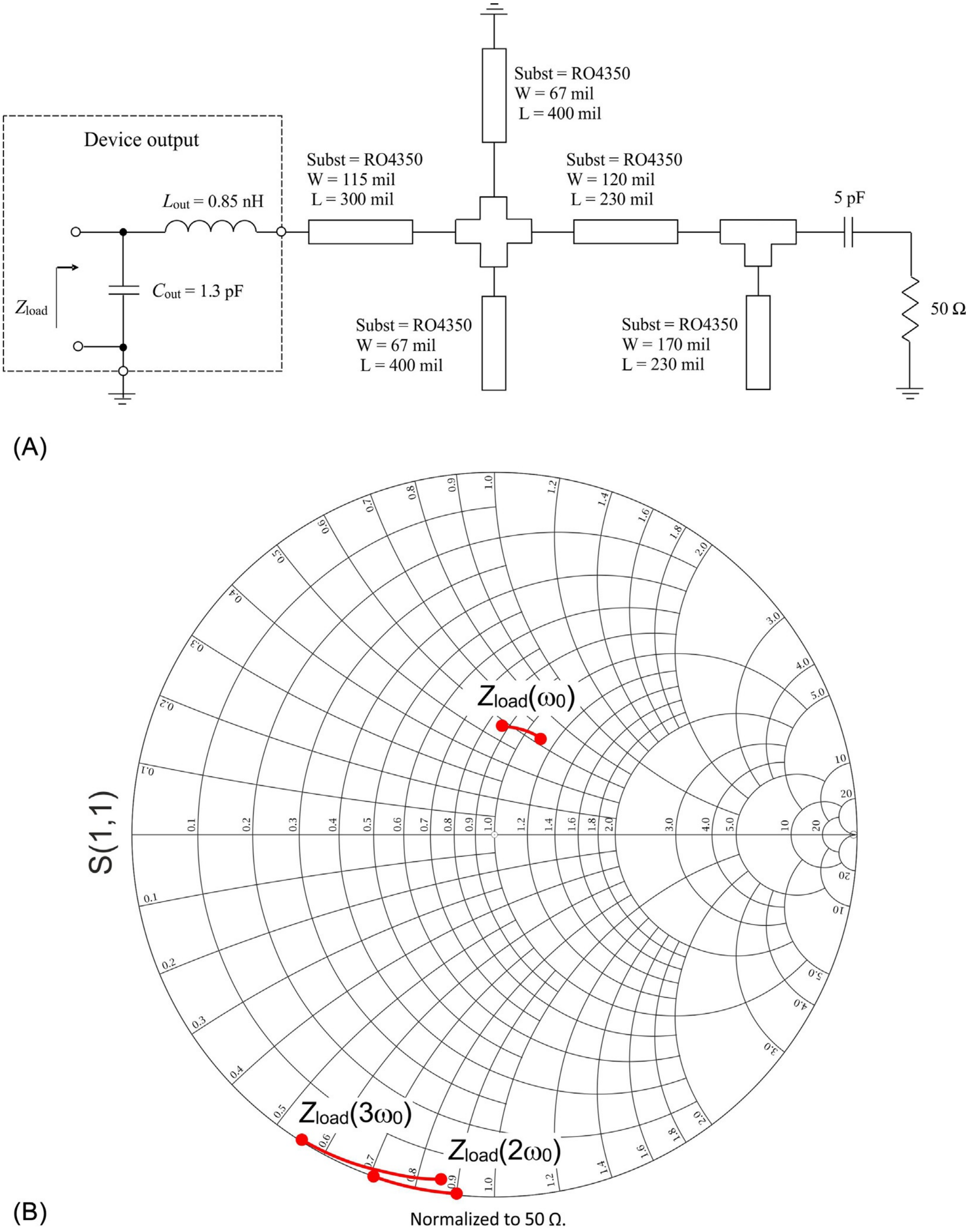

Device output
L_{out} = 0.85 nH
C_{out} = 1.3 pF
Z_{load}
Subst = RO4350
W = 115 mil
L = 300 mil
Subst = RO4350
W = 67 mil
L = 400 mil
Subst = RO4350
W = 67 mil
L = 400 mil
Subst = RO4350
W = 120 mil
L = 230 mil
Subst = RO4350
W = 170 mil
L = 230 mil
5 pF
50 Ω
(A)
S(1,1)
$Z_{load}(\omega_0)$
$Z_{load}(3\omega_0)$
$Z_{load}(2\omega_0)$
Normalized to 50 Ω.
(B)

FIG. 7.22

Class-E load network with transmission-line filter and harmonic impedances.

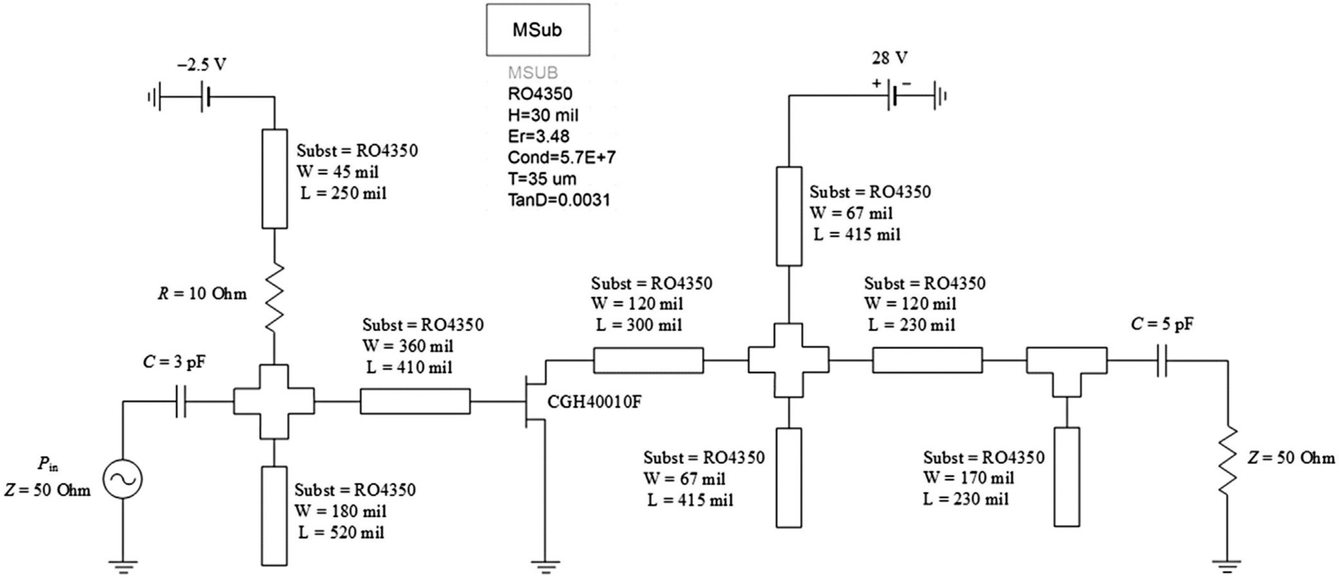

MSub
MSUB
RO4350
H=30 mil
Er=3.48
Cond=5.7E+7
T=35 um
TanD=0.0031
−2.5 V
Subst = RO4350
W = 45 mil
L = 250 mil
R = 10 Ohm
C = 3 pF
Subst = RO4350
W = 360 mil
L = 410 mil
P_{in}
Z = 50 Ohm
Subst = RO4350
W = 180 mil
L = 520 mil
CGH40010F
Subst = RO4350
W = 120 mil
L = 300 mil
28 V
+
−
Subst = RO4350
W = 67 mil
L = 415 mil
Subst = RO4350
W = 120 mil
L = 230 mil
C = 5 pF
Subst = RO4350
W = 67 mil
L = 415 mil
Subst = RO4350
W = 170 mil
L = 230 mil
Z = 50 Ohm

FIG. 7.23

Circuit schematic of Class-E GaN HEMT power amplifier with transmission-line filter.

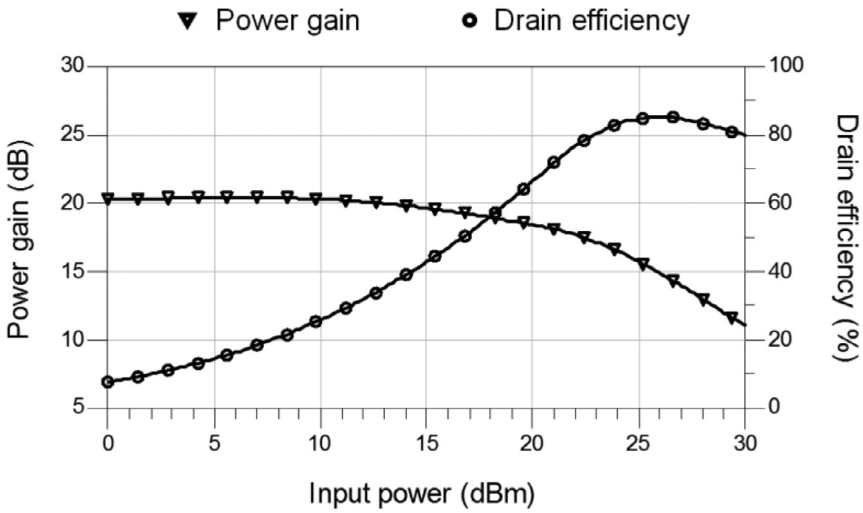


FIG. 7.24

Simulated results of Class-E GaN HEMT power amplifier with transmission-line filter.

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CHAPTER

Class-E with shunt capacitance and shunt filter

8

An analysis of a Class-E mode with shunt capacitance and shunt filter with explicit derivation of the idealized optimum voltage and current waveforms and load-network parameters with their verification by frequency-domain simulations is presented in this chapter. The ideal collector voltage and current waveforms demonstrate a possibility of 100% efficiency. A multiplicity of solutions for the load-network parameters can be achieved for Class-E with shunt capacitance and shunt filter when an additional reactance is introduced between the shunt filter and the load, which can generally have inductive, zero, or capacitive reactance. Several practical implementations of the Class-E power amplifier with shunt filter and series reactance with load networks based on lumped elements and transmission lines at different operating frequencies are described.

8.1 Switchmode vacuum-tube amplifier with shunt filter: Historical aspect

To improve the switchmode power amplifier spectral performance at the load, the load-network schematic with a shunt filter instead of a series filter, as shown in Fig. 8.1A, was proposed by Anatoly Artym at the end of 1960s.[1–4] Here, the shunt filter is tuned to the frequency close to the operating frequency and provides close to sinewave load current due to its high-Q filtering properties, which can be easily realized by lowering the filter capacitor value. This circuit was analyzed by solving the second-order differential equation for voltage across the shunt capacitor C, assuming zero-voltage and zero voltage-derivative switching conditions at the moment the tube is turned on when there are no jumps in anode current and voltage because the shunt capacitor is fully discharged. However, the final design equations for the load-network parameters were not derived in explicit form.

The anode voltage and current waveforms shown in Fig. 8.1B were obtained for a particular case of $q=\frac{1}{\omega}\sqrt{LC}=2$, where ω is the operating angular frequency, although a multiplicity of solutions for operating in the switching mode with different q was possible. In this case, the phase angle of the detuned shunt filter and the load resistance are approximately 54 degrees and $0.7E_0/I_0$, respectively, where E_0 is the DC supply voltage and I_0 is the anode DC current. It was shown that an output power of 5 kW with an anode efficiency of 90% (including losses in the tube and load network) can be achieved with a DC supply voltage of 5 kV at an operating frequency of 1 MHz.

Fig. 8.2 illustrates the practical implementation of a switchmode vacuum-tube amplifier with a waveform control using the load network with a shunt capacitor composed of two parallel-connected capacitors, a series inductance L, and a parallel $L_K C_K$ resonant circuit.[1, 5] The load-network parameters of the amplifier were calculated according to the design approach given in Ref. 4, resulting in a measured efficiency of 96.5% for a 3-kW vacuum-tube amplifier operating at 13.5 kHz.

Switchmode RF and Microwave Power Amplifiers. https://doi.org/10.1016/B978-0-12-821448-0.00011-2
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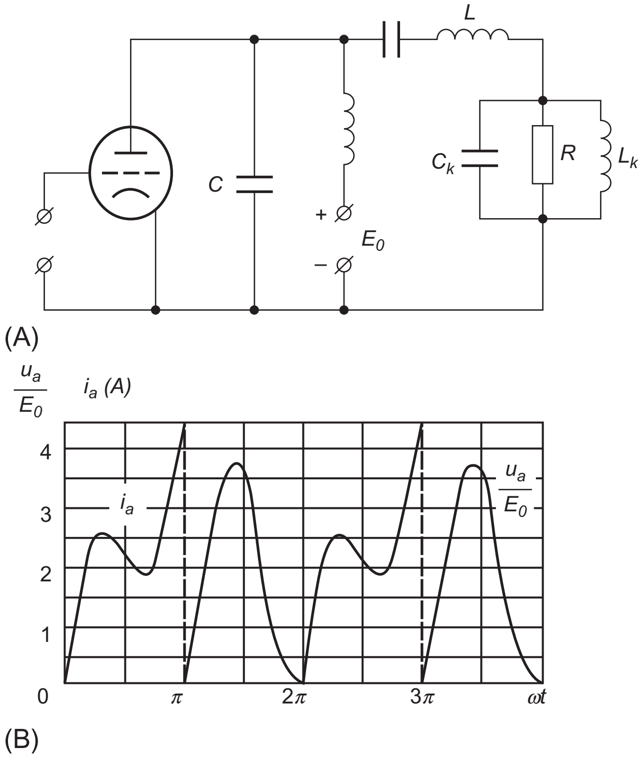

L
C
C_k
R
L_k
+
E_0
−
(A)
$\frac{u_a}{E_0}$
i_a (A)
4
3
2
1
0
i_a
$\frac{u_a}{E_0}$
π
2π
3π
ωt
(B)

FIG. 8.1

Switchmode vacuum-tube amplifier with shunt filter and anode waveforms.

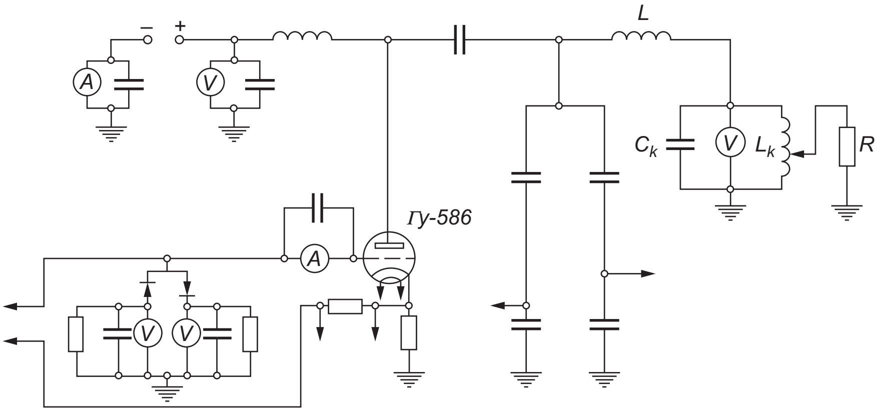

−
+
A
V
L
C_k
V
L_k
R
Гу-586
A
V
V

FIG. 8.2

Switchmode vacuum-tube amplifier with parallel resonant circuit.

8.2 Load network with shunt capacitance and shunt filter

The optimum parameters of a single-ended Class-E power amplifier with shunt capacitance and shunt filter can be determined based on an analytical derivation of its steady-state collector voltage and current waveforms.[6] Fig. 8.3A shows the basic circuit configuration of a Class-E power amplifier with shunt capacitance and shunt filter, where the load network consists of a shunt capacitance C, a series inductor L, a blocking capacitor C_b, a shunt fundamentally tuned L_0C_0 circuit, and a load resistor R. In this case, the shunt L_0C_0 circuit operates as a harmonic filter creating zero impedance at the second- and higher-order harmonics instead of the open-circuit harmonic conditions corresponding to the conventional Class-E power amplifier with shunt capacitance and series filter. In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The DC power supply is connected by an radio-frequency (RF) choke with infinite reactance at the fundamental and any higher-order harmonic component. The active device is considered an ideal switch that is driven at the operating frequency to provide instantaneous switching between its on-state and off-state operation conditions.

To simplify the analysis of a single-ended Class-E power amplifier with shunt filter, whose equivalent circuit is shown in Fig. 8.3B, the following several assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.
- The shunt capacitance is assumed to be constant.
- The RF choke allows only a constant DC current and has no resistance.
- The shunt L_0C_0 filter has zero impedance at the second- and higher-order harmonics.
- There are no losses in the circuit except only in the load R.
- For simplicity, a 50% duty ratio is used.

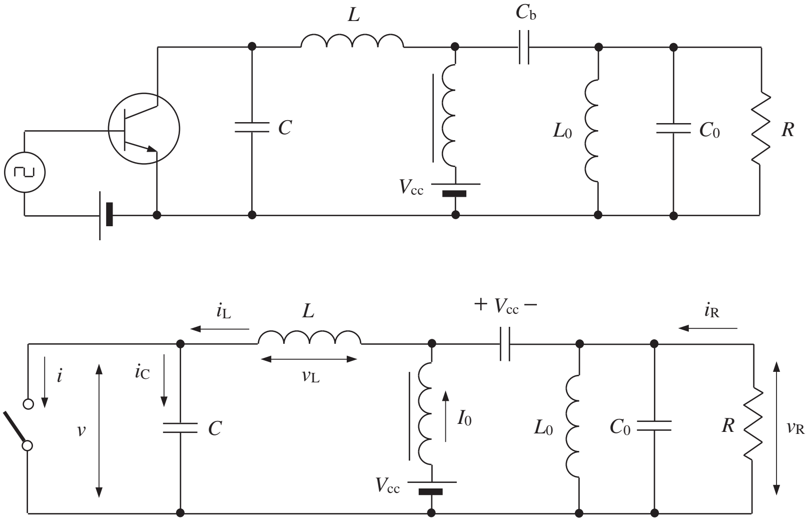


FIG. 8.3

Basic circuits of Class-E power amplifier with shunt filter.

For a lossless operation mode, it is necessary to provide the following idealized optimum (or nominal) conditions for voltage across the switch (just before the start of the switch on) at the moment $\omega t = 2\pi$, when the transistor is saturated:

$$v(\omega t)\big|_{\omega t=2\pi} = 0, \tag{8.1}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0, \tag{8.2}$$

where $v(\omega t)$ is the voltage across the switch. Note that these nominal or idealized optimum Class-E switching conditions do not correspond to minimum dissipated power losses for the nonideal transistor switch with finite value of its saturation resistance.

Let the output current i_R flowing through the load be sinusoidal,

$$i_R(\omega t) = I_R \sin(\omega t + \varphi), \tag{8.3}$$

where φ is the initial phase shift.

When the switch is turned on for of $0 \le \omega t \le \pi$, the voltage on the switch is

$$v(\omega t) = V_{cc} - v_L(\omega t) - v_R(\omega t) = 0, \tag{8.4}$$

where

$$v_L(\omega t) = \omega L \frac{di_L(\omega t)}{d\omega t}, \tag{8.5}$$

$$v_R(\omega t) = V_R \sin(\omega t + \varphi), \tag{8.6}$$

where $V_R = I_R R$ is the voltage amplitude across the load.

As the current flowing through the shunt capacitance C is

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = 0, \tag{8.7}$$

consequently,

$$i(\omega t) = i_L(\omega t), \tag{8.8}$$

where

$$i_L(\omega t) = \frac{1}{\omega L}\int_0^{\omega t} V_{cc}\, d\omega t + \frac{V_R}{\omega L}\cos(\omega t + \varphi) + i_L(0). \tag{8.9}$$

Because $i(0) = 0$, the initial value for the current $i_L(\omega t)$ flowing through the series inductor L at time instant $\omega t = 0$ can be defined using Eqs. (8.8) and (8.9) as

$$i_L(0) = -\frac{V_R}{\omega L}\cos\varphi. \tag{8.10}$$

As a result, from Eqs. (8.8) to (8.10), it follows that

$$i(\omega t) = \frac{V_{cc}}{\omega L}\omega t + \frac{V_R}{\omega L}[\cos(\omega t + \varphi) - \cos\varphi]. \tag{8.11}$$

When the switch is turned off for $\pi \le \omega t < 2\pi$, there is no current flowing through the switch, that is, $i(\omega t) = 0$, and the current flowing through the capacitor C can be written as $i_C(\omega t) = i_L(\omega t)$, or

$$i_C(\omega t) = \omega C \frac{dv}{d\omega t} = \frac{1}{\omega L} \int_{\pi}^{\omega t} [V_{\text{cc}} - v(\omega t) - v_{\text{R}}(\omega t)] d\omega t + i_{\text{L}}(\pi), \tag{8.12}$$

under the initial off-state conditions $v(\pi) = 0$ and

$$i_{\text{C}}(\pi) = \frac{\pi V_{\text{cc}} - 2V_{\text{R}} \cos \varphi}{\omega L}. \tag{8.13}$$

Eq. (8.12) can be represented in the form of the linear nonhomogeneous second-order differential equation by

$$\omega^2 LC \frac{d^2 v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{\text{cc}} + V_{\text{R}} \sin(\omega t + \varphi) = 0, \tag{8.14}$$

whose general solution can be given in the normalized form as

$$\frac{v(\omega t)}{V_{\text{cc}}} = C_1 \cos q\omega t + C_2 \sin q\omega t + 1 + \frac{q^2}{1-q^2} \frac{V_{\text{R}}}{V_{\text{cc}}} \sin(\omega t + \varphi), \tag{8.15}$$

where

$$q = \frac{1}{\omega\sqrt{LC}}, \tag{8.16}$$

and the coefficients C_1 and C_2 are determined from the initial off-state conditions by

$$\begin{aligned} C_1 = &-\cos q\pi - q\pi \sin q\pi + \frac{q}{1-q^2} \frac{V_{\text{R}}}{V_{\text{cc}}} \\ &\times [q \cos q\pi \sin \varphi + (1-2q^2) \sin q\pi \cos \varphi], \end{aligned} \tag{8.17}$$

$$\begin{aligned} C_2 = &-\sin q\pi + q\pi \cos q\pi + \frac{q}{1-q^2} \frac{V_{\text{R}}}{V_{\text{cc}}} \\ &\times [q \sin q\pi \sin \varphi - (1-2q^2) \cos q\pi \cos \varphi]. \end{aligned} \tag{8.18}$$

In this case, when compared to Class-E with shunt capacitance and series filter where the circuit electrical behavior is described by the first-order differential equation, the general solution is derived from the second-order differential equation, similarly to that for Class-E with parallel circuit.

8.3 Optimum load-network parameters

The fundamental-frequency voltage $v_1(\omega t)$ across the switch consists of the two quadrature components, as shown in Fig. 8.4, with an amplitude of the real component defined by Fourier formula as

$$V_{\text{R}} = -\frac{1}{\pi} \int_0^{2\pi} v(\omega t) \sin(\omega t + \varphi) d\omega t. \tag{8.19}$$

As a result, by solving a system of three equations—two of them defined by the Class-E switching conditions given by Eqs. (8.1) and (8.2) and the third one for V_{R} given by Eq. (8.19)—the three unknown parameters can be calculated as

$$\varphi = -41.614°, \tag{8.20}$$

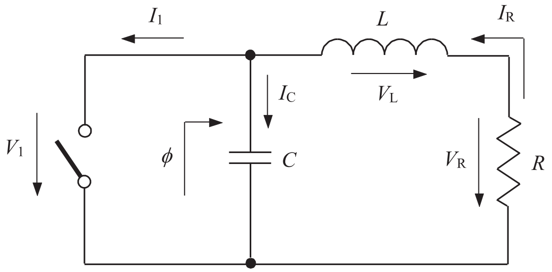


FIG. 8.4

Equivalent Class-E load network at fundamental frequency.

$$q = 1.607, \tag{8.21}$$

$$\frac{V_R}{V_{cc}} = 0.9253. \tag{8.22}$$

For an idealized collector efficiency of 100%, the DC power $P_0 = I_0 V_{cc}$ and the fundamental-frequency output power $P_{out} = V_R^2/(2R)$ delivered to the load are equal,

$$I_0 V_{cc} = \frac{V_R^2}{2R}. \tag{8.23}$$

The DC current I_0 can be determined by applying Fourier-series expansion to Eq. (8.11) as

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)d\omega t = \frac{V_{cc}}{2\pi\omega L}\left[\frac{\pi^2}{2} - \frac{V_R}{V_{cc}}(2\sin\varphi + \pi\cos\varphi)\right]. \tag{8.24}$$

By using Eqs. (8.23) and (8.24), equation for the optimum normalized series inductance L can be derived as

$$\frac{\omega L}{R} = \frac{1}{\pi}\left[\frac{\pi^2}{2} - \frac{V_R}{V_{cc}}(2\sin\varphi + \pi\cos\varphi)\right] \bigg/ \left(\frac{V_R}{V_{cc}}\right)^2. \tag{8.25}$$

Hence, the optimum normalized series inductance L and shunt capacitance C can be calculated using Eqs. (8.16), (8.20)–(8.22), and (8.25) as

$$\frac{\omega L}{R} = 1.4836, \tag{8.26}$$

$$\omega CR = 0.261. \tag{8.27}$$

The optimum load resistance R can be obtained from Eqs. (8.22) and (8.23) for the DC supply voltage V_{cc} and fundamental-frequency output power P_{out} delivered to the load as

$$R = \frac{1}{2}\frac{V_R^2}{P_{out}} = \frac{1}{2}\left(\frac{V_R}{V_{cc}}\right)^2 \frac{V_{cc}^2}{P_{out}} = 0.4281\frac{V_{cc}^2}{P_{out}}. \tag{8.28}$$

Fig. 8.5 shows the normalized collector voltage and current waveforms and sinusoidal current waveform for idealized optimum Class-E mode with shunt capacitance and shunt filter during the entire

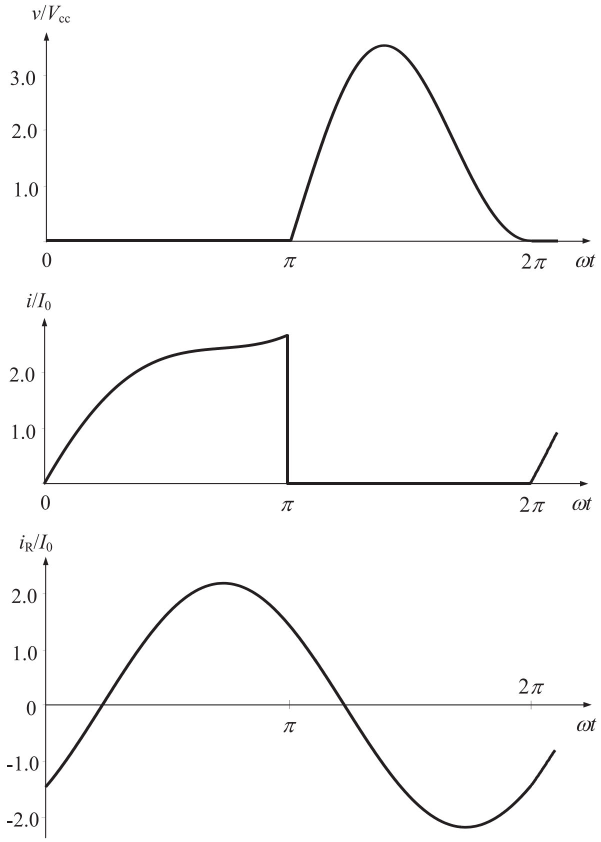


FIG. 8.5

Ideal waveforms for nominal Class-E mode with shunt filter.

interval $0 \le \omega t \le 2\pi$.[6] From the collector voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch and the current from the inductor flows through the switch. However, when the transistor is turned off, this current flows through the capacitor C. In this case, there is no nonzero voltage and current simultaneously, which means a lack of the power losses that gives an idealized collector efficiency of 100% written by Eq. (8.23). Note that the collector voltage and current waveforms of Class-E with shunt capacitance and shunt filter are very close to those corresponding to Class-E with quarterwave transmission line.

The phase angle ϕ of the load network at fundamental seen by the switch shown in Fig. 8.4 and required for an idealized optimum (or nominal) Class-E mode with shunt capacitance and shunt filter can be determined through the load-network parameters using Eqs. (8.26) and (8.27) as

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) - \tan^{-1}\left(\frac{\omega CR}{1 - \frac{\omega L}{R}\omega CR}\right) = 32.945^\circ. \tag{8.29}$$

The peak collector voltage $V_{\max}$ and current $I_{\max}$ can be determined from Eqs. (8.11) and (8.15) using Eq. (8.24) as

$$\frac{V_{\max}}{V_{cc}} = 3.677, \tag{8.30}$$

$$\frac{I_{\max}}{I_0} = 2.768, \tag{8.31}$$

that shows that the voltage peak factor is as high as in a conventional Class-E with shunt capacitance and series filter.[6] The normalized peak switch voltage reduces to approximately 2.5 as the duty ratio D reduces from 0.5 to 0.3, whereas $\omega L/R$ increases to 6.15 and ωCR reduces to 0.14 when D reduces from 0.5 to 0.2.[7]

The maximum operating frequency $f_{\max}$ in a nominal Class-E mode with shunt capacitance and shunt filter is limited by the device output (collector or drain-source) capacitance C_{out}. As a result, from Eqs. (8.27) and (8.28) it follows that

$$f_{\max} = 0.097 \frac{P_{\text{out}}}{C_{\text{out}} V_{cc}^2}, \tag{8.32}$$

which is 1.91 times higher than that for Class-E with shunt capacitance and series filter.

In Table 8.1, the optimum impedances seen by the device collector at the fundamental-frequency and higher-order odd- and even-harmonic components are illustrated by the appropriate circuit configurations. It can be seen that Class-E mode with shunt capacitance and shunt filter shows different

Table 8.1 Optimum impedance at fundamental and harmonics.

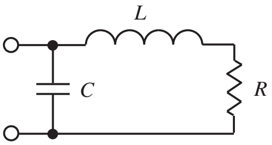
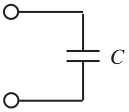
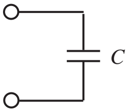
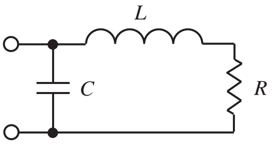
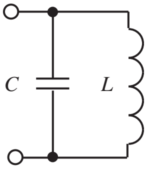
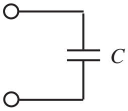
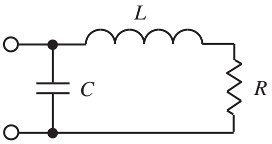
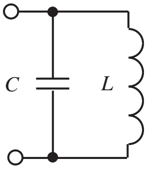
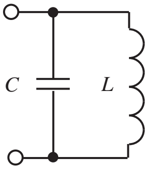
Class-E load network	**f_0 (fundamental)**	**$2nf_0$ (even harmonics)**	**$(2n+1)f_0$ (odd harmonics)**
Class-E with shunt capacitance and series filter			
Class-E with quarterwave line and series filter			
Class-E with shunt capacitance and shunt filter			

Table 8.2 Load-network parameters for different Class-E modes.

Normalized load-network parameter	Class-E with shunt capacitance and series filter	Class-E with quarterwave line and series filter[2]	Class-E with shunt capacitance and shunt filter
$\frac{\omega L}{R}$	1.1525	1.349	1.4836
ωCR	0.1836	0.2725	0.261
$\frac{P_{\text{out}}R}{V_{\text{cc}}^2}$	0.5768	0.465	0.4281
$\frac{f_{\max}C_{\text{out}}V_{\text{cc}}^2}{P_{\text{out}}}$	0.0507	0.093	0.097

impedance properties compared to other alternative Class-E load networks. At even harmonics, its optimum impedances can be established by the parallel *LC* circuit, similarly to Class-E with quarterwave line and series filter. However, at odd harmonics, the optimum impedances for Class-E with shunt capacitance and shunt filter differ from that of the Class-E with series filter and Class-E with quarterwave line where impedances are defined by the shunt capacitances because they are also provided by the parallel *LC* circuits.

The optimized load-network parameters of the different Class-E modes including Class-E with series filter, Class-E with quarterwave line, and Class-E with shunt filter are shown in Table 8.2 in a normalized form. As can be seen, Class-E with shunt filter offers the larger value of the shunt capacitance C for the same load R and much higher value of the maximum operating frequency $f_{\max}$ for the same DC supply voltage V_{cc}, device output capacitance C_{out}, and output power P_{out}, compared to Class-E with shunt capacitance and series filter. At the same time, difference between Class-E with quarterwave line and Class-E with shunt filter is not so significant because the quarterwave line being grounded at its end through bypass capacitor operates for even harmonics as a shunt filter.

8.4 ADS simulation setup

The Advanced Design System (ADS) simulation setup shown in Fig. 8.6 is used to obtain the nominal Class-E operation mode with infinite RF choke in a frequency domain, where the input source Vf_Pulse represents a voltage source with a Fourier series expansion of periodic rectangular wave with different pulse width characterized by a duty ratio used in a harmonic balance simulator.[6] Generally, using frequency domain enables the overall simulation procedure to be much faster than that in the time domain and can take a few seconds. However, because the number of harmonic components is not infinite, the simulation waveforms and numerical results for the optimum load-network parameters are not so accurate. The harmonic order is set to 100.

In this case, the optimization procedure can be applied with respect to efficiency as an optimization parameter. Since the simulation time is very short, a number of iterations can significantly be increased for more accuracy. Fig. 8.7 shows the normalized switch voltage and current waveforms obtained for the idealized optimum (or nominal) parameters of the Class-E load network with shunt capacitor and shunt filter given by Eqs. (8.26)–(8.28) with a 50% duty ratio.

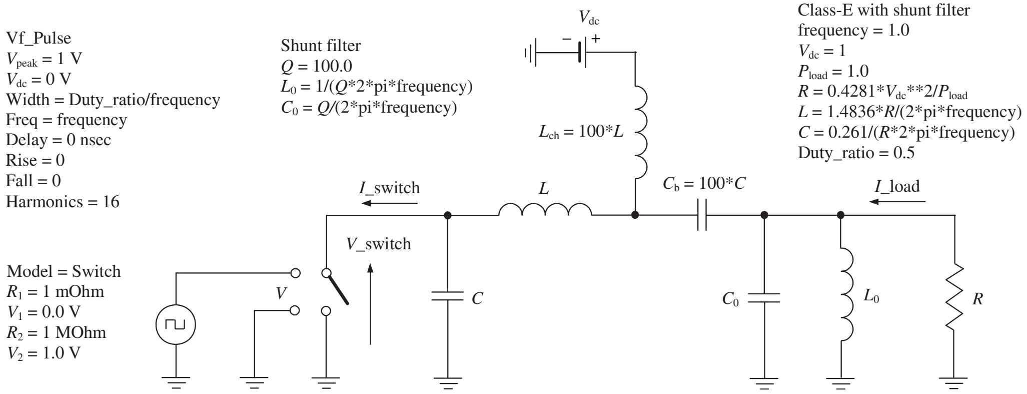

Vf_Pulse
V_{peak} = 1 V
V_{dc} = 0 V
Width = Duty_ratio/frequency
Freq = frequency
Delay = 0 nsec
Rise = 0
Fall = 0
Harmonics = 16
Shunt filter
Q = 100.0
L_0 = 1/(Q*2*pi*frequency)
C_0 = Q/(2*pi*frequency)
V_{dc}
−
+
L_{ch} = 100*L
Class-E with shunt filter
frequency = 1.0
V_{dc} = 1
P_{load} = 1.0
R = 0.4281*V_{dc}**2/P_{load}
L = 1.4836*R/(2*pi*frequency)
C = 0.261/(R*2*pi*frequency)
Duty_ratio = 0.5
I_switch
L
C_b = 100*C
I_load
V_switch
Model = Switch
R_1 = 1 mOhm
V_1 = 0.0 V
R_2 = 1 MOhm
V_2 = 1.0 V
V
C
C_0
L_0
R

FIG. 8.6

Simulation setup for idealized Class-E mode with series inductance and shunt filter in frequency domain.

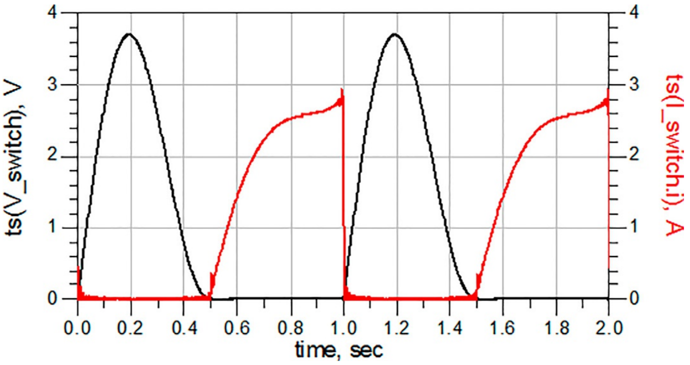


FIG. 8.7

Simulated switch voltage and current waveforms in frequency domain.

Unlike the simulations in a time domain, the frequency-domain simulations are characterized by smoother transitions between the positions when the switch is turned on and the switch is turned off and vice versa. Nevertheless, for $r_{sat} = 1\,\text{m}\Omega$ and lossless circuit elements except load resistance R, the efficiency is equal to 98.8%, and the simulated normalized switch voltage and current waveforms shown in Fig. 8.7 are similar to the same theoretical waveforms shown in Fig. 8.5.

8.5 Load network with transmission lines

The circuit schematics of a high-efficiency transmission-line Class-E power amplifier with shunt capacitor and shunt filter are shown in Fig. 8.8, where the optimum load resistance R is matched to the standard load impedance $R_L = 50\,\Omega$ at the fundamental frequency using a quarterwave transmission

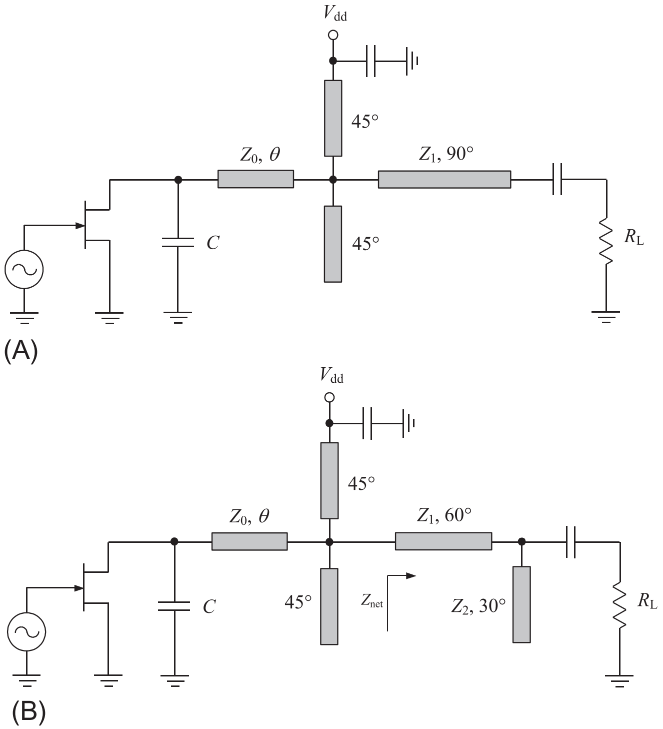


FIG. 8.8

Schematics of transmission-line Class-E power amplifier with shunt filter.

line, as shown in Fig. 8.8A, or using a transmission-line L-type impedance transformer, as shown in Fig. 8.8B.[6] Here, the shunt harmonic filter is composed of 45 degrees short- and open-circuit stubs to create short-circuit conditions at even harmonics. To create a short-circuit condition at the third harmonic at the right-hand side of the series inductor represented by a short-length series transmission line with the characteristic impedance Z_0 and electrical length θ, the series transmission line with electrical length of 60 degrees and an open-circuit stub with electrical length of 30 degrees are used.

For electrical length of a sufficiently short series transmission line with the characteristic impedance Z_0 and electrical length θ of less than 45 degrees, the required optimum value of θ for Class-E mode with shunt capacitance and shunt filter using Eq. (8.26) can be approximated by

$$\theta = \tan^{-1}\left(1.4836\frac{R}{Z_0}\right). \tag{8.33}$$

The output matching circuit is necessary to match to the required optimum Class-E resistance R calculated in accordance with Eq. (8.28) to the standard load resistance of 50 Ω. In addition, it is required to provide a short-circuit condition at the third-harmonic component. This can be easily done using the output matching topology in the form of an L-type transformer with the series transmission line and open-circuit stub. Its load-network impedance Z_{net} at the fundamental can be written as

$$Z_{\mathrm{net}} = Z_1 \frac{R_{\mathrm{L}}(Z_2 - Z_1 \tan 30° \tan 60°) + jZ_1 Z_2 \tan 60°}{Z_1 Z_2 + j(Z_1 \tan 30° + Z_2 \tan 60°)R_{\mathrm{L}}}, \tag{8.34}$$

where Z_1 and $\theta_1 = 60$ degrees are the characteristic impedance and electrical length of the series transmission line, and Z_2 and $\theta_2 = 30$ degrees are the characteristic impedance and electrical length of the open-circuit stub.

Hence the complex-conjugate matching with the load can be provided by a proper choice of the characteristic impedances Z_1 and Z_2. Separating Eq. (8.34) into real and imaginary parts and taking into account that $\mathrm{Re}Z_{\mathrm{net}} = R$ and $\mathrm{Im}Z_{\mathrm{net}} = 0$, the system of two equations with two unknown parameters can be written as

$$(Z_1 + 3Z_2)^2 R_{\mathrm{L}}^2 R - 3Z_1^2 Z_2^2 (4R_{\mathrm{L}} - 3R) = 0, \tag{8.35}$$

$$3Z_1^2 Z_2^2 + R_L^2 (Z_1 + 3Z_2)(Z_2 - Z_1) = 0, \tag{8.36}$$

which enables the characteristic impedances Z_1 and Z_2 to be properly calculated.

This system of two equations can be explicitly solved as a function of the parameter $r = R_{\mathrm{L}}/R$, resulting in

$$\frac{Z_1}{R_{\mathrm{L}}} = \frac{\sqrt{4r - 1}}{\sqrt{3}r}, \tag{8.37}$$

$$\frac{Z_1}{Z_2} = \frac{r - 1}{r}. \tag{8.38}$$

Consequently, for specified value of the parameter r with the required optimum load resistance R, corresponding to Class-E with shunt capacitance and shunt filter, and standard load $R_{\mathrm{L}} = 50\,\Omega$, first the characteristic impedance Z_1 is calculated from Eq. (8.37) and then the characteristic impedance Z_2 is calculated from Eq. (8.38). For example, if the required optimum load resistance is $R = 20\,\Omega$, resulting in $r = 2.5$, the characteristic impedance of the series transmission line is $Z_1 = 35\,\Omega$, and the characteristic impedance of the open-circuit stub is $Z_2 = 58\,\Omega$.

Fig. 8.9 shows the simulated circuit schematic, which approximates the transmission-line Class-E power amplifier with shunt filter, based on a 28-V 10-W Cree GaN high-electron-mobility transistor (HEMT) power transistor CGH40010F and transmission-line load network shown in Fig. 8.8B. The input matching circuit provides a complex-conjugate matching with the standard 50-Ω source. The load network was slightly modified by optimizing the parameters of the series and shunt transmission lines because the device output capacitance C_{out} and series inductance L_{out} formed by drain bondwires and package lead do not match the required exact values of C and L for a nominal Class-E with shunt filter.

For the transmission-line GaN HEMT Class-E power amplifier with shunt filter using a 30-mil RO4350 substrate, the simulated drain efficiency of 83%, a power-added efficiency (*PAE*) of 80.4%, and a power gain of 15 dB at an output power of 40.3 dBm with a quiescent current of 30 mA are achieved at an operating frequency of 2.14 GHz with a supply voltage of 28 V, as shown in Fig. 8.10. The second and third harmonics were suppressed by >50 dB.

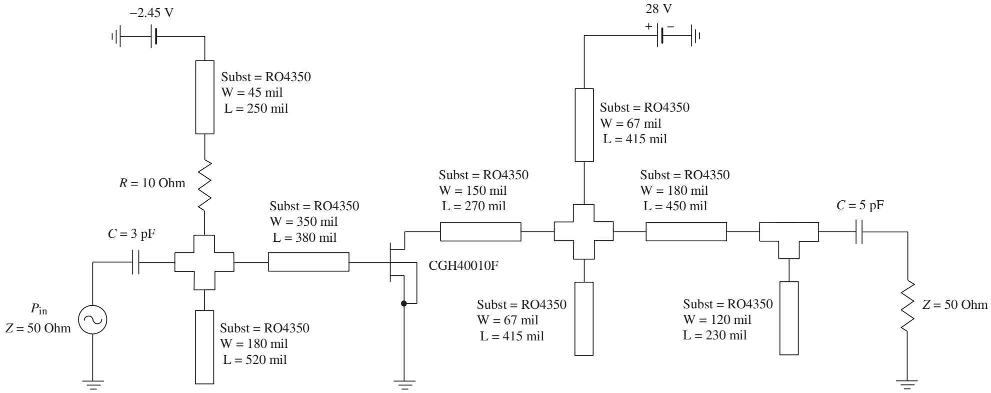

−2.45 V
Subst = RO4350
W = 45 mil
L = 250 mil
R = 10 Ohm
C = 3 pF
Subst = RO4350
W = 350 mil
L = 380 mil
Pin
Z = 50 Ohm
Subst = RO4350
W = 180 mil
L = 520 mil
CGH40010F
Subst = RO4350
W = 150 mil
L = 270 mil
28 V
Subst = RO4350
W = 67 mil
L = 415 mil
Subst = RO4350
W = 180 mil
L = 450 mil
C = 5 pF
Subst = RO4350
W = 67 mil
L = 415 mil
Subst = RO4350
W = 120 mil
L = 230 mil
Z = 50 Ohm

FIG. 8.9

Circuit schematic of transmission-line Class-E GaN HEMT power amplifier with shunt filter.

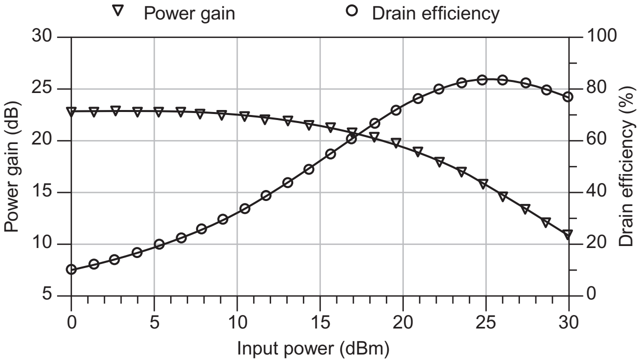


FIG. 8.10

Simulated results of transmission-line Class-E GaN HEMT power amplifier with shunt filter.

8.6 Class-E/F$_3$ with series tank circuit and shunt filter

To reduce the collector voltage peak factor, a series resonant circuit tuned to the third harmonic can be used in the Class-E load network with series filter, when the voltage peak factor reduces by 13.4% compared to a conventional Class-E mode.[8, 9] Alternatively, a parallel *LC* resonator tuned to the second harmonic can be added in series to the load network being connected directly to the drain. However, when a shunt filter tuned to the fundamental is used in the load network, the voltage waveform varies insignificantly, unlike the current waveform which can be shaped flat topped when q is approximately 1.5.[10] However, the voltage peak factor can be reduced with a flat-top voltage waveform when, for a sufficiently low optimum loaded Q_L-factor of the second-harmonic resonator, efficiency drops by almost 20% due to power dissipation at harmonics using the load network with a series filter with optimized parameters.[11] In this case, the proposed load network with shunt filter can be rearranged to

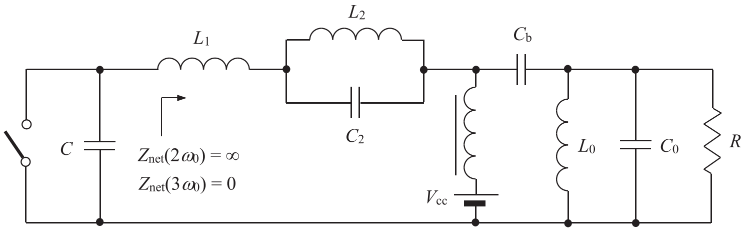


FIG. 8.11

Load network of Class-E/F$_3$ with series tank circuit and shunt filter.

correspond to Class-E/F$_3$ mode without power loss at harmonics by providing a short-circuit condition at the third harmonic when the L_2C_2 tank circuit connected in series is tuned to the second harmonic and provides a zero reactance at the third harmonic together with the series inductance L_1, as shown in Fig. 8.11.[6]

In this case, the network reactance ImZ_{net} at the fundamental frequency at the input of this lumped network can be written as

$$\text{Im}\, Z_{net}(\omega_0) = \omega_0 L_1 + \frac{\omega_0 L_2}{1 - \omega_0^2 L_2 C_2} = \omega_0 L, \tag{8.39}$$

where L_1 is the series inductance and the series L_2C_2 tank circuit is tuned to the second harmonic,

$$1 - 4\omega_0^2 L_2 C_2 = 0. \tag{8.40}$$

To provide a short-circuit condition at the third harmonic ($\omega = 3\omega_0$), Eq. (8.39) can be rewritten as

$$\text{Im}\, Z_{net}(3\omega_0) = 3\omega_0 L_1 + \frac{3\omega_0 L_2}{1 - 9\omega_0^2 L_2 C_2} = 0. \tag{8.41}$$

As a result, the ratios between the load-network parameters can be obtained by

$$L_1 = \frac{3}{8} L, \tag{8.42}$$

$$L_2 = \frac{15}{32} L, \tag{8.43}$$

$$C_2 = \frac{8}{15\omega_0^2 L}, \tag{8.44}$$

where L is an optimum inductance defined by Eq. (8.26).

The lumped Class-E/F$_3$ power amplifier with shunt filter based on a 28-V 10-W Cree GaN HEMT power transistor CGH40010F was simulated at an operating frequency of 100 MHz, according to the simulation setup shown in Fig. 8.12. In this case, the required optimum load resistance given by Eq. (8.28) is close to 30 Ω, therefore it is enough to use a simple low-pass L-type matching section to match to the standard load of 50 Ω. An entire shunt capacitance defined by Eq. (8.27) includes both external capacitance and device output capacitance. The values of the series inductance and third-harmonic tank circuit are obtained by Eqs. (8.42)–(8.44) using Eq. (8.26). The input matching is

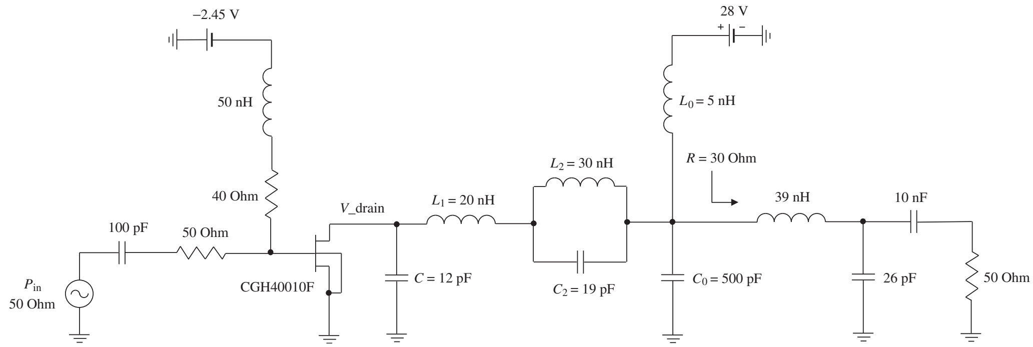


FIG. 8.12

Simulation setup for lumped GaN HEMT Class-E/F_3 power amplifier with shunt capacitance, second-harmonic tank, and shunt filter.

provided by a simple *RL* series circuit connected to the device input in parallel and followed by the series resistance.

As a result, for an infinite inductor quality factor in the load network, an output power of 40 dBm, a drain efficiency of 89.2%, and a *PAE* of 87% with a power gain of 16 dB were simulated for an input power of 24 dBm at a supply DC voltage of 28 V with a quiescent current of 30 mA, as shown in Fig. 8.13A. Because of the series second-harmonic tank and shunt filter, the second- and higher-order harmonic components are suppressed by greater than 50 dB, as shown in Fig. 8.13B. Fig. 8.13C shows the simulated drain waveform demonstrating the effect of an inverse Class-F_3 mode, resulting in a voltage peak factor of $80/28 = 2.86$, which is significantly less (by 1.29 times) than that for Class-E with shunt filter defined by Eq. (8.30).

8.7 Load network with shunt filter and series reactance

The Class-E load network with shunt filter shown in Fig. 8.3A can be modified by adding an additional capacitor in parallel to the shunt filter, as shown in Fig. 8.14A, where the shunt L_0C_0 filter is tuned to the fundamental frequency. This circuit represents the modified inverse Class-E configuration with a series-*L*/parallel-tuned load network to compensate for the parasitic device output capacitance C_{out} and simultaneously to provide zero-voltage and zero voltage-derivative switching conditions for particular case of $q = 1.29$.[12]

8.7.1 Variation of load-network parameters

However, similar to the generalized Class-E with finite DC-feed inductance and series filter, multiplicity of solutions for the load-network parameters can be achieved for Class-E with shunt capacitance and shunt filter if the parameter q is considered as a variable to introduce an additional reactance between the shunt filter and the load, which can generally can have inductive or capacitive reactance. Fig. 8.14B shows the basic circuit configuration of a Class-E power amplifier with shunt filter and series

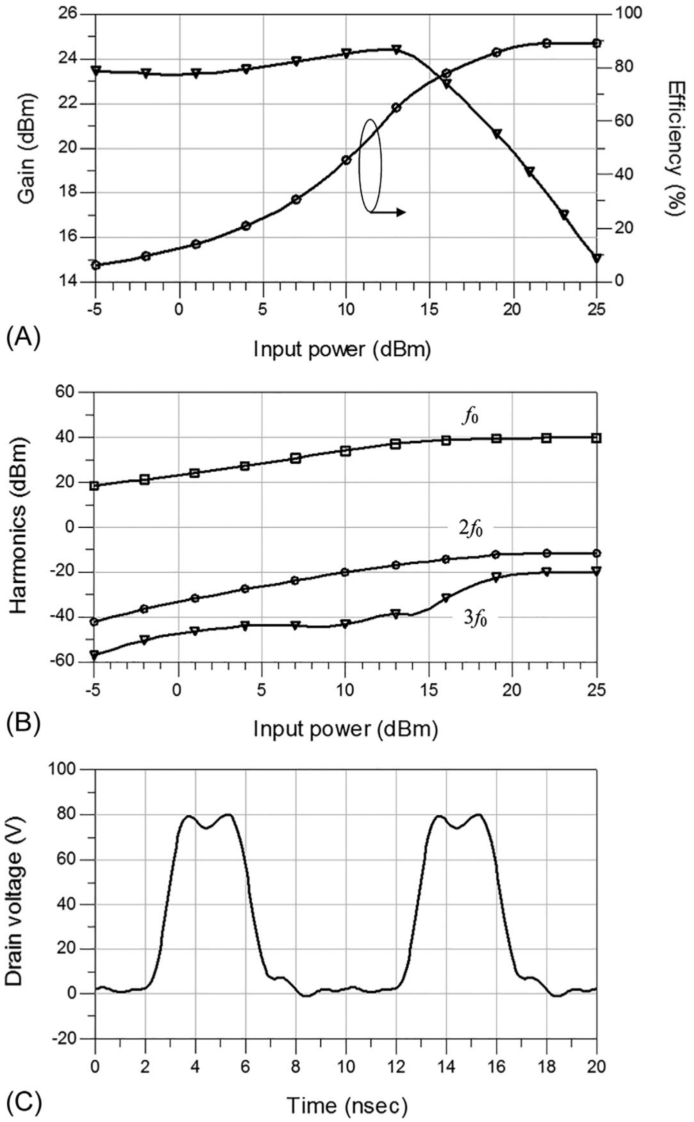


FIG. 8.13

Simulated results of lumped Class-E/F_3 GaN HEMT power amplifier.

reactance, where the load network consists of a shunt capacitor C, a series inductor L, a blocking capacitor C_b, a shunt fundamentally tuned L_0C_0 circuit, a series reactance X, and a load resistor R. In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network, a series inductance L can include the bondwire and lead inductance, and a series reactance X can be positive (inductance), zero, or negative (capacitance),

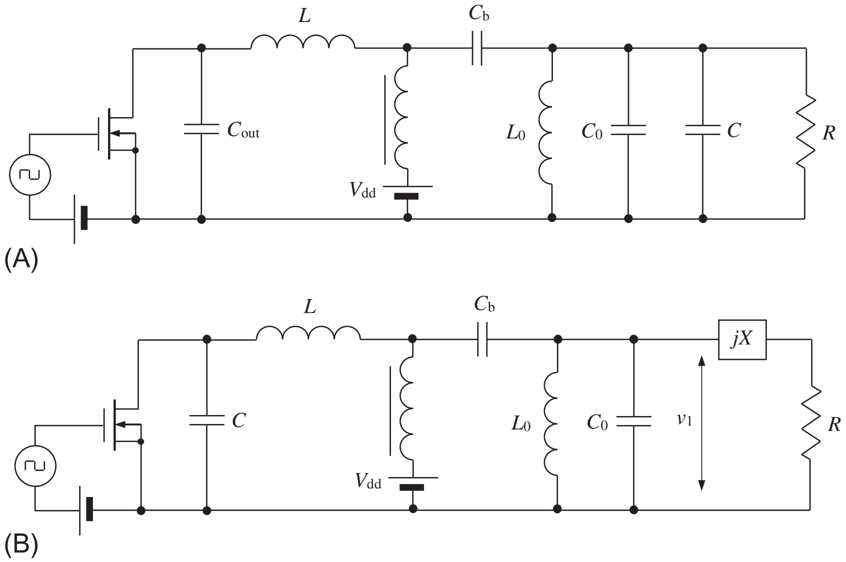


FIG. 8.14

(A) Circuit schematic of Class-E power amplifier with shunt filter and additional reactance and (B) generalized circuit schematic of Class-E power amplifier with shunt filter.

depending on the particular mode of the generalized Class-E load network with shunt filter and series reactance.

By providing similar circuit analysis, using the idealized optimum zero-voltage and zero voltage-switching switching conditions given by Eqs. (8.1) and (8.2) and assuming the sinusoidal voltage across the shunt L_0C_0 filter as $v_1(\omega t) = V_1 \sin(\omega t + \varphi_1)$, a general nonhomogeneous second-order differential equation for the switch voltage $v(\omega t)$ can be derived whose general solution can be given in the normalized form similar to Eq. (8.15) as

$$\frac{v(\omega t)}{V_{dd}} = C_1 \cos q\omega t + C_2 \sin q\omega t + 1 + \frac{q^2}{1-q^2}\frac{V_1}{V_{dd}} \cos(\omega t + \varphi_1), \tag{8.45}$$

where V_1 is the fundamental voltage amplitude across the shunt filter, φ_1 is the initial phase angle of a complex load, and C_1 and C_2 are the coefficients determined from the initial off-state conditions obtained from Eqs. (8.17) and (8.18), respectively, after replacing V_R and φ by V_1 and φ_1, respectively.[13]

In this case, for a given DC supply voltage V_{dd}, Eq. (8.45) generally contains three unknown parameters q, V_1/V_{dd}, and φ_1. However, since the parameter q is treated as a variable, the other two parameters V_1/V_{dd} and φ_1 are determined from a system of two equations resulting from applying the idealized optimum Class-E switching conditions given by Eqs. (8.1) and (8.2). Fig. 8.15A shows the dependences of parameters V_1/V_{dd} and φ_1 on q, from which it can be seen that for $q = 1.607$, $\varphi_1 = -41.6°$ and $V_1/V_{dd} = 0.9253$ that corresponds to the results given by Eqs. (8.20)–(8.22).

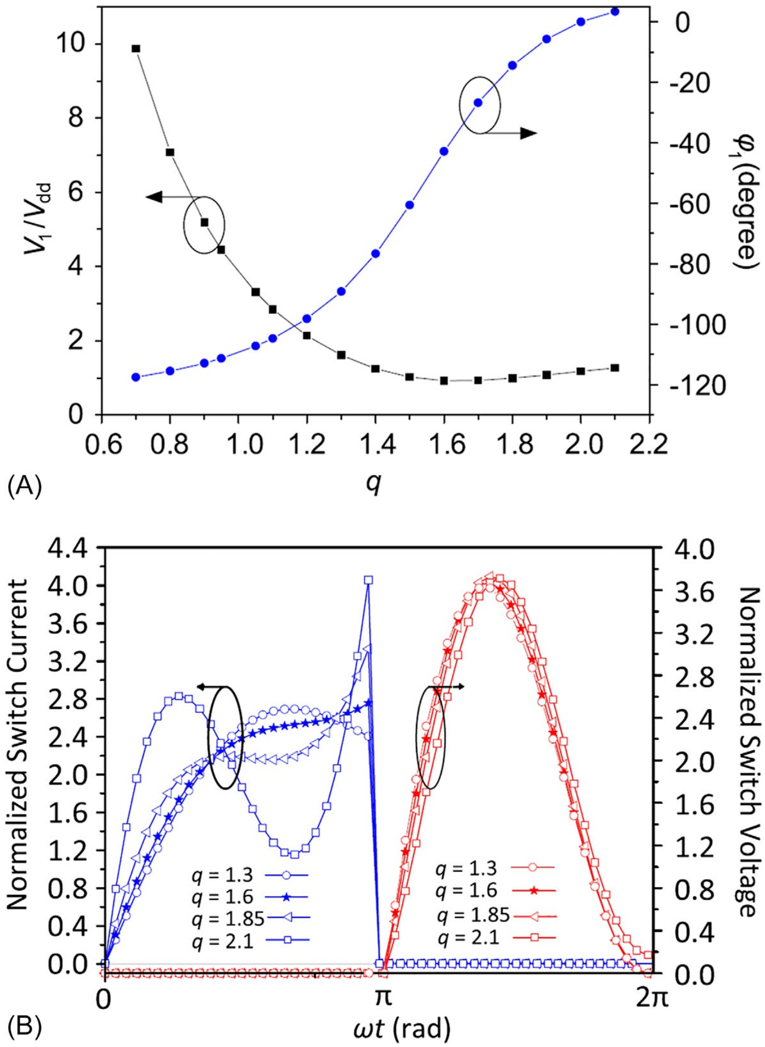


FIG. 8.15

Optimum Class-E parameters and normalized switch voltage and current waveforms.

The normalized switch voltage and current waveforms calculated for $q=1.3$, 1.6, 1.85, and 2.1 are shown in Fig. 8.15B, where the switch voltage waveforms satisfy the idealized optimum Class-E conditions for all q values. As q increases, the peak switch voltage varies insignificantly, whereas the current waveform changes its shape dramatically, creating a spike at the end of the turn-on interval for higher q, similar to that shown in Fig. 8.1B for $q=2$.

By using Eqs. (8.23) and (8.24) with V_1 and φ_1, the optimum series inductance L and shunt capacitance C can be written as

$$\omega L = \frac{V_{dd}^2}{2\pi P_{out}} \left[\frac{\pi^2}{2} - \frac{V_1}{V_{dd}} (2\sin\varphi_1 + \pi\cos\varphi_1) \right], \tag{8.46}$$

$$\omega C = \frac{1}{q^2 \omega L}. \tag{8.47}$$

The optimum load resistance R can be obtained from Eq. (8.23) for the DC supply voltage V_{dd} and fundamental-frequency output power P_{out} delivered to the load as

$$R = \frac{1}{2} \frac{V_R^2}{P_{out}} = \frac{1}{2} \left(\frac{V_R}{V_{dd}} \right)^2 \frac{V_{dd}^2}{P_{out}}, \tag{8.48}$$

where

$$\frac{V_R}{V_{dd}} = \frac{V_1}{V_{dd}} \Big/ \sqrt{1 + \left(\frac{X}{R} \right)^2}, \tag{8.49}$$

and V_R is the voltage amplitude across the load R. The optimum reactance X in Eq. (8.49) can be determined using Eq. (8.19) when $v_1(\omega t)$ can be rewritten as

$$v_1(\omega t) = V_R \sin(\omega t + \varphi) + V_X \cos(\omega t + \varphi), \tag{8.50}$$

where $\varphi = \varphi_1 - \tan^{-1}(X/R)$ is the initial phase.

The normalized optimum series inductance $\omega L P_{out}/V_{dd}^2$,series reactance $X P_{out}/V_{dd}^2$, shunt capacitance $\omega C V_{dd}^2/P_{out}$, and load resistance $R P_{out}/V_{dd}^2$ are plotted versus parameter q in Fig. 8.16.[13] From Fig. 8.16A, it follows that a larger value of ωL corresponds to a lower value of q. To compensate for such an increased inductive value, the reactance X must, therefore, be decreased. The series reactance X changes from negative (capacitive) to positive (inductive) values as q increases. Fig. 8.16B shows that, as q increases, the value of ωC increases and, consequently, for a specific value of C representing the device output capacitance ($C = C_{out}$), the maximum operating frequency f_{max} increases with the increasing q. Thus f_{max} of the generalized Class-E power amplifier with shunt capacitance and shunt filter can be written as

$$f_{max} = k \frac{P_{out}}{C_{out} V_{dd}^2}, \tag{8.51}$$

where k is plotted versus q in Fig. 8.16B.

The maximum operating frequency f_{max} can also defined in terms of the transistor output series inductance ($L = L_{out}$) according to

$$f_{max} = m \frac{V_{dd}^2}{L_{out} P_{out}}, \tag{8.52}$$

where $m = 1/k(2\pi q)^2$ is plotted versus q in Fig. 8.16B. From Eq. (8.52), it follows that f_{max} decreases with increasing q.

8.7.2 Load network with lumped parameters

Fig. 8.17A shows the simulated schematic of a Class-E power amplifier with series inductance L, shunt L_0C_0 filter, and series inductive reactance L_X based on a GaN HEMT CGH40010F device having an

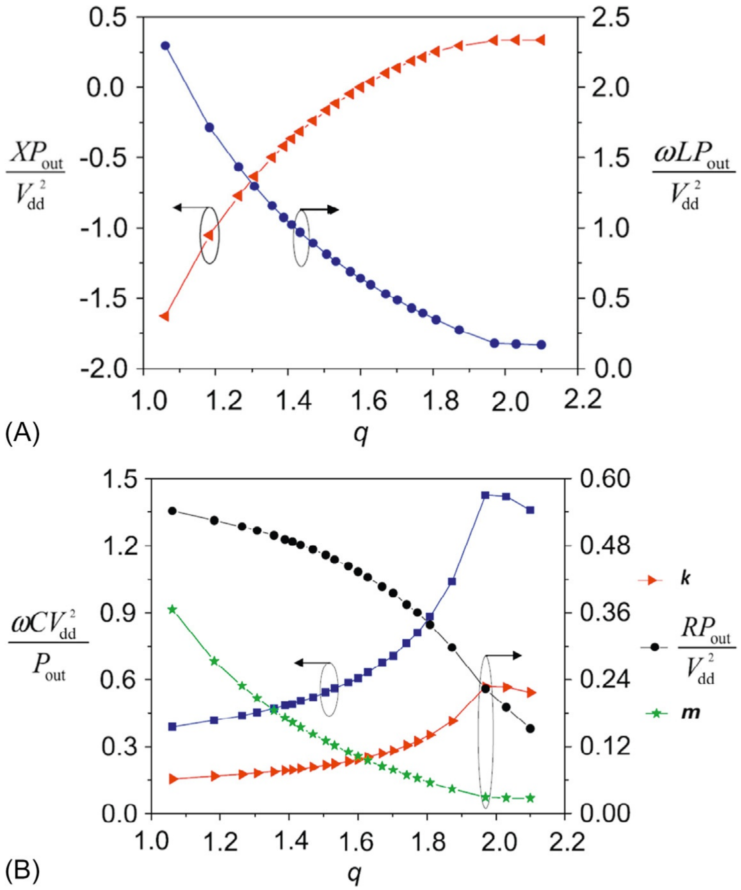


FIG. 8.16

Normalized optimum load-network parameters.

output capacitance $C_{out} = 1.3$ pF and an output inductance $L_{out} = 0.653$ nH, which is considered as a part of the series inductance L, and biased with $V_g = -2.7$ V and $V_{dd} = 28$ V when delivering an output power of 10 W at 1.5 GHz.[13] In this case, the value of $q = 1.85$ was chosen to obtain $C = 1.272$ according to Fig. 8.16B, which is close to $C_{out} = 1.3$ pF, which results in $k = 0.1496$, extending the f_{max} of the Class-E with shunt capacitance and series filter given by Eq. (5.35) in Chapter 5 by a factor of 2.95. The value of $L = 2.66$ nH is obtained from Fig. 8.16A for $q = 1.85$. For the given V_{dd} and P_{out}, the values of $X = 20.4\,\Omega$ and $R = 25.1\,\Omega$ are determined from Fig. 8.16A and B, respectively. As a result, a peak *PAE* of 84.3% and a peak output power of 39 dBm are achieved at 1.5 GHz. If designed at f_{max} corresponding to Eq. (5.35), which is equal to 497.4 MHz, the same $q = 1.85$ results in $C = 3.84$ pF when a peak *PAE* of 87.89% and a peak output power of 39.9 dBm are achieved, as shown in Fig. 8.17B. In this case, a larger size (higher power capability) transistor with a $C_{out} = 3.84$ pF can be used for this Class-E power amplifier design with shunt filter and series inductive reactance.

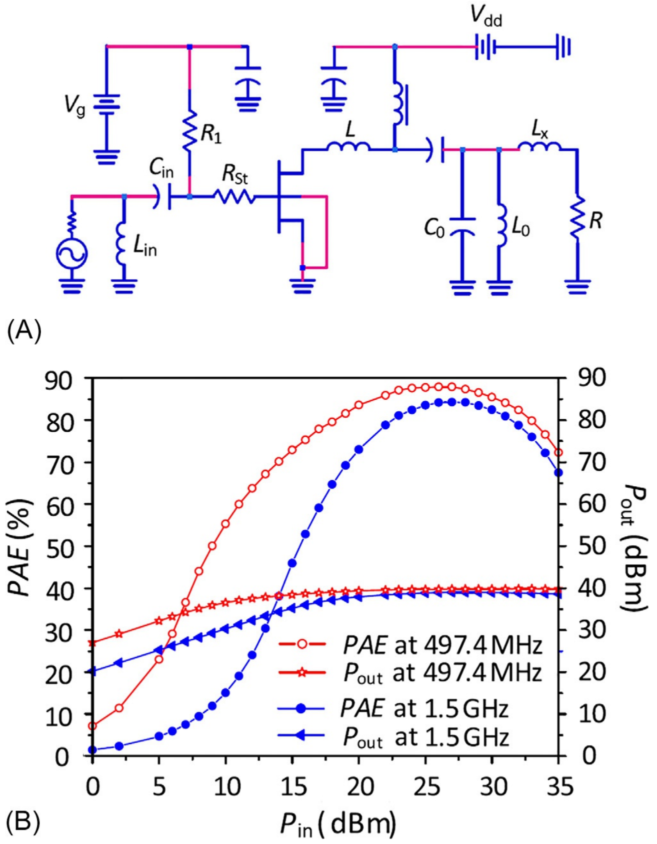


FIG. 8.17

Simulated (A) circuit schematic and (B) performance of Class-E power amplifier with shunt filter and series inductive reactance.

8.7.3 Load network with transmission lines

The circuit schematics of a load network with transmission lines is shown in Fig. 8.18, where the excess series inductance is realized using a series transmission line with a characteristic impedance of Z_1 and electrical length of θ_1. For electrical length of a sufficiently short series transmission line of less than 45 degrees, the required optimum value of θ_1 for Class-E mode with shunt filter and series reactance at an operating frequency ω_0 can be approximated by

$$\theta_1 = \tan^{-1}\left(\frac{\omega_0 L}{Z_1}\right), \tag{8.53}$$

when an optimum series inductance L is defined by Eq. (8.46). Here, a short-circuit stub together with an open-circuit stub, both having high characteristic impedance Z_2 and electrical length of 45 degrees, provide a short-circuit termination at even-harmonic frequencies and an open-circuit termination at

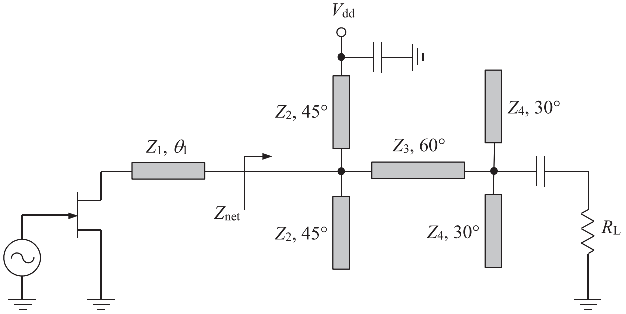


FIG. 8.18

Load network with transmission lines.

fundamental and odd-harmonic frequencies.[6, 14] A series transmission line with the characteristic impedance Z_3 and electrical length of 60 degrees in conjunction with two open-circuit stubs, both having the characteristic impedance Z_4 and electrical length of 30 degrees, provide a short-circuit termination at the third harmonic.

At the same time, the transmission-line characteristic impedances Z_3 and Z_4 are calculated to match the required Class-E load-network impedance $\mathrm{Re}Z_{net} = R + jX = (25.1 + j20.4)\ \Omega$ to the standard load R_L at the fundamental frequency. The load-network impedance Z_{net} at the fundamental can be written as

$$Z_{net} = Z_3 \frac{3Z_3Z_4 + j\sqrt{3}(2Z_3 - Z_4)R_L}{(2Z_3 + 3Z_4)R_L - j\sqrt{3}Z_3Z_4}, \tag{8.54}$$

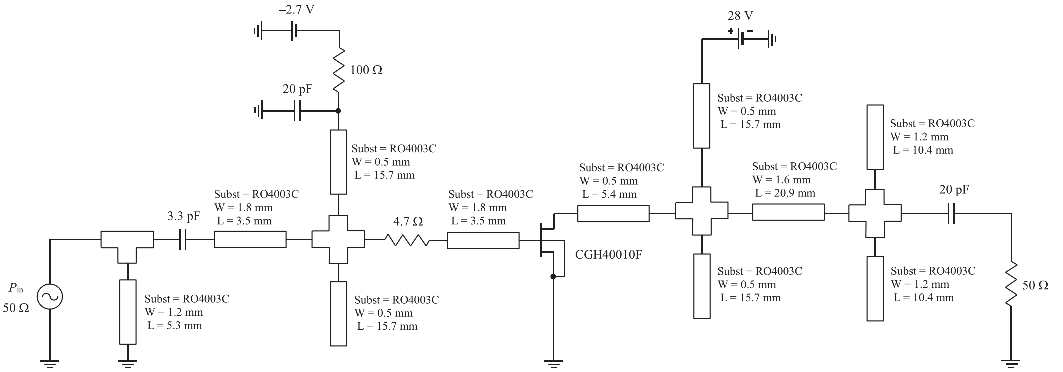
where R_L is the load resistance, usually equal to $50\,\Omega$. Separating the real and imaginary parts of Eq. (8.53) and considering that $\mathrm{Re}Z_{net} = R$ and $\mathrm{Im}Z_{net} = X$, the system of two equations with two unknown parameters can be written as

$$3Z_3^2Z_4^2(4R_L - R) - R_L^2R(2Z_3 + 3Z_4)^2 = 0, \tag{8.55}$$

$$3Z_3^2Z_4^2\left(\sqrt{3}Z_3 - X\right) + R_L^2(2Z_3 + 3Z_4)\left[\sqrt{3}Z_3(2Z_3 - Z_4) - X(2Z_3 + 3Z_4)\right] = 0, \tag{8.56}$$

from which the characteristic impedances Z_3 and Z_4 are obtained as 50 and $63.5\,\Omega$, respectively.

Fig. 8.19 shows the simulated circuit schematic, which approximates the transmission-line Class-E power amplifier with shunt filter and series inductive reactance, based on a 28-V 10-W Cree GaN HEMT power transistor CGH40010F and transmission-line load network shown in Fig. 8.18. The input matching circuit provides a complex-conjugate matching with the standard 50-Ω source, with a series resistor of $4.7\,\Omega$ to provide the operation stability. The simulated maximum drain efficiency of 89.2%, peak *PAE* of 83.7%, and maximum output power of 38.6 dBm with a small-signal gain of 22.9 dB are achieved at 1.5 GHz.



−2.7 V
100 Ω
20 pF
Subst = RO4003C W = 0.5 mm L = 15.7 mm
Subst = RO4003C W = 1.8 mm L = 3.5 mm
3.3 pF
4.7 Ω
Subst = RO4003C W = 1.8 mm L = 3.5 mm
Subst = RO4003C W = 0.5 mm L = 5.4 mm
CGH40010F
28 V
Subst = RO4003C W = 0.5 mm L = 15.7 mm
Subst = RO4003C W = 1.6 mm L = 20.9 mm
Subst = RO4003C W = 1.2 mm L = 10.4 mm
20 pF
P_{in}
50 Ω
Subst = RO4003C W = 1.2 mm L = 5.3 mm
Subst = RO4003C W = 0.5 mm L = 15.7 mm
Subst = RO4003C W = 0.5 mm L = 15.7 mm
Subst = RO4003C W = 1.2 mm L = 10.4 mm
50 Ω

FIG. 8.19

Simulated circuit schematic of transmission-line Class-E GaN HEMT power amplifier.

8.8 Implementation and test

To validate the theory and simulation results achieved for Class-E mode with shunt capacitance and series reactance, two power amplifier prototypes were fabricated: one based on lumped elements with an IRF630 metal-oxide-semiconductor field-effect transistor (MOSFET) to operate at 1 MHz and the other one based on microstrip lines with a GaN HEMT CGH40010F device to operate at 1.5 GHz.

8.8.1 High-frequency Class-E power amplifier with lumped parameters

Fig. 8.20A shows that the test board of a lumped MOSFET Class-E power amplifier with a load network whose parameters were extracted from Fig. 8.16 for two arbitrary values of q (1.364 and 1.831) results in a capacitive and inductive reactance X, respectively.[13] Here, the load is realized using four parallel connected 2-W resistors. For the specified DC-supply voltage $V_{dd}=24$ V and output power of 5 W, the values of the shunt capacitance $C=667.98$ pF, series inductance $L=20.42$ µH, series capacitance $C_X=2.99$ nF, and load resistor $R=55.99\,\Omega$ for $q=1.364$ and $C=1.182$ nF, $L=6.39$ µH, $L_X=4.488$ µH, and $R=39.158\,\Omega$ for $q=1.831$ were determined. The shunt filter was implemented for $Q_L=5$, resulting in $L_0=1.57$ µH and $C_0=16.14$ nF. The component values were slightly tuned to take into account the nonlinearity effect of the transistor output capacitance of 200 pF and parasitic resistances of the reactive components to satisfy the nominal Class-E switching conditions. Fig. 8.20B shows the measured drain and output voltage waveforms with zero-voltage and zero voltage-derivative conditions required for soft-switching and high-efficiency operation. As a result, an output power of 5 W with a drain efficiency of 93.3% for $q=1.364$ and an output power of 4.3 W with a drain efficiency of 88.6% for $q=1.831$ were achieved.

For $q=1.607$ when $X=0$ and the calculated load-network parameters are $C=100$ pF, $L=214.7$ nH, $L_0=28.9$ nH, $C_0=4760$ pF, and $R=12.3\,\Omega$, a drain efficiency of 92.5% with an output power of 3.33 W was measured at an operating frequency of 13.56 MHz with a DC-supply voltage of 12 V using an

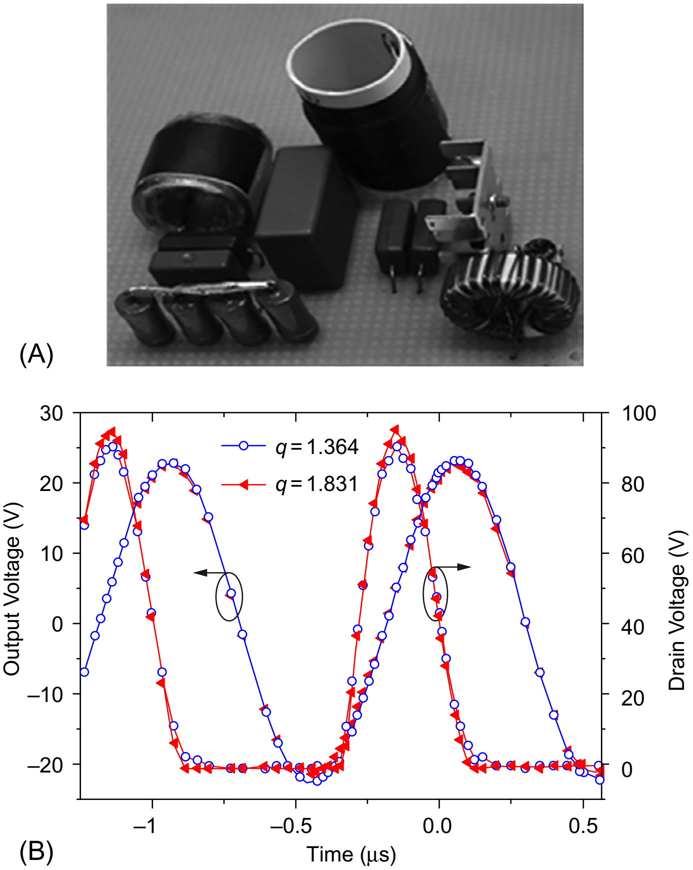


FIG. 8.20

Test prototype and measured drain and output voltage waveforms.

IRF520 MOSFET device.[15] Because of a sufficiently small value of the shunt filter inductance with a filter loaded quality factor of 5 and due to the inductance low-loss implementation using silver-coated wire, the level of the second-harmonic suppression of approximately 50 dB can be achieved.

8.8.2 Microwave transmission-line Class-E power amplifier

Fig. 8.21A shows the test board of the transmission-line Class-E power amplifier with shunt filter and series inductive reactance based on a GaN HEMT CGH40010F device using a 20-mil RO4003C substrate (dielectric constant of 3.55 and loss tangent of 0.0027), where the characteristic impedances and electrical lengths of all microstrip lines correspond to the simulation setup shown in Fig. 8.19.[13]

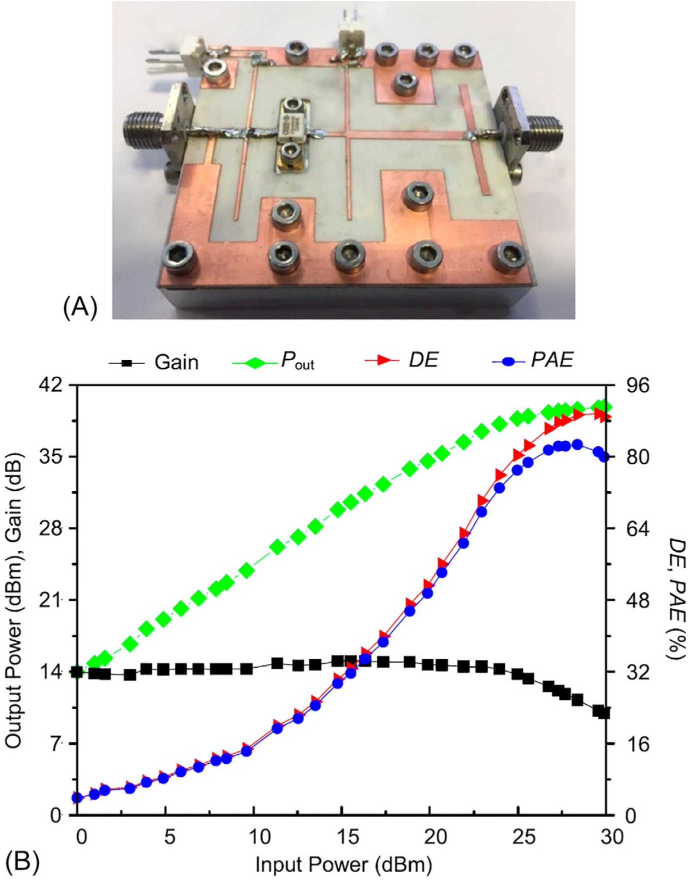


FIG. 8.21

Test prototype and measured performance of a GaN HEMT transmission line Class-E power amplifier.

The measured power amplifier performance shown in Fig. 8.21B demonstrates a peak drain efficiency of 90.2%, a peak *PAE* of 82.6%, a peak output power of 39.8 dBm, and a linear power gain of 14 dB at an operating frequency of 1.37 GHz, with a large-signal power gain of 11.5 dB at the peak *PAE*. At the same time, a drain efficiency and a *PAE* over 60% with an output power of 38.6 ± 1 dBm and a power gain approximately 10 dB are achieved across the 180-MHz frequency range. The power amplifier maintains its high-efficiency operation with a drain efficiency over 85% and a *PAE* over 60% when the drain DC-supply voltage varies from 14 to 32 V.

Fig. 8.22 shows the measured output power spectrum with the second- and third-harmonic suppression levels of −25 and −39.7 dBc, respectively, which shows the effectiveness of such a transmission-line load network with one $\lambda/8$ open-circuit stub and two parallel $\lambda/12$ open-circuit stubs separated by a series $\lambda/16$ microstrip line.

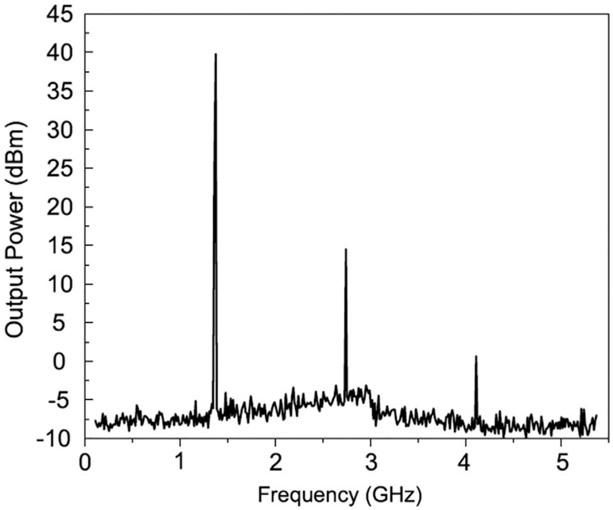


FIG. 8.22

Measured output power spectrum.

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CHAPTER

Broadband Class-E

9

In this chapter, the reactance-compensation technique applied to the circuits with lumped elements and transmission lines to provide a broadband operation of Class-E power amplifiers is introduced and analyzed. This technique can be directly used to design a parallel-circuit Class-E power amplifier because its load-network configuration represents exactly the same structure with shunt and series resonant circuits. Similarly, reactance-compensation technique can be also applied to Class-E power amplifiers with series and shunt filters. Different circuit configurations and Class-E load-network techniques corresponding to broadband high-power RF power amplifiers operating in VHF and UHF bands, microwave monolithic integrated circuits of power amplifiers, and CMOS power amplifiers operating in a wide frequency range with high efficiency are described.

9.1 Reactance-compensation technique

The conventional design of a high-efficiency switchmode Class-E power amplifier requires a high Q_L-factor to satisfy the necessary harmonic impedance conditions at the device output terminal. However, if a sufficiently small value of the loaded quality factor Q_L is chosen, a high-efficiency broadband operation of the Class-E power amplifier can be realized. For example, a simple network consisting of a series resonant *LC* circuit tuned to the fundamental frequency and a parallel inductor provides a constant load phase angle of 50 degrees in a frequency range of about 50%.[1] From theoretical considerations it was found in the mid-1960s that the bandwidth response of a parametric amplifier can be improved using multiple-resonant bandpass filters for the signal and idling circuits rather than simple resonant circuits.[2, 3] At the same time, it was analytically calculated that the added resonant circuits should have an appropriate Q_L-factor to optimally reduce the rate of change of reactance of both the signal and idling circuits.[4] Adding additional resonators can increase the potential amplifier bandwidth even further, but the amount of improvement per additional resonator will decrease rapidly as the number of resonators is increased. Such a reactance-compensation technique using a single-resonant circuit had also been applied to the varactor-tuned Gunn oscillator.[5, 6] Moreover, it became possible to increase the tuning range of an oscillator by adding more stages of reactance compensation. For instance, for a resonant circuit having a 50-Ω load, an improvement of 4% in the tuning range can theoretically be achieved as a result of applying a double-resonant circuit reactance compensation, whereas an increase in the tuning range can reach 17% for a resonant circuit operating into 100-Ω load.[7]

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9.1.1 Load networks with lumped elements

To describe the reactance- or susceptance-compensation circuit technique, let us consider the simplified equivalent load networks, one with a shunt resonant L_pC_p circuit followed by a series resonant L_sC_s circuit shown in Fig. 9.1A and the other with a series resonant L_sC_s circuit followed by a shunt resonant L_pC_p circuit shown in Fig. 9.1B. In this case, all resonant circuits are tuned to the fundamental frequency and R is the load resistance. The reactances of the series and shunt resonant circuits vary with frequency, increasing in the case of a series resonant circuit and decreasing in the case of a loaded parallel resonant circuit near the resonant frequency. As a result, near the resonant frequency of the series circuit with positive slope of its reactance, the slope of a shunt circuit reactance is negative. That reduces the overall reactance slope of the load network. By correct choice of the components in the shunt circuit, the rate of change of reactance with frequency can be made exactly opposite to that of the series circuit, thus producing a zero total variation over a wide frequency bandwidth.

Consider the load-network admittance Y_{net} corresponding to a single-susceptance-compensation circuit shown in Fig. 9.1A, which can be written as

$$Y_{\text{net}}(\omega) = \left(j\omega C_p + \frac{1}{j\omega L_p} + \frac{1}{R + j\omega' L_s} \right), \tag{9.1}$$

where

$$\omega' = \omega \left(1 - \frac{\omega_0^2}{\omega^2} \right), \tag{9.2}$$

and $\omega_0 = 1/\sqrt{L_sC_s} = 1/\sqrt{L_pC_p}$ is the angular resonant frequency.

At the resonant frequency when $\omega' = 0$ (or $\omega = \omega_0$), the load-network admittance $Y_{\text{net}}(\omega)$ reduces to

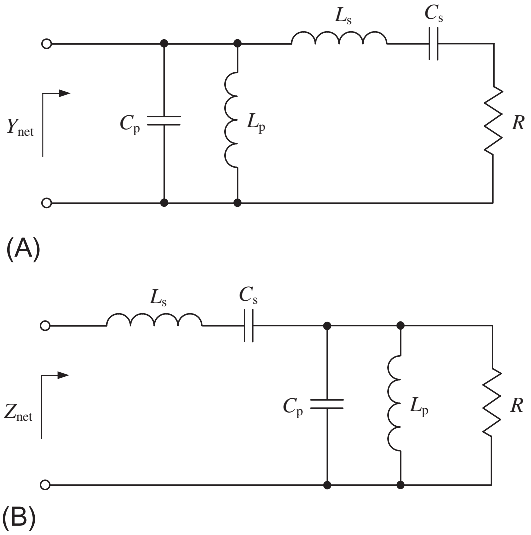


FIG. 9.1

(A) Single-susceptance- and (B) single-reactance-compensation circuits.

$$Y_{\text{net}}(\omega_0) = \left(j\omega_0 C_{\text{p}} + \frac{1}{j\omega_0 L_{\text{p}}} + G \right), \tag{9.3}$$

where $G = 1/R$ is the load conductance.

The frequency bandwidth with zero susceptance will be maximized if, at a resonant frequency ω_0,

$$\left.\frac{dB_{\text{net}}(\omega)}{d\omega}\right|_{\omega=\omega_0} = 0, \tag{9.4}$$

where

$$B_{\text{net}}(\omega) = \text{Im}Y_{\text{net}}(\omega) = \omega C_{\text{p}} - \frac{1}{\omega L_{\text{p}}} - \frac{\omega' L_{\text{s}}}{R^2 + (\omega' L_{\text{s}})^2}, \tag{9.5}$$

is the load-network susceptance.

As a result, an additional equation can be written as

$$C_{\text{p}} + \frac{1}{\omega_0^2 L_{\text{p}}} - \frac{2L_{\text{s}}}{R^2} = 0, \tag{9.6}$$

based on which the values of the series components L_{s} and C_{s} can, respectively, be obtained through the values of the shunt components L_{p} and C_{p} by

$$L_{\text{s}} = C_{\text{p}} R^2, \tag{9.7}$$

$$C_{\text{s}} = \frac{L_{\text{p}}}{R^2}. \tag{9.8}$$

In a similar manner, it may be shown that, for the load network with a series resonant $L_{\text{s}}C_{\text{s}}$ circuit followed by a shunt resonant $L_{\text{p}}C_{\text{p}}$ circuit shown in Fig. 9.1B, maximum bandwidth with zero reactance can be achieved if

$$\left.\frac{dX_{\text{net}}(\omega)}{d\omega}\right|_{\omega=\omega_0} = 0, \tag{9.9}$$

where

$$X_{\text{net}}(\omega) = \text{Im}Z_{\text{net}}(\omega) = \omega L_{\text{s}} - \frac{1}{\omega C_{\text{s}}} - \frac{\omega' C_{\text{p}}}{G^2 + \left(\omega' C_{\text{p}}\right)^2}, \tag{9.10}$$

is the load-network reactance, resulting in Eqs. (9.7) and (9.8). From Eq. (9.7), it follows that the loaded quality factor of the shunt circuit is equal to the loaded quality factor of the series compensating circuit, i.e., $Q_{\text{L}} = \omega C_{\text{p}} R = \omega L_{\text{s}}/R$.

Fig. 9.2A shows an example of a susceptance-compensation load network, whose conductance $\text{Re}Y_{\text{net}}$ is almost constant across the frequency range of 40% (from 4 to 6 MHz), as shown in Fig. 9.2B. The susceptance $\text{Im}Y_{\text{net}}$ of a shunt circuit varies with frequency, as shown in Fig. 9.2C by curve 1, with the gradient at ω_0 being equal to $2C_{\text{p}}$. The addition of a series circuit with the same resonant frequency of 5 MHz between the shunt circuit and the load gives an additional susceptance term with a negative slope, as shown in Fig. 9.2C by curve 2. The proper selection of the parameters of the series circuit enables the magnitude of the two slopes to be made identical, so that the total

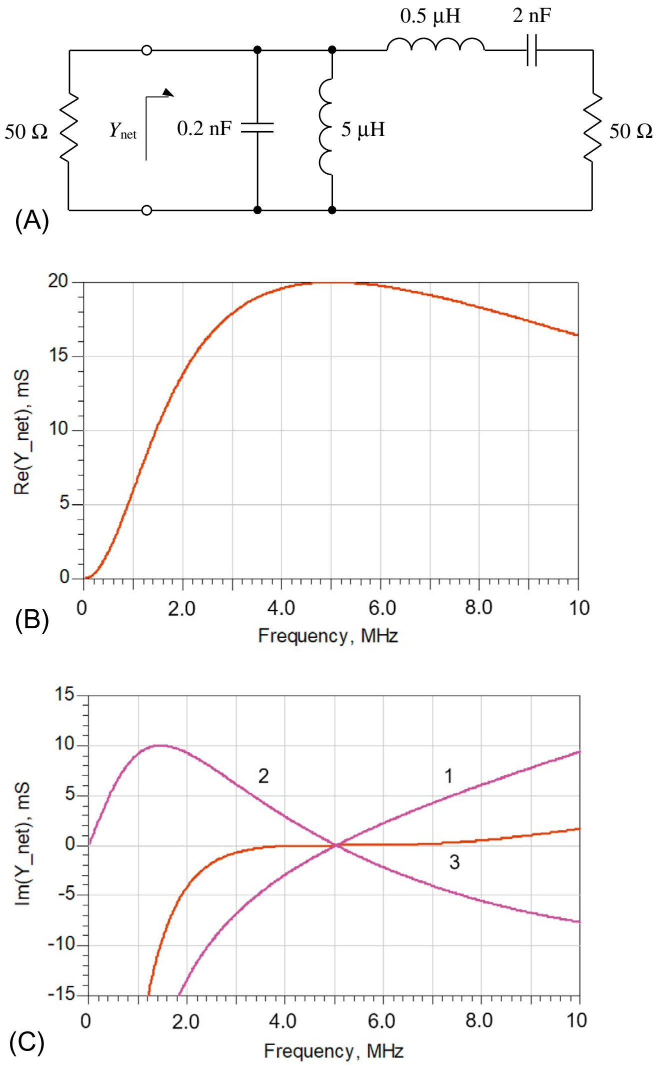


FIG. 9.2

Single-susceptance-compensation circuit and admittances.

susceptance slope around the resonance is zero in an octave frequency range from 3.5 to 7 MHz, as shown in Fig. 9.2C by curve 3.

The load network which provides reactance compensation is shown in Fig. 9.3A, where the shunt resonant circuit is connected between the series resonant circuit and the load. In this case, the resistance and reactance curves, the frequency behavior of which is similar to that for the conductance and susceptance curves characterizing the behavior of a susceptance-compensation load network, are shown in

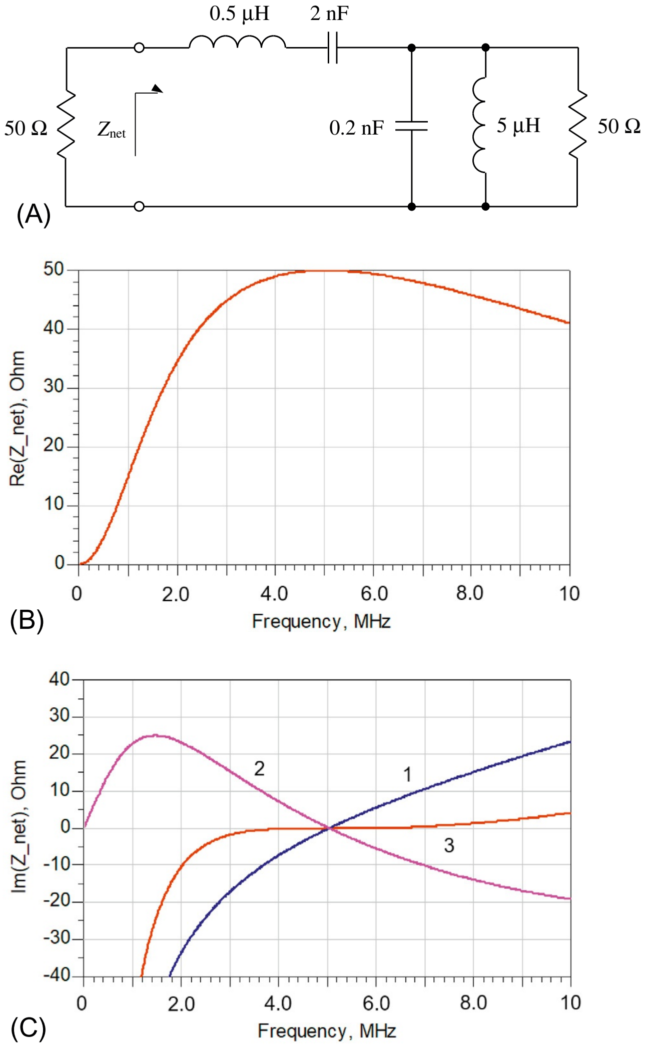


FIG. 9.3

Single-reactance-compensation circuit and impedances.

Fig. 9.3B and C, respectively. Here, the reactance of a series resonant circuit with a positive slope is shown by curve 1; the reactance of a shunt resonant circuit with a negative slope is shown by curve 2; and the total reactance slope shown by curve 3 is zero from 3.5 to 7 MHz.

Wider frequency bandwidth can be achieved using a double-susceptance-compensation circuit shown in Fig. 9.4A, where L_sC_s and L_1C_1 are the series and parallel compensating circuits, respectively. In this case, a system of two additional equations to maximize the frequency bandwidth can be used, where the first and the third derivatives are set to zero according to

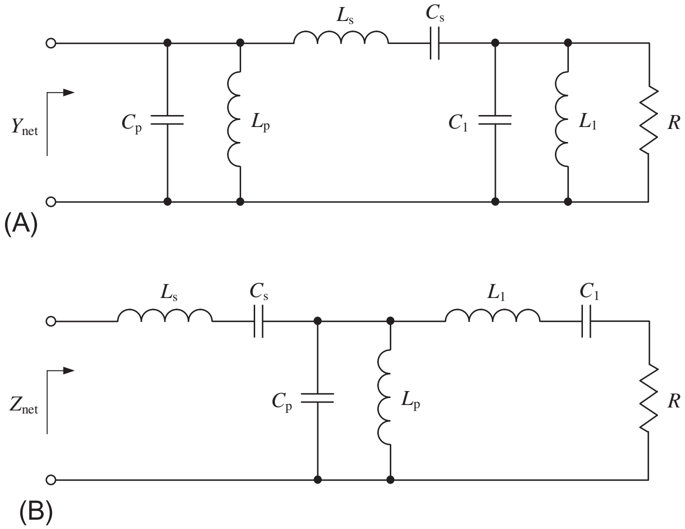


FIG. 9.4

Double-reactance-compensation circuits.

$$\left.\frac{dB_{\text{net}}(\omega)}{d\omega}\right|_{\omega=\omega_0}=\left.\frac{d^3B_{\text{net}}(\omega)}{d\omega^3}\right|_{\omega=\omega_0}=0, \tag{9.11}$$

as the second derivative cannot provide an appropriate analytical expression.

To determine the load-network parameters for a double-susceptance-compensation circuit with the load-network susceptance,

$$B_{\text{net}}(\omega)=\omega C_{\text{p}}-\frac{1}{\omega L_{\text{p}}}+\omega'\frac{C_1R^2\left[1-(\omega')^2L_{\text{s}}C_1\right]-L_{\text{s}}}{R^2\left[1-(\omega')^2L_{\text{s}}C_1\right]^2+(\omega'L_{\text{s}})^2}, \tag{9.12}$$

where $B_{\text{net}}=\text{Im}Y_{\text{net}}$, it is necessary to solve simultaneously the two following equations at the resonant frequency ω_0:

$$C_{\text{p1}}+\frac{1}{\omega_0^2L_{\text{p}}}-2\frac{C_1R^2-L_{\text{s}}}{R^2}=0, \tag{9.13}$$

$$\frac{1}{\omega_0^2L_{\text{p}}}+\frac{C_1R^2-L_{\text{s}}}{R^2}-8\omega_0^2L_{\text{s}}\left[C_1^2+\frac{(C_1R^2-L_{\text{s}})(L_{\text{s}}-2C_1R^2)}{R^4}\right]=0. \tag{9.14}$$

As a result, the parameters of the series and shunt compensating resonant circuits with the corresponding loaded quality factors $Q_{\text{s}}=\omega_0L_{\text{s}}/R$ and $Q_1=\omega_0C_1R$, which are close to unity and greater, can be calculated as a starting point for circuit optimization from

$$L_{\text{s}}=\frac{R}{\omega_0}\frac{2}{\sqrt{5}-1}\qquad C_{\text{s}}=\frac{1}{\omega_0^2L_{\text{s}}}, \tag{9.15}$$

$$C_1 = \frac{L_s}{R^2}\frac{3-\sqrt{5}}{2} \qquad L_1 = \frac{1}{\omega_0^2 C_1}. \tag{9.16}$$

Similarly, the elements for the double-reactance-compensation load network shown in Fig. 9.4B can be calculated from

$$L_1 = L_s\frac{\sqrt{5}-1}{2} \qquad C_1 = C_s\frac{2}{\sqrt{5}-1}, \tag{9.17}$$

$$L_p = C_s\frac{2R^2}{\sqrt{5}+1} \qquad C_p = L_s\frac{\sqrt{5}+1}{2R^2}, \tag{9.18}$$

where an inductance L_s and a capacitance C_s are known.[7] An example of the load network which provides double-reactance compensation is shown in Fig. 9.5A, whose resistance $\text{Re}Z_{\text{net}}$, shown in Fig. 9.5B by curve 1, provides less deviation from 50 Ω in a slightly wider frequency bandwidth compared to the single-resonance load network (curve 2) with $L_s = 0.5\,\mu\text{H}$, $C_s = 2$ nH, $L_p = 5\,\mu\text{H}$, and $C_p = 0.2\,\text{nF}$. The reactance $\text{Im}Z_{\text{net}}$ of a double-reactance-compensation circuit shown in Fig. 9.5C by curve 1 is close to zero near resonance across the frequency range from 3 to 8 MHz, which is wider than that for a single-resonance compensation circuit (curve 2).

9.1.2 Load networks with transmission lines

The reactance-compensation circuit technique can also be used for bandwidth improvement of microwave transistor amplifiers because the input and output transistor impedances generally can be represented by series or shunt *RLC* circuits. For compensating the reactive part and transforming the real part of the equivalent output transistor impedance to the conventional load impedance at the fundamental frequency, the quarter- and half-wavelength transmission lines can be used. For the first time, a quarter-wavelength transmission-line transformer was used for active reactance compensation when, by connecting two identical active devices together with a quarter-wavelength transformer, the inverted impedance of one device compensates the impedance of the other by reducing the total circuit reactance.[8]

Let us consider the characteristics of the transmission line as an element of a susceptance-compensation circuit shown in Fig. 9.6. For a parallel equivalent circuit, which represents the device output, the load-network input susceptance $B_{\text{net}} = \text{Im}Y_{\text{net}}$ can be defined as

$$B_{\text{net}}(\omega) = \omega L_p C_p\left(1 - \frac{\omega_0^2}{\omega^2}\right) + \frac{\tan\theta}{Z_0}\frac{R_L^2 - Z_0^2}{R_L^2 + Z_0^2\tan^2\theta}, \tag{9.19}$$

where

$$\theta = \frac{\pi f}{2f_0}k, \tag{9.20}$$

is the transmission-line electrical length, Z_0 is the transmission-line characteristic impedance, $f_0 = \omega_0/2\pi$ is the transmission-line resonant frequency, $k = 1, 2, \ldots, \infty$.

Applying the zero susceptance-derivative condition given by Eqs. (9.4)–(9.19) allows us to obtain the susceptance-compensation circuit parameters for different electrical lengths of a transmission line according to

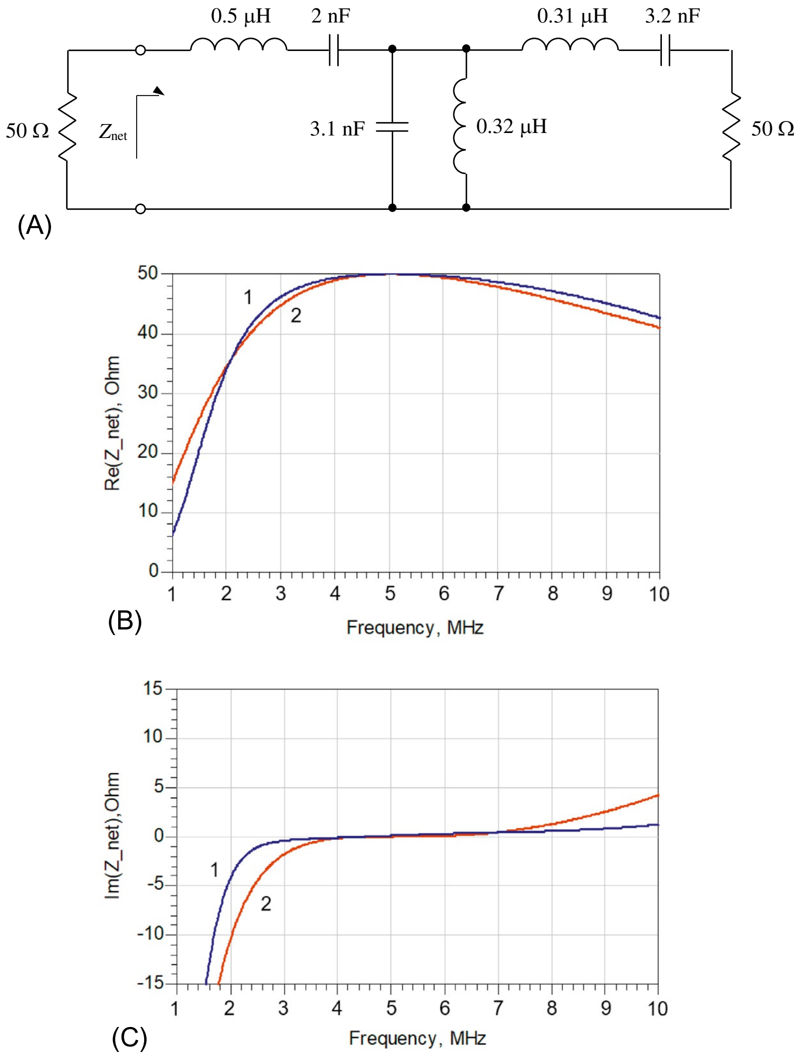


FIG. 9.5

Double-reactance-compensation circuit and impedances.

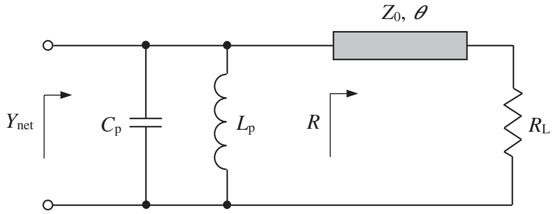

Z_0, θ
Y_{net}
C_p
L_p
R
R_L

FIG. 9.6

Transmission-line susceptance-compensation circuit.

$$2C_{\mathrm{p}}+\frac{\pi}{2Z_0\omega_0}\frac{R_{\mathrm{L}}^2-Z_0^2}{\cos^2\theta}\frac{R_{\mathrm{L}}^2-Z_0^2\tan^2\theta}{\left(R_{\mathrm{L}}^2+Z_0^2\tan^2\theta\right)^2}=0. \tag{9.21}$$

For a quarter-wavelength transmission line when $k=1$ and $\theta=\pi/2$, the susceptance compensation will be performed under the condition $Z_0<R_{\mathrm{L}}$ with the characteristic impedance Z_0 defined from a quadratic equation

$$Z_0^2+4\frac{QR_{\mathrm{L}}}{\pi}Z_0-R_{\mathrm{L}}^2=0, \tag{9.22}$$

where $Q=\omega_0C_{\mathrm{p}}R$ and $R=Z_0^2/R_{\mathrm{L}}$.

As a result, the required value of the characteristic impedance Z_0 is obtained by

$$Z_0=R_{\mathrm{L}}\left(-\frac{2Q}{\pi}+\sqrt{\left(\frac{2Q}{\pi}\right)^2+1}\right) \tag{9.23}$$

or

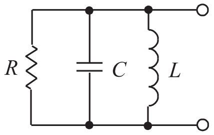
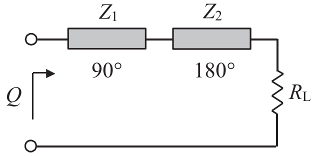
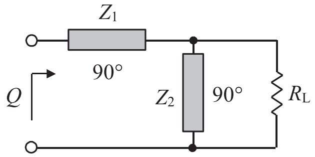
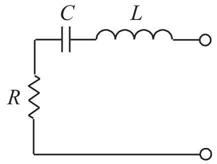
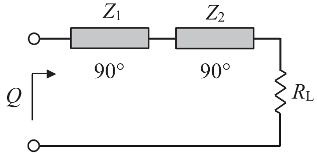
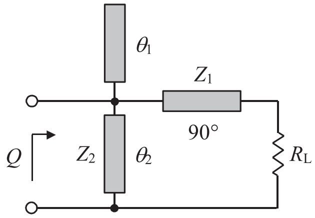
$$Z_0=R\bigg/\left(-\frac{2Q}{\pi}+\sqrt{\left(\frac{2Q}{\pi}\right)^2+1}\right). \tag{9.24}$$

Using the quarter- and half-wavelength transformers, the reactance- or susceptance-compensation load network generally can be realized differently for shunt and series equivalent output transistor circuits, as shown in Table 9.1 along with respective design equations.[9, 10] The two most important device parameters in the equations are the loaded quality factor Q and the real part R of the equivalent device output impedance or admittance. Depending on the values of the transmission-line characteristic impedances Z_1 and Z_2, each circuit provides either positive or negative parallel-resonant slope-reactance compensation.

Fig. 9.7A shows an example of a single-susceptance-compensation load network with a series quarter-wave transmission line having a characteristic impedance of 61.2 Ω to match a 50-Ω real part of the device equivalent output admittance to a 75-Ω load and an electrical length of 90 degrees at 50 MHz. The combination of the resistances of a shunt *LC* circuit (curve 1) and a series quarter-wave transmission line (curve 2) provides minimum variations of the total resistance $\mathrm{Re}Z_{\mathrm{net}}$ around 50 Ω in a very wide frequency range, as shown in Fig. 9.7B by curve 3. The susceptance $\mathrm{Im}Y_{\mathrm{net}}$ of a shunt circuit having a resonant frequency of 50 MHz varies with frequency with a positive slope, as shown in Fig. 9.7C by curve 1. The addition of a series quarter-wavelength transmission-line transformer between the shunt circuit and the load results in a negative slope, providing an additional susceptance, as shown in Fig. 9.7C by curve 2. Selection of the proper characteristic impedance of the series quarter-wave transmission line and the load resistance enables the magnitude of two slopes to be made identical, so that the total susceptance slope around resonance is zero in a frequency range from 45 to 65 MHz, as shown in Fig. 9.7C by curve 3.

From Eq. (9.23), it follows that the maximum value of the characteristic impedance Z_0 is limited by the load resistance R_{L}, and its value in some cases, especially for high value of Q, can be substantially smaller than 50 Ω, which causes a problem in the practical implementation of a transmission line. In this case, it is best to apply a single-frequency equivalence technique when a quarter-wave transmission line can be replaced by a symmetrical Π-type low-pass transmission-line section with two equal shunt capacitances at a frequency ω_0, as shown in Fig. 9.8.

Table 9.1 Transmission-line reactance compensation circuits and design equations.

Output circuit type	Matching network	Design equation
$Q = \omega_0 RC$ 		$Z_1 = \sqrt{RR_L}$ $T = \left(-\frac{2Q}{\pi} - \frac{1}{2}\right)\left(\frac{R_L}{Z_1} - \frac{Z_1}{R_L}\right)$ $Z_2 = -\frac{TR_L}{2} + \sqrt{\left(\frac{TR_L}{2}\right)^2 + R_L^2}$
		$Z_1 = \sqrt{RR_L}$ $Z_2 = \frac{\pi Z_1 R_L^2}{\pi Z_1^2 - \pi R_L^2 - 4QZ_1 R_L}$
$Q = 1/\omega_0 RC$ 		$Z_1 = AZ_2$ $Z_2 = BR_L$ $A = \sqrt{R/R_L}$ $B = \frac{A}{1+A}\left[-\frac{2Q}{\pi} + \sqrt{\left(\frac{2Q}{\pi}\right)^2 + \frac{(1+A)^2}{A}}\right]$
		$Z_2 = \sqrt{RR_L}$ $Z_1 = \left(\frac{TZ_2}{R_L}\right)^2 \frac{1}{\left(\frac{R_L}{Z_2} - \frac{Z_2}{R_L}\right) + \frac{4Q}{\pi}}$ $T = \frac{2}{\pi\cos\theta_2}(\theta_1 + \theta_2)$ $\theta_1 + \theta_2 = \frac{n\pi}{2} \to n = 1 \text{ or } 3$

The *ABCD*-matrix for a quarter-wave transmission line can be written as

$$ABCD_{90^\circ} = \begin{bmatrix} \cos 90^\circ & jZ_0 \sin 90^\circ \\ j\dfrac{\sin 90^\circ}{Z_0} & \cos 90^\circ \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ j\dfrac{1}{Z_0} & 0 \end{bmatrix}, \tag{9.25}$$

whereas, for a Π-type low-pass transmission-line section, we can write

$$\begin{aligned} ABCD_\pi &= \begin{bmatrix} 1 & 0 \\ j\omega C_T & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_T & jZ_T \sin\theta_T \\ j\dfrac{\sin\theta_T}{Z_T} & \cos\theta_T \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_T & 1 \end{bmatrix} \\ &= \begin{bmatrix} \cos\theta_T - \omega C_T Z_T \sin\theta_T & jZ_T \sin\theta_T \\ \dfrac{j}{Z_T}\left(2Z_T\omega C_T \cos\theta_T + \sin\theta_T - Z_T^2\omega^2 C_T^2 \sin\theta_T\right) & \cos\theta_T - \omega C_T Z_T \sin\theta_T \end{bmatrix}. \end{aligned} \tag{9.26}$$

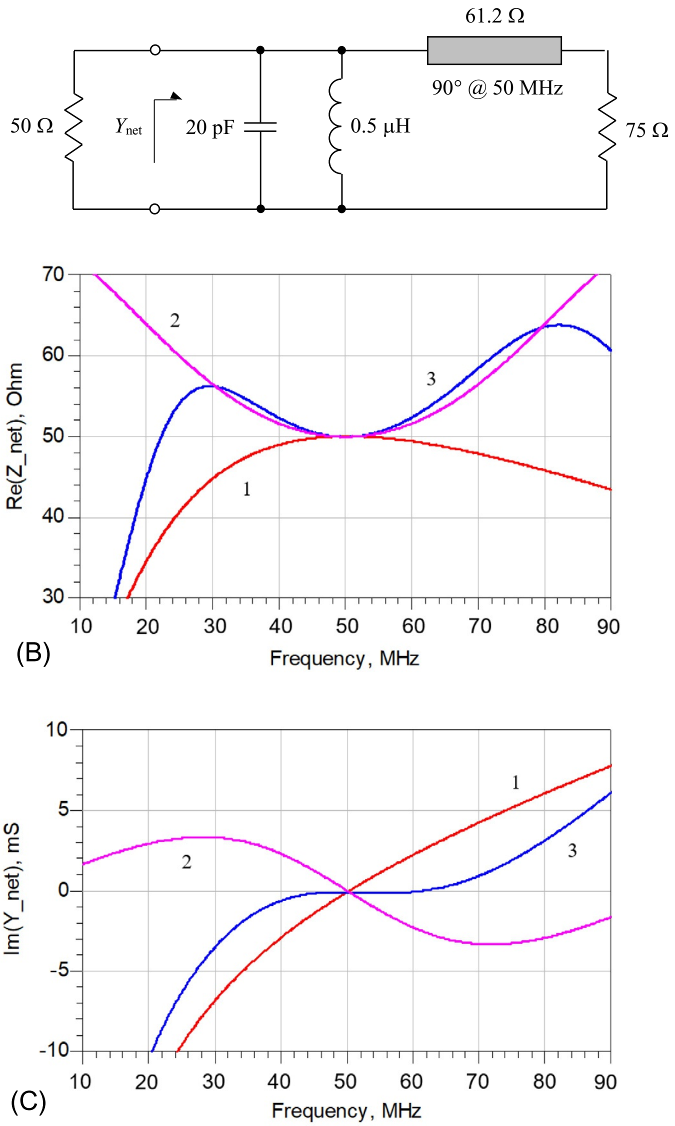


FIG. 9.7

Susceptance-compensation circuit with quarter-wavelength transmission line.

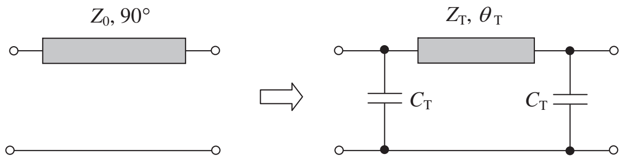

Z_0, 90°
Z_T, θ_T
C_T
C_T

FIG. 9.8

Transmission-line single frequency equivalence technique.

Hence, equating A and B elements from each matrix yields.

$$Z_{\mathrm{T}} = \frac{Z_0}{\sin\theta_{\mathrm{T}}}, \tag{9.27}$$

$$C_{\mathrm{T}} = \frac{\cos\theta_{\mathrm{T}}}{\omega Z_0}. \tag{9.28}$$

As a result, the characteristic impedance of the transmission line can be increased significantly by reducing its electrical length. Also, such a transformation is very important when the value of the device output capacitance exceeds the required optimum value for the optimum Class-E operation. In this case, the excess capacitance can be used as a part or entire shunt capacitance in the Π-type low-pass section, and the optimum switching Class-E conditions will be completely satisfied at the fundamental frequency.

9.2 Broadband Class-E with shunt capacitance and series filter

In the basic circuit of a Class-E amplifier with shunt capacitance shown in Fig. 9.9A, the harmonic impedance of the series fundamentally tuned L_0C_0 circuit is assumed to be high due to its high loaded quality factor. The value of the shunt capacitance C must also be correct to produce the correct voltage

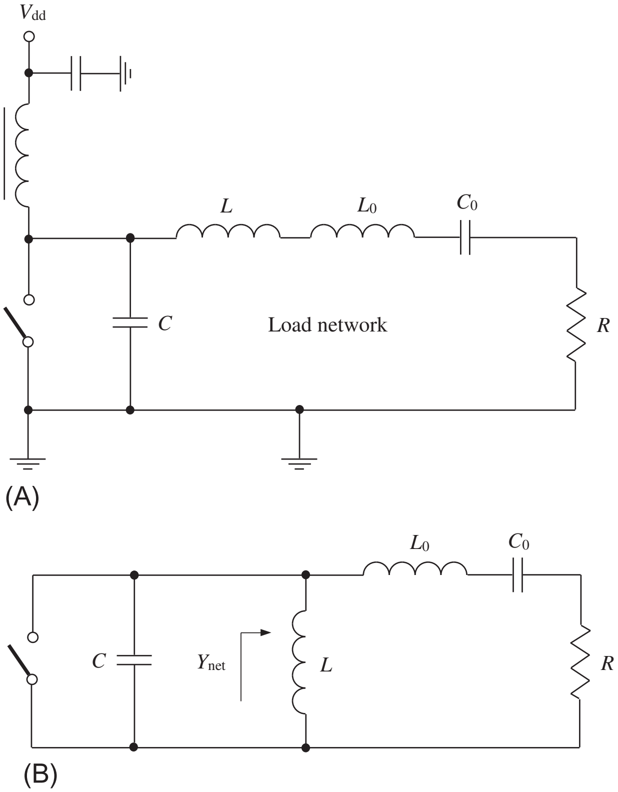


FIG. 9.9

Load networks of Class-E with shunt capacitance.

when the switch is turned off and to satisfy the steady-state switching conditions. In this case, the load phase angle of the series tuned circuit composed of the total inductor ($L+L_0$) and capacitor C_0, determining the optimum angle for producing the correct voltage waveform, can be obtained according to Eq. (5.31) in Chapter 5 at the resonant angular frequency $\omega_0 = 1/\sqrt{L_0 C_0}$ as

$$\theta = \tan^{-1}\left(\frac{\omega_0 L}{R}\right) = \tan^{-1} 1.1525 = 49.052^\circ. \tag{9.29}$$

If the load network is designed without incorporating a shunt capacitance, a simple broadband network with an optimum load angle $\theta = 49.052^\circ$ given in Eq. (9.29) can be designed. Then, this phase angle reduces to the required angle $\varphi = 35.945^\circ$, given by Eq. (5.34) in Chapter 5, when a shunt capacitance is added. The circuit schematic of a simple load network capable of presenting a constant load angle over a very wide bandwidth is shown in Fig. 9.9B.[1] The load network consists of a low-Q series L_0C_0 circuit connected between a shunt inductor and a load that allows a constant susceptance to be maintained over a wide bandwidth. The frequency behavior of the conductance ReY_{net} and susceptance ImY_{net} of such a load network with parameters $L = 42$ nH, $L_0 = 30$ nH, and $C_0 = 35$ pF are shown in Fig. 9.10A and B,

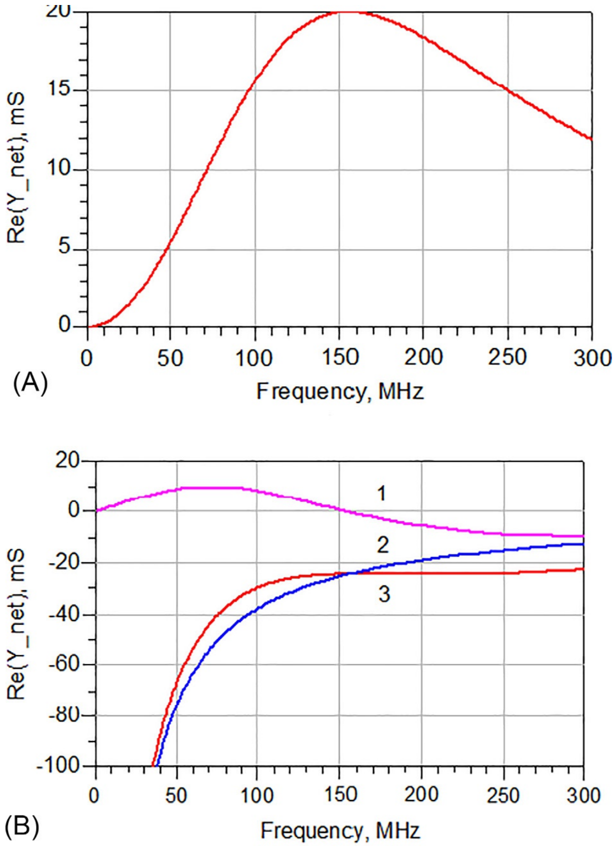


FIG. 9.10

Conductance and susceptance of broadband circuit.

respectively, where combining of the susceptance of the series resonant circuit with negative slope (curve 1) and the susceptance of the shunt inductor with positive slope (curve 2) provides a constant total susceptance over a very wide frequency range (curve 3).

In order to maintain the load angle constant in a wide frequency range, the slope of the susceptance provided by the inductance L should be cancelled by the slope provided by the resonant L_0C_0 circuit. The load-network admittance of Fig. 9.9B can be written as

$$Y_{\text{net}} = -\frac{j}{\omega L} + \frac{1}{R + j\left(\omega L_0 - \dfrac{1}{\omega C_0}\right)}, \tag{9.30}$$

which reduces at the resonant frequency ω_0 to

$$Y_{\text{net}} = -\frac{j}{\omega_0 L} + \frac{1}{R}. \tag{9.31}$$

For slope cancellation, it is necessary to apply a zero-derivative condition given by Eq. (9.4) into Eq. (9.30) for the load-network susceptance $B_{\text{net}} = \text{Im}Y_{\text{net}}$ at the resonant frequency ω_0. As a result,

$$\frac{1}{\omega_0^2 L} = \frac{2}{\omega_0^2 C_0 R^2}. \tag{9.32}$$

Thus, the design equations to calculate the parameters of a broadband Class-E load network providing maximum flatness can be calculated using Eqs. (9.29) and (9.32) from

$$L = \frac{R}{\omega_0 \tan\theta}, \tag{9.33}$$

$$C_0 = \frac{2L}{R^2}, \tag{9.34}$$

$$L_0 = \frac{1}{\omega_0^2 C_0}. \tag{9.35}$$

To reduce the output power at the harmonics, such a simple load network can be combined with a broadband matching network and a bandpass filter. As an example, a complete circuit based on a low-pass L-type matching section and a third-order Chebyshev bandpass filter, as shown in Fig. 9.11A, was designed to deliver 12 W into a 50-Ω load across the frequency bandwidth of 130–180 MHz using a 12-V power supply.[1] From Fig. 9.11B, it follows that this load network presents a constant magnitude of input impedance of 12 Ω (curve 1) and a load phase angle of around 36 degrees (curve 2) over the required wide frequency range. As a result, the broadband MOSFET Class-E power amplifier was capable of providing a fairly constant efficiency at approximately 60% with suppression of the second, third, and fourth harmonics better than 45 dB below fundamental. The drain efficiency of a GaN HEMT power amplifier with a Butterworth bandpass filter in the load network can be increased to greater than 80% in a frequency bandwidth of 600–800 MHz with an output power greater than 45 dBm.[11, 12] To provide the frequency bandwidth of 30% around the center bandwidth frequency of 1 GHz, the load network was composed of a series transmission line and a shunt open-circuit stub.[13]

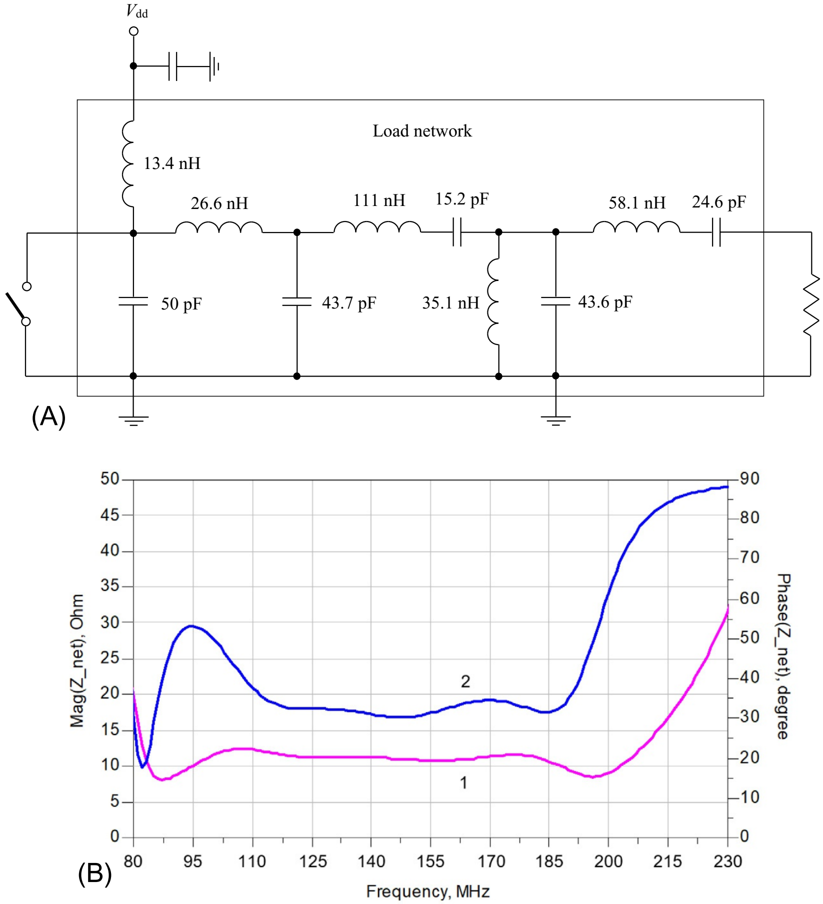

V_{dd}
Load network
13.4 nH
26.6 nH
111 nH
15.2 pF
58.1 nH
24.6 pF
50 pF
43.7 pF
35.1 nH
43.6 pF
50 Ω
(A)
Mag(Z_net), Ohm
Phase(Z_net), degree
Frequency, MHz
50
45
40
35
30
25
20
15
10
5
0
90
80
70
60
50
40
30
20
10
0
80
95
110
125
140
155
170
185
200
215
230
1
2
(B)

FIG. 9.11

Broadband Class-E load network with bandpass filter and impedance.

9.3 Broadband Class-E with shunt capacitance and shunt filter

To extend the reactance-compensation technique, let us consider the simplified equivalent load network with a shunt capacitance C, a series inductance L, and a shunt L_0C_0 circuit tuned to the fundamental, as shown in Fig. 9.12. In order to maintain the load phase angle constant in a wide frequency range, the positive slope of the reactance provided by the L-type circuit should be cancelled by the negative slope of the reactance provided by the shunt L_0C_0 circuit. In this case, the load-network admittance $Y_{\text{net}} = 1/Z_{\text{net}}$ can be written as

$$Y_{\text{net}} = j\omega C + \frac{1 + j\omega' C_0 R}{R(1 - j\omega\omega' L C_0) + j\omega L}, \tag{9.36}$$

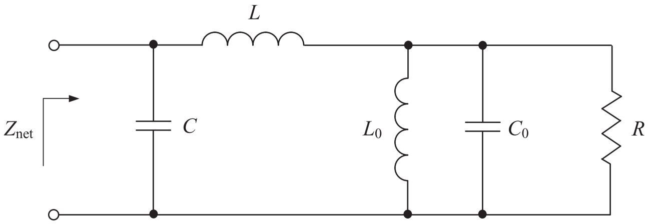


FIG. 9.12

Equivalent circuit of Class-E with shunt capacitance and shunt filter.

where

$$\omega' = \omega\left(1 - \frac{\omega_0^2}{\omega^2}\right), \tag{9.37}$$

and $\omega_0 = 1/\sqrt{L_0 C_0}$ is the resonant angular frequency. For a nominal Class-E with shunt capacitance and shunt filter, the normalized inductance L and capacitance C are determined by Eqs. (8.26) and (8.27), respectively.

The frequency bandwidth with a constant load phase angle will be maximized by applying Eqs. (9.4)–(9.36) when the load-network susceptance $B_{\text{net}} = \text{Im}Y_{\text{net}}$ is defined by

$$B_{\text{net}} = \omega C + \frac{\omega' C_0 R^2 (1 - j\omega\omega' L C_0) - \omega L}{R^2 (1 - j\omega\omega' L C_0)^2 + (\omega L)^2}. \tag{9.38}$$

As a result, an additional equation can be derived as

$$2\omega_0 C_0 R - \frac{\omega_0 L}{R} - \omega_0 C R \frac{\left(\frac{\omega_0 L}{R}\right)^2 + 1}{\left(\frac{\omega_0 L}{R}\right)^2 - 1} = 0. \tag{9.39}$$

Finally, the shunt capacitance C_0 and inductance L_0 can be obtained by

$$C_0 = \frac{1.0896}{\omega_0 R}, \tag{9.40}$$

$$L_0 = \frac{1}{\omega_0^2 C_0}. \tag{9.41}$$

Fig. 9.13A shows an example of a reactance-compensation load network for Class-E power amplifier with shunt filter using lumped elements. In this case, the reactance of the circuit with shunt capacitance and series inductance varies similar to that of the series resonant circuit with positive slope, whereas the required negative slope is provided by the parallel resonant circuit. Selection of the proper circuit parameters according to Eqs. (8.26)–(8.28) for Class-E with shunt filter together with Eqs. (9.40) and (9.41) for shunt-filter elements enables the magnitude of the two slopes to be made identical, so as to achieve a constant total reactance and phase of the load-network impedance Z_{net} over a wide frequency range.

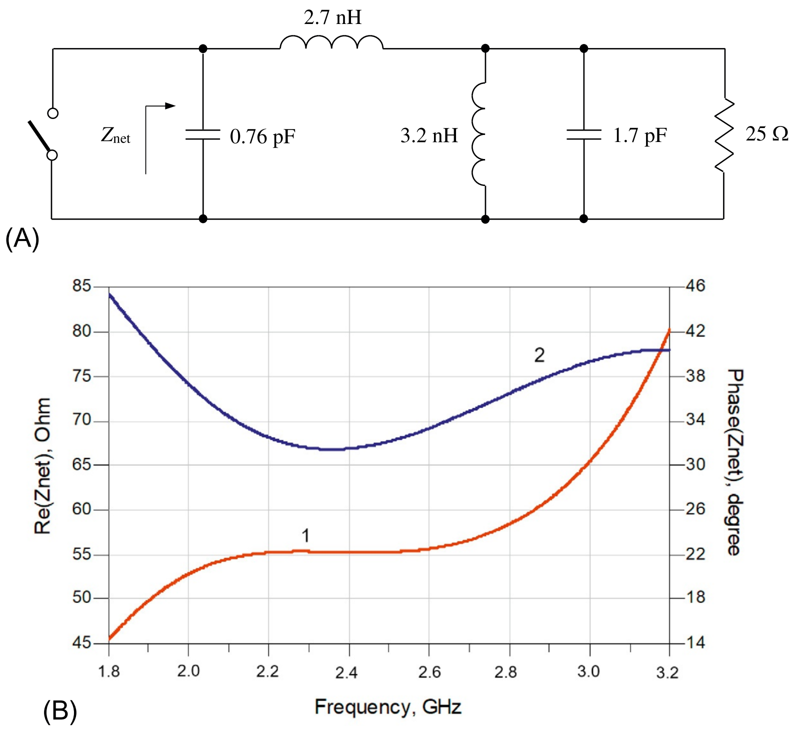


FIG. 9.13

Reactance-compensation Class-E circuit with lumped elements and its performance.

The simulation results at the fundamental frequency show that the resistance ReZ_{net} varies from 50 Ω at 1.9 GHz to 65 Ω at 3.0 GHz, as shown in Fig. 9.13B by curve 1, whereas the load-network phase varies between 31.5 and 41 degrees from 1.9 to 3.2 GHz (curve 2).

Generally, the design of a practical multisection *LC* filter is based on some approximate equivalence between lumped and distributed elements, which can be established by applying a Richards' transformation.[14] This implies that the distributed circuits composed of equal-length open- and short-circuited transmission lines can be treated as lumped elements under the transformation

$$s = j \tan \frac{\pi\omega}{2\omega_0}, \tag{9.42}$$

where $s = j\omega/\omega_c$ is the conventional normalized complex frequency variable, ω_c is the cutoff angular frequency, and ω_0 is the angular frequency, for which the transmission lines are a quarter wavelength.[15]

As a result, for a unity characteristic impedance and cutoff frequency, the one-port impedance of a short-circuited transmission line corresponds to the reactive impedance of a lumped inductor Z_L as

$$Z_L = sL = jL \tan \frac{\pi\omega}{2\omega_0}. \tag{9.43}$$

Similarly, the one-port admittance of an open-circuited transmission line corresponds to the reactive admittance of a lumped capacitor Y_C as

$$Y_C = sC = jC\tan\frac{\pi\omega}{2\omega_0}. \tag{9.44}$$

The results obtained by Eqs. (9.43) and (9.44) show that an inductor L can be replaced with a short-circuit stub of electrical length $\theta = \pi\omega/2\omega_0$ and characteristic impedance $Z_0 = L$, whereas a capacitor C can be replaced with an open-circuit stub of electrical length $\theta = \pi\omega/2\omega_0$ and characteristic impedance $Z_0 = 1/C$.

From Eq. (9.42), it follows that the cutoff occurs when $\omega = \omega_c$, resulting in

$$\tan\frac{\pi\omega_c}{2\omega_0} = 1, \tag{9.45}$$

which gives a stub length $\theta = 45°$ (or $\pi/4$) with $\omega_c = \omega_0/2$. Hence, the inductors and capacitors of a lumped-element filter can be replaced with short-circuit and open-circuit stubs, as shown in Fig. 9.14. Because the lengths of all stubs are the same and equal to $\lambda/8$ at the cutoff frequency ω_c, these lines are called the commensurate lines. At the frequency $\omega = \omega_0$, the transmission lines will be a quarter-wavelength long, resulting in an attenuation pole. However, at any frequency away from ω_c, the impedance of each stub will no longer match the original lumped-element impedances, and the filter response will differ from the desired filter prototype response. Note that the response will be periodic in frequency, repeating every $4\omega_c$.

Fig. 9.15A shows an example of a reactance-compensation load network for a Class-E power amplifier with shunt filter using both lumped elements and transmission lines. In this case, the shunt filter is represented by open- and short-circuit stubs replacing lumped capacitor and inductor, respectively, each having the characteristic impedance of 50 Ω and electrical length of 45 degrees at 2.2 GHz. The series inductive reactance is created by lumped inductor that can be represented by the device bondwire and package lead and short transmission line. The simulation results at the fundamental frequency show that the load-network resistance ReZ_{net} and phase vary between 40 and 57 Ω (curve 1) and between 25 and 41 degrees (curve 2) from 1.8 to 3.2 GHz, as shown in Fig. 9.15B.

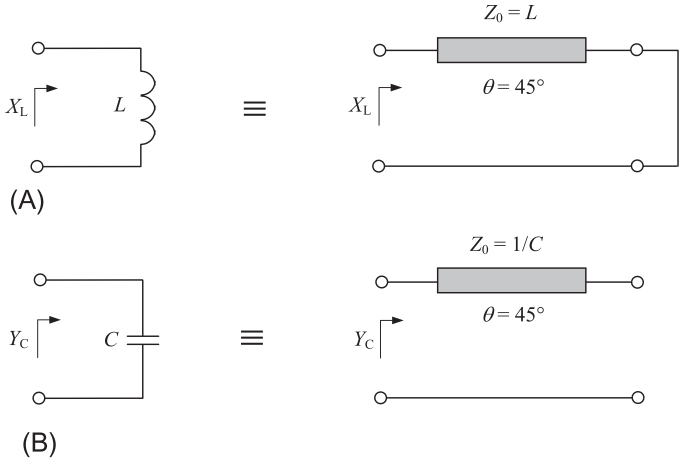


FIG. 9.14

Equivalence between lumped elements and transmission lines.

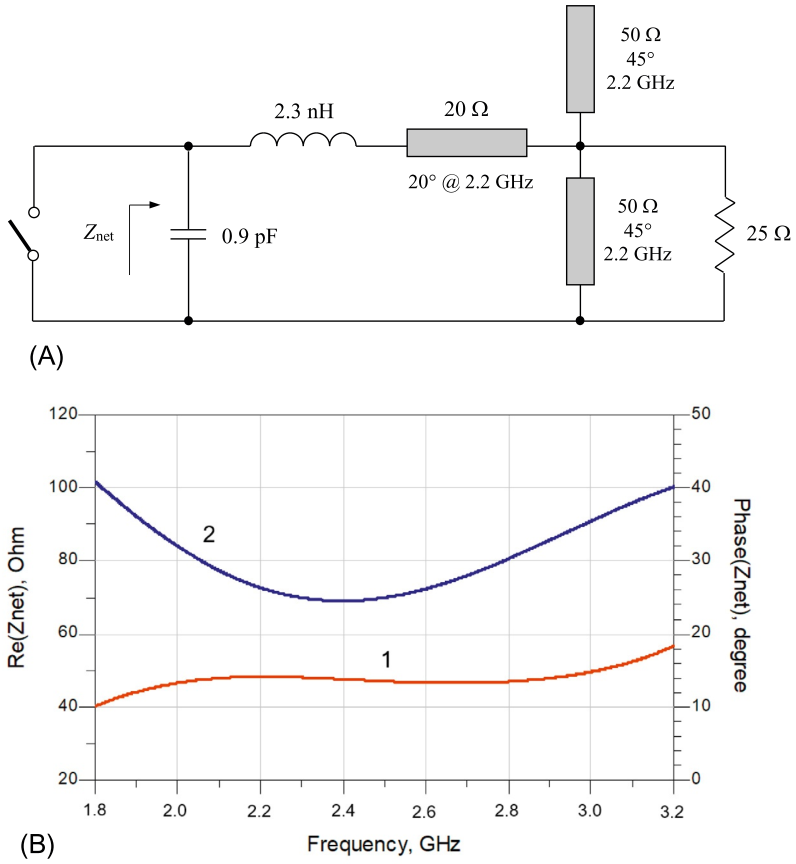

50 Ω
45°
2.2 GHz
2.3 nH
20 Ω
20° @ 2.2 GHz
50 Ω
45°
2.2 GHz
25 Ω
Z_{net}
0.9 pF
(A)
120
100
80
60
40
20
50
40
30
20
10
0
2
1
Re(Znet), Ohm
Phase(Znet), degree
1.8
2.0
2.2
2.4
2.6
2.8
3.0
3.2
Frequency, GHz
(B)

FIG. 9.15

Reactance-compensation Class-E circuit with lumped elements and transmission lines and its performance.

Generally, a very broadband power amplifier design employs an input lossy *LCR* matching circuit to minimize the input return loss and output power variations over very wide frequency bandwidths with an output *LC* network to compensate for the device output reactance.[16, 17] As an alternative, to provide an input broadband matching over octave bandwidth, it is possible to use a multisection matching transformer consisting of stepped transmission-line sections with different characteristic impedances and electrical lengths.[18, 19] Such an input matching structure is convenient in practical implementation since there is no need to use any tuning capacitors.

Fig. 9.16A shows the idealized simulation setup of a 10-W 28-V broadband Class-E power amplifier circuit designed to operate over a frequency bandwidth from 1.7 to 2.7 GHz and based on a GaN HEMT CGH40010 device, where both the input matching circuit and load network are composed of ideal transmission lines.[19, 20] For an input broadband matching, a multisection matching transformer consisting of three stepped transmission-line sections with different characteristic impedances and

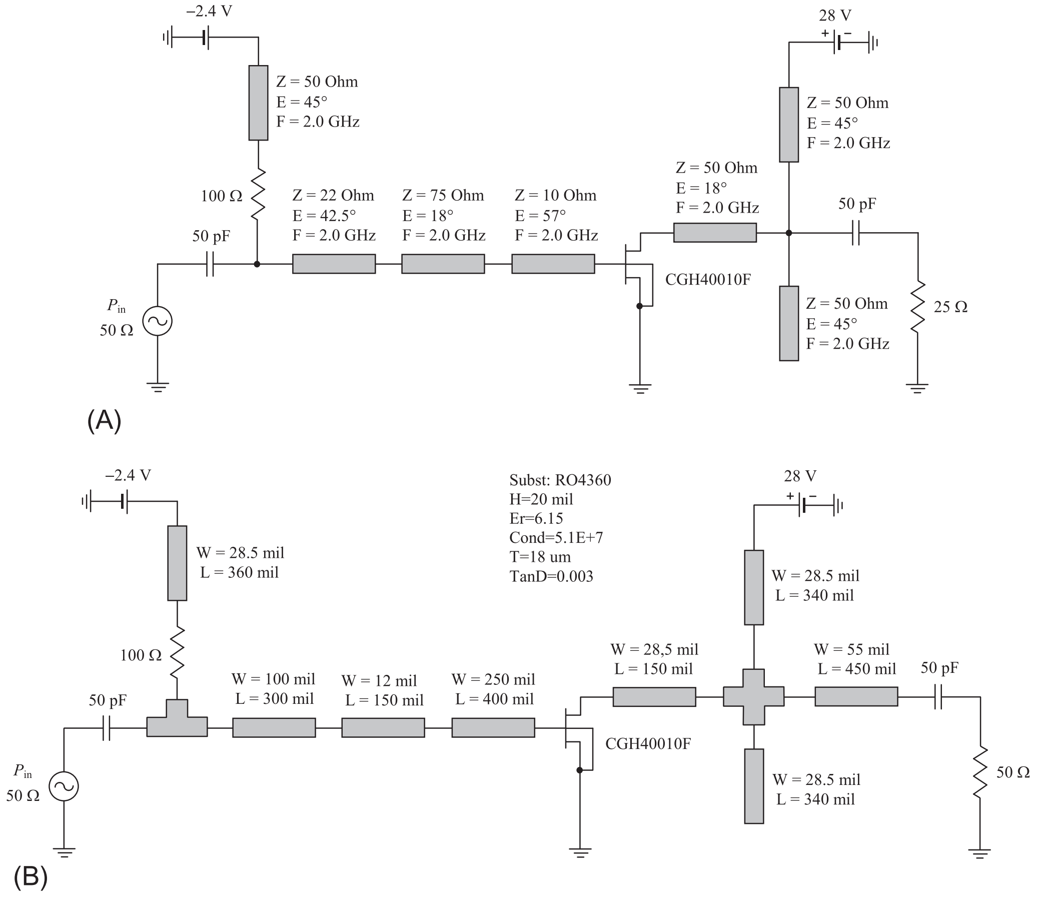

−2.4 V
Z = 50 Ohm
E = 45°
F = 2.0 GHz
100 Ω
50 pF
Z = 22 Ohm
E = 42.5°
F = 2.0 GHz
Z = 75 Ohm
E = 18°
F = 2.0 GHz
Z = 10 Ohm
E = 57°
F = 2.0 GHz
Z = 50 Ohm
E = 18°
F = 2.0 GHz
CGH40010F
28 V
Z = 50 Ohm
E = 45°
F = 2.0 GHz
50 pF
Z = 50 Ohm
E = 45°
F = 2.0 GHz
25 Ω
P_in
50 Ω
(A)
−2.4 V
W = 28.5 mil
L = 360 mil
100 Ω
50 pF
W = 100 mil
L = 300 mil
W = 12 mil
L = 150 mil
W = 250 mil
L = 400 mil
Subst: RO4360
H=20 mil
Er=6.15
Cond=5.1E+7
T=18 um
TanD=0.003
W = 28,5 mil
L = 150 mil
CGH40010F
28 V
W = 28.5 mil
L = 340 mil
W = 55 mil
L = 450 mil
50 pF
W = 28.5 mil
L = 340 mil
50 Ω
P_in
50 Ω
(B)

FIG. 9.16

Idealized circuit schematic of broadband GaN HEMT Class-E power amplifier.

electrical lengths. The nominal Class-E load resistance can be calculated for $P_{\text{out}} = 15\,\text{W}$, $V_{\text{dd}} = 28\,\text{V}$, and $V_{\text{sat}} = 2.5\,\text{V}$ according to Eq. (5.33) in Chapter 5 as

$$R = 0.5768\,\frac{(V_{\text{dd}} - V_{\text{sat}})^2}{P_{\text{out}}} = 25\,\Omega, \tag{9.46}$$

where P_{out} is the output power at the fundamental frequency, V_{dd} is the drain supply voltage, and V_{sat} is the saturation voltage defined from the device output current-voltage characteristics. In this case, the parallel resonant circuit in the broadband Class-E load network connected in parallel to a 25-Ω load is represented by open- and short-circuit stubs, each having a characteristic impedance of 50 Ω and electrical length of 45 degrees at 2 GHz. An additional series transmission line with low characteristic impedance having a quarter wavelength at the high bandwidth frequency can be used to match an idealized 25-Ω load with a standard 50-Ω load.

Fig. 9.16B shows the ADS implementation of an idealized circuit of a broadband GaN HEMT Class-E power amplifier shown in Fig. 9.16A into a 20-mil RO4360 substrate, where an additional series microstrip line with low characteristic impedance is used to match an idealized 25-Ω load with a standard 50-Ω load. As a result, an output power greater 41 dBm with a power gain of around 10 dB was simulated for an input power of 31 dBm, as shown in Fig. 9.17A. In this case, a drain efficiency of over 73% and a power-added efficiency (*PAE*) of over 67% were achieved across the required frequency range from 1.7 to 2.7 GHz, as shown in Fig. 9.17B.

Fig. 9.18A shows the test PCB board of an implemented broadband Class-E GaN HEMT power amplifier using a Cree CGH40010P device in a pill-type package.[20] The input matching circuit, output load network, and gate and drain bias circuits (having bypass capacitors on their ends) are fully based on microstrip lines fabricated on a 20-mil RO4360 substrate according to their simulation parameters shown in Fig. 9.16B. Only the width of a series microstrip line connected to the drain terminal was slightly increased to make it longer. Fig. 9.18B shows the measured results of a transmission-line broadband Class-E GaN HEMT power amplifier with an output power of 40.6 ± 0.9 dBm and an average drain efficiency of about 68% (from 63% to 73%). In this case, a power gain around 9.5 dB at a drain supply voltage of 24 V in a frequency bandwidth from 1.4 to 2.7 GHz was achieved without any tuning of the input matching circuit and load network.

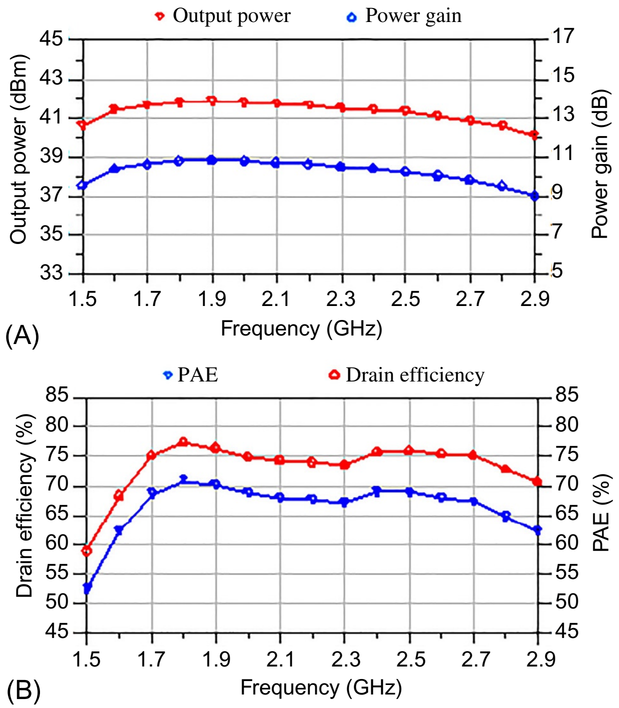


FIG. 9.17

Output power, power gain, and efficiency versus frequency.

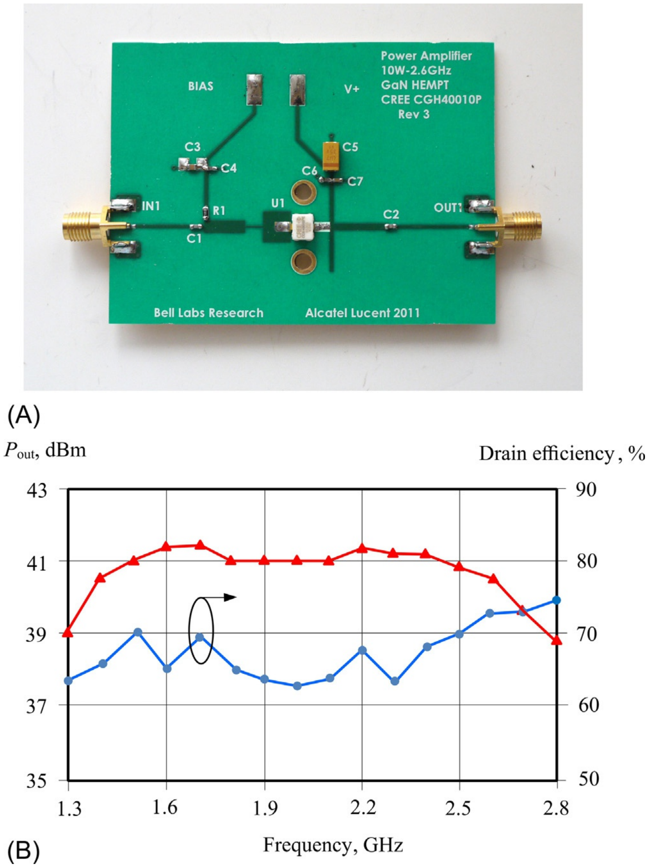


FIG. 9.18

Test board and performance of broadband Class-E GaN HEMT amplifier.

Previously, a *PAE* above 60% was achieved between 1.87 and 2.11 GHz with an output power varying from 20 to 23 dBm for a medium-power broadband pHEMT Class-E power amplifier using a transmission-line parallel resonant circuit with short- and open-circuit stubs.[21] For a harmonically tuned GaN HEMT broadband power amplifier using open-circuit stubs in the load network incorporating a three-section bandpass filter, an output power of around 100 W with a drain efficiency greater than 65% in a frequency bandwidth from 1.55 to 2.25 GHz was achieved.[22] Using a six-order low-pass load network in a GaN HEMT Class-E power amplifier, where the series inductors are replaced by short-length transmission lines and the shunt capacitors are replaced by open-circuit stubs, a drain efficiency of 63%–89% with an output power of 10–20 W and a power gain of 10–13 dB was measured in a frequency bandwidth of 0.9–2.2 GHz at a supply voltage of 26 V.[23]The Class-E approximation with inductive load impedance at the fundamental and capacitive reactance at the second harmonic over wide frequency range can be achieved by using synthesized bandpass and low-pass matching topologies in the form of a multisection microstrip line structure in the input matching circuit and load network, respectively. As a result, such a broadband power amplifier using a 10-W GaN HEMT device (CGH40010F) achieved a *PAE* of 58%–72% and an output power of 41 ± 0.5 dBm with a power gain of 12 ± 0.5 dB across the frequency bandwidth of 2.0–2.9 GHz.[24]

9.4 Broadband parallel-circuit Class-E

The susceptance-compensation technique can be directly applied to the switchmode parallel-circuit Class-E power amplifier because its load-network configuration has exactly the same structure as shunt and series resonant circuits, as shown in Fig. 9.19A.[25, 26] In this case, the nominal load resistance R and phase angle ϕ of the parallel-circuit Class-E load network can be obtained from Eqs. (6.79) and (6.83) in Chapter 6, respectively. The parallel inductance L and shunt capacitance C required for an optimum

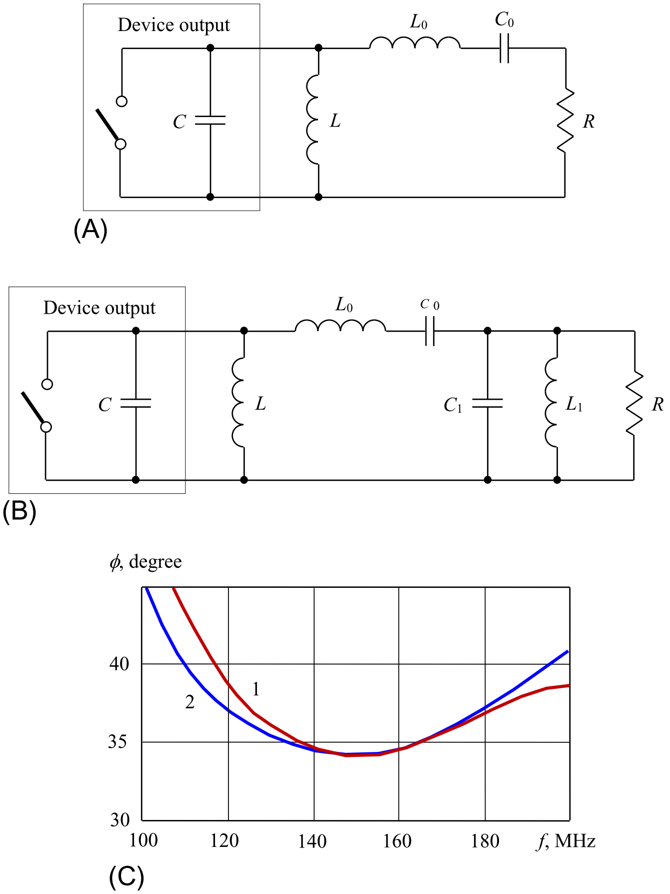

Device output
L_0
C_0
C
L
R
(A)
Device output
L_0
C_0
C
L
C_1
L_1
R
(B)
ϕ, degree
40
35
30
100
120
140
160
180
f, MHz
1
2
(C)

FIG. 9.19

Single- and double-susceptance-compensation circuits.

parallel-circuit Class-E operation are calculated as functions of the load resistance R at the operating from Eqs. (6.80) and (6.81) in Chapter 6, respectively. The parameters of the series resonant L_0C_0 circuit must be chosen to provide a constant phase angle of the load network over a required wide frequency bandwidth.

As a result, by substituting Eqs. (6.80) and (6.81) into Eq. (9.6), the series capacitance C_0 and inductance L_0 can be calculated at the center bandwidth frequency ω_0 by

$$L_0 = 1.026\frac{R}{\omega_0}, \tag{9.47}$$

$$C_0 = \frac{1}{\omega_0^2 L_0}. \tag{9.48}$$

Wider frequency bandwidth with high-efficiency performance can be achieved using a double-susceptance-compensation circuit shown in Fig. 9.19B, where L_0C_0 and L_1C_1 are the series and parallel resonant circuits, respectively.[19, 27] In this case, similar to the broadband design in a Class-E mode with shunt capacitance using a double-susceptance-compensation, the parameters of the series and shunt resonant circuits for the broadband design in a parallel-circuit Class-E mode with the corresponding loaded quality factors $Q_0 = \omega_0 L_0/R$ and $Q_1 = \omega_0 C_1 R$, which are close to unity and greater, can approximately be calculated from Eqs. (9.15) and (9.16), where the load angle $\theta = \tan^{-1}(R/\omega_0 L)$ is taken into account using Eq. (6.80). Such a load network can be considered as a broadband matching-forming circuit, which provides simultaneously the Class-E switching conditions and matching with a standard 50-Ω load over wide frequency bandwidth.[28]

The circuit simulations for these two types of susceptance-compensation load networks were performed at a center bandwidth frequency $f_0 = 150\,\text{MHz}$ for a standard load resistance $R = 50\,\Omega$. Fig. 9.19C shows the frequency dependencies of the load-network phase angle ϕ for the single-susceptance- (curve 1) and double-susceptance- (curve 2) compensation circuits, demonstrating their very broadband operation capability. Using just a single-susceptance load network yields a significant widening of the operating frequency bandwidth with a minimum deviation of the magnitude and phase of the load-network impedance. A double-susceptance-compensation load network obtains the maximum deviation from the optimum value of about 34 degrees by only 3 degrees in a frequency range from 120 to 180 MHz.

To achieve a high-efficiency broadband operation mode with a high-power gain in VHF frequency band, it is best to design the power amplifier based on silicon LDMOSFET devices. In this case, it is easy to provide a very broadband input matching using lossy-matching circuit, especially at operating frequencies about 10 times lower than the device transition frequency f_T. Fig. 9.20 shows the circuit schematic of an LDMOSFET power amplifier designed to operate in a 2:1 frequency bandwidth from 100 to 200 MHz using a double-susceptance-compensation load network with broadband matching properties at the fundamental frequency.[19] The input lossy-matching circuit includes a simple L-transformer connected in parallel with a series circuit consisting of an inductance of 20 nH and a resistance of 50 Ω. This provides a minimum input return loss at 200 MHz of about 15 dB and an input *VSWR* less than 1.4 over the entire frequency bandwidth from 100 to 200 MHz.

From Fig. 9.21A, it follows that, for such an octave-band VHF Class-E power amplifier with an input power of 1 W using a 1.25-μm LDMOSFET device with a total gate width of 28 × 1.44 mm, a power gain of 10 ± 0.5 dB (curve 2) can be achieved with a drain efficiency of about 70% and higher

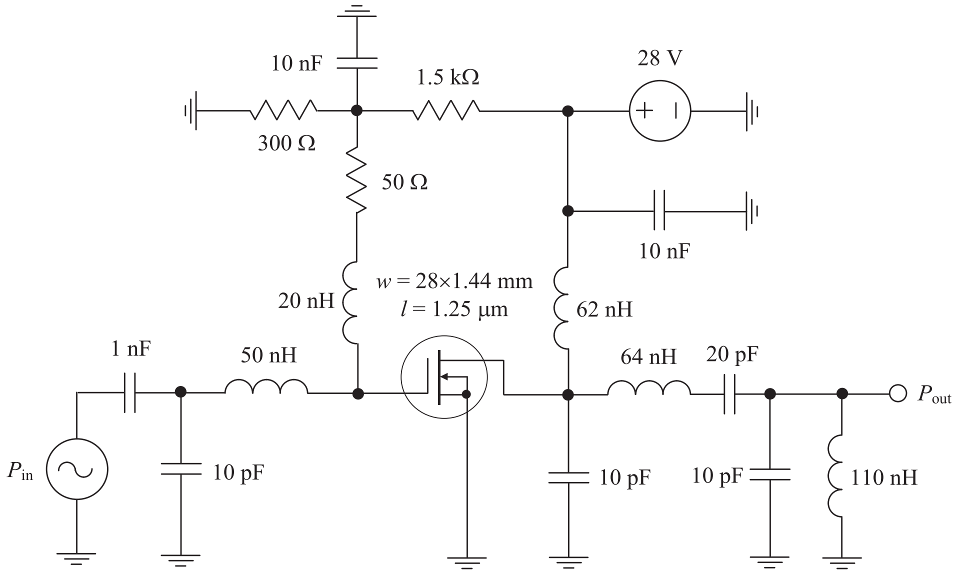


FIG. 9.20

Simulated broadband Class-E LDMOSFET power amplifier.

(curve 1). An analysis of the simulated drain voltage and current waveforms at the center bandwidth frequency of 150 MHz shown in Fig. 9.21B demonstrates that the broadband operating mode is very close to a nominal parallel-circuit Class-E operation mode, although the impedance conditions at higher harmonics are not controlled properly. As seen from the plots when the transistor is turned on, high values of drain current (up to 1.3 A) are achieved with small saturation voltages of 0–4 V. On the other hand, when the transistor is turned off, the drain current continues to flow, but now through the device gate-drain capacitance C_{gd} and drain-source capacitance C_{ds} but not through the active channel. A drain efficiency of 74% with an output power of 8 W across the frequency range from 136 to 174 MHz with a gain flatness of 0.7 dB was measured for a parallel-circuit Class-E LDMOSFET power amplifier with a low supply voltage of 7.2 V.[29] The power-added efficiency can be increased to 80% and greater in a frequency range from 140 to 180 MHz with an output power of 34.4 ± 1.5 dBm using a GaN HEMT device.[30]

Fig. 9.22 shows the circuit schematic of a broadband parallel-circuit LDMOSFET power amplifier with a second-harmonic trap represented by a mixed parallel-series resonant circuit with $C_1 = 16$ pF, $L_1 = 93$ nH, and $L_2 = 31$ nH.[31] The second-harmonic trap circuit presents a low impedance for the second harmonic when the parallel L_1C_1 circuit behaving as a capacitance is resonated with the series inductance L_2 to provide a short circuit. Using an MRFE6VS25N device with a drain-source breakdown voltage of 142 V, a drain efficiency of 79%–82.2%, a *PAE* of 74%–80.5%, a power gain of 20–22 dB, and an output power of 41.5–44.0 dBm were achieved across the frequency bandwidth of 115–155 MHz at a supply voltage of 35 V, with the second and third harmonic levels of better than −30 dBc from 125 to 160 MHz. The simulated drain voltage and current waveforms for power amplifier at three different bandwidth frequencies (115, 135, and 155 MHz) are shown in Fig. 9.23, demonstrating close to Class-E mode waveforms.

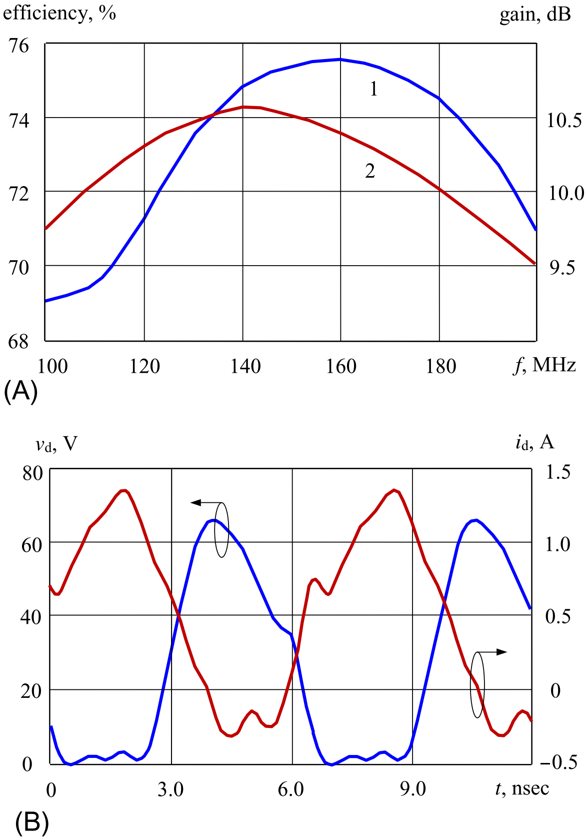


FIG. 9.21

Broadband performance of Class-E LDMOSFET power amplifier.

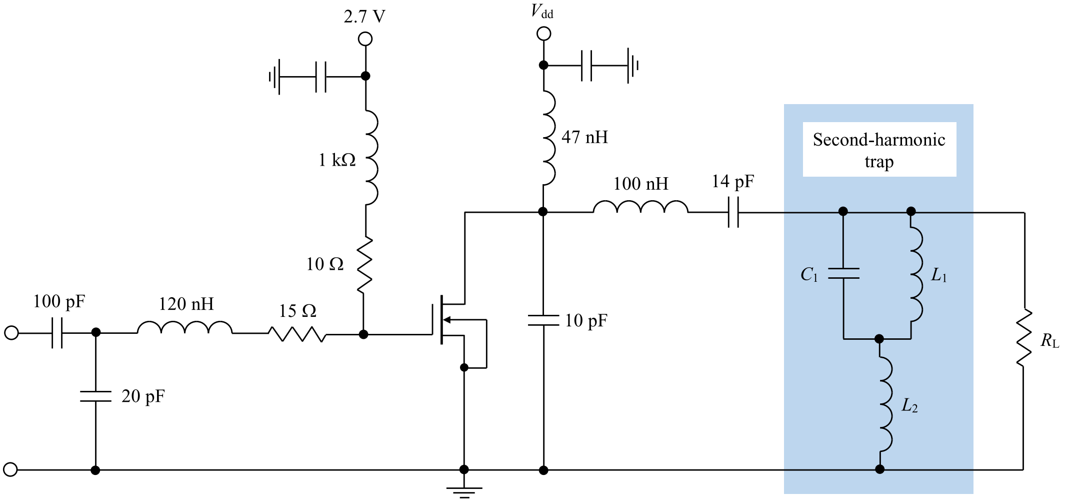

2.7 V
V_{dd}
1 kΩ
10 Ω
47 nH
100 nH
14 pF
Second-harmonic trap
100 pF
120 nH
15 Ω
10 pF
20 pF
C_1
L_1
L_2
R_L

FIG. 9.22

Circuit schematic of broadband parallel-circuit LDMOSFET power amplifier with second-harmonic trap.

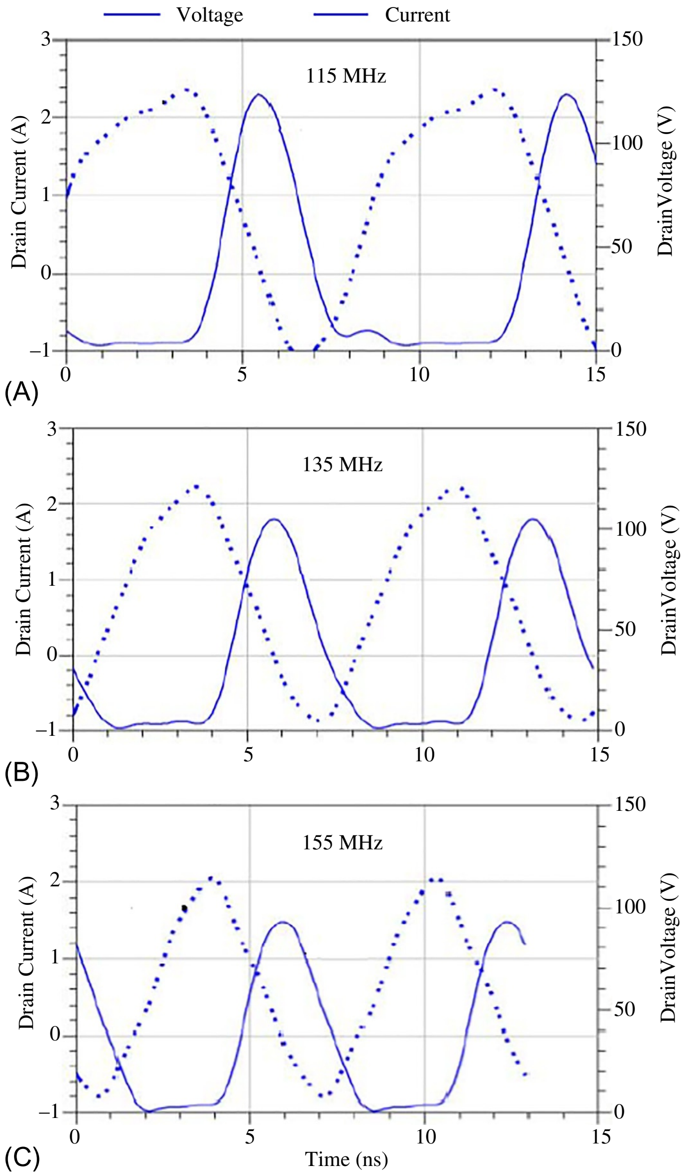


FIG. 9.23

Simulated drain voltage and current waveforms for power amplifier of Fig. 9.21.[31]

Similarly, the transmission-line susceptance-compensation technique can also be applied to a parallel-circuit Class-E power amplifier, where the series transmission line of a quarter wavelength at the center bandwidth frequency can be used instead of a series L_0C_0 resonant circuit, as shown in Fig. 9.24A. In some practical cases, the series quarter-wave line can be replaced by an equivalent

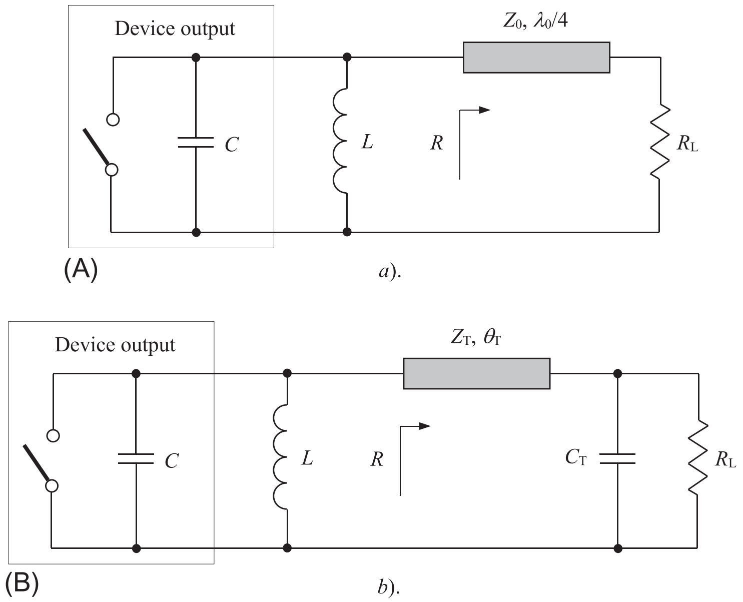


FIG. 9.24

Transmission-line susceptance-compensation circuit.

low-pass Π-type circuit consisting of a series transmission line with higher characteristic impedance and electrical length much less than 90 degrees and two shunt capacitors when the capacitance adjacent to the device output can be counted within the total shunt capacitance required for a nominal parallel-circuit Class-E mode. If it is necessary to additionally provide an output matching between the nominal Class-E load resistance and 50-Ω load, a series quarter-wave line can be replaced by a low-pass L-type matching circuit with a series transmission line and a shunt capacitor, as shown in Fig. 9.24B.

Fig. 9.25A shows an example of the transmission-line broadband Class-E load network where the parallel inductance is replaced by a short-length short-circuited transmission line, which can be easily implemented on a printed-circuit board as microstrip lines providing minimum insertion loss. The electrical lengths of the transmission lines are given at the center bandwidth frequency of 300 MHz. In this case, the input load-network resistance varies from 17 Ω at 225 MHz to 47.5 Ω at 400 MHz, as shown in Fig. 9.25B by curve 1, with much less variation from 18.5 to 27 Ω in a frequency range from 250 to 350 MHz. The phase stays almost constant, around 33 degrees, in a frequency range from 250 to 350 MHz and varies from 22.5 degrees at 225 MHz to 39.5 degrees at 400 MHz (curve 2).

Fig. 9.26A shows the circuit schematic of a broadband high-efficiency microstrip LDMOSFET power amplifier with an output power of around 20 W and a power gain greater than 12 dB in a frequency range from 225 to 400 MHz at a DC-supply voltage of 28 V. Here, to approximate the parallel-circuit Class-E mode in a wide frequency range, the load network was designed to realize a single-susceptance-compensation technique using a parallel short-length transmission line in conjunction with a single L-type transmission-line transformer, because a ratio between the device equivalent output resistance required for an optimum Class-E mode and the standard load of 50 Ω is not

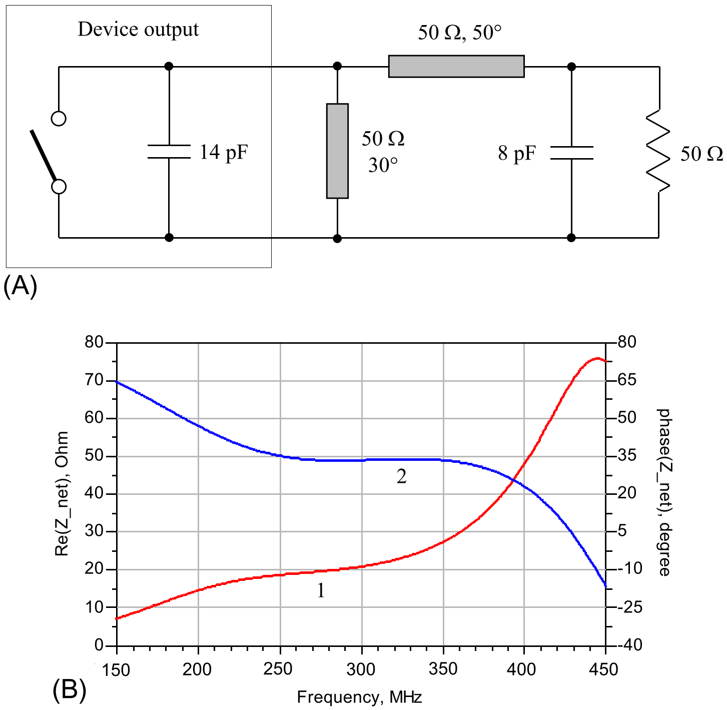


FIG. 9.25

Transmission-line Class-E load network with susceptance compensation.

significant. The input matching circuit includes two low-pass L-type matching sections to compensate for the device input capacitance over the entire frequency range. A lossy parallel resistor of 75 Ω is necessary to simplify the matching procedure and to improve the input return loss. In the first step, each matching network structure is calculated at the center bandwidth frequency based on the technical requirements and device equivalent circuit parameters. Then, to optimize the power amplifier performance over the entire frequency bandwidth, the simplest and fastest way is to apply an optimization procedure using computer simulators to satisfy certain criteria. For such a broadband power amplifier, the minimum output power ripple and input return loss with maximum power gain and efficiency can be chosen as the criteria. Generally, by applying a nonlinear broadband optimization technique (e.g., using ADS software) and setting the ranges of electrical length of the transmission lines between 0 and 90 degrees and parallel capacitances from 0 to 100 pF, we can obtain the parameters of the input matching and output load network.

However, to speed up this procedure, it is best to optimize circuit parameters separately for the input and output circuits. In this case, the input matching circuit is loaded by the device equivalent input series RC circuit, consisting of its gate resistance and gate-source capacitance. The load network must include at its input the device equivalent output shunt *RC* circuit consisting of an optimum Class-E load resistance required for a specified output power and supply voltage and drain-source capacitance. In this case, it is sufficient to use a fast linear optimization process, which will take only a few minutes to

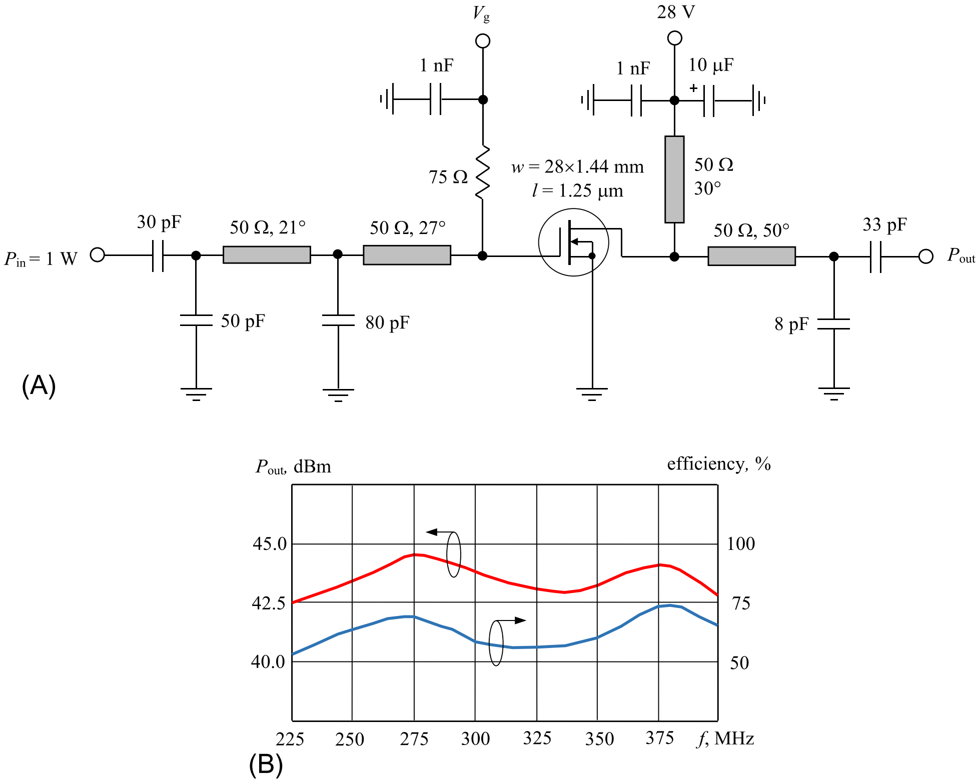


FIG. 9.26

Broadband high-efficiency microstrip LDMOSFET power amplifier.

complete the circuit design procedure. Finally, the resulting optimized values are incorporated into the overall power amplifier circuit for each element and final optimization is performed using a nonlinear active device model. The optimization process is finalized by choosing the nominal level of input power with optimizing elements in narrower ranges of their values of about 10%–20% for most critical elements. For practical convenience, it is possible to choose the characteristic impedances of all transmission lines of $50\,\Omega$. Fig. 9.26B shows the simulated broadband high-efficiency power amplifier performance achieving an output power of 42.5–44.5 dBm, a power gain of 13.5 ± 1 dB, and a drain efficiency of $64\% \pm 10\%$ in a frequency bandwidth from 225 to 400 MHz.[19]

The circuit schematic of a broadband two-stage InGaP/GaAs HBT power amplifier intended to operate in the WCDMA handset transmitters is shown in Fig. 9.27.[24, 25] The MMIC part of this power amplifier contains the transistors with emitter areas of the first and second stages as large as 540 and $3600\,\mu m^2$, respectively, input matching circuit, interstage matching circuit, and bias circuits on a die with total size of less than $1\,mm^2$. The MMIC implemented in a $3 \times 3\,mm^2$ package was mounted on an FR4 substrate which contains the output matching circuit and microstrip lines. Standard ceramic chip capacitors were used in the output matching circuit, and no further additional tuning was necessary.

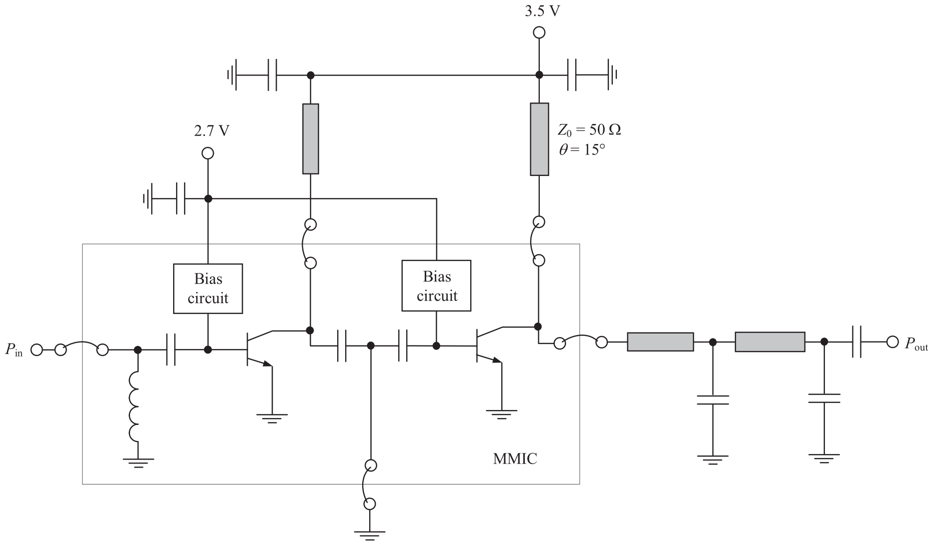


FIG. 9.27

Circuit schematic of parallel-circuit GaAs HBT Class-E MMIC power amplifier.

In this case, a very short microstrip line operating as a DC-feed inductance is required to approximate parallel-circuit Class-E switching conditions.

Fig. 9.28A shows that the small-signal gain varies within 22.5 ± 0.5 dB and the input return loss is greater than 13 dB in a frequency range from 1.6 GHz to higher than 2 GHz, thus confirming the broadband operation of the amplifier. Without any tuning of the output matching circuit, a saturated output power of over 30 dBm and a *PAE* of over 50% were obtained. These single-tone measurements shown in Fig. 9.28B were performed at the corresponding center bandwidth frequencies of 1.75 GHz (DCS band) and 1.88 GHz (PCS band). Using high-*Q* capacitors in output matching circuit can improve the power-added efficiency by about 8%, resulting in a *PAE* close to 60%. At the same time, the power amplifier provides high-linearity performance in a handset WCDMA band (1920–1980 MHz) at a 3.5-dB backoff output power of 27 dBm with a power gain of 22.6 dB and a sufficiently high efficiency. The measured *PAE* reached a value of 38.3% at center bandwidth frequency of 1.95 GHz with an *ACLR* of −37 dBc at a 5-MHz offset and *ACLR* of −56 dBc at a 10-MHz offset.

9.5 High-power RF Class-E power amplifiers

The load network of a high-power broadband VHF Class-E power amplifier can be based on lumped low-pass *LC* matching sections to match the nominal Class-E load with the standard 50-Ω load. When the frequency bandwidth is not very wide, of about 50%, it is possible to use the simplest single-section low-pass Π-transformer to provide a drain efficiency greater than 60% over a frequency bandwidth from 80 to 135 MHz with an average output power of 20 W using a 28-V 60-W SiC MESFET device.[32] However, variation of both the output power (>3 dB) and drain efficiency (>15%) across this

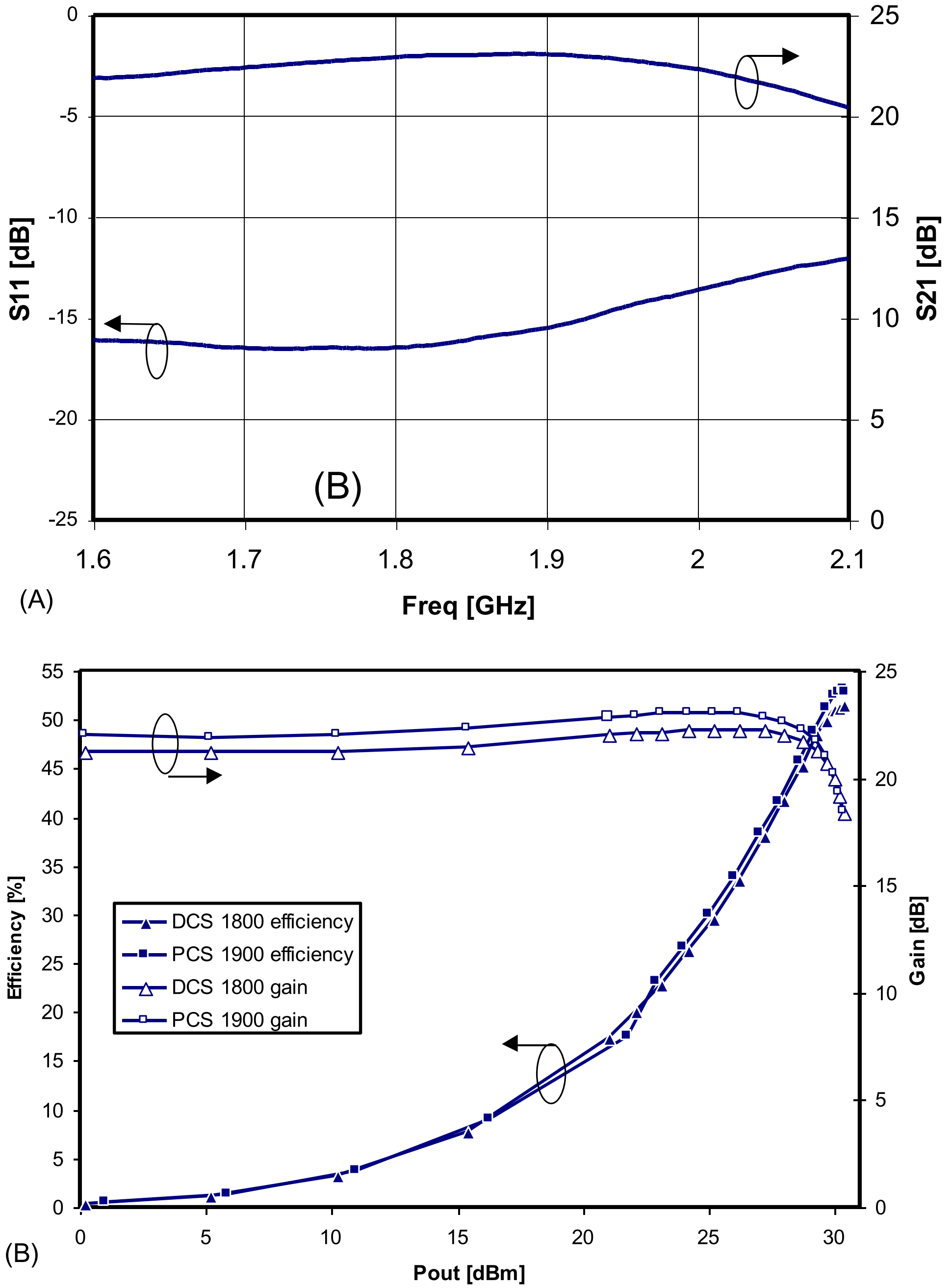


FIG. 9.28

Input return loss, gain, and efficiency versus frequency.

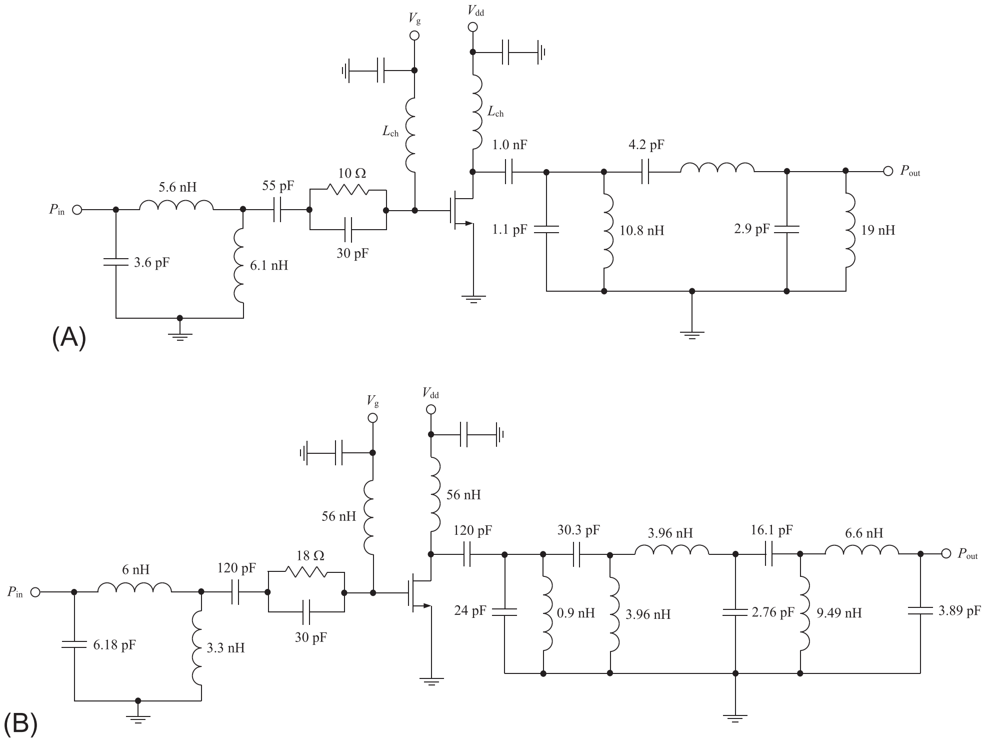

V_g
V_{dd}
L_{ch}
L_{ch}
1.0 nF
4.2 pF
P_{out}
10 Ω
5.6 nH
55 pF
P_{in}
1.1 pF
10.8 nH
2.9 pF
19 nH
30 pF
3.6 pF
6.1 nH
(A)
V_g
V_{dd}
56 nH
56 nH
120 pF
30.3 pF
3.96 nH
16.1 pF
6.6 nH
P_{out}
18 Ω
6 nH
120 pF
P_{in}
24 pF
0.9 nH
3.96 nH
2.76 pF
9.49 nH
3.89 pF
30 pF
6.18 pF
3.3 nH
(B)

FIG. 9.29

Circuit schematics of broadband UHF power amplifier with double-reactance compensation.

frequency bandwidth is significant, because such a simple load network cannot maintain the required real and imaginary parts of the Class-E load network constant enough over the entire frequency range. In this case, the imaginary part of the load network increases from a low-band frequency to a high-band frequency, characterized by the positive slope.

Fig. 9.29A shows the circuit schematic of broadband UHF power amplifier with double-reactance compensation using an NPTB00025 transistor representing a 25-W GaN HEMT on Si device.[33] Here, the corresponding load impedance for optimal wideband Class-E operation was found to be approximately 34 Ω. Therefore, instead of adding an additional matching section, the value of the load network was optimized to provide simultaneously the load-network angle of around 49 degrees, being almost flat with variation of only a few degrees, and impedance matching with a 50-Ω load over the required frequency bandwidth. The close-to-Class-E operation was confirmed by the simulated drain voltage and current waveforms. The input matching network was realized by cascading low-pass and high-pass L-type matching sections. As a result, an output power of 10 W was achieved with a *PAE* better than 70% over the frequency bandwidth of 480–730 MHz.

At the same time, very high efficiency at UHF frequencies can be achieved using an LDMOSFET device, which can significantly reduce cost and improve reliability. In this case, because the maximum switching frequency $f_{\max}$ is much lower than the operating frequency due to higher value of the output capacitance $C_{\text{out}} = C_{\text{ds}} + C_{\text{gd}}$, where C_{ds} is the drain-source capacitance and C_{gd} is the gate-drain capacitance, the suboptimum Class-E mode should be used to achieve high efficiency well above $f_{\max}$. The suboptimum Class-E mode also reduces the peak drain voltage, making it much smaller than obtained in a nominal Class-E. Fig. 9.29B shows the circuit schematic of a broadband UHF power amplifier with double-reactance compensation using a BLF642 transistor representing a 35-W LDMOSFET device.[34] Here, an additional two-stage output matching network based on a bandpass filter structure is used to transform the desired load impedance of 24 Ω to the 50-Ω load. The resistor of 18 Ω and capacitor of 30 pF connected in parallel are used in the input circuit to provide stable operation condition. The inductors in the input circuit and load network are implemented in a PCB as narrow microstrip lines. As a result, a *PAE* greater than 70% with an output power of 10 W was achieved across the frequency bandwidth of 470–780 MHz.

Fig. 9.30 shows the circuit schematic of a push-pull Class-E power amplifier using a 50-V balanced (gemini) MOSFET device, producing an output power up to 200 W and operating in a frequency range from 1.8 to 128 MHz.[35] The circuit incorporates a broadband input matching circuit so that the frequency changes require only retuning or switching of the output filter. In this case, the drain efficiency varies from 90% at 1.8 MHz to 70% at 128 MHz. The input signal is transformed and split by a broadband 4:1 Guanella transformer, whose outputs represent two 10-W 6.25-Ω resistors shunting the MOSFET gates and providing the required resistive loads for the input transformer. Such an input circuit is operated in a broadband mode until the reactances of the MOSFET gates become less than 6.25 Ω. Operation at higher frequencies requires the addition of inductors to cancel the MOSFET gate capacitances. The drain loads of 3.125 Ω in a Class-E mode with shunt capacitance allow about 100 W to be produced in each side of the MOSFET with a peak drain voltage below the breakdown voltage. The total drain capacitance is approximately correct for optimum Class-E operation at about 85 MHz. At lower frequencies, the drain shunt capacitors C_1 and C_2 are therefore added to achieve optimum Class-E operation. The broadband output transformer represents a balun that splits its 6.25-Ω load into two 3.125-Ω drain loads. The output impedance-transforming filter is a low-pass two-section ladder-type network, where the shunt variable capacitors C_3 and C_4 are responsible for load control and efficiency adjustment and the first series inductor provides sufficient reactance to ensure adequate suppression of the third harmonic. In this case, the power amplifier is operated in a suboptimum Class-E mode when the drain voltage waveforms approximate the idealized Class-E

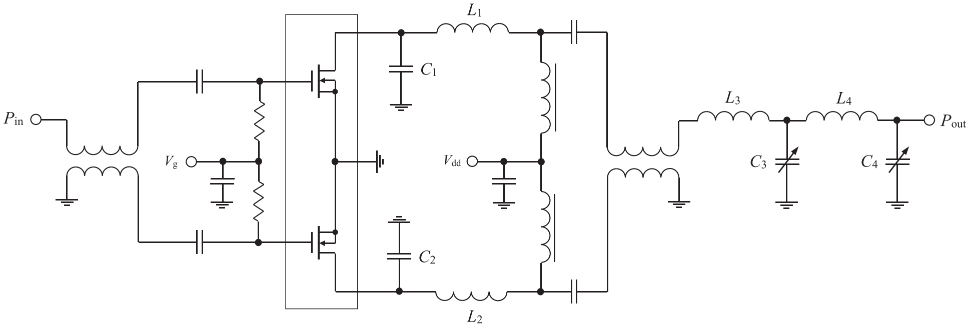


FIG. 9.30

Push-pull MOSFET Class-E power amplifier and drain-voltage waveforms.

waveforms across the entire frequency range.[35] Using two cells of high-power GaN HEMTs CGH40180PP in a balanced package, the power amplifier in a balanced configuration with two 3-dB hybrids could deliver an output power up to 180 W with a drain efficiency of over 80% and a *PAE* of over 75% from 900 to 1400 MHz when operating in a suboptimum Class-E mode.[36]

The third-order bandpass broadband Class-E load network can be optimized to provide not only the required optimum inductive impedance at the fundamental frequency, but also purely capacitive optimized reactances at the second and third harmonics. Fig. 9.31A shows such a third-order parallel-circuit Class-E load network, where the impedance-transforming network is used to transform the standard 50-Ω load to the load required for proper termination of the Class-E load network.[37] As a result, a drain efficiency near 70% and better can be achieved over the frequency bandwidth from 95 to 135 MHz for a 12-W 12-V MOSFET power amplifier with a 4:1 Ruthroff transmission-line transformer in an impedance-transforming network providing 12.5 Ω to the Class-E load network at a fundamental and several higher-order harmonics. Fig. 9.31B shows the output circuit of a high-power broadband 28-V LDMOSFET power amplifier with a broadband low-loss impedance transformer connected to the

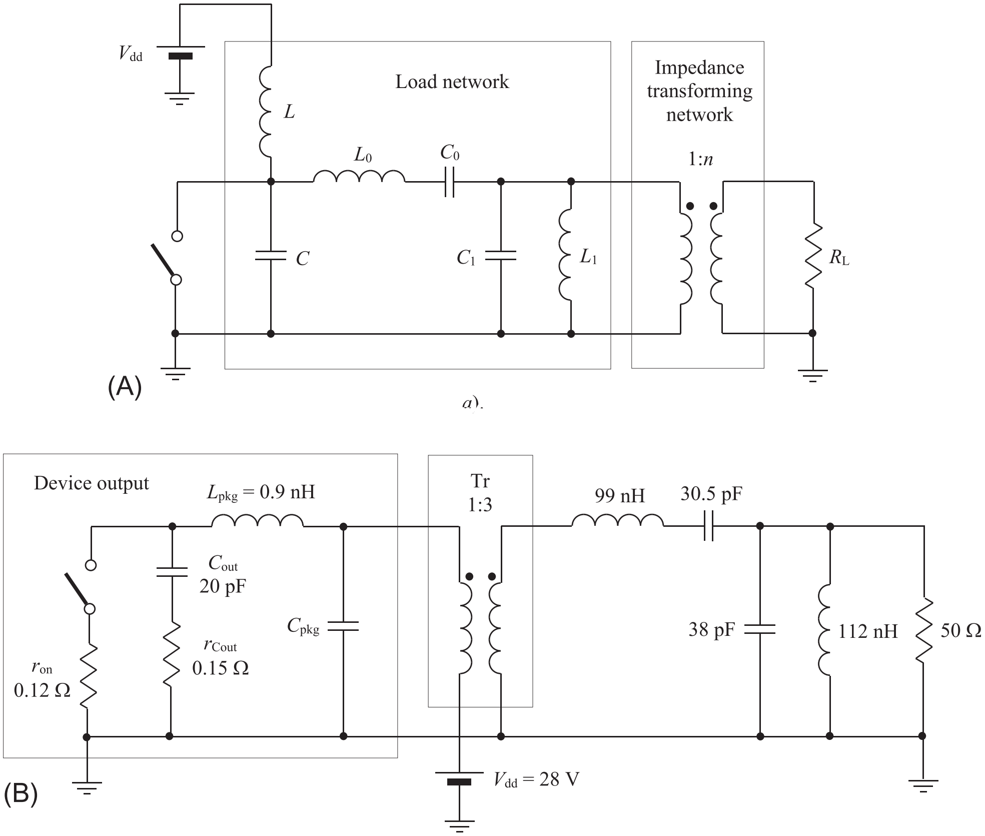

V_{dd}
Load network
L
L_0
C_0
Impedance transforming network
1:n
C
C_1
L_1
R_L
(A)
a).
Device output
L_{pkg} = 0.9 nH
Tr
1:3
99 nH
30.5 pF
C_{out}
20 pF
C_{pkg}
r_{Cout}
0.15 Ω
r_{on}
0.12 Ω
38 pF
112 nH
50 Ω
(B)
V_{dd} = 28 V

FIG. 9.31

Output circuits of broadband VHF Class-E power amplifiers.

output port of the power transistor.[38] The transformer is made of three rings of a 15-Ω semirigid coaxial cable, where the cable outer jackets are connected in parallel to form the primary of the transformer and the inner conductors are connected in series to form the secondary of the transformer. In order to reduce losses to minimum, no magnetic core is used. A lumped passband network is located after the transformer to provide proper loads at both the harmonics and the fundamental frequency for a nominal Class-E with shunt capacitance. In this case, high drain efficiencies of up to 86% with output powers of greater than 120 W were measured in a frequency bandwidth of VHF broadcasting from 88 to 114 MHz.

Fig. 9.32A shows the test board of a broadband high-power push-pull power amplifier based on a balanced 65-V 1.8-kW MRFX1K80H device using two LDMOS cells in a single package. To maximize the drain efficiency, a parallel-circuit Class-E mode was used to conveniently implement the required parallel inductor using the effect of virtual grounding when a thick bonding wire with a total

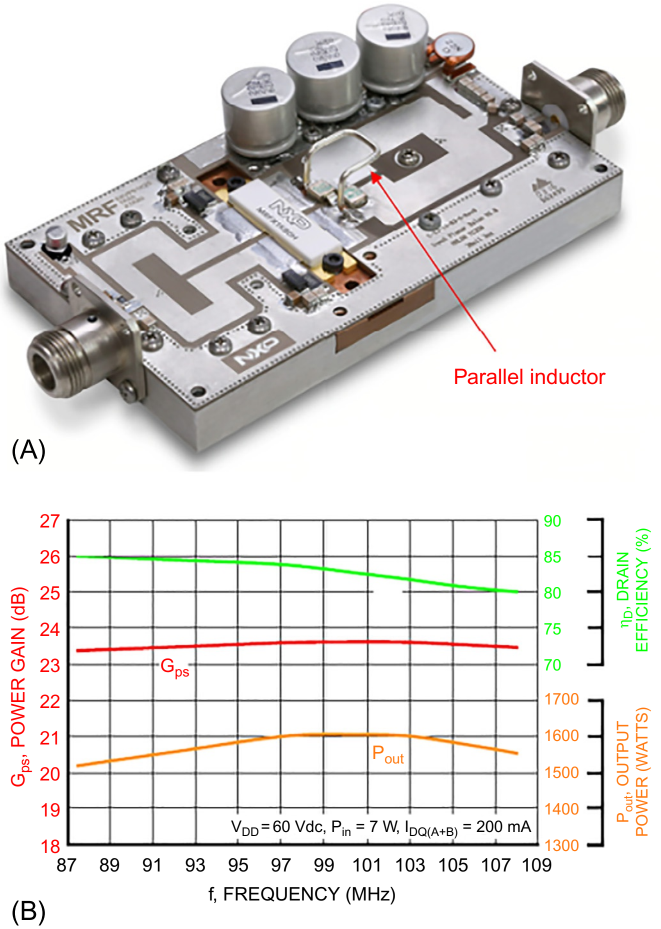


FIG. 9.32

Test board and performance of high-power VHF FM LDMOSFET power amplifier.

length of 43 mm is connected directly between two drains. As a result, an output power greater than 1.5 kW with a drain efficiency of 80%–85% and a power gain of about 23.5 dB was achieved over the entire VHF FM band of 87.5–108 MHz in a continuous-wave (CW) mode, as shown in Fig. 9.32B.[39]

9.6 Microwave monolithic Class-E power amplifiers

Generally, by providing an open-circuit termination for the second- and third-harmonic components, the collector efficiency of a microwave Class-E power amplifier can be increased by 10%.[40] In this case, the second-harmonic termination has the highest impact on the collector efficiency, whereas effect of an open-circuit termination for the fourth harmonic is negligible. Moreover, the variation of the second-harmonic load reflection coefficient by 10% in magnitude from 1.0 to 0.9 and ±20 degrees in phase angle results in an insignificant efficiency variation within 1% only. Fig. 9.33A shows the circuit

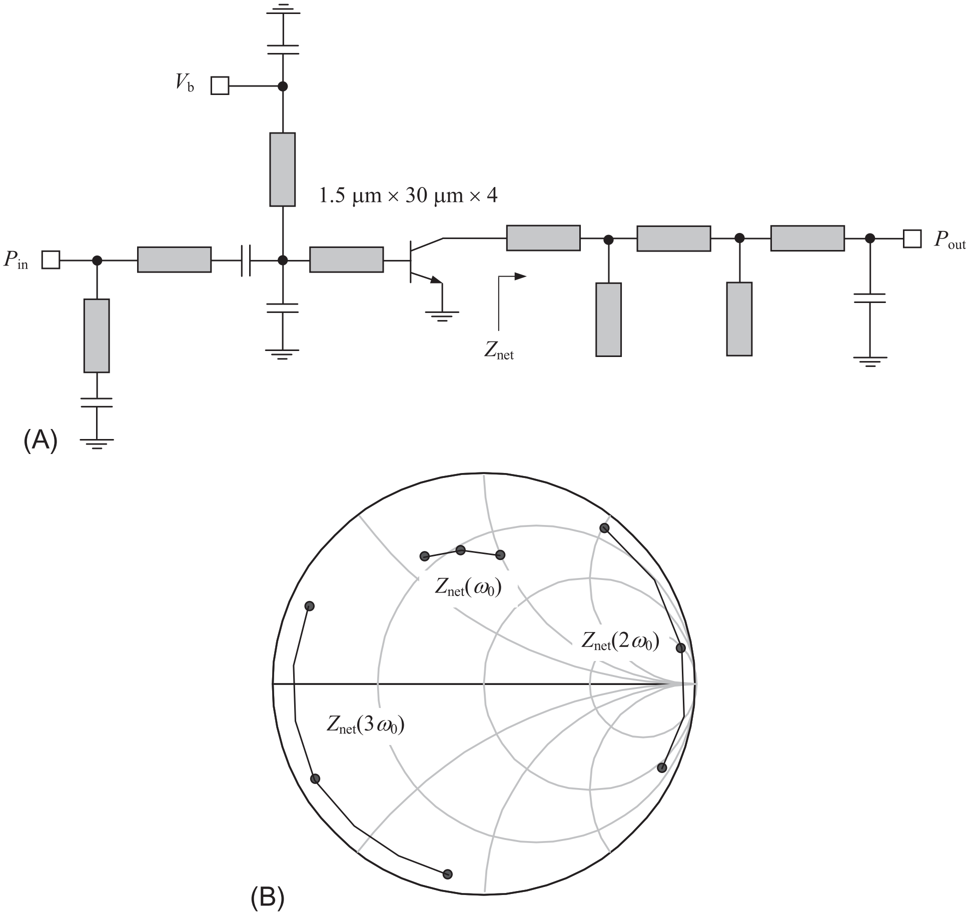


FIG. 9.33

Broadband *X*-band In DHBT Class-E power amplifier and impedance conditions.

schematic of a monolithic broadband Class-E power amplifier with a chip size of 2 × 2.2 mm^2. The load network is a compromise solution between having a low insertion loss and meeting the necessary requirements for the optimum Class-E operation with nonzero voltage and voltage-derivative switching conditions.[41] This is accomplished using two open-circuit stubs in conjunction with a shunt capacitor, where the first open-circuit stub in combination with the series transmission line presents broadband high-impedance terminations for the second harmonics within 18–22 GHz, whereas the combination of the second open-circuit stub and the shunt capacitor presents broadband low impedances at the third harmonics within 27–33 GHz and also transforms the optimum load impedances at the fundamental frequencies. The simulated loading conditions presented to the output of the device at the fundamental (inductive impedance), second (high impedance), and third harmonic (low impedance) frequencies are shown in Fig. 9.33B, which are proven to be adequate for broadband Class-E power amplifiers. As a result, using an indium phosphide (InP) double HBT (DHBT) technology, a *PAE* of 49%–65% with an output power of 18–22 dBm was achieved over the frequency bandwidth from 9 to 11 GHz.[40] Based on an InP DHBT technology, a single-stage broadband *X*-band Class-E power amplifier can also achieve a *PAE* of 45%–60% with an output power of 19–21.5 dBm and a power gain of 9–11.5 dB over a 34% bandwidth from 8.2 to 11.6 GHz.[42]

To increase the overall efficiency of a two-stage power amplifier, it may be assumed that it is worthwhile to optimize both amplifying stages to operate in a Class-E mode. For example, for a hybrid microwave GaAs MESFET Class-E power amplifier using the same devices in both stages, the maximum two-stage PAE was achieved as high as 52% (including connector loss) with a corresponding power gain of 16 dB and an output power of 20 dBm at a carrier frequency of 10 GHz and a DC-supply voltage of 4.2 V.[43] However, due to Class-E operation mode of the driver stage, the overall power gain is sufficiently small, thus affecting the overall efficiency. Therefore, using a Class-AB driver stage, similar efficiency can be achieved with a substantially higher power gain. As a result, for a monolithic microwave two-stage high-efficiency InP DHBT power amplifier shown in Fig. 9.34A, where the driver stage is operated in a Class-AB mode and the output stage is operated in a Class-E mode, a *PAE* of 52% with an output power of 24.6 dBm and a power gain of 24.6 dB was achieved at an operating frequency of 8 GHz and a DC-supply voltage of 4 V. The total emitter area of the driver-stage device was chosen to be 90 μm^2, providing a *PAE* of the driver stage above 40% and an adequate power to push the output stage deep into compression, as required for a switchmode Class-E operation. The output stage consists of two active devices with a total emitter area of 360 μm^2 combined in parallel reactively, with odd-mode instability suppression resistors between the base and collector of each transistor. The *PAE* is maintained at a value higher than 40% over a frequency bandwidth from 7.7 to 10.5 GHz, as shown in Fig. 9.34B.[43]

Fig. 9.35 shows the circuit schematic of a two-stage broadband Class-E power amplifier implemented in a 0.5-μm enhancement/depletion pHEMT process with a chip size of 2 × 2 mm^2, which is intended to operate in a frequency range from 1.5 to 3.8 GHz with a *PAE* better than 62% and an output power over 27 dBm at $V_{dd} = 6$ V.[44] In this case, to provide high operation efficiency in a wide frequency range, the Class-E load network with reactance-compensation technique followed by the low-pass matching network is used. The driver stage is designed to operate in a Class-AB mode with a small quiescent current for high gain and high efficiency when both input and interstage matching circuits are conjugately matched. For a 0.5-μm pHEMT two-stage broadband Class-E power amplifier with a chip size of 5.25 × 2.8 mm^2, a *PAE* above 50% with an output power over 36 dBm at a drain supply voltage of 6 V was obtained in a frequency range from 3.0 to 3.75 GHz.[45]

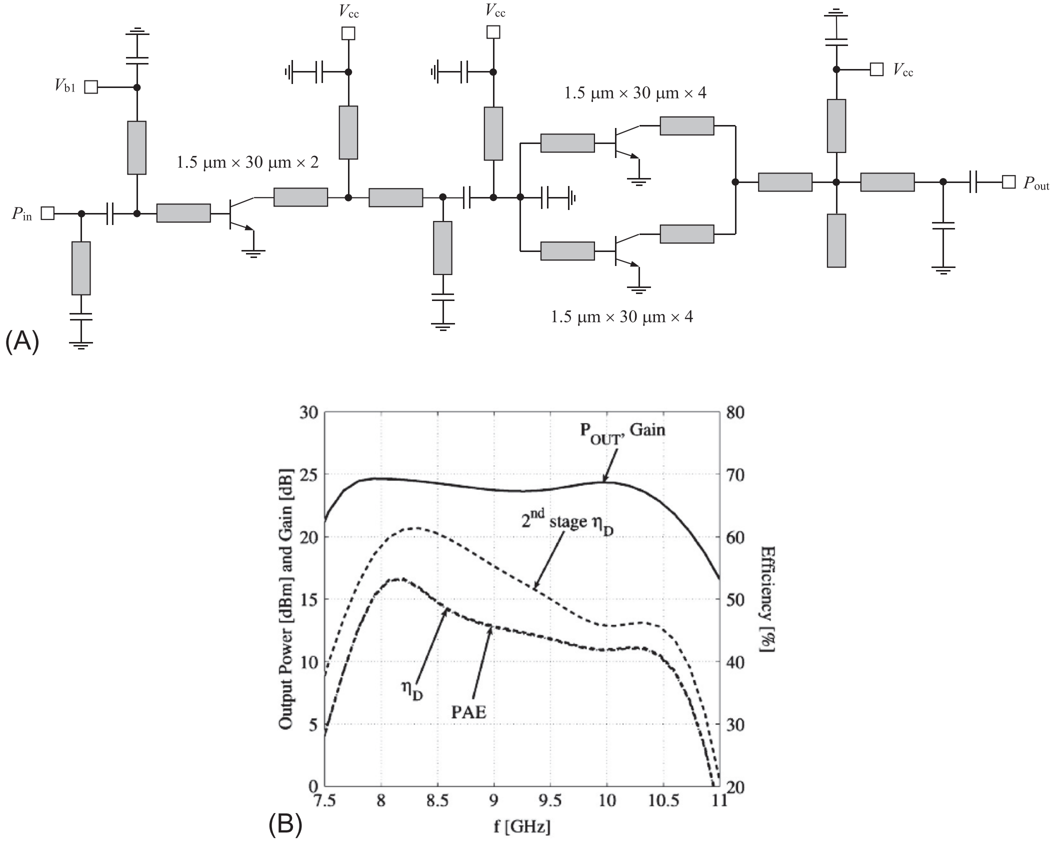

V_{cc}
V_{cc}
V_{b1}
V_{cc}
1.5 µm × 30 µm × 4
1.5 µm × 30 µm × 2
P_{in}
P_{out}
1.5 µm × 30 µm × 4
(A)
30
25
20
15
10
5
0
80
70
60
50
40
30
20
P_{OUT}, Gain
2^{nd} stage η_D
η_D
PAE
Output Power [dBm] and Gain [dB]
Efficiency [%]
7.5
8
8.5
9
9.5
10
10.5
11
f [GHz]
(B)

FIG. 9.34

Broadband two-stage *X*-band In DHBT Class-E power amplifier and its performance.

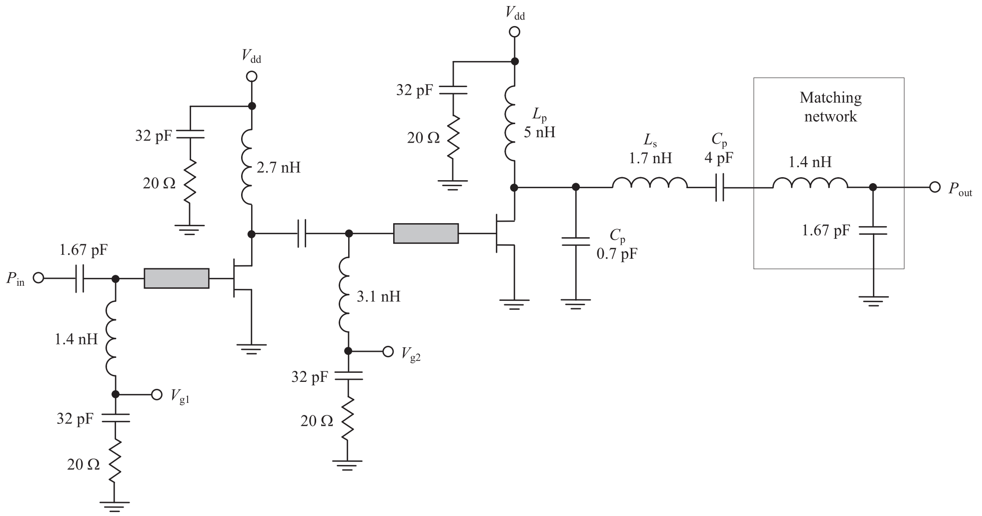

V_{dd}
V_{dd}
32 pF
20 Ω
L_p
5 nH
Matching network
32 pF
20 Ω
2.7 nH
L_s
1.7 nH
C_p
4 pF
1.4 nH
P_{out}
1.67 pF
P_{in}
C_p
0.7 pF
1.67 pF
3.1 nH
1.4 nH
V_{g2}
32 pF
V_{g1}
32 pF
20 Ω
20 Ω

FIG. 9.35

Circuit schematic of broadband Class-E pHEMT power amplifier.

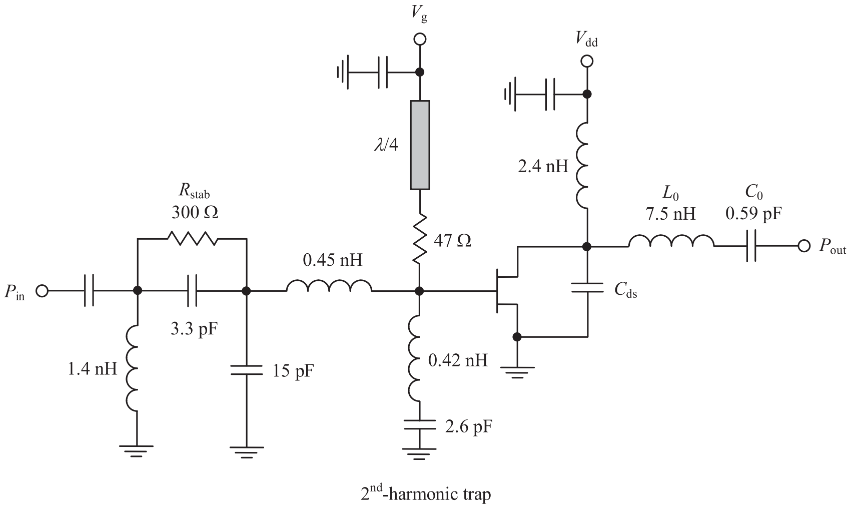


FIG. 9.36

Circuit schematic of broadband Class-E GaN HEMT power amplifier.

Fig. 9.36 shows the circuit schematic of a compact single-stage broadband Class-E GaN HEMT power amplifier, where the load network is based on reactance-compensation technique with a parallel circuit followed by the low-Q series resonant circuit.[46] The use of a finite DC-feed inductance has advantages in terms of the output power and maximum frequency of operation and results in a higher load resistance than that in the classical Class-E configuration with infinite RF choke. To shape the gate voltage waveform, the second-harmonic signal is short-circuited at the gate by the series resonant circuit representing a second-harmonic trap. The high- and low-pass matching sections form a bandpass input matching circuit, where a 300-Ω parallel resistor with a 37-Ω bias resistor provide an unconditional stability of the power amplifier at both low and high frequencies. The actual size of a broadband Class-E power amplifier with the input matching circuit and load network implemented in a bilayer Rogers laminate with a dielectric permittivity of 3.5 is only $1.1 \times 1.6\,\text{cm}^2$. As a result, a drain efficiency above 74% and an output power over 7 W with an input power of 600 mW at $V_{dd} = 40\,\text{V}$ was achieved across the frequency bandwidth of 2.0–2.5 GHz. A wider frequency bandwidth of 2.1–2.7 GHz with a drain efficiency exceeding 63% and an output power above 9.3 W can be provided without input of the second-harmonic trap and retuning of the finite DC-feed inductance. Using a two-section LC ladder output matching circuit in a GaN HEMT Class-E power amplifier, a drain efficiency of over 68% with an output power of 42–65 W in a frequency bandwidth from 1.7 to 2.3 GHz at a supply voltage of 35 V was achieved for a compact hybrid implementation of the power amplifier with effective area of $2 \times 2\,\text{cm}^2$, where the bondwire inductors and MIM capacitors are used.[47]

9.7 CMOS Class-E power amplifiers

The use of cascode topologies is extremely attractive for CMOS power amplifiers, especially at high output powers and DC-supply voltages. Optimization of the cascode topology shown in Fig. 9.37A requires setting the bias voltage V_g of the common-gate transistor to minimize the voltage drop across the oxide of each transistor, M_1 and M_2, when these voltage drops become equal, allowing the use of

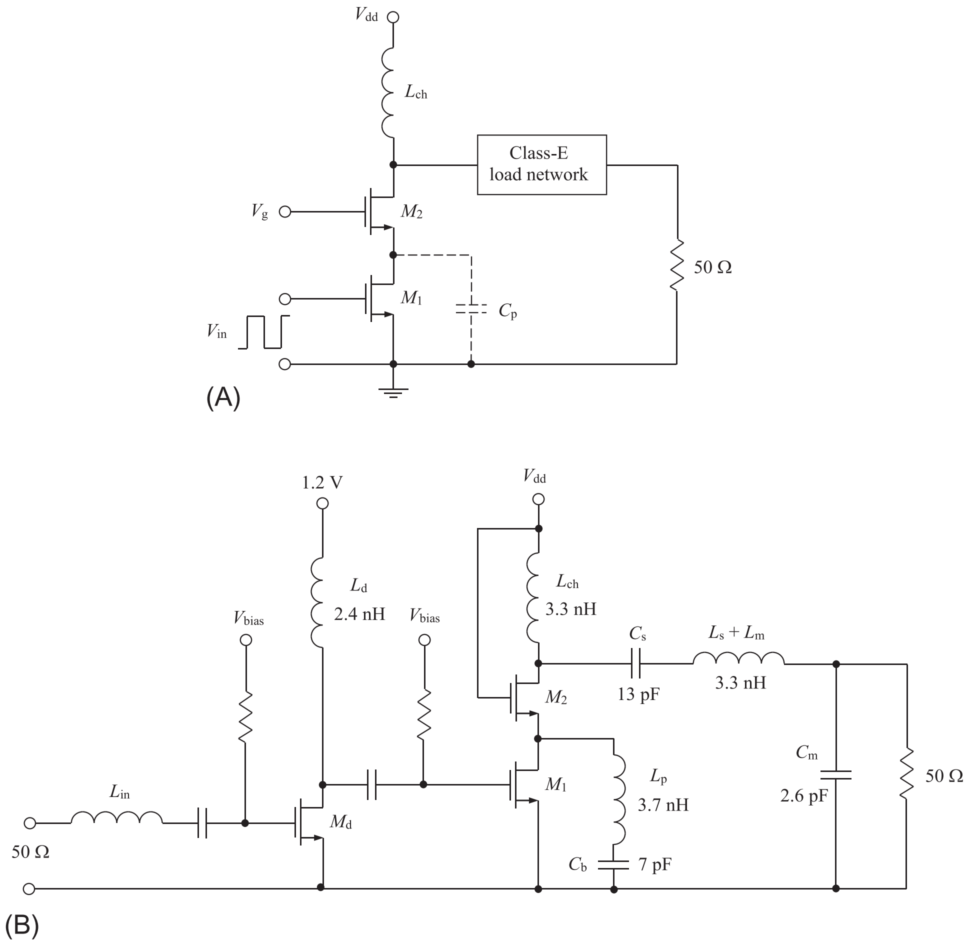

V_{dd}
L_{ch}
Class-E load network
V_g
M_2
M_1
C_p
V_{in}
50 Ω
(A)
1.2 V
V_{dd}
L_d
2.4 nH
V_{bias}
V_{bias}
L_{ch}
3.3 nH
C_s
$L_s + L_m$
13 pF
3.3 nH
M_2
C_m
L_p
3.7 nH
2.6 pF
50 Ω
L_{in}
M_1
M_d
50 Ω
C_b
7 pF
(B)

FIG. 9.37

Broadband cascode Class-E power amplifier with compensating inductor.

approximately twice the supply voltage.[48, 49] However, there is an additional power loss mechanism as a specific property of a cascode configuration in a switching Class-E mode when the common-source device M_1 is turned off, which is associated with charging and discharging processes of the shunt parasitic capacitor C_p, consisting of the drain-bulk capacitance of the device M_1 and gate-source and source-bulk capacitances of the device M_2. This results in a finite switching time of the common gate device M_2 when it cannot be instantly switched from the saturation mode to the pinch-off mode and operates in the active region when simultaneously output current and output voltage are positive with the output power dissipation within the device. The parasitic capacitance C_p can be three to four times larger than the drain-bulk capacitance of the device M_2, resulting in a power loss as large as 20% of the output power. A simple and effective way to minimize this power loss contribution is to use a parallel inductor L_p resonating the parasitic capacitor C_p at the operating frequency, as shown in Fig. 9.37B, where C_b is the blocking capacitor. The series resonant circuit required to provide a sinusoidal current flowing to the load is replaced by the series inductor L_m and shunt capacitor C_m, forming a low-pass L-type lumped transformer to match the optimum Class-E load resistance with a standard resistance of 50 Ω. As a result, the two-stage cascode Class-E power amplifier with a compensating inductor implemented in a 0.13-μm CMOS process achieved a drain efficiency of 71% and a *PAE* of 67% when delivering an output power of 23 dBm at an operating frequency of 1.7 GHz with a DC-supply voltage of 2.5 V. The driving stage with a DC-supply voltage of 1.2 V is biased in a Class-C. The value of an inductor L_d is chosen to compensate for the gate-source capacitance of the device M_1. The *PAE* above 60% was measured over the frequency bandwidth of 1.4–2.0 GHz.

To realize the broadband high-efficiency operation of the fully-integrated CMOS Class-E power amplifier, a broadband and low-loss 1:4 Ruthroff-type transmission-line transformer based on the broadside-coupled transmission lines can provide an impedance transformation from 12.2 ± 0.1 Ω to 50 Ω over a wide frequency range.[50] In a six-layer 0.18-μm CMOS process, the thickest top metal 6 is used as the primary winding, the identical thick metal stacked from metal 1 to metal 4 is used as the secondary winding to improve insertion loss, and both windings are wound in loops keeping the 1:1 turns ratio to reduce the transformer size. Fig. 9.38A shows the circuit schematic of a 0.18-μm CMOS Class-E power amplifier composed of the two nMOS transistors in a cascode configuration and one shunt capacitor in the load network required for optimum Class-E operation. Here, the series *LC* resonant circuit at the fundamental frequency of the Class-E power amplifier is replaced by the 1:4 transmission-line transformer operating as a broadband bandpass filter. To enhance the reliability of the transistors, the thick-oxide transistor M_2 is used for the common-gate stage, and the thin-oxide transistor M_1 is used for the common-source stage. The fully integrated CMOS Class-E power amplifier with a 1:4 transmission-line transformer exhibits a broadband and flat output power level of 24 ± 0.2 dBm from 2.4 to 3.5 GHz at a DC-supply voltage of 3.6 V, with a maximum *PAE* of 33.2% at 2.6 GHz.

Fig. 9.38B shows the circuit schematic of a two-stage broadband Class-E CMOS power amplifier, where the power output stage is formed by a high-voltage, extended-drain, thick-oxide nMOS device implemented in a standard 65-nm CMOS technology.[51] The total gate width of the transistor is 3.84 mm with a channel length of 0.28 μm, realizing an on-resistance of 0.7 Ω, an off-resistance of 10 kΩ, and a drain-source capacitance of approximately 4.14 pF. To drive the output stage as a switch, a square-wave signal is generated by an inverter-based driver implemented using standard thick-oxide MOS devices with a gate length of 0.28 μm. To reduce the peak drain voltage and improve operation reliability, a suboptimum Class-E operation is applied. The broadband load network represents an off-chip two-section *LC* ladder circuit. As a result, a measured output power of 30.5 ± 0.5 dBm, a power gain of 16.5 ± 0.5 dB, a drain efficiency above 67%, and a *PAE* above 52% are achieved across the frequency bandwidth from 550 to 1050 MHz.

Fig. 9.39 shows the simplified schematic of a push-pull Class-E power amplifier implemented in a 90-nm CMOS technology.[52] Using a parallel-circuit load for each transistor with optimum Class-E parameters to provide a broadband high-efficiency operation and differential topology to suppress even harmonics, the high operation efficiency over wide band and simple overall circuit implementation can be obtained. Here, the load network is combined with an on-chip lumped differential-to-single-ended balun, and the device drain-source capacitances C_ds1 and C_ds2 are included in the load network as parts of the parallel circuits consisting of L_3, C_3 and L_4, C_4, respectively. The measured results demonstrated

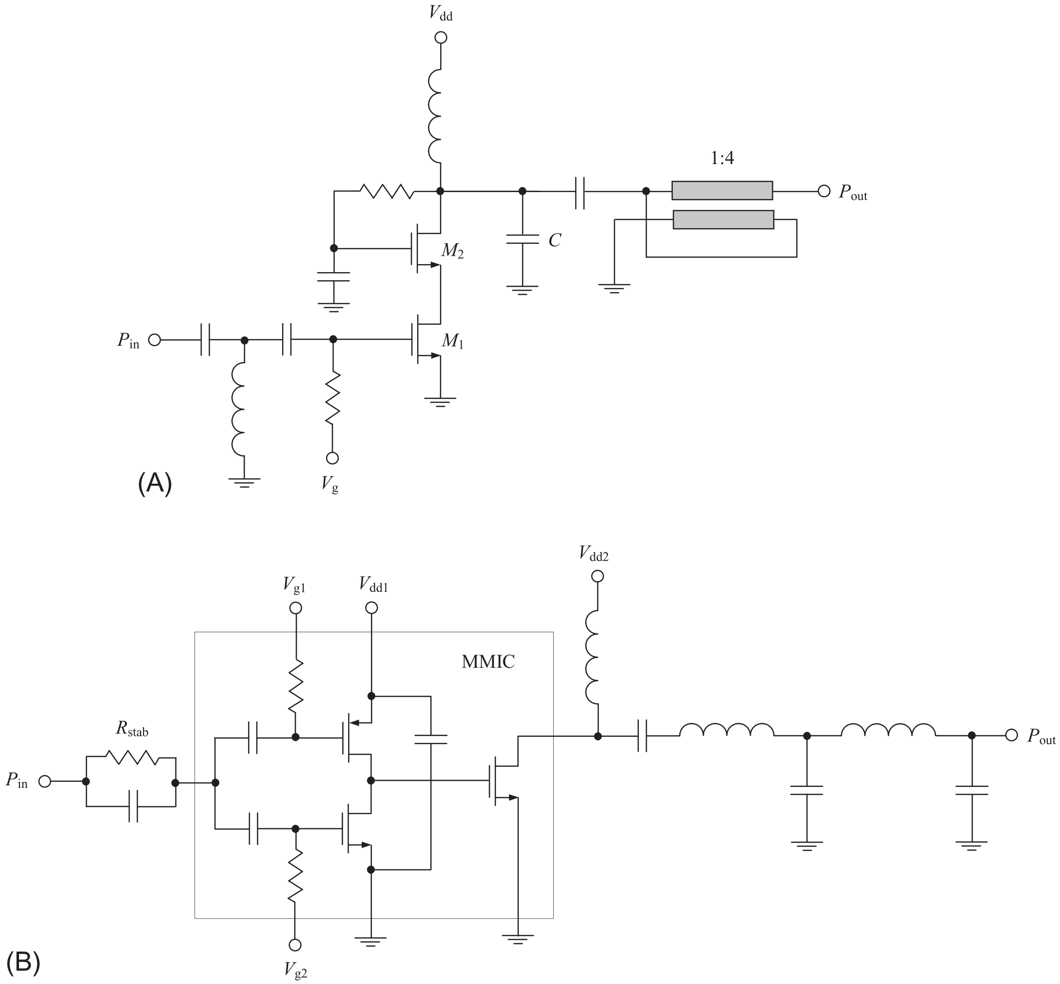


FIG. 9.38

Circuit schematics of broadband Class-E CMOS power amplifiers.

a peak power of 28.7 dBm, a drain efficiency of 55%, and a *PAE* of 48% at 2.3 GHz with a DC-supply voltage of 2.5 V. At the same time, a *PAE* over 42% and an output power over 25 dBm were measured in a frequency bandwidth of 1.7–2.7 GHz.

CMOS power amplifier technology can be used to design broadband low-cost and high-efficiency power amplifiers for modern 4G/5G LTE handset transmitters. Such a technology becomes very attractive in view of current availability of high-resistivity silicon substrates (above 1 kΩcm) to minimize substrate resistive losses and through silicon vias (TSVs) that connect the front-side metallization of the die to the backside ground metal and provide a low impedance path to the common ground plane and a good thermal conductor. Fig. 9.40A shows the simplified circuit schematic of a broadband two-stage

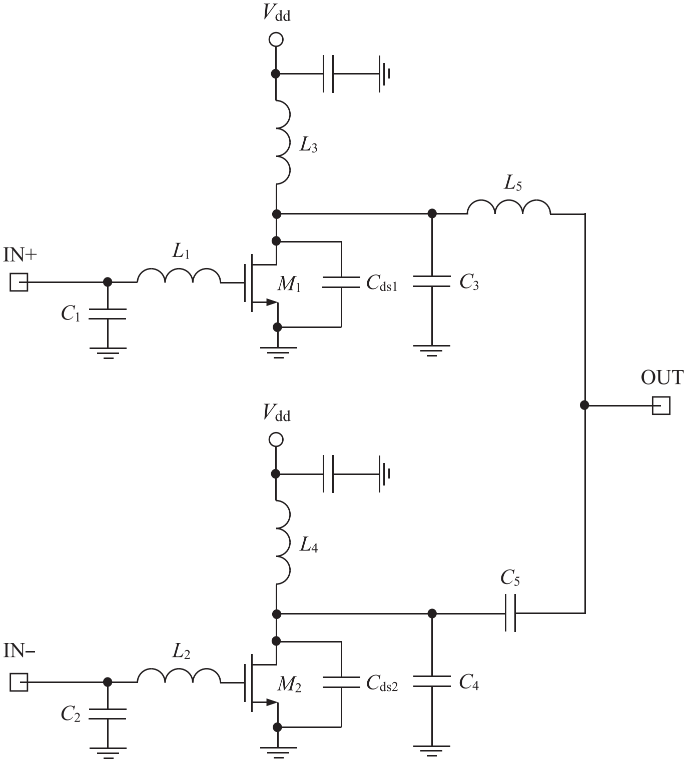


FIG. 9.39

Circuit schematics of push-pull Class-E CMOS power amplifier.

parallel-circuit Class-E power amplifier implemented in a standard 0.18-µm CMOS process, where the third-harmonic trap (RF short to ground) and second-harmonic tank are used to suppress higher-order harmonic components. Both amplifying stages are designed using 1.8 V/3.3 V cascode structures. The use of the low-size common-source 1.8 V transistors for RF drive does help to increase power, the power gain, and *PAE*. The top common-gate transistors are thick-gate 3.3-V devices which handle the high voltage stress. All the power transistors sit in a separate deep n-well to increase linearity by extending the breakdown CMOS region. Here, the fast envelope tracker (ET) block is shown, which can be integrated on the same die with the power amplifier and can operate together with a buck DC/DC converter, providing approximately 20% of the DC-supply power required by the power amplifier. For example, for an output power of 26.5 dBm, the buck DC voltage is set at $V_{dd} = 2.7$ V and provides 80% of the output power with greater than 94% efficiency.[53] This low DC-supply voltage provides protection for CMOS devices, but it does require the power amplifier to operate at low load line. The envelope signal is used to dynamically bias the top cascode device and keeps the main RF transistor in the

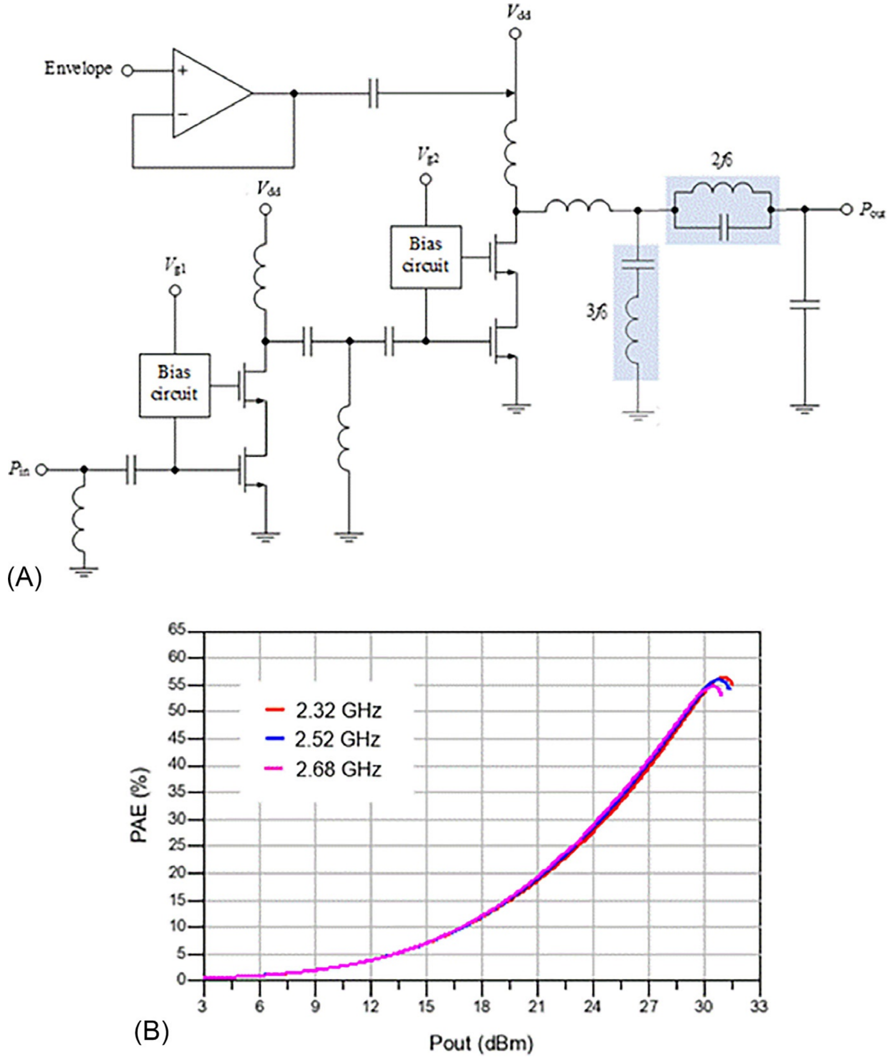

V_{dd}
Envelope
+
−
V_{g2}
$2f_0$
P_{out}
V_{dd}
Bias circuit
V_{g1}
Bias circuit
$3f_0$
P_{in}
(A)
65
60
55
50
45
40
35
30
25
20
15
10
5
0
PAE (%)
2.32 GHz
2.52 GHz
2.68 GHz
3
6
9
12
15
18
21
24
27
30
33
Pout (dBm)
(B)

FIG. 9.40

Circuit schematic and efficiency of broadband two-stage cascode CMOS power amplifier.

approximate constant-g_m region. Generally, the ET system includes a differential amplifier to convert the differential envelope signal into a single-ended one which feeds a linear error amplifier connected to the DC-supply path. Fig. 9.40B shows the simulated *PAE* versus output power at a DC-supply voltage of 3.3 V for three frequencies within the frequency range of 2.3–2.7 GHz where a *PAE* over 50% is achieved at a saturated output power of around 31 dBm.

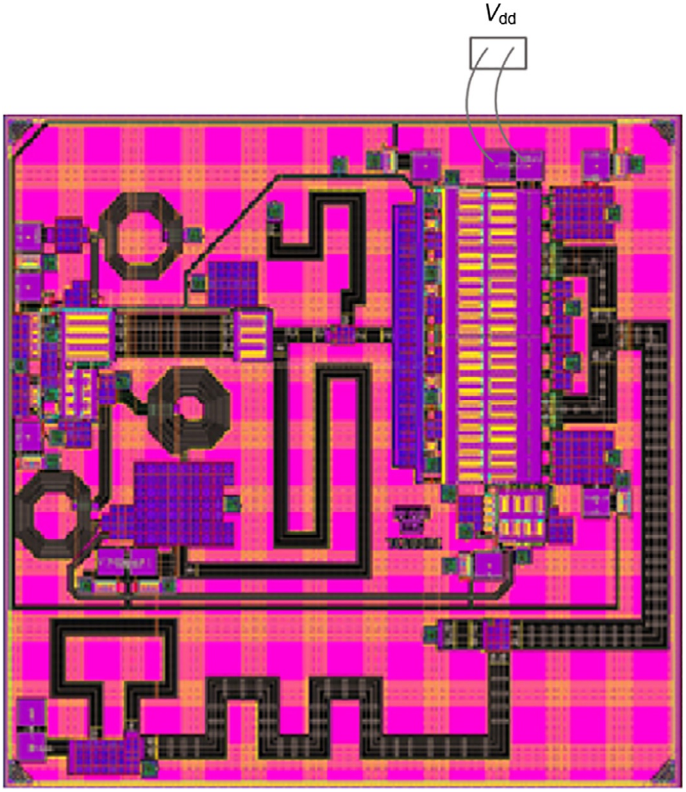
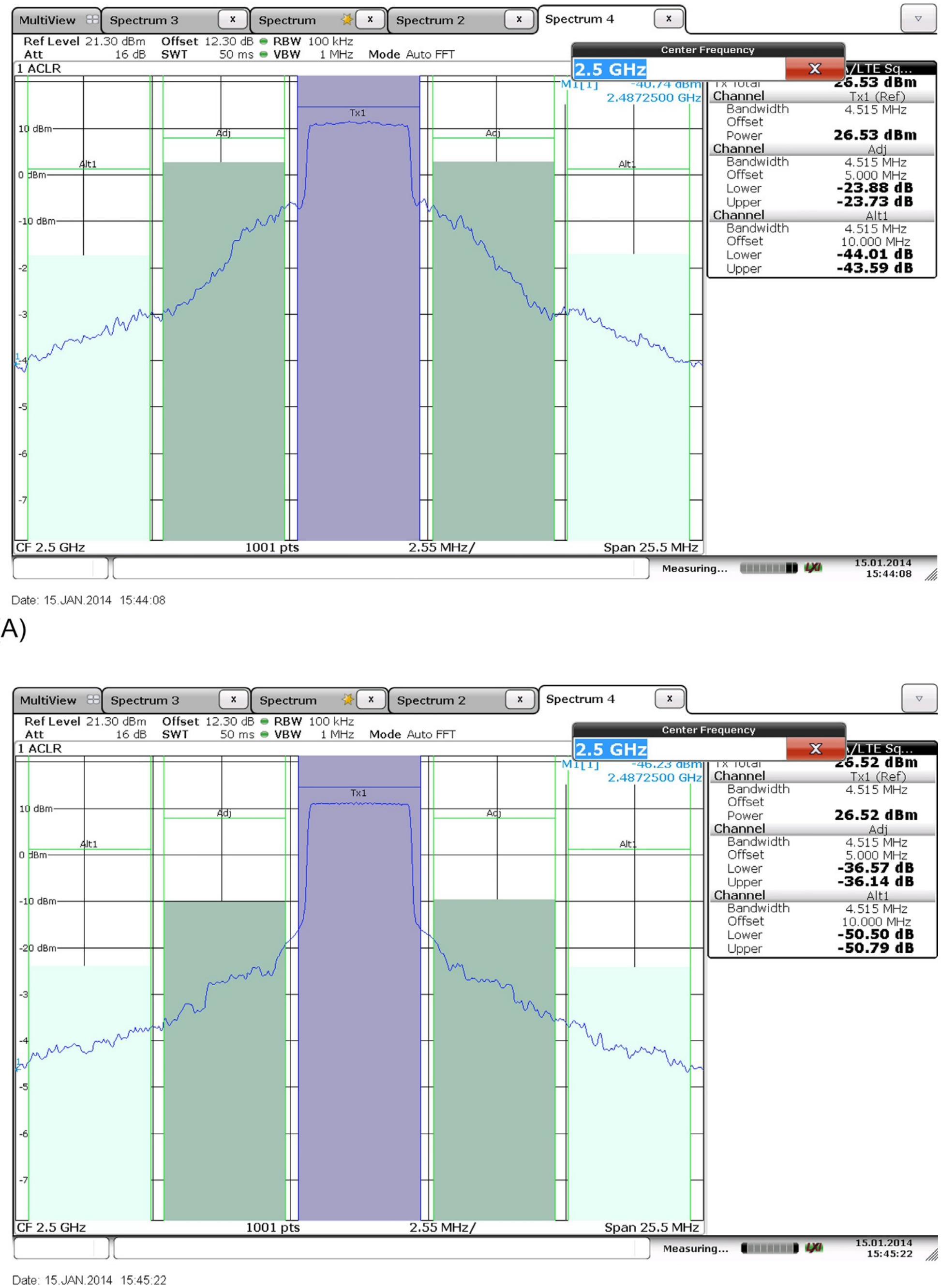


FIG. 9.41

Layout of broadband two-stage cascode CMOS power amplifier.

Fig. 9.41 shows the layout of the broadband two-stage Class-E cascode CMOS power amplifier of size $1.7 \times 1.6\,\text{mm}^2$, where the inductors in the load network are implemented using microstrip lines to minimize power losses and to increase efficiency.[53, 54] Here, the required parallel Class-E inductance is provided by two bondwire inductances in a DC-supply path and a shunt capacitance is fully represented by the output device capacitance. As a result, an average *PAE* of 41.5% and overall (including ET circuit) efficiency of 37% were achieved at a modulated output power of 26.5 dBm for a single-carrier 5-MHz LTE signal, as shown in Fig. 9.42. By proper fixing of the required time delay between the ET and power amplifier paths for envelope signal, a significant linearity improvement was achieved, from an initial level of −23.7 dBc to better than −36 dBc for $ACLR_1$ (improvement by about 13 dB) and from −43.5 dBc to −50.5 dBc for $ACLR_2$ (improvement by 7 dB).


MultiView
Spectrum 3
Spectrum
Spectrum 2
Spectrum 4
Center Frequency
1 ACLR
10 dBm
0 dBm
-10 dBm
-20 dBm
-2
-3
-4
-5
-6
-7
Alt1
Adj
Tx1
Adj
Alt1
/LTE Sq...
Measuring...

Ref Level 21.30 dBm **Offset** 12.30 dB **RBW** 100 kHz
Att 16 dB **SWT** 50 ms **VBW** 1 MHz **Mode** Auto FFT

2.5 GHz

M1[1] -40.74 dBm
2.4872500 GHz

Tx Total 26.53 dBm
Channel Tx1 (Ref)
Bandwidth 4.515 MHz
Offset
Power **26.53 dBm**
Channel Adj
Bandwidth 4.515 MHz
Offset 5.000 MHz
Lower **-23.88 dB**
Upper **-23.73 dB**
Channel Alt1
Bandwidth 4.515 MHz
Offset 10.000 MHz
Lower **-44.01 dB**
Upper **-43.59 dB**

CF 2.5 GHz 1001 pts 2.55 MHz/ Span 25.5 MHz

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(A)

Ref Level 21.30 dBm **Offset** 12.30 dB **RBW** 100 kHz
Att 16 dB **SWT** 50 ms **VBW** 1 MHz **Mode** Auto FFT

2.5 GHz

M1[1] -46.23 dBm
2.4872500 GHz

Tx Total 26.52 dBm
Channel Tx1 (Ref)
Bandwidth 4.515 MHz
Offset
Power **26.52 dBm**
Channel Adj
Bandwidth 4.515 MHz
Offset 5.000 MHz
Lower **-36.57 dB**
Upper **-36.14 dB**
Channel Alt1
Bandwidth 4.515 MHz
Offset 10.000 MHz
Lower **-50.50 dB**
Upper **-50.79 dB**

CF 2.5 GHz 1001 pts 2.55 MHz/ Span 25.5 MHz

15.01.2014
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(B)

FIG. 9.42

Linearity performance of broadband two-stage cascode CMOS power amplifier.

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CHAPTER

Alternative and mixed-mode high-efficiency power amplifiers

10

In this chapter, the different alternative and mixed-mode configurations of high-efficiency power amplifiers (PAs) are presented and discussed. A Class-DE PA is based on the combination of a voltage-switching Class-D mode with Class-E switching conditions, thus extending the switching Class-D operation to higher frequencies. Effects of the saturation resistance and nonlinear capacitance, driving waveforms, and some practical examples of Class-DE PAs are discussed. The switchmode Class-FE or Class-E/F PA can provide lower voltage peak factors when zero voltage and zero voltage-derivative conditions corresponding to Class-E mode, required to eliminate discharge loss of the shunt capacitance, are accompanied by harmonic tuning using the resonant circuits tuned to selected harmonic components realizing Class-F or inverse Class-F mode. Also, the biharmonic Class-E_M mode is described, which can eliminate the efficiency degradation of a Class-E operation mode at higher frequencies due to the increased switching power losses with increasing values of the turn-off switching time. The requirements of both jumpless voltage and current waveforms and sinusoidal load waveform with nonzero output power delivered to the load can be provided by using nonlinear reactive elements in the load network to convert fundamental-frequency power to a desired harmonic frequency or by injecting the harmonic-frequency power into the load network from an external source. An inverse Class-E PA represents an inverse version of a classical Class-E PA with a shunt capacitance where the load-network inductor and capacitor replace each other. Generally, it is limited to low operating frequencies or low output powers since it is based on zero-current and zero current-derivative switching conditions. However, to compensate for the device output capacitor finite discharging process, it is necessary to provide zero voltage-derivative condition at the same time, and collector efficiency will drop drastically if this capacitance is significant. Harmonic-control techniques for designing microwave PAs are given with a description of a systematic procedure of multiharmonic load-pull simulation using the harmonic-balance method and active load-pull measurement system. Finally, outphasing modulation systems are considered where a variable envelope output is created by the sum of two constant-envelope signals with varying phases which, therefore, can be amplified by highly efficient PA operated in a switching Class-D, Class-E, or Class-F operation mode, or their combinations.

10.1 Class-DE PA

The complementary voltage-switching Class-D PA with a series filter, whose equivalent circuit is shown in Fig. 10.1A, has the advantage of a lower voltage peak factor, compared with the current-switching Class-D PAs. The maximum peak factor for the voltage-switching Class-D PA, as a ratio

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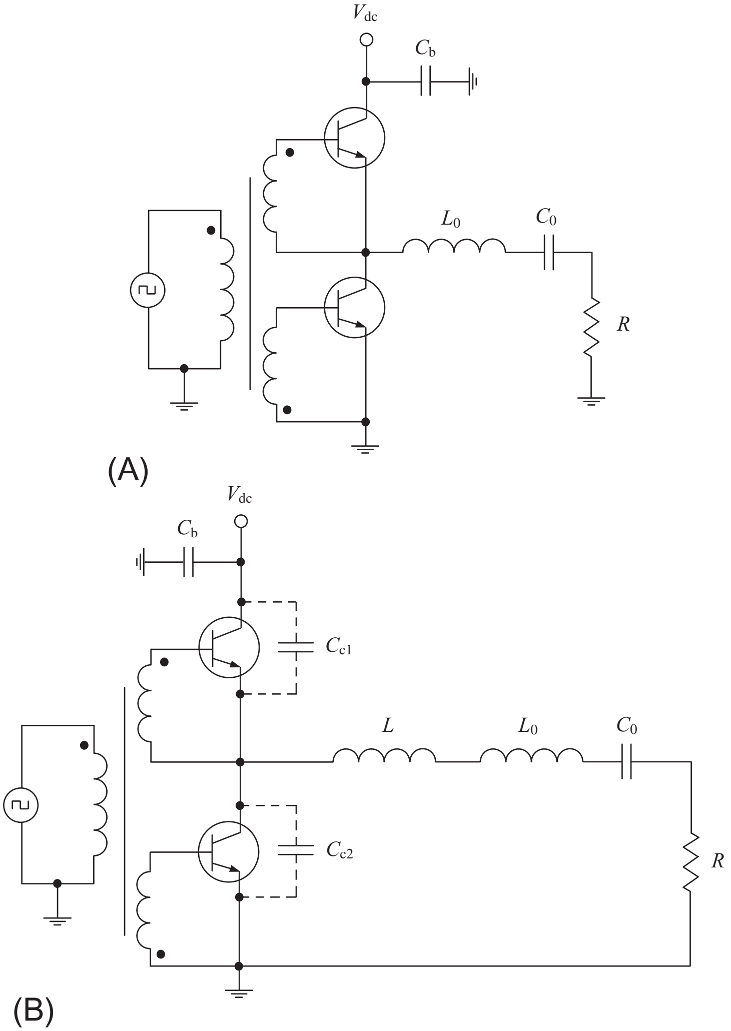


FIG. 10.1

Complementary voltage-switching Class-D and Class-DE PAs with series filter.

of the maximum collector voltage, which is equal to the DC supply voltage, and the DC component of the collector voltage waveform does not exceed 2. This results in a higher output power which can be delivered to the load. Besides, the transitions from a pinch-off mode to a saturation mode and vice versa occur at zero collector currents, thus avoiding the device active modes and eliminating additional power losses. However, the frequency limitations of such a voltage-switching Class-D PA are provided by the device parasitic collector shunt capacitances, as shown in Fig. 10.1B, resulting in the increased switching transition times due to the capacitor charging and discharging processes.

A possible way to eliminate these power losses and to extend the voltage-switching Class-D mode to higher frequencies is to introduce a dead time during the period when one device has already turned off but the other one has not turned on yet, and the inductive load network is used to charge and discharge the shunt capacitances. This can be done by introducing the Class-E switching conditions when the switching loss during off-to-on transition is reduced to zero by the operating requirements of zero voltage at zero-voltage slope at the end of the period. Since the shunt capacitor must be discharged at that exact time, an additional series inductor L with optimum value should be included into the load network, as shown in Fig. 10.1B. As a result, the switching current and voltage waveforms have the characteristics of both Class-D and Class-E operation modes. The series L_0C_0 filter is still necessary to suppress the harmonic components to allow only the sinusoidal signal to flow into the load R.

Such a Class-DE PA was first described and proposed by Zhukov and Kozyrev in Ref. 1 and has found some particular applications due to its high operation efficiency at higher operating frequencies.[2, 3] The optimum parameters of a voltage-switching Class-DE PA can be determined based on its steady-state collector voltage and current waveforms. Fig. 10.2 shows three different Class-DE switching circuits that occur during a switching cycle, the load network of which consists of the shunt collector capacitances C_{c1} and C_{c2}, a series inductor L, a series fundamentally tuned L_0C_0 circuit, and a load resistor R. Each of active devices Q_1 and Q_2 is considered an ideal switch that is driven so as to provide the device switching between its on-state and off-state operation conditions. The collector of the top device Q_1 is connected to the DC-supply voltage and the emitter of the bottom device Q_2 is connected to the ground. To simplify the analysis of a Class-DE PA, the following several assumptions are introduced:

- The transistors have zero saturation voltage, zero saturation resistance, infinite off-resistance, and their switching is instantaneous and lossless.
- The shunt capacitances are independent of the collector and are assumed linear.
- The loaded quality factor $Q_L = \omega L_0/R = 1/\omega C_0 R$ of the series resonant L_0C_0 circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal at the switching frequency.
- There are no losses in the circuit except into the load R.

The Class-E switching conditions for each device can be written as.

$$v_1(\omega t)|_{\omega t=\pi} = 0 \quad \left.\frac{dv_1(\omega t)}{d\omega t}\right|_{\omega t=\pi} = 0 \tag{10.1}$$

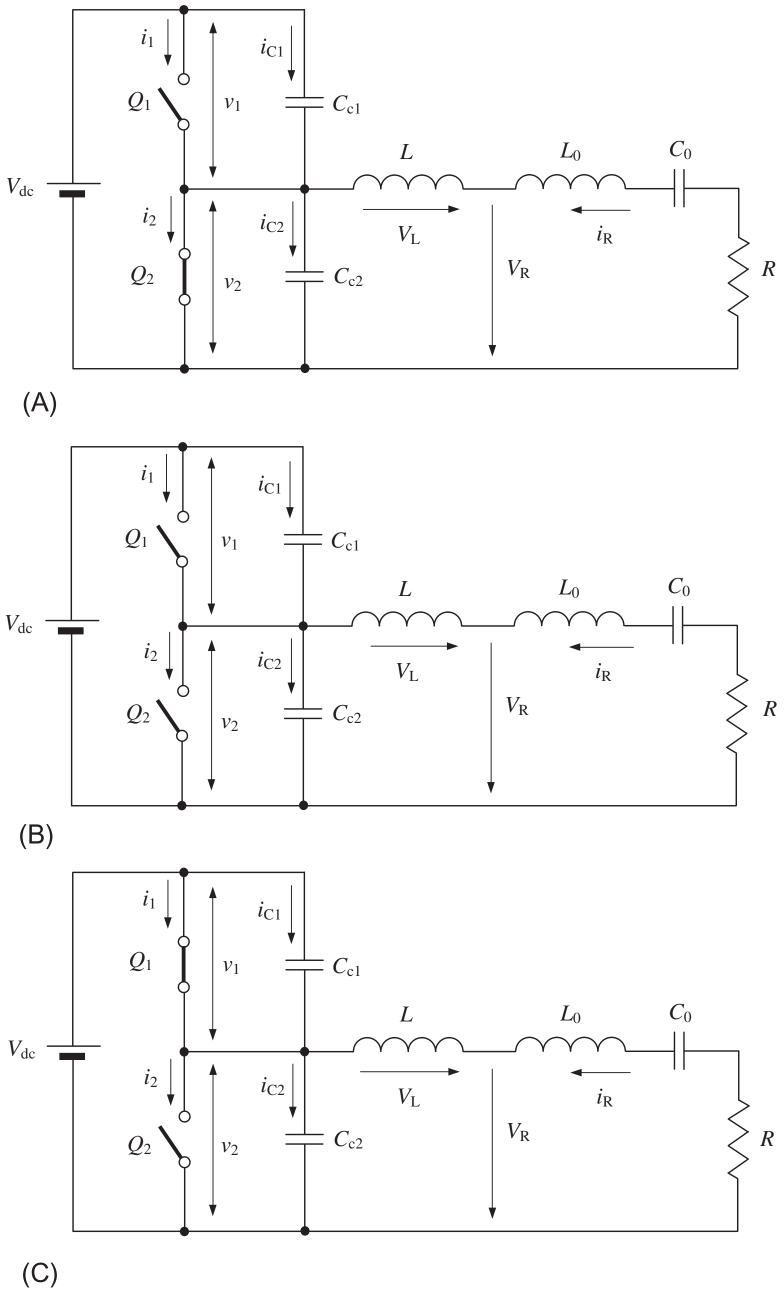
$$v_2(\omega t)|_{\omega t=2\pi} = 0 \quad \left.\frac{dv_2(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0 \tag{10.2}$$

where v_1 and v_2 are the voltages across switches Q_1 and Q_2, respectively.

The detailed theoretical analysis of a Class-DE PA in a general form is given in Ref. 1, where the output current is assumed sinusoidal written as

$$i_R(\omega t) = I_R \sin(\omega t + \varphi) \tag{10.3}$$

where I_R is the current amplitude and φ is the initial phase shift.


i_1
i_{C1}
Q_1
v_1
C_{c1}
L
L_0
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i_R
Q_2
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C_{c2}
V_R
R
(C)

FIG. 10.2

Equivalent circuits of voltage-switching Class-DE PA.

The analysis is performed in the interval $0 \le \omega t \le 2\pi$ with a dead time τ_d during which each of switches Q_1 and Q_2 is turned off. The basic Kirchhoff equations, characterizing the electrical behavior of the equivalent circuits of a voltage-switching Class-DE PA, are written as

$$i_2(\omega t) + i_{C_2}(\omega t) = i_1(\omega t) + i_{C_1}(\omega t) + i_R(\omega t) \tag{10.4}$$

$$v_1(\omega t) = V_{DC} - v_2(\omega t) \tag{10.5}$$

$$i_{C_1}(\omega t) = \omega C_{c_1} \frac{dv_1(\omega t)}{d\omega t} \tag{10.6}$$

$$i_{C_2}(\omega t) = \omega C_{c_2} \frac{dv_2(\omega t)}{d\omega t} \tag{10.7}$$

During the interval of $0 \le \omega t \le \pi - \tau_d$ before the switching instant, the switch Q_1 is turned off and the switch Q_2 is turned on, conducting the load current, as shown in Fig. 10.2A, resulting in the current and voltage conditions

$$i_1(\omega t) = 0 \tag{10.8}$$

$$i_2(\omega t) = i_R(\omega t) \tag{10.9}$$

$$i_{C_1}(\omega t) = i_{C_2}(\omega t) = 0 \tag{10.10}$$

$$v_1(\omega t) = V_{DC} \tag{10.11}$$

$$v_2(\omega t) = 0 \tag{10.12}$$

where $V_{DC} = 2V_{cc}$ is the DC-supply voltage.

During the interval of $\pi - \tau_d \le \omega t \le \pi$ or dead time, the switch Q_1 is still turned off, while the switch Q_2 is then turned off, as shown in Fig. 10.2B, and currents continue to flow through the device shunt capacitors. The current discharges the capacitor of one device, while it charges the capacitor of the other device. If it is assumed that these capacitors are identical, then the load current is equally divided between them. Using Eqs. (10.5)–(10.7) and an initial condition of $v_2(\pi - \tau_d) = 0$ yields

$$i_1(\omega t) = i_2(\omega t) = 0 \tag{10.13}$$

$$i_{C2}(\omega t) - i_{C1}(\omega t) = i_R(\omega t) \tag{10.14}$$

$$v_2(\omega t) = \frac{1}{\omega C} \int_{\pi-\tau_d}^{\omega t} i_{C2}(\omega t)\, d\omega t + v_2(\pi - \tau_d) = -\frac{I_R}{\omega C}\left[\cos(\tau_d + \varphi) + \cos(\omega t + \varphi)\right] \tag{10.15}$$

where $C = C_{c1} + C_{c2}$.

Eq. (10.15) can also be written in a differential form using Eqs. (10.3), (10.6), and (10.7) as

$$\frac{dv_2(\omega t)}{d\omega t} = \frac{I_R}{\omega C} \sin(\omega t + \varphi) \tag{10.16}$$

Applying the switching conditions given in Eq. (10.2) to Eq. (10.16) results in

$$\sin(2\pi + \varphi) = 0 \tag{10.17}$$

from which it follows that the initial phase φ can be set to zero.

During the interval of $\pi \leq \omega t \leq 2\pi$ - τ_d before the switching instant, the switch Q_1 is then turned on and the switch Q_2 is still turned off, as shown in Fig. 10.2C, resulting in

$$i_1(\omega t) = -i_R(\omega t) \tag{10.18}$$

$$i_2(\omega t) = 0 \tag{10.19}$$

$$i_{C_1}(\omega t) = i_{C_2}(\omega t) = 0 \tag{10.20}$$

$$v_1(\omega t) = 0 \tag{10.21}$$

$$v_2(\omega t) = V_{DC} \tag{10.22}$$

During the interval of 2π - $\tau_d \leq \omega t \leq 2\pi$ or dead time, both switches Q_1 and Q_2 are turned off, as shown in Fig. 10.2B, and currents flow through the device shunt capacitors charging the upper one and discharging the lower one. Using Eqs. (10.5)–(10.7) and an initial condition of $v_2(2\pi - \tau_d) = V_{ds}$ yields

$$i_1(\omega t) = i_2(\omega t) = 0 \tag{10.23}$$

$$i_{C_2}(\omega t) - i_{C_1}(\omega t) = i_R(\omega t) \tag{10.24}$$

$$v_2(\omega t) = \frac{1}{\omega C}\int\limits_{2\pi-\tau_d}^{\omega t} i_{C2}(\omega t)\, d\omega t + v_2(2\pi - \tau_d) = \frac{I_R}{\omega C}(\cos\tau_d - \cos\omega t) + V_{DC} \tag{10.25}$$

Fig. 10.3 shows the current and voltage waveforms of a voltage-switching Class-DE PA in an optimum operation mode during the entire interval $0 \leq \omega t \leq 2\pi$ corresponding to its equivalent circuits shown in Fig. 10.2.

From the boundary condition $v_2(\pi) = V_{dc}$ or $v_2(2\pi) = 0$, by using the corresponding Eq. (10.15) or Eq. (10.25), one can write

$$\frac{\omega C V_{dc}}{I_R} = 1 - \cos\tau_d \tag{10.26}$$

The fundamental-frequency component of the voltage $v_2(\omega t)$ across the switch Q_2 can be represented by two quadrature components shown in Fig. 10.2, whose amplitudes can be found using Fourier formulas as

$$V_R = -\frac{1}{\pi}\int\limits_{\pi-\tau_d}^{2\pi} v_2(\omega t)\sin\omega t\, d\omega t = \frac{1+\cos\tau_d}{\pi} V_{dc} = I_R R \tag{10.27}$$

$$V_L = -\frac{1}{\pi}\int\limits_{\pi-\tau_d}^{2\pi} v_2(\omega t)\cos\omega t\, d\omega t = \frac{\tau_d - \sin\tau_d\cos\tau_d}{\pi}\frac{I_R}{\omega C} \tag{10.28}$$

As a result, the optimum normalized total shunt capacitance C and series inductance L as the functions of a dead time τ_d can be calculated using Eq. (10.26) from

$$\omega C R = \frac{\sin^2\tau_d}{\pi} \tag{10.29}$$

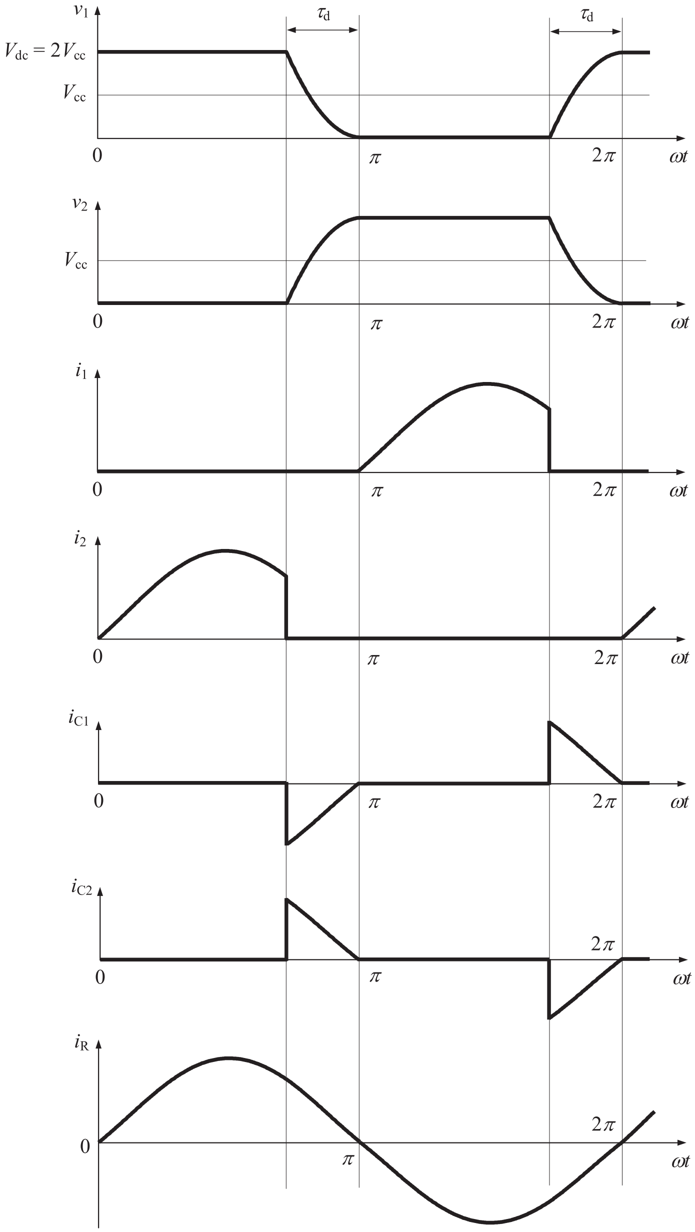


FIG. 10.3

Waveforms for optimum Class-DE operation mode.

$$\frac{\omega L}{R}=\frac{V_L}{V_R}=\frac{\tau_d-\sin\tau_d\cos\tau_d}{\sin^2\tau_d} \tag{10.30}$$

The optimum load resistance R can be obtained using Eq. (10.27) for the DC-supply voltage V_{DC} and fundamental-frequency output power P_{out} delivered to the load as

$$R=\frac{1}{2}\frac{V_R^2}{P_{out}}=\frac{(1+\cos\tau_d)^2}{2\pi^2}\frac{V_{dc}^2}{P_{out}} \tag{10.31}$$

The maximum fundamental-frequency output power P_{out} delivered to the load as a function of the dead time τ_d and capacitance C can be obtained using Eqs. (10.29) and (10.31) for the DC-supply voltage V_{DC} as

$$P_{out}=\frac{1}{2\pi}\left(\frac{1+\cos\tau_d}{\sin\tau_d}\right)^2\omega CV_{dc}^2 \tag{10.32}$$

For practical design procedure, it is important to know the dependence

$$\tau_d=\cos^{-1}\frac{2\pi\dfrac{P_{out}}{\omega CV_{dc}^2}-1}{2\pi\dfrac{P_{out}}{\omega CV_{dc}^2}+1} \tag{10.33}$$

It should be mentioned that the parasitic device lead inductors L_{c1} and L_{c2} shown in Fig. 10.4, which are located between the output shunt capacitance of each device (C_{c_1} and C_{c_2}) and load network inductor L, do not cause the power losses if their quality factors are high enough. However, their presence results in an increased peak collector voltage, which will exceed V_{DC}, due to the parasitic oscillations with the oscillation frequency

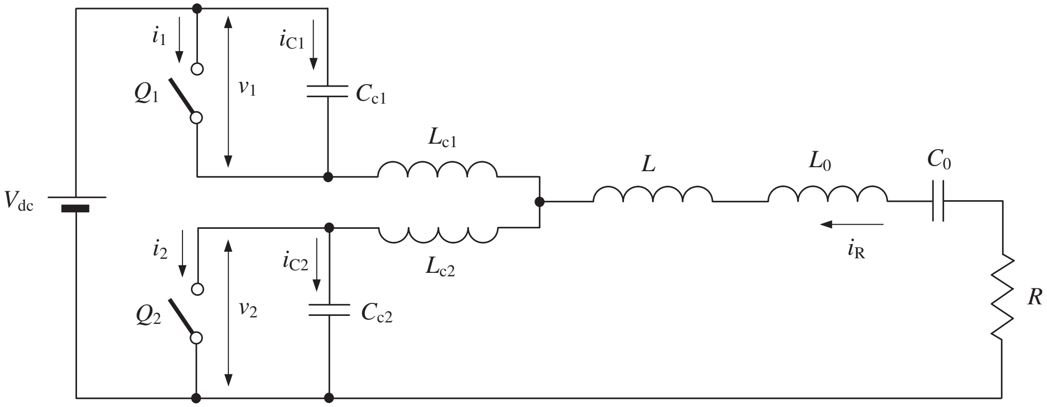


FIG. 10.4

Equivalent circuit of voltage-switching Class-DE PA with parasitic inductors.

$$\omega_1 = \frac{1}{\sqrt{(L_{c_1} + L_{c_2})\dfrac{C_{c_1}C_{c_2}}{C_{c_1} + C_{c_2}}}} \tag{10.34}$$

when both switches Q_1 and Q_2 are turned off, and with the oscillation frequency

$$\omega_2' = \frac{1}{\sqrt{(L_{c_1} + L_{c_2})C_{c1}}} \tag{10.35}$$

or

$$\omega_2'' = \frac{1}{\sqrt{(L_{c_1} + L_{c_2})C_{c_2}}} \tag{10.36}$$

when either switch Q_1 or switch Q_2 is turned on.

To minimize such an increase in the collector voltage peak factor to only 10%, their values must be sufficiently small at the switching frequency defined by

$$L_{c_1} < \frac{0.01}{\omega^2 C_{c_1}} \tag{10.37}$$

$$L_{c_2} < \frac{0.01}{\omega^2 C_{c_2}} \tag{10.38}$$

Fig. 10.5A shows the equivalent circuit of a voltage-switching Class-DE PA using switching devices with nonzero saturation resistances r_{sat_1} and r_{sat_2}. In this case, during the interval of $0 \le \omega t \le \pi - \tau_d$ when the device Q_2 is saturated, the collector voltage $v_2(\omega t)$ shown in Fig. 10.5B can be defined as $v_{2_{\mathrm{sat}}}(\omega t) = i_2(\omega t) r_{2_{\mathrm{sat}}} > 0$. Similar changes of the collector voltage shape occur during the interval of $\pi \le \omega t \le 2\pi - \tau_d$ when the device Q_2 is pinched off which is a result of nonzero saturation voltage across the device Q_1 equal to $v_{2_{\mathrm{sat}}}(\omega t) = i_2(\omega t) r_{2_{\mathrm{sat}}} > 0$. Hence, assuming identical devices when $r_{\mathrm{sat}} = r_{\mathrm{sat}_1} = r_{\mathrm{sat}_2}$, the collector efficiency of the device Q_2 as function of a dead time τ_d can be written as

$$\eta = 0.5 + 0.5\sqrt{1 - 16\xi^2(\tau_d)\frac{r_{\mathrm{sat}} P_{\mathrm{out}_2}}{V_{\mathrm{dc}}^2}} \tag{10.39}$$

where

$$\xi(\tau_d) = \frac{\pi}{\sqrt{(1 + \cos\tau_d)^2 + \left(\dfrac{\tau_d - \sin\tau_d \cos\tau_d}{1 - \cos\tau_d}\right)^2}} \tag{10.40}$$

is the ratio between the DC-supply voltage V_{DC} and the fundamental-frequency component of the collector voltage v_2 when $r_{\mathrm{sat}} = 0$, and P_{out_2} is the output power from the device Q_2.[1]

The maximum operating frequency $f_{\max}$ in an optimum mode is limited by the device collector capacitances C_{c_1} and C_{c_2}. To correctly compare the collector efficiencies corresponding to the push–pull Class-DE and single-ended Class-E operation modes, it is better to determine $f_{\max}$ for a Class-DE PA

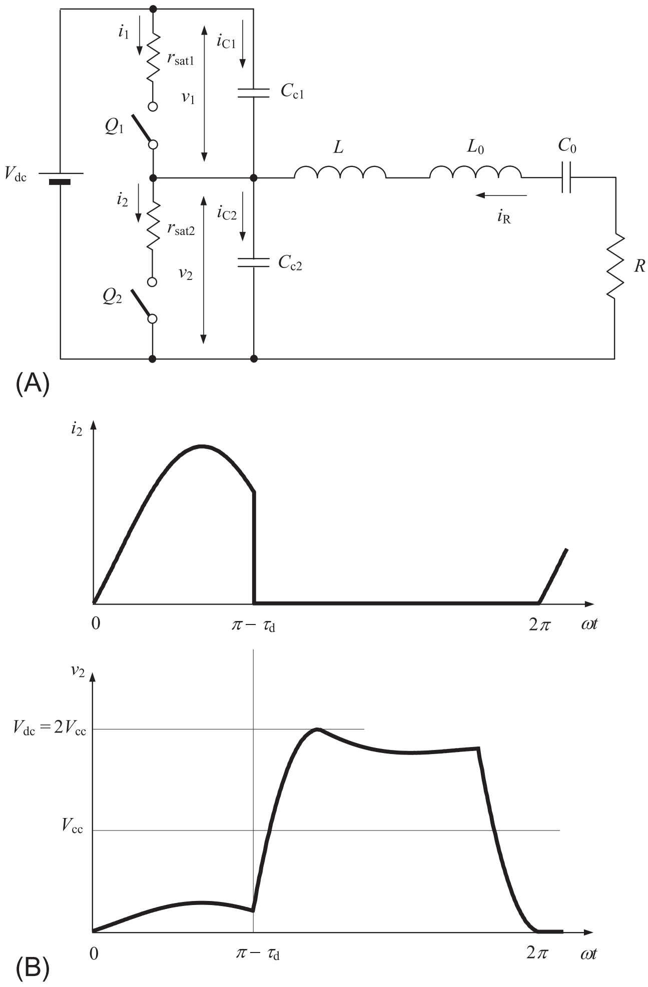

i_1
r_{sat1}
i_{C1}
C_{c1}
v_1
Q_1
V_{dc}
L
L_0
C_0
i_2
r_{sat2}
i_{C2}
C_{c2}
i_R
R
v_2
Q_2
(A)
i_2
0
$\pi - \tau_d$
2π
ωt
v_2
$V_{dc} = 2V_{cc}$
V_{cc}
0
$\pi - \tau_d$
2π
ωt
(B)

FIG. 10.5

Equivalent circuit of voltage-switching Class-DE PA with saturation resistances.

through the parameters of a single transistor. Then, considering that $V_{cc} = V_{DC}/2$, $C_{c_2} = C/2$, and $P_{out_2} = P_{out}/2$, from Eq. (10.32) we can derive that

$$f_{max} = 0.25 \left(\frac{\sin \tau_d}{1 + \cos \tau_d} \right)^2 \frac{P_{out_2}}{C_{c_2} V_{cc}^2} \tag{10.41}$$

The comparison of both Class-DE and Class-E modes as functions of the saturation time period $\tau_{sat} = \pi - \tau_d$ shows that a complementary voltage-switching Class-DE PA provides a substantially lower maximum operating frequency in an optimum mode. For example, for $\tau_d = 60$ degrees and

$\tau_{sat} = 120$ degrees, the maximum operating frequency of a Class-E PA is greater by a factor of more than three.[1, 4] However, when using a Class-DE mode, the operating frequency range with collector (or drain) efficiencies of about 90% can be two to three times wider when compared with a Class-D mode.[5]

Fig. 10.6 shows the equivalent circuit of a voltage-switching Class-DE PA with nonlinear shunt capacitances, since generally the output device capacitance is nonlinear. For example, the drain-source capacitance of a power metal-oxide-semiconductor field-effect transistor (MOSFET) can be represented as a junction capacitance with linearly graded (or abrupt) junction, while the collector capacitance of a bipolar transistor is normally modeled as a junction capacitance with abrupt junction having a reverse square-root dependence on the voltage between the collector and the emitter.[4, 6] The nonlinear behavior of the drain-source capacitance C_{ds} of a MOSFET device can be described by

$$C_{ds} = \frac{C_{j0}}{\left(1 + \frac{v}{V_{bi}}\right)^{m}} \tag{10.42}$$

where V_{bi} is the built-in potential, which typically ranges from 0.5 to 0.9 V, v is the drain-source voltage, C_{ds0} is the capacitance at $v = 0$, and m is the grading coefficient.[7] The results of numerical calculations show that an abrupt-junction nonlinearity of the output capacitances when $m = 2$ does not affect the value of a normalized inductance $\omega L/R$. However, the normalized total shunt capacitance ωCR is $\sqrt{2}$ times smaller compared to the case with the constant capacitances.[5] It is shown analytically that the DC-supply voltage and current are always proportional to the amplitudes of the output voltage and current, and the grading coefficient m is an important parameter to satisfy the Class-E switching conditions.[8, 9] It should be mentioned that, for loaded quality factors of the series resonant L_0C_0 circuit $Q_L > 3$, the current flowing into the load is nearly sinusoidal. However, if $Q_L < 3$, the design and performance values of a Class-DE PA are strongly affected Q_L, especially for values of τ_{sat} close to 0.5, resulting in the significant harmonic content as well.[4]

Practically, it is difficult to drive a Class-DE PA operating at high frequencies using a rectangular driving signal, since the dead time must be controlled with high accuracy (of the order of 1 ns) that also requires the very wideband input transformer. In this case, it is better and easier to apply a sinusoidal drive because it reduces the driving power requirements, and control of the dead time can be provided

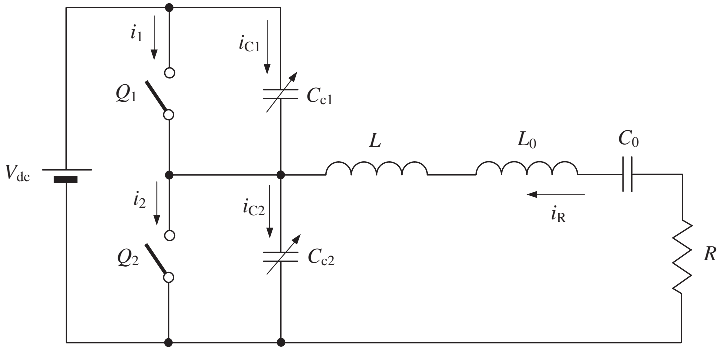


FIG. 10.6

Equivalent circuit of voltage-switching Class-DE PA with nonlinear shunt capacitances.

by the driving amplitude. Besides, the transition from a pinch-of mode to a saturation mode for the power switching MOSFETs occurs very fast once the device gate threshold (or pinch-off) voltage is crossed. Consider the 180 degree out-of-phase sinusoidal signals driving each device, as shown in Fig. 10.7.[2] When the gate voltage of one device will cross its pinch-off voltage V_p to turn that device off at angular time $\pi - 0.5\tau_d$, the gate voltage across the other device is still below threshold. Thus, during this crossover period from $\pi - 0.5\tau_d$ to $\pi + 0.5\tau_d$, both devices are turned off simultaneously.

For a sinusoidal gate voltage across the gate-source capacitance,

$$v_g(\omega t) = V_g \sin \omega t \tag{10.43}$$

where V_g is the voltage amplitude, this voltage is equal to the device pinch-off voltage V_p at angular times $0.5\tau_d$, $\pi - 0.5\tau_d$, and $\pi + 0.5\tau_d$, respectively, that gives

$$V_p = V_g \sin\frac{\tau_d}{2} = V_g \sin\left(\pi - \frac{\tau_d}{2}\right) = -V_g \sin\left(\pi + \frac{\tau_d}{2}\right) \tag{10.44}$$

Eq. (10.44) can be rewritten as

$$V_g = \frac{V_p}{\sin\frac{\tau_d}{2}} \tag{10.45}$$

representing a dependence of the required gate voltage amplitude V_g for a given device dead time τ_d.

On the other hand, it is important first to examine the range of dead times versus gate voltage amplitude of a sinusoidal drive. By rearranging Eq. (10.45), we can write

$$\tau_d = 2\sin^{-1}\left(\frac{V_p}{V_g}\right) \tag{10.46}$$

For example, if the peak gate voltage of the devices is limited to 20 V, then, assuming $V_p = 3.5$ V, the minimum dead time is equal to approximately 20 degrees. The other limit occurs when the gate voltage becomes too low to turn on the device properly. Usually, this means that, in practice, the gate voltage amplitude must not be lower than about 6.5 V. Hence, the maximum dead time that can be achieved is about 65 degrees.

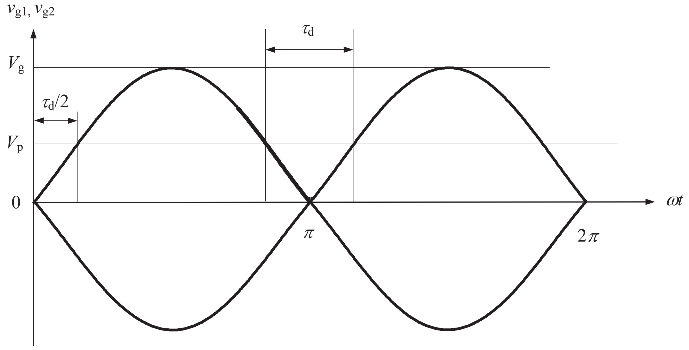


FIG. 10.7

Sinusoidal 180 degree out-of-phase driving waveforms.

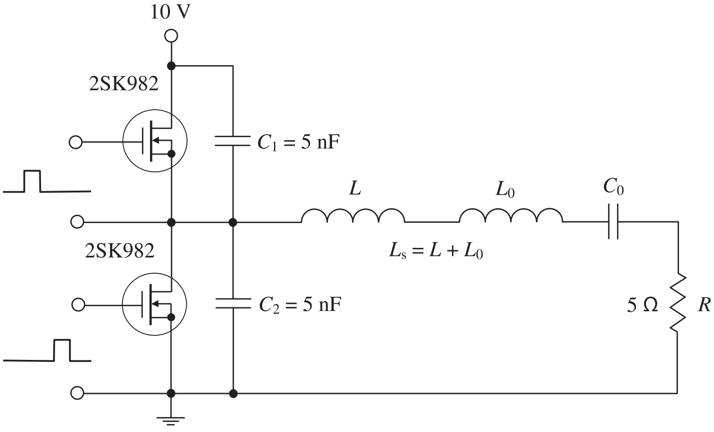


FIG. 10.8

Circuit diagram of experimental Class-DE PA with rectangular drive.

Fig. 10.8 shows the experimental circuit of a Class-DE PA operating at 1 MHz with a rectangular drive.[3] To obtain the output power of 1 W at a supply voltage of 10 V, two MOSFET devices 2SK982 were used as the switching active devices. Assuming that the device dead time $\tau_d = 90$ degrees and load network quality factor $Q = 10$, the load resistance R can be calculated from Eq. (10.31) as equal to 5.07 Ω, the shunt capacitances C_1 and C_2 ($C_1 = C_2 = C/2$) can be determined from Eq. (10.29) as equal to 5 nF each, while the series inductance L_s, combining the additional compensating inductance L and series filter inductance L_0, can be calculated from $L_s = QR/\omega$ as equal to 8.07 μH. In this case, the inductance L_0 can be found using Eq. (10.30) as

$$L_0 = L_s - L = \left(Q - \frac{\pi}{2}\right)\frac{R}{\omega} = 6.8\,\mu\text{H} \tag{10.47}$$

Then, the series capacitance C_0 can be obtained by

$$C_0 = \frac{1}{\omega^2 L_0} = 1/\omega R\left(Q - \frac{\pi}{2}\right) = 3.73\,\text{nF} \tag{10.48}$$

As a result, the drain efficiency was measured as high as 96.2% with an output power of 0.51 W at an operating frequency of 1.04 MHz. The output power was reduced by increasing the operating frequency from 1.0 to 1.04 MHz. In this case, the smoothest switching voltage waveforms were observed. Generally, the output power could be changed from 30% to 136% by controlling the operating frequency within 10%.

Fig. 10.9 shows the experimental circuit of a high-power Class-DE PA operating at 13.56 MHz with a sinusoidal drive.[2] The gates of both switching MOSFET devices IRF540 are driven from two transformers with series-connected primary windings and secondary windings connected with opposite polarities to provide the phase shift of 180 degrees between the gate voltages. Both gates could be driven with a single transformer with one primary winding. However, using the separate primary windings has the advantage of eliminating a positive feedback mechanism due to the device feedback gate-source capacitances. The output power $P_{out} = 300$ W was achieved at an operating frequency of 13.56 MHz

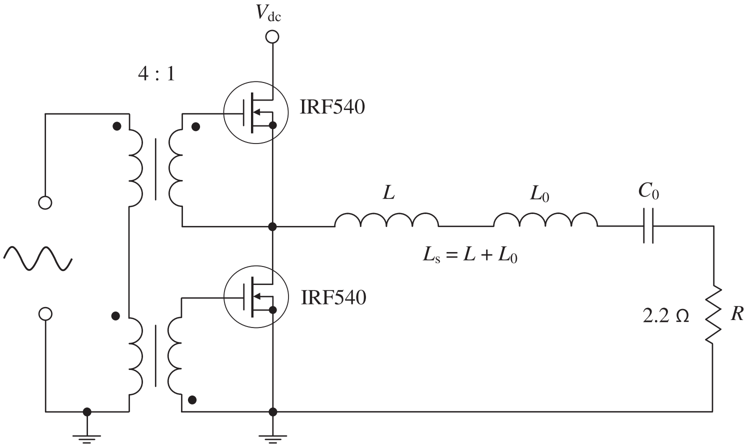


FIG. 10.9

Circuit diagram of experimental Class-DE PAs with sinusoidal drive.

with a supply voltage $V_{DC} = 72.5\,\text{V}$. The DC supply is bypassed by several 0.1-μF ceramic capacitors, which have a self-resonance at close to 13.56 MHz. By assuming the load current amplitude $I_R = 15.3$ A, the load resistance R can be obtained as

$$R = \frac{2P_{\text{out}}}{I_R^2} = 2.56\,\Omega \tag{10.49}$$

For a load network quality factor $Q = 10$, the series inductance L_s can be calculated as

$$L_s = \frac{QR}{\omega} = 0.3\,\mu\text{H} \tag{10.50}$$

The dead time τ_d can be obtained from Eq. (10.27) as equal to approximately 45 degrees. By using Eq. (10.30), the series inductance L required to compensate for the device output capacitance of 500 pF (at $V_{ds} = 25\,\text{V}$) is equal to 17.2 nH. Then, the series capacitance C_0 can be obtained as

$$C_0 = \frac{1}{\omega^2 (L_s - L)} = 487\,\text{pF} \tag{10.51}$$

As a result, the measured output power of 298.2 W with a drain efficiency of 94.2% was achieved at a supply voltage of 73.1 V. The total power dissipated in the gate circuit was only 9.6 W with a gate voltage amplitude of 7 V. By using two IRFP450 MOSFETs fed by the supply voltages of +150 V and −150 V (300 V with the center point at ground, allowing a direct connection from the switching node to a grounded load), an output power of 1 kW can be achieved in a frequency range of 50 kHz to 5 MHz with an efficiency over 91%.[10]

As in the complementary voltage-switching Class-DE PA, the transformer-coupled voltage switching Class-DE PA operating in a push–pull mode requires the driving signals to cause both transistors to switch on and off alternately. Fig. 10.10 shows the push–pull configuration of a voltage-switching Class-DE PA with an output transformer where the DC-supply voltage is connected to the center

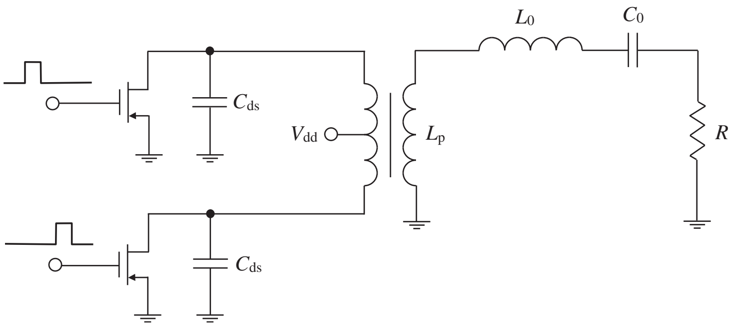


FIG. 10.10

Voltage-mode push–pull Class-DE with inherent parallel inductance.

tap of the transformer primary winding.[11] In this case, the transformer parasitic parallel inductance L_p can be used instead of a series inductance L required for a Class-DE operation, in conjunction with the drain-source capacitances C_{ds} of the transistors. When using a 28-V GaN high-electron-mobility transistor (HEMT) device characterized by a maximum DC current of 1.75 A and having a C_{ds} of 0.5 pF, a maximum drain efficiency of 89% was simulated at the transistor plane for a 30% duty ratio (or cycle). Moreover, high efficiency can also be achieved over a wide dynamic range of the load impedances, thus demonstrating the potential of such a configuration to achieve high efficiency for a Chireix outphasing configuration.

To reduce the influence of the parasitic series inductances, especially at higher frequencies when their values exceed their optimum values required for Class-DE operation, the current-switching Class-DE configuration can be used when zero-current and zero current-derivative conditions, corresponding to optimum inverse Class-E mode, are satisfied. In this case, the switch voltages and currents obtained in a current-mode Class-DE PA are inversed in comparison to the voltage-mode Class-DE PA by using a simple output matching network with a series inductance and a shunt capacitance when an active time τ_a is used instead of a dead time τ_d during which both switches are turned on. Fig. 10.11 shows the

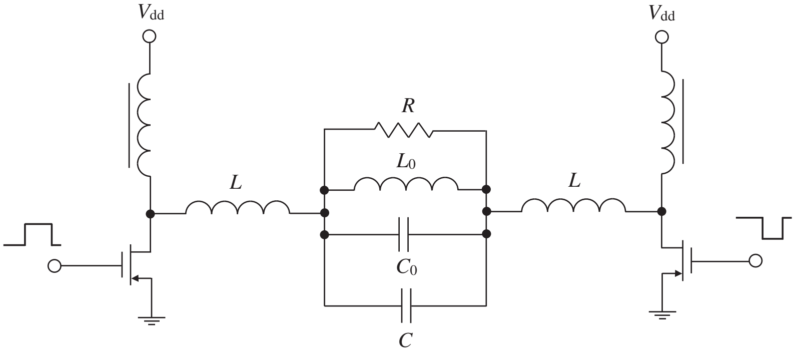


FIG. 10.11

Circuit schematic of current-mode Class-DE PA.

simplified circuit schematic of a symmetrical current-mode Class-DE PA, where L is a series inductance included in each amplifying path, C is a parallel capacitance, L_0C_0 is a parallel filter tuned to the fundamental, and R is a load resistance.[12] The measured results show that, when using two LDMOSFET MRFE6VS25N devices, a drain efficiency of 88% with a power gain of about 22 dB and an output power of 42 dBm at an operating frequency of 4 MHz was achieved when an active time $\tau_a = 90$ degrees was used. Some reduction in efficiency was caused by finite values of the parasitic drain-source capacitances C_{ds} when the idealized current-switching Class-DE conditions are not fully satisfied.

10.2 Class-FE PAs

In practice, the idealized collector voltage and current waveforms corresponding to Class-F mode can be realized at sufficiently low frequencies when the effect of the device collector capacitance is negligible. At higher frequencies, the effect of the collector capacitance contributes to a finite switching time, resulting in time periods when the collector voltage and collector current exist at the same time when simultaneously $v > 0$ and $i > 0$. As a result, such a load network with shunt capacitor cannot provide the switchmode operation with an instantaneous transition from the device pinch-off mode to saturation mode. Therefore, during a finite time interval the device is operated in the active region as a nonlinear current source with the reverse-biased collector–base junction, and the collector current is provided by this current source. To minimize the power losses during transients, the optimum zero-voltage and zero voltage-derivative Class-E conditions can be applied to a Class-F circuit with additionally connected shunt capacitor and series inductor, providing soft-switching operation mode, and that was proposed and called as Class-Φ.[13] Experimental results demonstrate that high drain efficiency >80% can be achieved with a Class-C biasing at an operating frequency of 13.56 MHz with a maximum peak factor of about two, which is significantly lower than that in a switchmode Class-E mode. Therefore, it is important to expand the experimental results by providing an analytical insight to this mixed operation mode, which can be simply called the Class-FE similar to Class-DE, with the derivation of the optimum parameters for the load network and by deriving the additional Class-FE PA configurations.[14]

It should be mentioned that the rectangular voltage and half-sine current collector waveform can be provided by a push–pull voltage-switching Class-D PA with the fundamentally tuned series L_0C_0 filter, whose circuit schematic is shown in Fig. 10.12A. In this case, the bipolar transistors must be driven so as to provide an alternate voltage switching between the on-state and off-state modes. However, in a single-ended Class-F PA with a parallel quarterwave transmission line shown in Fig. 10.12B, the symmetrizing action of the transmission-line behavior can easily provide a function of the voltage inverter, resulting in the same collector waveforms with a voltage peak factor of two. The quarterwave line stores the voltage waveform in a traveling wave along its length, which returns delayed by one-half fundamental period and inverted because of power reflection condition at the short-circuit termination. However, the presence of parasitic collector capacitances degrades the amplifying performances of both transistor stages due to finite time of the charging and discharging processes. As a result, the frequency limitation is provided by the device parasitic collector shunt capacitances, resulting in the increased switching transition times due to the capacitor charging and discharging processes, and the fact that the transistor switches charge and discharge the shunt capacitances, dissipating power in the charging and discharging processes.

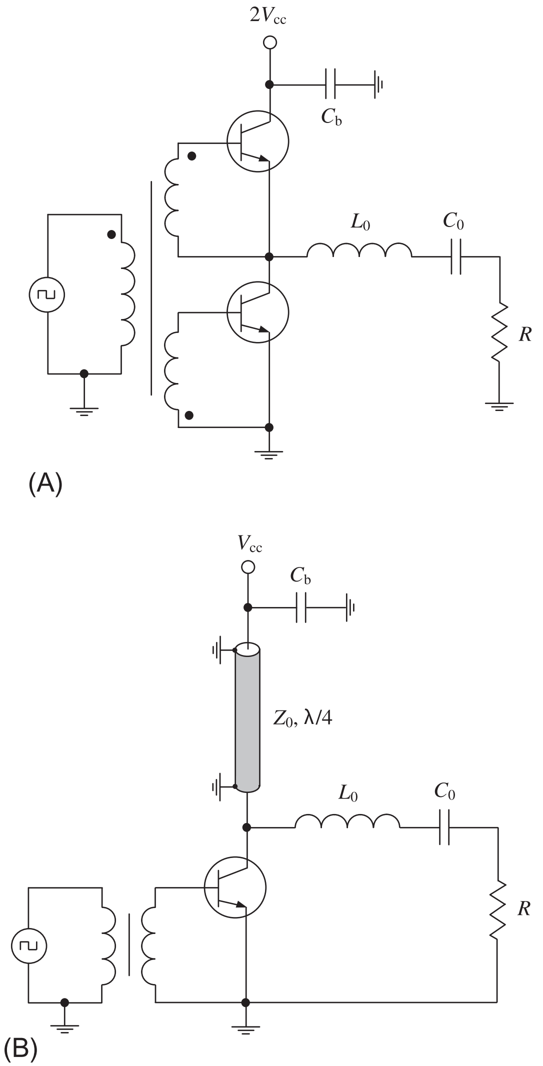


FIG. 10.12

Schematics of voltage-switching Class-D and Class-F PAs.

A possible way to eliminate these power losses and increase efficiency by compensating for the device output capacitances is to introduce a dead time during the period when one device has already turned off but the other has not turned on yet, and the inductive load network is used to charge and discharge the shunt capacitances. This can be provided by introducing the Class-E switching conditions when the switching loss during off-to-on transition is reduced to zero by the operating requirements of zero voltage at zero-voltage slope at the end of period. Since the shunt capacitor C must be discharged

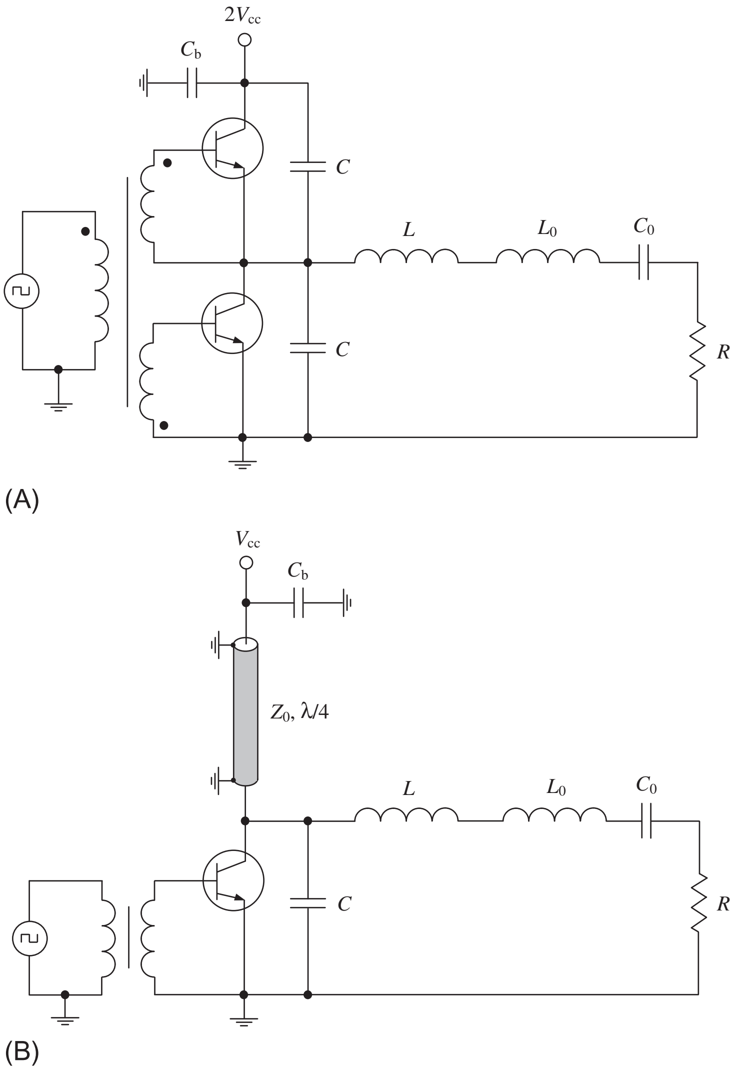


FIG. 10.13

Schematics of voltage-switching Class-DE and Class-FE PAs.

at that time instant, an additional series inductor L with optimum value should be included into the load network, as shown in Fig. 10.13A for a Class-DE PA. Similarly, a quarterwave transmission line can be used as a voltage inverter resulting in a single-ended Class-FE (or Class-EF) PA which combines a Class-F operation mode with Class-E switching conditions, as shown in Fig. 10.13B.

The optimum parameters of a Class-FE PA can be determined based on its steady-state collector voltage and current waveforms.[14] Fig. 10.14 shows the two equivalent Class-FE switching circuits that

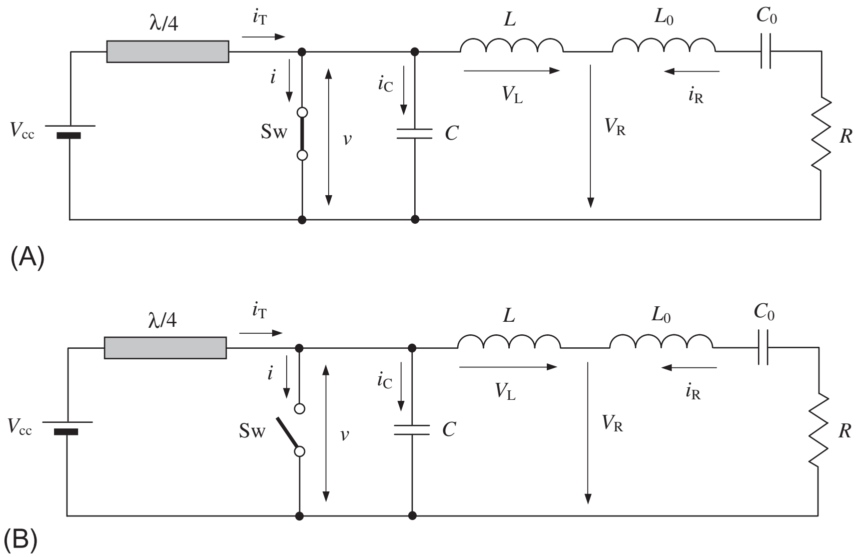


FIG. 10.14

Equivalent circuits of Class-FE PA.

occur during a switching cycle, the load network of which consists of an RF grounded parallel quarter-wave transmission line, a shunt capacitor C, a series inductor L, a series fundamentally tuned L_0C_0 circuit, and a load resistor R. The active device is considered an ideal switch that is driven so as to provide the device switching between its on-state and off-state operation conditions. To simplify the analysis of a Class-FE PA, the same assumptions which were used to analyze a Class-DE PA are introduced.

The Class-E switching conditions for the transistor switch can be written as

$$v(\omega t)|_{\omega t=2\pi}=0 \tag{10.52}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi}=0 \tag{10.53}$$

where v is the voltage across the switch.

Let the output current flowing through the load is written as sinusoidal,

$$i_R(\omega t)=I_R\sin(\omega t+\varphi) \tag{10.54}$$

where I_R is the current amplitude and φ is the initial phase shift.

The basic Kirchhoff's equations characterizing the electrical behavior of the equivalent circuits of a Class-FE PA are

$$i(\omega t)\ +i_C(\omega t)=i_T(\omega t)\ +i_R(\omega t) \tag{10.55}$$

$$i_C(\omega t)=\omega C\frac{dv(\omega t)}{d\omega t} \tag{10.56}$$

During the interval of $0 \le \omega t \le \pi - \tau_d$ before the switching instant, where τ_d is the dead time, the switch is turned on conducting the load current, as shown in Fig. 10.14A, resulting in the current and voltage conditions

$$i_C(\omega t) = 0 \tag{10.57}$$

$$i(\omega t) = i_R(\omega t) + i_T(\omega t) \tag{10.58}$$

$$v(\omega t) = 0 \tag{10.59}$$

During the interval of $\pi - \tau_d \le \omega t \le \pi$ or dead time, the switch is turned off, as shown in Fig. 10.14B, and currents continue to flow through the shunt capacitance charging the capacitor. Using Eq. (10.56) and initial condition $v(\pi - \tau_d) = 0$ yields

$$i(\omega t) = i_T(\omega t) = 0 \tag{10.60}$$

$$i_C(\omega t) = i_R(\omega t) \tag{10.61}$$

$$v(\omega t) = \frac{1}{\omega C}\int_{\pi-\tau_d}^{\omega t} i_C(\omega t)d\omega t + v(\pi - \tau_d) = -\frac{I_R}{\omega C}[\cos(\tau_d + \varphi) + \cos(\omega t + \varphi)] \tag{10.62}$$

During the interval of $\pi \le \omega t \le 2\pi - \tau_d$ before the switching instant, the switch is still turned off, resulting in

$$i_T(\omega t) = -i_R(\omega t) \tag{10.63}$$

$$i(\omega t) = i_C(\omega t) = 0 \tag{10.64}$$

$$v(\omega t) = 2V_{cc} \tag{10.65}$$

During the interval of $2\pi - \tau_d \le \omega t \le 2\pi$ or dead time, the switch is turned off, and currents flow through the shunt capacitance discharging the capacitor. Using Eq. (10.56) and initial condition $v(2\pi - \tau_d) = 2V_{cc}$ yields

$$i(\omega t) = i_T(\omega t) = 0 \tag{10.66}$$

$$i_C(\omega t) = i_R(\omega t) \tag{10.67}$$

$$v(\omega t) = \frac{1}{\omega C}\int_{2\pi-\tau_d}^{\omega t} i_C(\omega t)d\omega t + v(2\pi - \tau_d) = \frac{I_R}{\omega C}[\cos(\tau_d + \varphi) - \cos(\omega t + \varphi)] + 2V_{cc} \tag{10.68}$$

Eq. (10.67) can also be written in a differential form using Eqs. (10.54) and (10.56) as

$$\frac{dv(\omega t)}{d\omega t} = \frac{I_R}{\omega C}\sin(\omega t + \varphi) \tag{10.69}$$

Applying the switching condition given in Eq. (10.53) to Eq. (10.69) results in

$$\sin(2\pi + \varphi) = 0 \tag{10.70}$$

from which it follows that the initial phase φ can be set to zero.

Fig. 10.15 shows the ideal current and voltage waveforms of a Class-FE PA in an idealized optimum operation mode during the entire interval $0 \le \omega t \le 2\pi$ corresponding to its equivalent circuits shown in

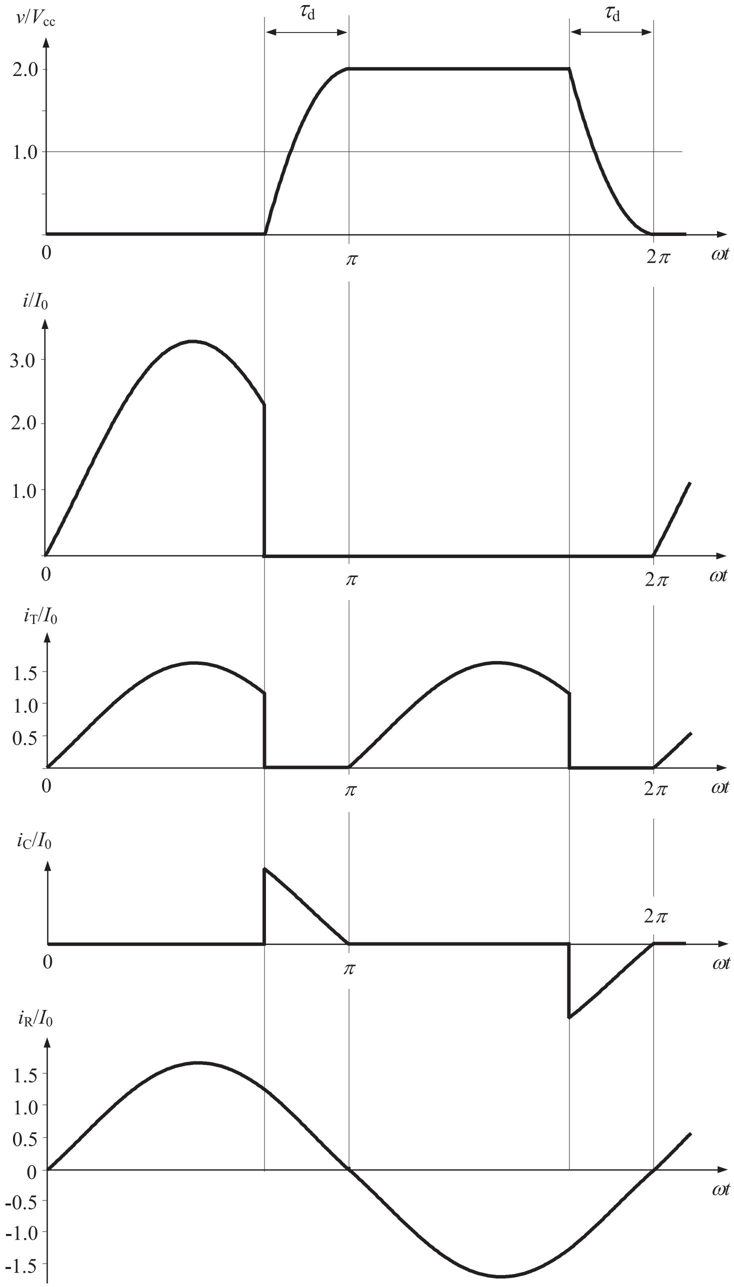


FIG. 10.15

Waveforms for optimum Class-FE operation mode.

Fig. 10.14. The quarterwave transmission line provides a half-wave symmetry, which means that the line attempts to do the same work in the first and second halves of the cycle. Therefore, the transmission-line half-repeating current must necessarily instantaneously fall to zero at $\pi - \tau_d$ and $2\pi - \tau_d$, being zero during both collector voltage edges. Note that, for the sinusoidal driving signals, the transistor must be biased in a Class-C mode to provide duty ratio $D < 50\%$ ($D < 0.5$), because the period of time when the device is turned off must exceed the period of time when the device is turned on.

From the boundary condition $v(\pi) = 2V_{cc}$ or $v(2\pi) = 0$ by using the corresponding Eq. (10.62) or Eq. (10.68), one can write

$$\frac{\omega C V_{cc}}{I_R} = \frac{1 - \cos\tau_d}{2} \tag{10.71}$$

The fundamental-frequency component of the voltage $v(\omega t)$ across the switch can be represented by two quadrature components shown in Fig. 10.14, whose amplitudes can be found using Fourier formulas by

$$V_R = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\,\sin\omega t\,d\omega t = \frac{2(1 + \cos\tau_d)}{\pi} V_{cc} = I_R R \tag{10.72}$$

$$V_L = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\,\cos\omega t\,d\omega t = \frac{\tau_d - \sin\tau_d\cos\tau_d}{\pi}\,\frac{I_R}{\omega C} \tag{10.73}$$

In an idealized Class-FE operation mode, there is no nonzero voltage and current simultaneously that gives an idealized collector efficiency of 100% when the DC power P_0 and fundamental-frequency output power P_{out} are equal. Consequently, the load current amplitude I_R as a function of the dead time τ_d can be obtained from Eq. (10.72) as

$$I_R = \frac{\pi}{1 + \cos\tau_d} I_0 \tag{10.74}$$

As a result, the optimum normalized shunt capacitance C and series inductance L as functions of a dead time τ_d can be calculated using Eq. (10.71) from

$$\omega C R = \frac{\sin^2\tau_d}{\pi} \tag{10.75}$$

$$\frac{\omega L}{R} = \frac{V_L}{V_R} = \frac{\tau_d - \sin\tau_d\cos\tau_d}{\sin^2\tau_d} \tag{10.76}$$

The optimum load resistance R can be obtained using Eq. (10.72) for the DC-supply voltage V_{cc} and fundamental-frequency output power P_{out} delivered to the load as

$$R = \frac{1}{2}\frac{V_R^2}{P_{out}} = \frac{2(1 + \cos\tau_d)^2}{\pi^2}\frac{V_{cc}^2}{P_{out}} \tag{10.77}$$

The maximum fundamental-frequency output power P_{out} delivered to the load as a function of the dead time τ_d and capacitance C can be obtained from Eqs. (10.75) and (10.77) for the DC-supply voltage V_{cc} as

$$P_{\text{out}} = \frac{2}{\pi}\left(\frac{1+\cos\tau_{\text{d}}}{\sin\tau_{\text{d}}}\right)^2 \omega C V_{\text{cc}}^2 \tag{10.78}$$

The maximum operating frequency f_{max} in an optimum Class-FE mode is limited to the device output (collector or drain-source) capacitance C_{out}. As a result, from Eq. (10.78) it follows that

$$f_{\text{max}} = 0.25\left(\frac{\sin\tau_{\text{d}}}{1+\cos\tau_{\text{d}}}\right)^2 \frac{P_{\text{out}}}{C_{\text{out}} V_{\text{cc}}^2} \tag{10.79}$$

Fig. 10.16 shows the dependence of the normalized maximum operating frequency $(f_{\text{max}} C_{\text{out}} V_{\text{cc}}^2)/P_{\text{out}}$ on the dead time τ_{d}. From Eq. (10.79) and Fig. 10.16, it follows that the maximum operating frequency f_{max} increases with smaller dead times, and

$$f_{\text{max}} = 0.043\,\frac{P_{\text{out}}}{C_{\text{out}} V_{\text{cc}}^2} \tag{10.80}$$

for a $\tau_{\text{d}} = 45$ degrees, which is the same as for a Class-DE and close to the maximum operating frequency of a Class-E with a 50% duty ratio. However, for a saturation period of π - $\tau_{\text{d}} = 180$ degrees - 45 degrees = 135 degrees when the transistor is turned on, the maximum operating frequency f_{max} of a Class-E PA is more than three times greater.[4] At the same time, for a saturation period of 135 degrees, the collector peak voltage of a Class-E PA is three times larger than the applied DC-supply voltage V_{cc}.[15] Note that the maximum collector voltage peak factor of a Class-FE PA never exceeds a factor of two for any saturation periods.

In Table 10.1, the optimum impedances seen from the device collector at the fundamental and higher-order harmonic components are illustrated by the appropriate circuit configurations. It can be seen that Class-F mode with a quarterwave transmission line shows purely resistive impedance at the fundamental, short-circuit conditions at even harmonics, and open-circuit conditions at odd harmonics. As opposed to Class-F mode, Class-E mode with shunt capacitance requires inductive impedance at the fundamental and capacitive reactance at any other harmonic component. As a result, Class-FE with a quarterwave transmission line provides simultaneously the harmonic impedance conditions typical for both Class-F with a quarterwave transmission line and Class-E with a shunt capacitance.

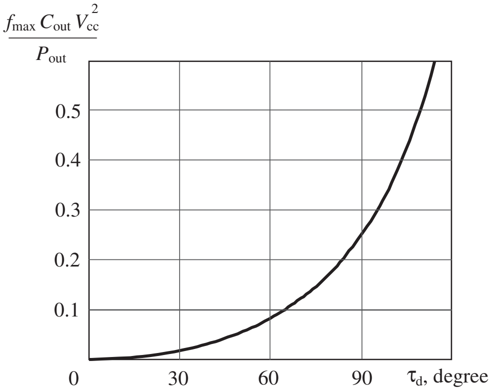


FIG. 10.16

Normalized maximum operating frequency versus dead time.

Table 10.1 Optimum impedances at fundamental and harmonics.

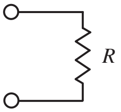
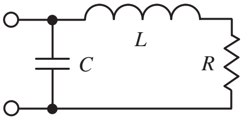
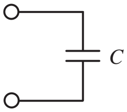
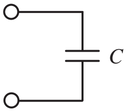
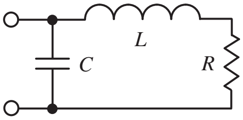
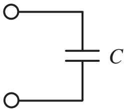
High-efficiency mode	f_0 (fundamental)	$2nf_0$ (even harmonics)	$(2n+1)f_0$ (odd harmonics)
Class-F with quarterwave line		Short	Open
Class-E with shunt capacitance			
Class-FE with quarterwave line		Short	

Fig. 10.17 shows the simulation setup for an ideal Class-FE operation in frequency domain. Generally, using the frequency domain enables the overall simulation procedure to be much faster than that in time domain and can take a few seconds. However, because the number of harmonic components is not infinite, the simulation waveforms and numerical results for the optimum load-network parameters are not so accurate. In this case, the input source represents a voltage source with Fourier-series expansion of a periodical rectangular wave with different pulse width characterized by a duty ratio used in a harmonic balance simulator. The harmonic order is set to 100.

The optimization procedure can also be applied with respect to the efficiency as an optimization parameter. Since the simulation time is very short, a number of iterations can be increased significantly to provide better calculation accuracy. Fig. 10.18 shows the normalized switch (*a*) voltage and (*b*) current waveforms obtained for the idealized optimum or nominal parameters of the Class-FE load network given by Eqs. (10.75)–(10.77) with a dead time $\tau_d = 45$ degrees or duty ratio (or cycle) $D = 0.375$ defined as the ratio of the switch-on time to one period of the switching frequency. The simulated waveforms of the currents flowing into the quarterwave transmission line and shunt capacitor are shown in Fig. 10.19A and Fig. 10.19B, respectively.

Unlike the time-domain simulations, the smoother transitions between the positions take place when the switch is turned on and the switch is turned off and vice versa. Nevertheless, for $r_{sat}/R = 0.01$ and lossless circuit elements except load resistance R, the efficiency is equal to 98.2%, and the simulated normalized switch and load-network voltage and current waveforms are similar to the same theoretical waveforms shown in Fig. 10.15.

Fig. 10.20 shows the circuit schematic of a Class-FE PA with a series quarterwave transmission line consisting of a shunt capacitor C, a series quarterwave transmission line loaded by a parallel resonant L_0C_0 circuit tuned to the fundamental frequency, a shunt capacitor C_L, and a load resistor R_L. In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The RF choke is necessary to isolate DC power supply from RF circuit, whereas the blocking capacitor C_b is necessary to separate DC supply circuit from the load network. The operation principle of such a Class-FE PA with a series quarterwave line is

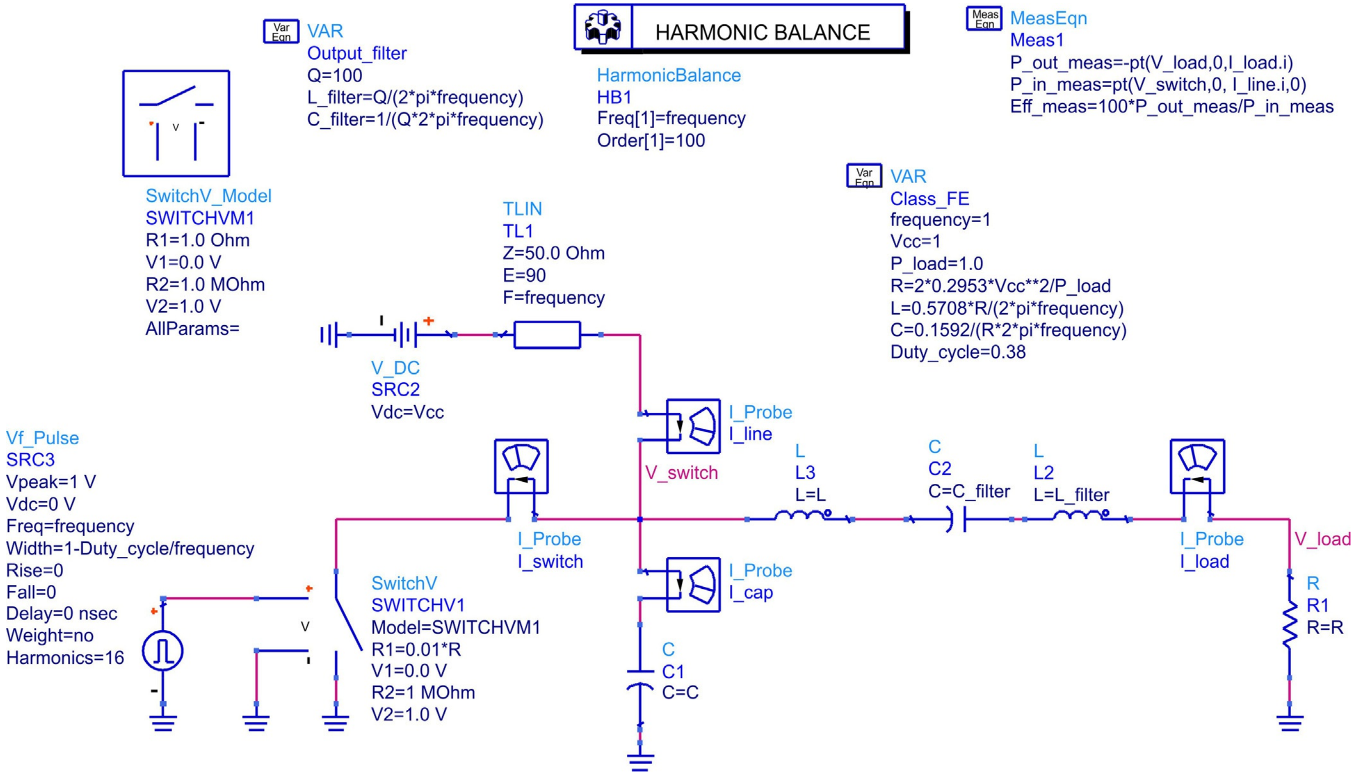

VAR
Output_filter
Q=100
L_filter=Q/(2*pi*frequency)
C_filter=1/(Q*2*pi*frequency)
HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=frequency
Order[1]=100
MeasEqn
Meas1
P_out_meas=-pt(V_load,0,I_load.i)
P_in_meas=pt(V_switch,0, I_line.i,0)
Eff_meas=100*P_out_meas/P_in_meas
SwitchV_Model
SWITCHVM1
R1=1.0 Ohm
V1=0.0 V
R2=1.0 MOhm
V2=1.0 V
AllParams=
TLIN
TL1
Z=50.0 Ohm
E=90
F=frequency
VAR
Class_FE
frequency=1
Vcc=1
P_load=1.0
R=2*0.2953*Vcc**2/P_load
L=0.5708*R/(2*pi*frequency)
C=0.1592/(R*2*pi*frequency)
Duty_cycle=0.38
V_DC
SRC2
Vdc=Vcc
I_Probe
I_line
Vf_Pulse
SRC3
Vpeak=1 V
Vdc=0 V
Freq=frequency
Width=1-Duty_cycle/frequency
Rise=0
Fall=0
Delay=0 nsec
Weight=no
Harmonics=16
V_switch
L
L3
L=L
C
C2
C=C_filter
L
L2
L=L_filter
I_Probe
I_switch
I_Probe
I_load
V_load
SwitchV
SWITCHV1
Model=SWITCHVM1
R1=0.01*R
V1=0.0 V
R2=1 MOhm
V2=1.0 V
I_Probe
I_cap
R
R1
R=R
C
C1
C=C

FIG. 10.17

Simulation setup for idealized Class-FE mode in frequency domain.

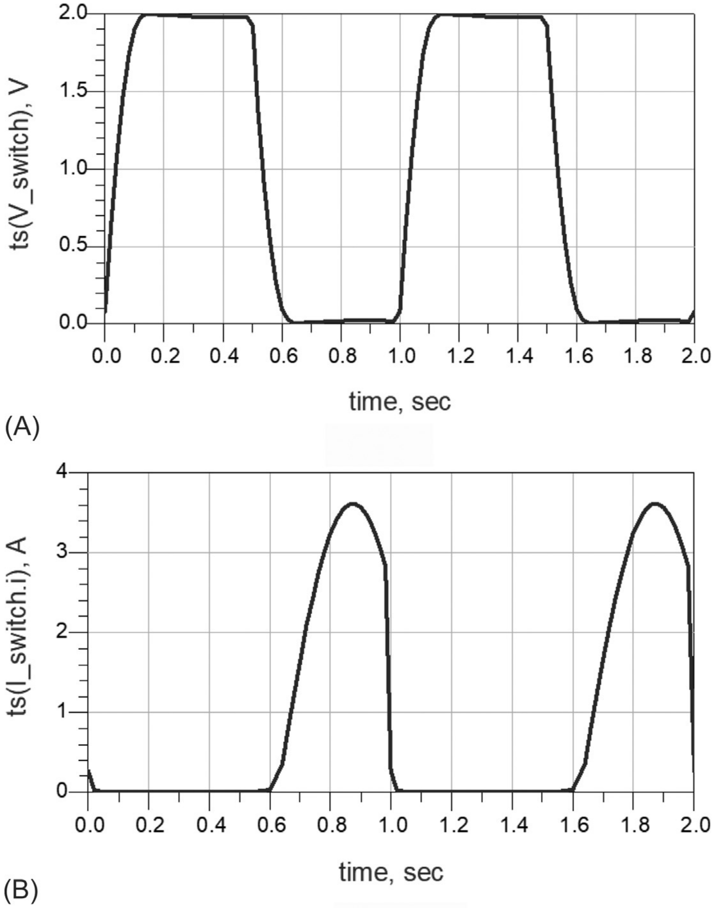


FIG. 10.18

Simulated Class-FE switch voltage and current waveforms.

similar to that with a parallel quarterwave line, assuming that the parallel L_0C_0 filter is ideal having infinite impedance at the fundamental frequency and zero impedances at the second- and higher-order harmonic components. In this case, the short circuit on the load side of the quarterwave transmission line produces a short circuit at its input for even harmonics and open circuit at its input for odd harmonics, with resistive load at the fundamental frequency.

Unlike the parallel quarterwave transmission line, a series quarterwave transmission line can serve as an impedance transformer at the fundamental frequency. In this case, there is no need for an additional output impedance matching circuit required for a Class-FE PA with a parallel quarterwave transmission line. The impedance Z_{in} at the input of the loaded quarterwave transmission line with the characteristic impedance Z_0 and electrical length θ at the fundamental frequency can be written as

$$Z_{\text{in}} = Z_0 \frac{Z_{\text{L}} + jZ_0 \tan\theta}{Z_0 + jZ_{\text{L}} \tan\theta}\bigg|_{\theta=90^\circ} = \frac{Z_0^2}{Z_{\text{L}}} \tag{10.81}$$

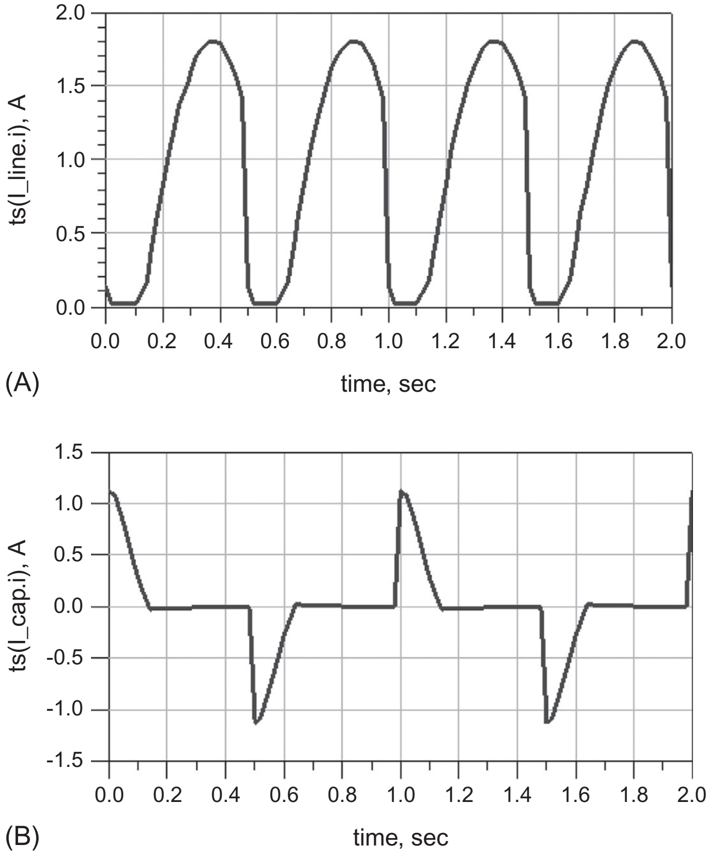


FIG. 10.19

Simulated Class-FE load-network current waveforms.

where

$$Z_L = \frac{R_L}{1 + j\omega C_L R_L} \tag{10.82}$$

Separating Eq. (10.81) into real and imaginary parts enables the standard load resistance R_L and shunt capacitance C_L to be expressed through the optimum load resistance R and series inductance L corresponding to the Class-FE mode according to Eqs. (10.76) and (10.77) for a particular value of the transmission-line characteristic impedance Z_0 as

$$R_L = \frac{Z_0^2}{R} \tag{10.83}$$

$$C_L = \frac{L}{Z_0^2} \tag{10.84}$$

The total series inductances $L + L_0$ in the load network of a Class-FE PA shown in Fig. 10.13B typically has a large value accompanied by high parasitic series resistance and low self-resonant frequency.

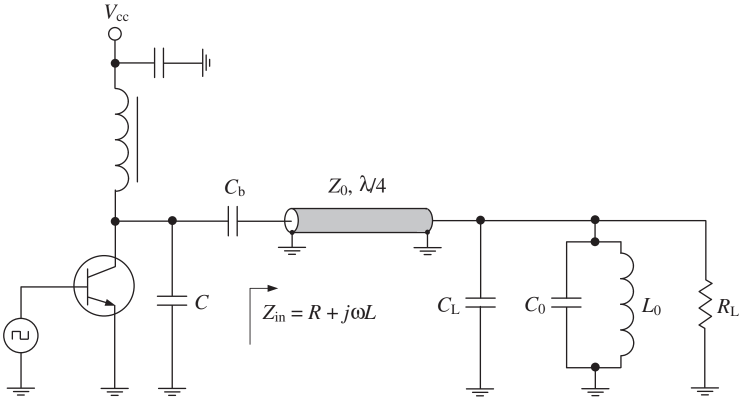


FIG. 10.20

Schematic of Class-FE PA with series quarterwave transmission line.

Fig. 10.21A shows the circuit schematic of a Class-E_3F (or Class-FE_3) with a reduced synthesized inductance value where the tank L_3C_3 circuit is tuned to the third-harmonic component to provide an open-circuit condition.[16] Since the impedance of the tank circuit is inductive at the fundamental, the equivalent series inductor L_1 (which is a part of total series inductance $L + L_1$) together with the shunt capacitor C_1 represents a simple L-type output matching circuit at the fundamental. In this case, close to the ideal Class-FE voltage waveform at the collector is provided by the quarterwave transmission line suppressing even harmonics and open-circuit tank for the third-harmonic open-circuit condition.

The values of an inductance L_3 and a capacitance C_3 can be calculated from

$$L_3 = \frac{8}{9}(L + L_1) \tag{10.85}$$

$$C_3 = \frac{1}{9\omega_0^2 L_3} \tag{10.86}$$

where an equivalent series inductance L_1 and a shunt capacitance C_1 required to match the optimum Class-FE load resistance R defined by Eq. (10.77) and standard load resistance R_L can be obtained by

$$L_1 = \frac{R}{\omega_0}\sqrt{\frac{R_L}{R} - 1} \tag{10.87}$$

$$C_1 = \frac{1}{\omega_0 R_L}\sqrt{\frac{R_L}{R} - 1} \tag{10.88}$$

The transmission-line implementation of a Class-FE PA is shown in Fig. 10.21B.[16] Since the transmission-line load network controls only the first three harmonics with an inductive impedance at the fundamental, a short-circuit termination for the second harmonic, and an open-circuit condition for the third harmonic, such a transmission-line Class-FE approximation is called the Class-E_3F_2 PA. Unlike the schematics with a parallel quarterwave transmission line, this topology incorporates a series inductance L so as to eliminate the effect that the parasitic device output bondwire and package lead inductance has on the amplifier performance at high frequencies. At the third-harmonic frequency, the first series transmission-line and open-circuit stub, both having an electrical length of 90 degrees at $3f_0$,

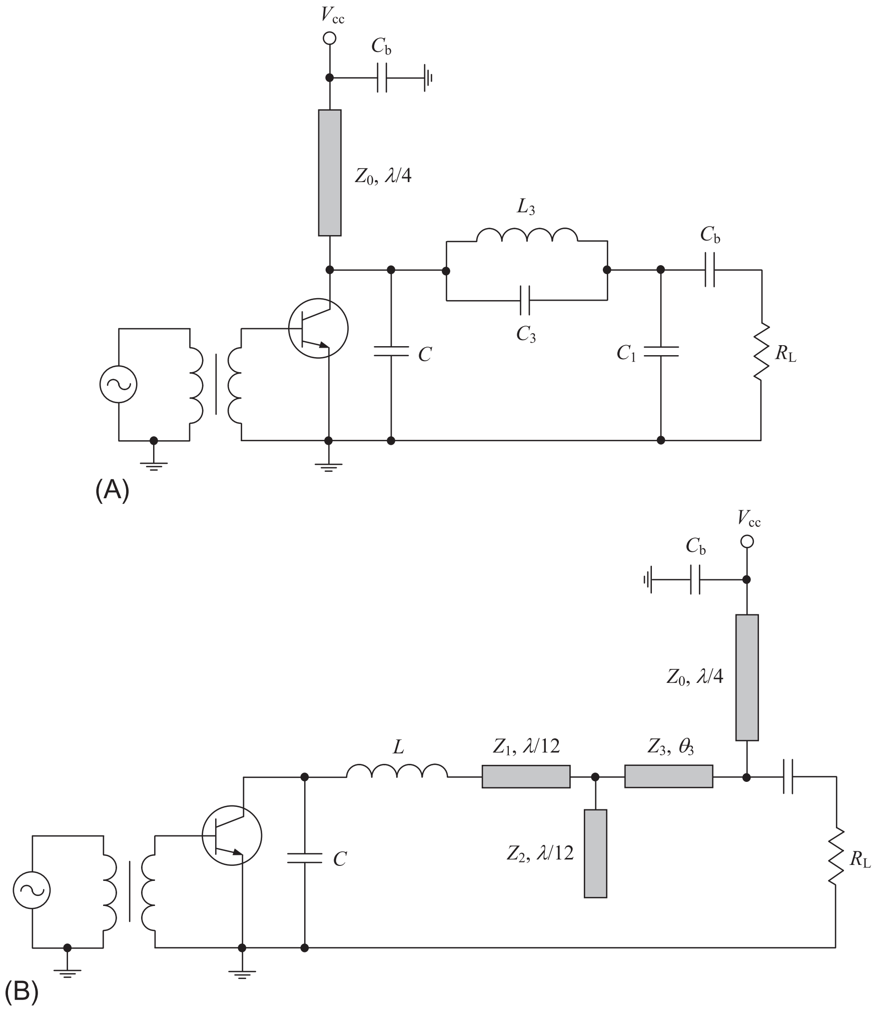


FIG. 10.21

Schematics of Class-E$_3$F and Class-E$_3$F$_2$ PAs.

provide an open-circuit condition seen by the inductor L. At the second-harmonic frequency, the quarterwave transmission line creates a short-circuit condition for the series transmission line with an electrical length θ_3, thus providing its input inductive reactance. Since the open-circuit stub has a capacitive reactance when its electrical length is 60 degrees, both the short- and open-circuit transmission lines represent a second-harmonic tank. As a result, the first series open-circuited transmission line with an electrical length of 60 degrees behaving as a capacitor provides with a series inductor L a short circuit seen by the device collector. In this case, the transmission-line characteristic impedances Z_1 and Z_2 can be defined as

$$Z_1 = \sqrt{3} Z_3 \tan 2\theta_3 \tag{10.89}$$

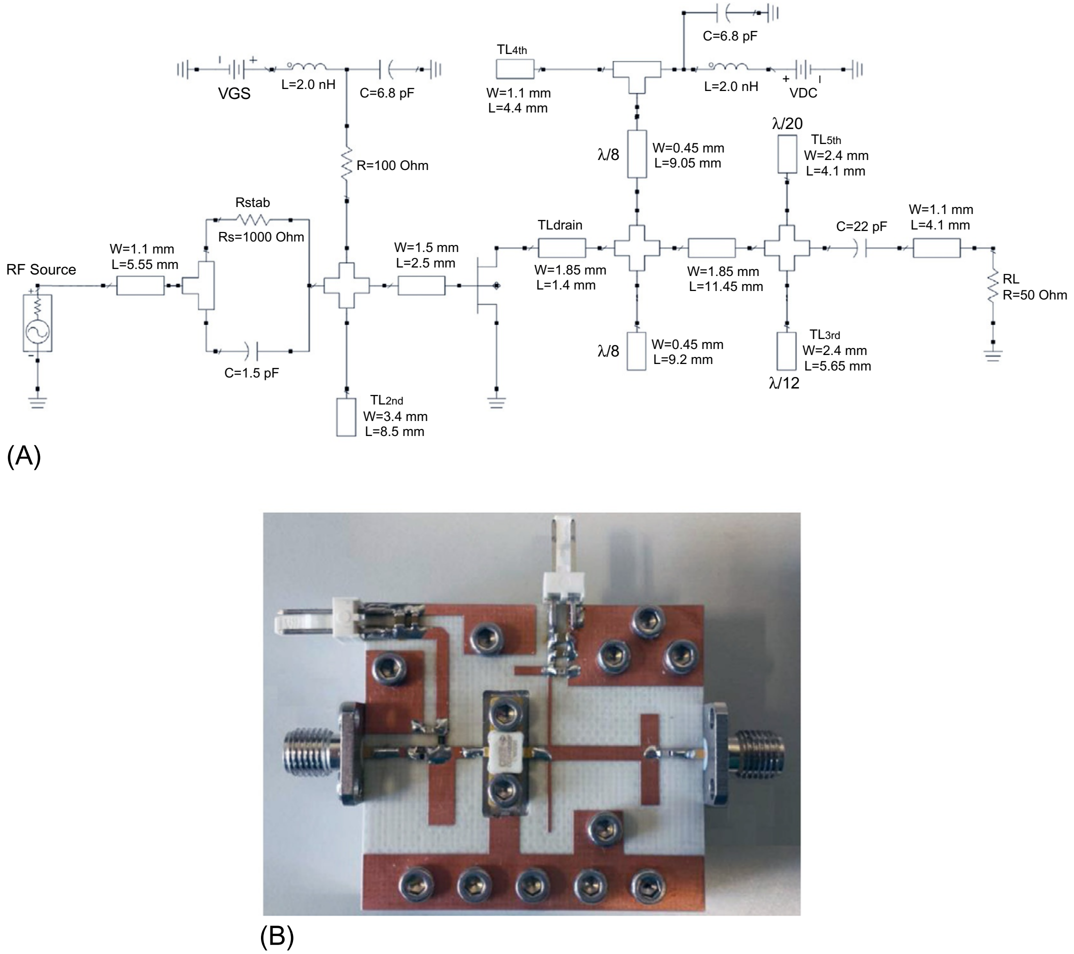

VGS
L=2.0 nH
C=6.8 pF
R=100 Ohm
Rstab
Rs=1000 Ohm
C=1.5 pF
RF Source
W=1.1 mm
L=5.55 mm
W=1.5 mm
L=2.5 mm
TL2nd
W=3.4 mm
L=8.5 mm
TL4th
W=1.1 mm
L=4.4 mm
C=6.8 pF
L=2.0 nH
VDC
λ/8
W=0.45 mm
L=9.05 mm
λ/20
TL5th
W=2.4 mm
L=4.1 mm
TLdrain
W=1.85 mm
L=1.4 mm
W=1.85 mm
L=11.45 mm
C=22 pF
W=1.1 mm
L=4.1 mm
RL
R=50 Ohm
λ/8
W=0.45 mm
L=9.2 mm
TL3rd
W=2.4 mm
L=5.65 mm
λ/12
(A)
(B)

FIG. 10.22

Circuit schematic and test board of transmission-line Class-EF PA with third-harmonic peaking.[17]

$$Z_2 = 2\sqrt{3}\,\omega_0 L \tag{10.90}$$

where the inductance L can be calculated from Eq. (10.76).

To improve the bandwidth properties of the Class-FE PA with a quarterwave line, the $\lambda/8$ open-circuit and short-circuit stubs can be used instead of a parallel $\lambda/4$ transmission line. At the fundamental frequency, $\lambda/8$ open-circuit stub behaves like a shunt capacitor, whereas a $\lambda/8$ short-circuit stub behaves like a shunt inductor, thus resulting in a parallel resonant circuit, and together they facilitate better and wider short-circuit termination at all even harmonics compared to that provided by a $\lambda/4$ transmission line. Fig. 10.22A shows the simulation setup of a transmission-line third-harmonic-peaking Class-EF PA with RC stabilizing circuit at the input.[17] At the third harmonic, $\lambda/12$ open-circuit stub in the load network provides a short-circuit termination to the series transmission line which behaves like an inductance together with TL_{drain}. This inductance should resonate with a drain-source capacitance of the transistor to provide the required Class-EF open circuit at the third harmonic. Here, $\lambda/20$ open-circuit stub is added to improve suppression at the fifth harmonic. In this case, the series line and two open-circuit stubs compose the L-type output matching circuit with series inductance and shunt capacitance. The test board of the transmission-line Class-EF PA with third-harmonic peaking based on a CGH40010F GaN HEMT device is shown in Fig. 10.22B. The maximum drain efficiency of 91% and a power-added efficiency (*PAE*) of 80% with an output power of 39.5 dBm and a power gain of 9.2 dB were measured at an operating frequency of 2.22 GHz. At the same time, the PA was able to deliver an output power of 38.8 ± 1.5 dBm with a drain efficiency of at least 58% across the frequency bandwidth of 1.82–2.28 GHz.

In special applications when it is difficult to implement a quarterwave line, for example, in monolithic integrated circuits or at sufficiently low frequencies, it is possible to consider a Class-FE approximation based on the lumped resonant circuits. Fig. 10.23A shows the circuit schematic of a Class-FE PA with a second-harmonic control using an additional series resonant circuit L_2C_2 which provides a short circuit for the second harmonic at the device drain.[18, 19] Such a load network corresponds to Class-EF$_2$ (or Class-F$_2$E) when, for a second-harmonic short-circuit termination, the idealized optimum Class-E zero-voltage and zero voltage-derivative conditions are satisfied at the end of period, as shown in Fig. 10.23B for the duty ratio $D = 0.35$. From comparison of the theoretical and simulated output voltage and current waveforms shown in Figs. 10.15 and 10.18 for a general Class-FE and in Fig. 10.23B for a second-harmonic Class-EF$_2$, respectively, it follows that, if the voltage peak factors for both cases are practically the same, however the peak current value for the latter case is substantially higher. In addition, the higher duty ratio is used, the higher voltage peak factor of the Class-EF$_2$ mode is achieved, approaching the factor of 4 for duty ratios close to $D = 0.5$.[18] As a result, for a duty ratio $D = 0.3$, an output power of over 500 W with a drain efficiency above 92% was achieved at a switching frequency of 30 MHz using a 500-V vertical MOSFET device.[19] However, for duty ratios >0.5, it is preferable to use a Class-E/F$_3$ mode where the series resonant circuit L_2C_2 represents a third-harmonic short circuit, resulting in a third-harmonic approximation of a Class-E/F where the Class-E idealized optimum conditions are applied to an inverse Class-F. For example, when $D = 0.55$, the peak factor of the flattened drain voltage waveform only slightly exceeds the factor of 3.[18]

Fig. 10.24 shows the circuit schematic of a Class-EF$_2$ PA with two parallel resonant *LC* circuits tuned to the fundamental and third harmonic components, respectively. In this case, to provide the short-circuit condition at the second-harmonic frequency, the parameters of these resonant circuits must be properly optimized. The network impedance Z_{net} at the input of two cascaded tank circuits tuned to fundamental ($\omega = \omega_0$) and third harmonic ($\omega = 3\omega_0$) that provides the open-circuit conditions for these components, respectively, can be written as

$$Z_{\text{net}} = \frac{j\omega L_1}{1 - \omega^2 L_1 C_1} + \frac{j\omega L_2}{1 - \omega^2 L_2 C_2} \tag{10.91}$$

To provide the short-circuit condition at the second harmonic ($\omega = 2\omega_0$), Eq. (10.91) can be rewritten in the form

$$Z_{\text{net}}(2\omega_0) = \frac{j2\omega_0 L_1}{1 - 4\omega_0^2 L_1 C_1} + \frac{j2\omega_0 L_2}{1 - 4\omega_0^2 L_2 C_2} = 0 \tag{10.92}$$

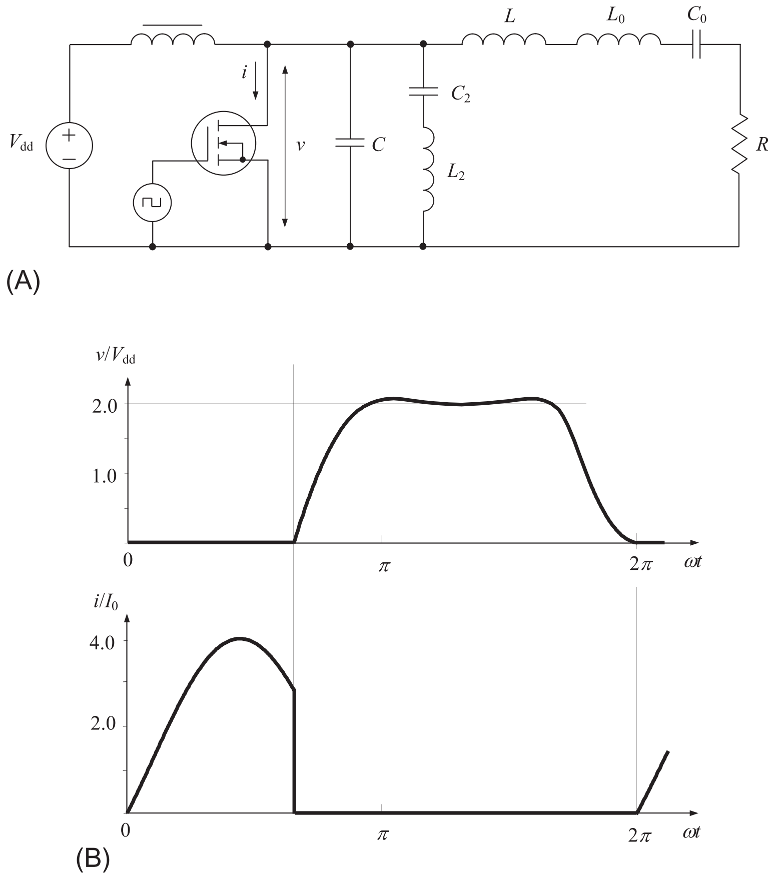


FIG. 10.23

Class-EF$_2$ PA and corresponding optimum drain waveforms.

As a result, the ratios between the circuit elements for a certain value of C_1 are expressed as

$$L_1 = \frac{1}{\omega_0^2 C_1} \tag{10.93}$$

$$L_2 = \frac{5}{27} L_1 \tag{10.94}$$

$$C_2 = \frac{1}{9\omega_0^2 L_2} \tag{10.95}$$

Fig. 10.25A shows the circuit schematic of a Class-E$_3$F$_2$ PA where short-circuit and open-circuit conditions are presented to the device drain at the second (Class-F$_2$) and third (Class-E$_3$) harmonics, respectively.[20] Here, the L_2C_2 resonator is tuned to the second harmonic to provide a short to the ground. At the third harmonic, the reactance formed by the L_2C_2 resonator is inductive and forms a

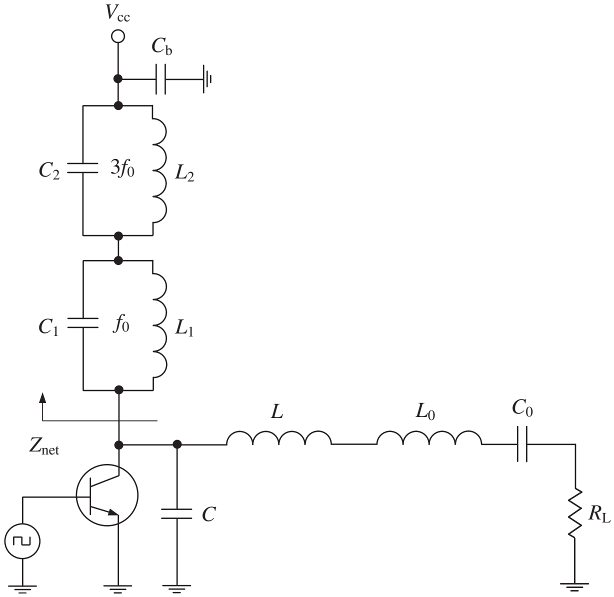


FIG. 10.24

Class-EF$_2$ with two parallel resonant circuits.

parallel third-harmonic resonator with the capacitance C_1 and inductance L_1. However, the L_2C_2 branch becomes capacitive at the fundamental creating an open-circuited condition with the capacitance C_1 and inductance L_1. As a result, the ratios between the Class-E$_3$F$_2$ load-network parameters can be derived as

$$C_1 = \frac{4}{9\omega_0^2 L_1} \quad C_2 = \frac{1}{9\omega_0^2 L_2} \tag{10.96}$$

$$L_2 = \frac{3}{5} L_1 \tag{10.97}$$

$$C_2 = \frac{15}{16} C_1 \tag{10.98}$$

assuming that the inductance L_1 provides the required optimum inductive impedance at the fundamental to fully discharge the shunt capacitor during the dead time according to Eq. (10.10), and the L_3C_3 resonator is tuned to the third harmonic. The simulated idealized drain voltage and current waveforms are shown in Fig. 10.25B, where the quasi-rectangular voltage waveform is similar to that of the Class-F with the second- and third-harmonic control, whereas the current waveform corresponds to the Class-E with almost instantaneous drop to zero at the moment when the device is turned off.[20]

Fig. 10.26A shows the circuit schematic of a two-stage cascode Class-E$_3$F$_2$ PA using a 65-nm CMOS technology, where the driver stage is operated in an inverse Class-B mode to approximate the rectangular driving waveform for faster switching.[20] For reliable and efficient operation, a

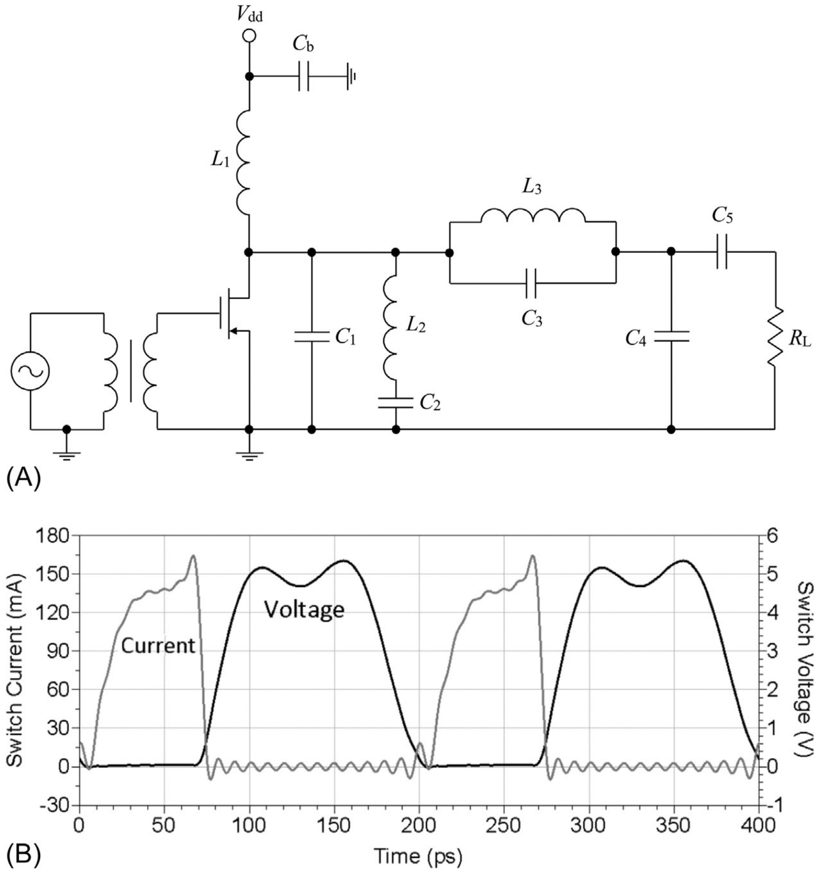


FIG. 10.25

Basic circuit schematic of Class-E_3F_2 PA and drain voltage and current waveforms.

mixed-voltage cascode topology was selected, which is comprised of a fast low-voltage common-source transistor and a higher-voltage common-gate transistor, when the common-source transistor can switch faster to achieve higher efficiency while the common-gate transistor enables the use of higher DC-supply voltages. The drain DC bias of the driver stage is applied directly to the gate of the second stage that significantly simplifies the interstage network. The series L_6C_8 circuit is used to compensate for the parasitic output capacitance of the common-source device. A T-type network is used to match the optimum inductive load impedance at the fundamental with a 50-Ω load when the required series inductance is provided by the third-harmonic L_3C_3 resonator having an inductive reactance at the fundamental. As a result, an output power of 21 dBm with a *PAE* of 51% and a power gain of 26 dB was simulated at an operating frequency of 5 GHz.

In a two-stage cascode Class-EF_2 CMOS PA, whose circuit schematic is shown in Fig. 10.26B, the series L_2C_2 circuit is tuned to the second harmonic to provide a short circuit to the ground at the second harmonic.[21] Here, the driver stage operated in a Class-AB mode amplifies the input signal with correct

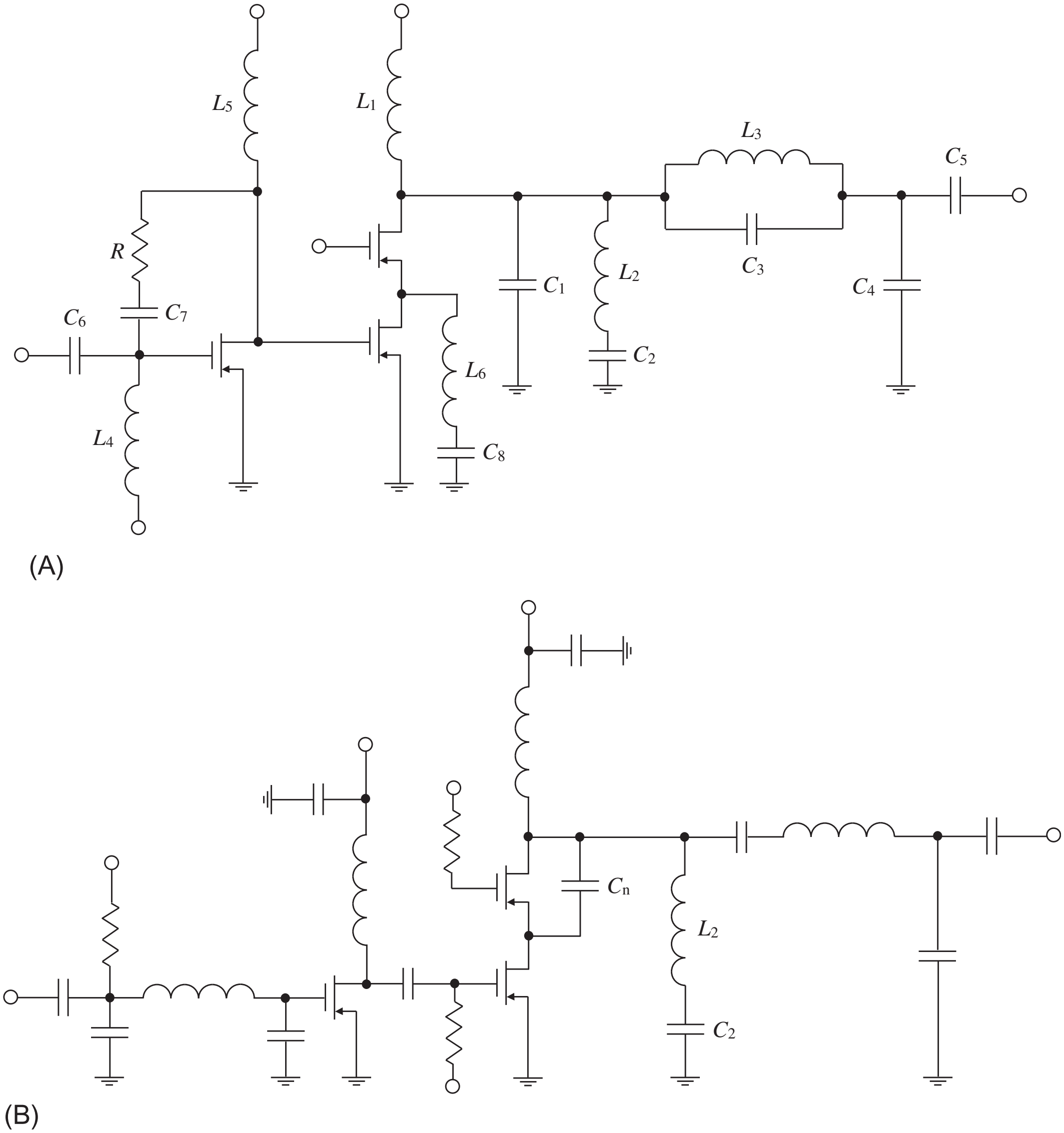


FIG. 10.26

Circuit schematics of two-stage cascode (A) Class-E$_3$F$_2$ and (B) Class-EF$_2$ CMOS PAs.

duty ratio to drive the cascode stage. The drain-bulk parasitic capacitance C_n of the common-gate transistor is used to implement the capacitance across the switch. As a result, being implemented in a standard 0.13-μm CMOS process, such a PA was able to achieve an output power of 19 dBm, a power gain of 31 dB, and a *PAE* of 32% at an operating frequency of 2.5 GHz using a 2-V DC-supply voltage, with the harmonic suppression better than 33 dB.

The theoretical switch voltage and current waveforms for different $k = C_1/C_2$ and $q_1 = 1/\omega\sqrt{L_2C_2}$ when an additional series inductive reactance is included in the load network with a series-tuned resonant circuit to provide idealized switching conditions are given in,[22] where the switch voltage and current waveforms for $k = 1$ and $q_1 = 2$ are similar to those shown in Fig. 10.25B. Generally, very high drain efficiencies were measured for a 23-W MOSFET Class-EF$_2$ PA for different k using the current probe with accuracy of 2%: 91.1% for $k = 0.867$ at 6.78 MHz and 88.7% for $k = 1.567$ at 8.6 MHz. Note that the Class-EF PAs can maintain zero-voltage switching condition corresponding to high operation efficiency across a wide load range when the series L_2C_2 circuit is tuned in between the fundamental and the second harmonic, which is very important for wireless power transfer (WPT) applications.[23]

10.3 Class-E/F PAs

When comparing Class-E to its two counterparts such as conventional Class-F and inverse Class-F, both advantages and disadvantages can be found with respect to each class. For example, using a switchmode Class-E can result in high operation efficiency with a simple load network, whereas an efficiency improvement by using a Class-F is achieved at the expense of the circuit complexity. Even with tuning up to seventh-harmonic component, the collector (or drain) voltage and current waveforms exhibit significant overlapping, and the maximum theoretical collector efficiency cannot exceed 90%. The switching speed of the Class-E PA is limited only by the active device, provided the optimum parameters of the load network are properly set. However, the switching speed of the Class-F PA is defined by both the active device and a limited number of the controlled harmonic components composing the collector voltage and current waveforms. In addition, Class-E can incorporate the device output capacitance into the load-network topology, but a large capacitance becomes a limiting factor at high frequencies. In the presence of large output capacitance, it is possible to realize a simple Class-F topology with control of only a few harmonics. However, the collector voltage peak factor in a Class-F mode cannot exceed a maximum value of 2, while the maximum collector voltage peak factor in a Class-E mode can be >3.5.

Fig. 10.27 shows the generalized block schematic of a switchmode Class-E/F PA where zero-voltage and zero voltage-derivative conditions corresponding to Class-E mode can be used to eliminate discharge loss of the shunt capacitance, and harmonic tuning can be provided by using the resonant circuits tuned to selected harmonic components approximating Class-F mode with improved collector waveforms.[24] Each resonant circuit or filter presents a desired impedance at the corresponding harmonic component that it tunes, while leaving other harmonics unaffected. Consequently, the load network describes a family of switching PAs, for which the impedance seen by the switch is capacitive at all harmonics, except for a selected number of tuned harmonics.

To achieve Class-E optimum conditions, the choice of an inverse Class-F mode is natural to provide mixed Class-E/F mode since it provides a zero-voltage condition for a half-sinusoidal collector voltage waveform, unlike the conventional Class-F, which presents voltage discontinuity at the switching instant in the ideal case of infinite harmonic tuning. The Class-E/F name is chosen to indicate that this mixed mode is based on Class-E and inverse Class-F (or Class-1/F) rather than the conventional Class-F. Generally, some selection for even harmonics may be open circuited, some selection of odd harmonics may be short circuited, and the remaining harmonics are presented with a fixed capacitance. According to a Class-E mode, the load resistance R, shunt capacitance C, and series inductance L

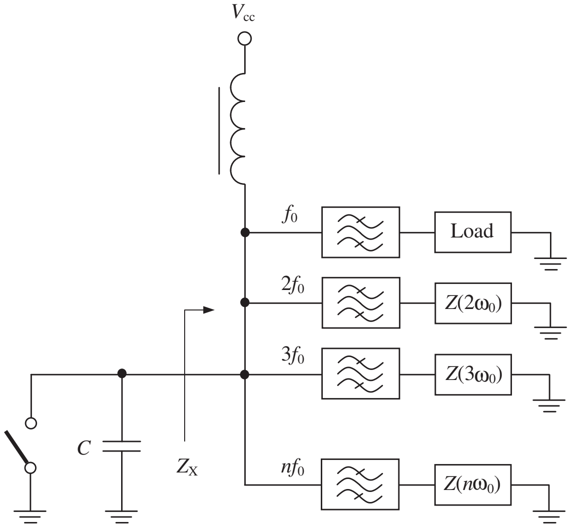


FIG. 10.27

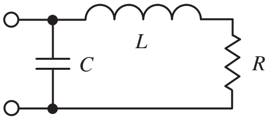
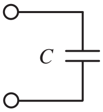
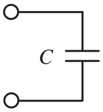
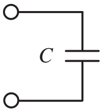
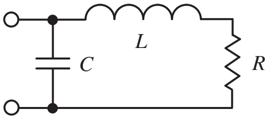
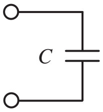
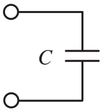
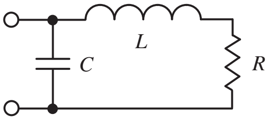
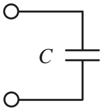
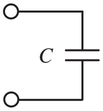
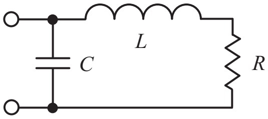
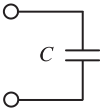
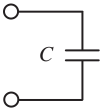
Generalized block schematic of harmonic-tuned Class-E/F PA.

shown in Table 10.2 are adjusted at the fundamental frequency to achieve the required inductive impedance to obtain the overall zero-voltage and zero voltage-derivative conditions in an ideal case with different tuning at the harmonics. To differentiate these harmonic tunings between each other, different names can be used of the form Class-E/$F_{n1,n2,n3,\ldots}$, where the numerical subscripts indicate the number of tuned harmonics in an inverse Class-F mode. Table 10.2 shows the load-network harmonic-impedance specifications of several Class-E/F PAs. Even-harmonic tuning tends to primarily affect the current waveform, whereas odd-harmonic tuning tends to have the most effect on the voltage waveform. As a result, tuning of several harmonics can minimize the peak voltage amplitude with current waveform approximating a square wave. The minimum peak factor of 3.08 is realized for Class-E/$F_{2,3,4}$, which is lower than that of 3.12 in an inverse Class-F and much lower than that of 3.56 in a Class-E with shunt capacitance.

10.3.1 Symmetrical push–pull configurations

In practice, it is difficult to eliminate the effects of the resonant circuits tuned to different harmonics on each other. For example, if a series resonator is tuned to create a short circuit for the third-harmonic component in a Class-E/F_3 mode, it will present a capacitance at the second harmonic, reducing the second-harmonic impedance and degrading the voltage waveform. In this case, either a very high loaded quality factor of this resonator is required, or additional resonances must be introduced into the circuit. The easiest and most convenient way to separate the effects of even and odd harmonics is to use a symmetrical push–pull switching PA configuration. By using the effects of a virtual ground for odd harmonics and a virtual open for even harmonics, a push–pull Class-E/F_3 PA can be constructed by placing the third-harmonic short circuit as a differential load. In this case, the shorting of the third

Table 10.2 Optimum Class-E/F impedances at fundamental and harmonics.

Class-E/F type	f_0 (fundamental)	$2f_0$	$3f_0$	$4f_0$	nf_0, $n = 5, 6, \ldots$
Class-E/F_3			short		
Class-E/$F_{2,3}$		open	short		
Class-E/$F_{2,4}$		open		open	
Class-E/$F_{3,4}$			short	open	

harmonic can be provided by a low-Q_L resonator without reducing the impedances at any even harmonics. Similar strategy may be used to selectively tune the impedances at even harmonics. Fig. 10.28A shows the Class-E/F_{odd} circuit implementation with short-circuiting of all odd harmonics by placing a differential short circuit between two switches.[24] To avoid the short circuiting of a fundamental-frequency component, a bandstop filter such as a parallel *LC* tank can be used to provide a differential short circuit at all odd harmonics other than the fundamental.

The bandstop filter between two switches forces the differential voltage v_2 - v_1 to be sinusoidal,

$$v_2(\omega t) - v_1(\omega t) = V \sin(\omega t + \varphi) \tag{10.99}$$

where V is the differential voltage amplitude and φ is the arbitrary initial phase shift.

Since one of the switches is always turned on during half a period and has zero voltage across it for an idealized case, the voltages v_1 and v_2 can be written, respectively, as

$$v_1(\omega t) = \begin{cases} 0 & 0 \le \omega t \le \pi \\ -V \sin(\omega t + \varphi) & \pi \le \omega t \le 2\pi \end{cases} \tag{10.100}$$

and

$$v_2(\omega t) = \begin{cases} V \sin(\omega t + \varphi) & 0 \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi \end{cases} \tag{10.101}$$

where V is the drain voltage amplitude and V_{cc} is the DC-supply voltage.

According to Class-E zero-voltage switching conditions, both voltages must be equal to zero at turn-on, resulting in the only trivial solution for φ to be zero. This means that the properly tuned switch voltages v_1 and v_2 are purely half-sinusoidal. Since each switch is connected to the DC-supply voltage

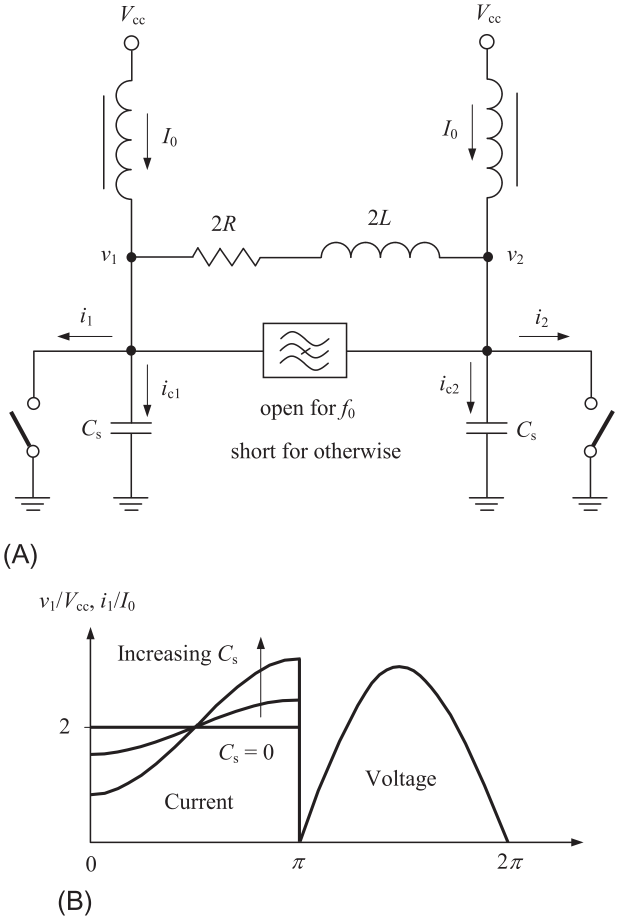

V_{cc}
V_{cc}
I_0
I_0
$2R$
$2L$
v_1
v_2
i_1
i_2
i_{c1}
i_{c2}
C_s
C_s
open for f_0
short for otherwise
(A)
v_1/V_{cc}, i_1/I_0
Increasing C_s
2
$C_s = 0$
Voltage
Current
0
π
2π
(B)

FIG. 10.28

Class-E/F$_{odd}$ circuit implementation and collector waveforms.

through the RF choke, the DC voltage of each switch voltage waveform is the supply voltage V_{cc}. Then, the peak voltage for a half-sine waveform can be written as $V = \pi V_{cc}$.

As a result, the currents i_{c1} and i_{c2} flowing through linear shunt capacitors can be obtained, respectively, by

$$i_{c1}(\omega t) = C_s \frac{dv_1(\omega t)}{d\omega t} = \begin{cases} 0 & 0 \le \omega t \le \pi \\ -\pi V_{cc} C_s \cos \omega t & \pi \le \omega t \le 2\pi \end{cases} \tag{10.102}$$

and

$$i_{c2}(\omega t) = C_s \frac{dv_2(\omega t)}{d\omega t} = \begin{cases} \pi V_{cc} C_s \cos \omega t & 0 \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi \end{cases} \tag{10.103}$$

During each one-half period, one of the transistors is open-circuited, while the other transistor is short-circuited. Hence, the switch currents i_1 and i_2 can be written, respectively, as

$$i_1(\omega t) = \begin{cases} 2I_0 - i_{c2}(\omega t) & 0 \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi \end{cases} \tag{10.104}$$

and

$$i_2(\omega t) = \begin{cases} 0 & 0 \le \omega t \le \pi \\ 2I_0 - i_{c1}(\omega t) & \pi \le \omega t \le 2\pi \end{cases} \tag{10.105}$$

The switch voltage and current waveforms for various values of the shunt capacitance C_s corresponding to a Class-E/F$_{odd}$ mode are shown in Fig. 10.28B. If the shunt capacitance is zero, the switch current i_1 (or i_2) represents a rectangular waveform corresponding to a well-known current-switching Class-D mode. However, according to Eq. (10.102) and (10.103), the increasing shunt capacitance C_s results in higher current peak values, also changing the shape of a current waveform.

The Class-E/F$_{odd}$ topology shown in Fig. 10.28A can be transformed to a similar circuit schematic with only one RF choke connected between the DC power supply and the center tap of the tank inductor L_1, where C_b is the bypass capacitor, and the resonator composed of the tank inductor L_1 and capacitor C is detuned to have the required inductance at the fundamental frequency to achieve Class-E switching conditions.[25] In some special cases, the RF choke can be replaced by an inductor L_2, as shown in Fig. 10.29A, which can be tuned to resonate with the shunt capacitors at the second harmonic, providing an open circuit to each switch at that frequency similar to a single-ended even-harmonic Class-E mode.[26]

The voltage v_{L_2} across the inductor L_2 can be written as

$$v_{L_2}(\omega t) = \frac{v_1(\omega t) + v_2(\omega t)}{2} = \begin{cases} \dfrac{\pi}{2} V_{cc} \sin\omega t & 0 \le \omega t \le \pi \\ -\dfrac{\pi}{2} V_{cc} \sin\omega t & \pi \le \omega t \le 2\pi \end{cases} \tag{10.106}$$

The current i_{L_2} flowing through the inductor L_2 during each one-half period can be obtained by

$$i_{L_2}(\omega t) = \frac{1}{\omega L_2} \int [V_{cc} - v_{L2}(\omega t)]\, d\omega t = \begin{cases} \dfrac{\pi}{2} \dfrac{V_{cc}}{\omega L_2} \left(\dfrac{2\omega t}{\pi} - 1 + \cos\omega t \right) & 0 \le \omega t \le \pi \\ \dfrac{\pi}{2} \dfrac{V_{cc}}{\omega L_2} \left(2 \dfrac{\omega t - \pi}{\pi} - 1 - \cos\omega t \right) & \pi \le \omega t \le 2\pi \end{cases} \tag{10.107}$$

Then, the switch currents i_1 and i_2 can be found, respectively, from

$$i_1(\omega t) = \begin{cases} i_{L2}(\omega t) - i_{c2}(\omega t) & 0 \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi \end{cases} \tag{10.108}$$

and

$$i_2(\omega t) = \begin{cases} 0 & 0 \le \omega t \le \pi \\ i_{L2}(\omega t) - i_{c1}(\omega t) & \pi \le \omega t \le 2\pi \end{cases} \tag{10.109}$$

where the capacitor currents i_{c1} and i_{c2} are defined by Eqs. (10.102) and (10.103).

The switch voltage and current waveforms for various values of an inductance L_2 corresponding to a Class-E/F$_{2,odd}$ mode are shown in Fig. 10.29B. For each inductance tuning, the voltage waveform is a half-sinusoidal. The current waveforms depend on the even-harmonic tuning and the switch shunt

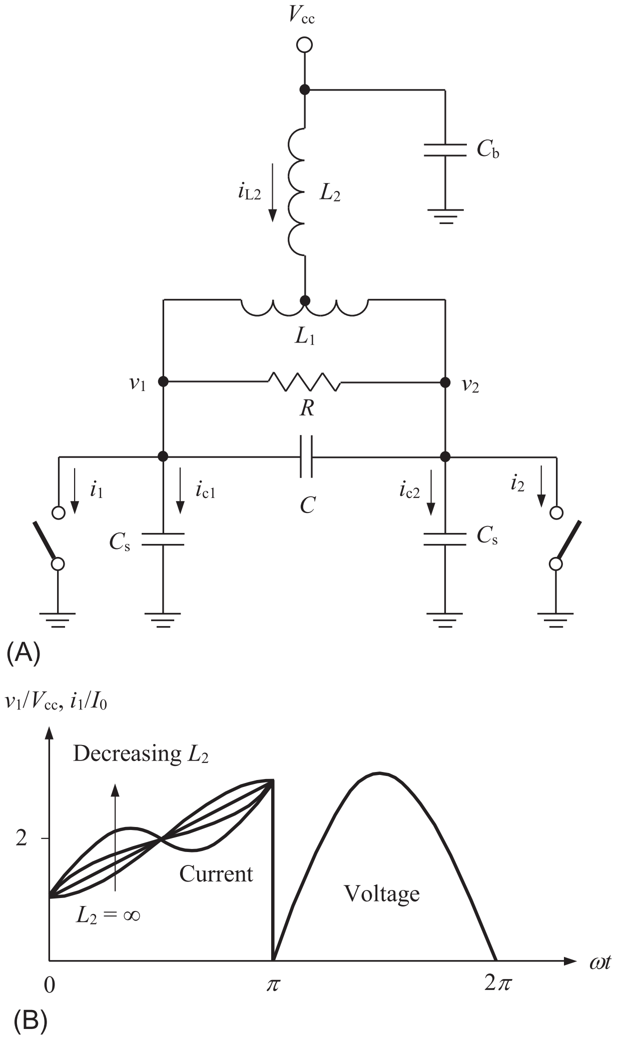

V_{cc}
C_b
i_{L2}
L_2
L_1
v_1
v_2
R
i_1
i_{c1}
C
i_{c2}
i_2
C_s
C_s
(A)
v_1/V_{cc}, i_1/I_0
Decreasing L_2
2
Current
Voltage
$L_2 = \infty$
0
π
2π
ωt
(B)

FIG. 10.29

Class-E/$F_{2,odd}$ PA and collector waveforms.

capacitance. For high values of L_2 corresponding to a basic Class-E/F_{odd} mode, the switch current represents a nearly trapezoidal waveform. However, for low values of L_2 with open-circuit even-harmonic tuning, the switch current approximates more closely the rectangular waveform with peak value at the turn-off switching instant, even for very large values of the shunt capacitance.[24] Classes-E/F_{odd} and E/$F_{2,odd}$ can tolerate twice the shunt capacitance of a Class-E for the same operating frequency, DC-supply voltage, and output power, without having a negative switch current. As a result, the maximum operating frequency can be doubled, compared to a single-ended Class-E mode using the same transistor size.

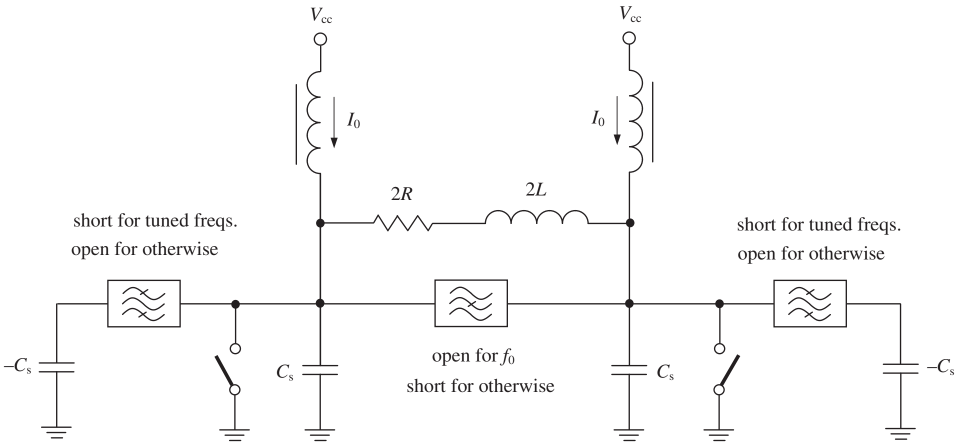


FIG. 10.30

Generalized Class-E/F$_{x,odd}$ circuit implementation.

The tuning of several even harmonics realizing a Class-E/F$_{x,odd}$ operation mode, where x is a set of tuned even harmonics, can be accomplished with the generalized circuit implementation shown in Fig. 10.30, where the additional resonators are connected in parallel to each switch.[24] Each additional resonator can be treated as a bandpass filter placed in series with negative capacitance —C_s. The filter connects this negative capacitance in parallel with the switch shunt capacitance at the tuned even harmonics, thus canceling the capacitance at these frequencies.

Fig. 10.31 shows the schematic of a high-power Class-E/F$_{2,odd}$ MOSFET PA designed to provide an output power of 1 kW at an operating frequency of 7 MHz.[25] The magnetizing inductance of an output air-core transformer was used as the tank inductance of 240 nH. To reduce a ringing transient superimposed on the drain voltage and current waveforms due to parasitic device package inductors resonating with the tank capacitor and drain-source capacitances, the loaded quality factor of the parallel LC resonator was lowered to 3.6. The second-harmonic tuning helps to keep the drain current positive, providing an additional peaking in the early part of the current waveform where the ringing has the highest amplitude. To suppress the third-harmonic component to an acceptable level, a third-harmonic trap was added in series with the load. As a result, the second- and third-harmonic components in the output spectrum were 33 and 35 dB below the fundamental-frequency component, respectively, and all other higher-order harmonic components were at least 40 dB below the fundamental. The Class-E/F$_{2,odd}$ PA exhibited an output power over 1.1 kW with a drain efficiency of 85% and a power gain of 17 dB.

Fig. 10.32 shows the circuit schematic of a high-power dual-band Class-E/F$_{odd}$ MOSFET PA designed to operate in the 7-MHz and 10-MHz frequency bands.[27] The input network consisting of the parallel capacitor C_{in}, parallel inductor L_{in}, balanced-to-unbalanced (balun) impedance transformer T_{in}, and two series inductors L_s converts a source impedance of 50 Ω to balanced impedance conjugately matched to each transistor input. The load network consists of the parallel capacitor C_p, series tank with L_{out} and C_{out}, output air-core transformer T_{out} representing a 1:1 balun, the magnetizing inductance of which is used in the load-network tuning. Such a load network provides an inductive, capacitive, and again inductive reactance as frequency increases, with the inductive reactance at the

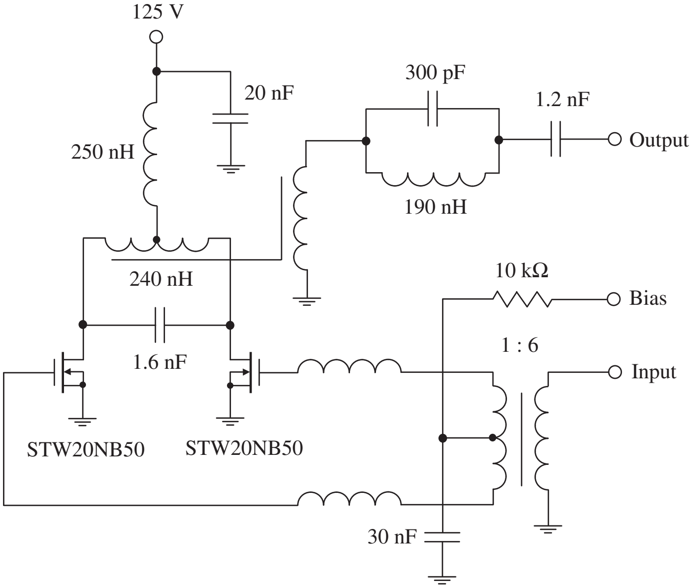

125 V
20 nF
250 nH
300 pF
1.2 nF
Output
190 nH
240 nH
10 kΩ
Bias
1.6 nF
1 : 6
Input
STW20NB50
STW20NB50
30 nF

FIG. 10.31

Schematic of Class-E/F$_{2,\text{odd}}$ PA with third-harmonic trap.

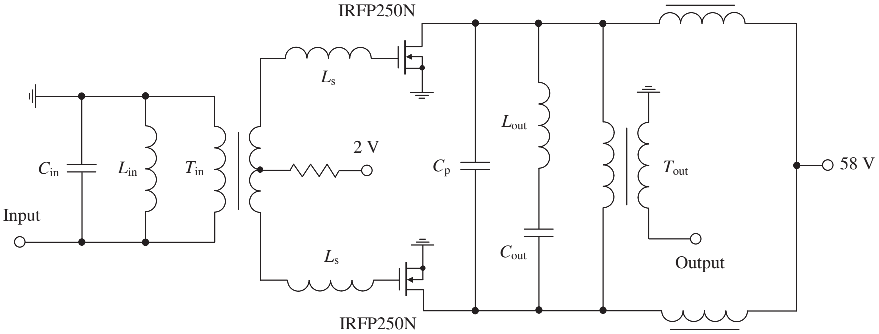

IRFP250N
L_s
C_{in}
L_{in}
T_{in}
2 V
L_{out}
C_p
T_{out}
58 V
Input
C_{out}
L_s
Output
IRFP250N

FIG. 10.32

Schematic of dual-band Class-E/F$_{\text{odd}}$ PA.

fundamental required for zero-voltage switching operation at each frequency band. At all odd harmonics of each frequency of operation, the load network including the device drain-source capacitances provides a low capacitive reactance to ground compared to the load resistance. Due to the differential topology, each transistor is represented only by its own output capacitance at even harmonics. As a result, an output power of 250 W with a drain efficiency of 94% and a power gain of 16 dB was achieved at 7.15 MHz, whereas an output power of 225 W with a drain efficiency of

90% and a power gain of 15 dB was measured at 10.1 MHz. The bandwidth in both bands was sufficient to allow high-efficiency operation from 7.0 to 7.3 MHz and from 10.0 to 10.18 MHz.

10.3.2 Single-ended Class-E/F_3 mode

The optimum parameters of a single-ended Class-E/F_n PA can be determined based on an analytical derivation of its steady-state collector voltage and current waveforms.[28] Fig. 10.33A shows the basic circuit configuration of a Class-E/F_n PA, where the load network consists of a shunt capacitor C, a series resonant L_nC_n circuit tuned to nth harmonic of the fundamental frequency and connected in parallel to the device output, a series inductor L, a series fundamentally tuned L_0C_0 circuit, and a load resistor R. In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The collector of the transistor is connected to the DC power supply by an RF choke with infinite reactance at the fundamental and any higher-order harmonic component. The active device is considered an ideal switch that is driven at the operating frequency so as to provide instantaneous switching between its on-state and off-state operation conditions.

To simplify the analysis of a Class-E/F_n PA, the corresponding equivalent circuit of which is shown in Fig. 10.33B, the same assumptions which were used to analyze a Class-DE or a Class-FE PA are introduced. The nominal Class-E switching conditions for the transistor switch are defined by Eqs. (10.52) and (10.53), where v is the voltage across the switch. Note that these nominal Class-E

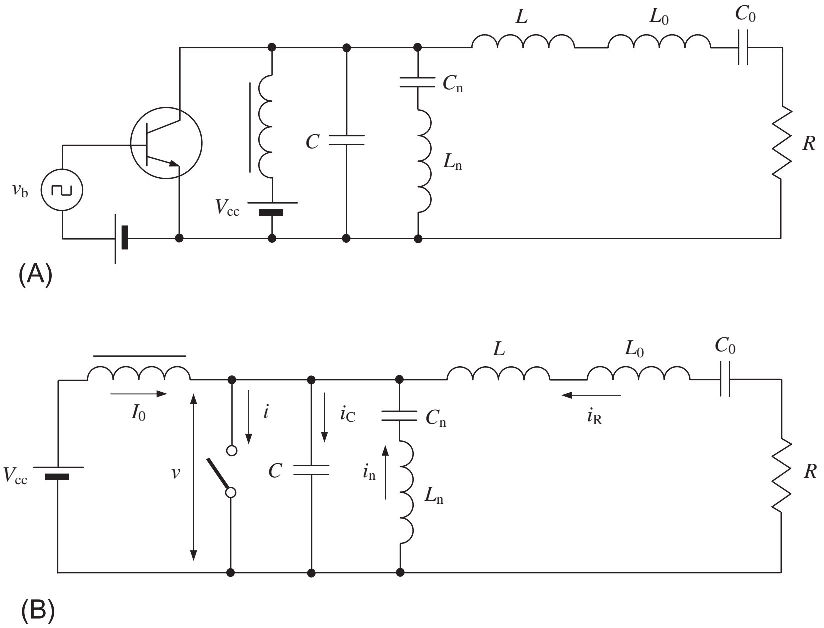


FIG. 10.33

Basic circuits of single-ended Class-E/F_n PA.

switching conditions do not correspond to minimum dissipated power losses for the nonideal transistor switch with nonzero value of its saturation resistance.

Let the output current i_R flowing through the load and nth-harmonic current i_n are written as sinusoidal,

$$i_R(\omega t) = I_R \sin(\omega t + \varphi) \tag{10.110}$$

$$i_n(\omega t) = I_n \sin n\omega t \tag{10.111}$$

where I_R is the fundamental-frequency current amplitude, I_n is the nth-harmonic current amplitude, and φ is the initial phase shift. It should be noted that generally a sum of sinusoidal harmonic components can be used in Eq. (10.111).

When the switch is turned on for of $0 \le \omega t \le \pi$, there is no current flowing through the capacitor C,

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = 0 \tag{10.112}$$

and, consequently,

$$i(\omega t) = I_0 + I_n \sin n\omega t + I_R \sin(\omega t + \varphi) \tag{10.113}$$

where I_0 is the DC-supply current.

For an initial on-state condition $i(0) = 0$, Eq. (10.113) reduces to

$$1 + \frac{I_R}{I_0} \sin\varphi = 0 \tag{10.114}$$

When the switch is turned off for $\pi \le \omega t < 2\pi$, there is no current flowing through the switch, i.e. $i(\omega t) = 0$, and the current flowing through the capacitor C can be written as

$$i_C(\omega t) = I_0 + I_n \sin n\omega t + I_R \sin(\omega t + \varphi) \tag{10.115}$$

producing the voltage across the switch by charging of this capacitor according to

$$v(\omega t) = \frac{1}{\omega C} \int_{\pi}^{\omega t} i_C(\omega t)\, d\omega t = \frac{1}{\omega C} \left\{ (\omega t - \pi) I_0 - \frac{I_n}{n} (1 + \cos n\omega t) - I_R [\cos(\omega t + \varphi) + \cos\varphi] \right\} \tag{10.116}$$

Applying a zero-voltage switching condition of Eq. (10.52) to Eq. (10.116) results in

$$\frac{\pi}{2} - \frac{I_n}{nI_0} - \frac{I_R}{I_0} \cos\varphi = 0 \tag{10.117}$$

where the relative amplitude of the nth-harmonic component I_n/I_0 can be obtained for any n by

$$I_n = \frac{1}{\pi} \int_0^{2\pi} i(\omega t) \sin n\omega t\, d\omega t = \frac{2I_0}{n\pi} (1 - \cos n\pi) \tag{10.118}$$

which is reduced for odd n to

$$\frac{I_n}{I_0} = \frac{4}{n\pi} \tag{10.119}$$

As a result, by substituting Eq. (10.114) and Eq. (10.119) into Eq. (10.117), the initial phase angle φ can be explicitly obtained for odd n by

$$\varphi = \tan^{-1}\left(\frac{2\pi n^2}{8-\pi^2 n^2}\right) \tag{10.120}$$

The DC-supply voltage V_{cc} can be determined by applying a Fourier-series expansion to Eq. (10.116) as

$$V_{\mathrm{cc}} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)\,d\omega t = \frac{I_0}{2\pi\omega C}\left[\frac{\pi^2}{2} - \frac{\pi I_{\mathrm{n}}}{n I_0} - \frac{I_{\mathrm{R}}}{I_0}(2\sin\varphi + \pi\cos\varphi)\right] \tag{10.121}$$

For an idealized collector efficiency of 100%, the DC power $P_0 = I_0 V_{\mathrm{cc}}$ and fundamental-frequency output power $P_{\mathrm{out}} = V_{\mathrm{R}}^2/2R$ delivered to the load are equal, i.e.,

$$I_0 V_{\mathrm{cc}} = \frac{V_{\mathrm{R}}^2}{2R} \tag{10.122}$$

where $V_{\mathrm{R}} = I_{\mathrm{R}} R$ is the voltage amplitude across the load resistor R.

The fundamental-frequency voltage $v_1(\omega t)$ across the switch consists of two quadrature components, as shown in Fig. 10.34, whose amplitudes can be found using Fourier formulas and Eq. (10.116) by

$$V_{\mathrm{R}} = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin(\omega t + \varphi)d\omega t = -\frac{2I_0}{\pi\omega C}\left[\sin\varphi + \cos\varphi\left(-\frac{\pi}{2} + \frac{1 I_n}{n I_0} + \frac{I_{\mathrm{R}}}{I_0}\cos\varphi\right)\right] \tag{10.123}$$

$$V_{\mathrm{L}} = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t + \varphi)d\omega t = -\frac{I_0}{\pi\omega C}\left[\sin\varphi\left(\pi - \frac{2I_{\mathrm{n}}}{n I_0}\right) + 2\cos\varphi - \frac{I_{\mathrm{R}}}{I_0}\left(\frac{\pi}{2} + \sin 2\varphi\right)\right] \tag{10.124}$$

As a result, for a particular case of the third-harmonic tuning when $n = 3$, we have

$$\varphi = \tan^{-1}\left(\frac{18\pi}{8-9\pi^2}\right) = -34.98\ \text{degrees} \tag{10.125}$$

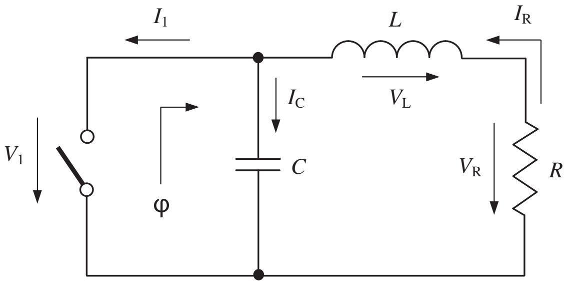


FIG. 10.34

Equivalent Class-E/F$_{\mathrm{n}}$ load network at fundamental frequency.

$$\frac{I_{\mathrm{R}}}{I_0} = -\frac{1}{\sin\varphi} = 1.7444 \tag{10.126}$$

$$\frac{I_{\mathrm{n}}}{I_0} = \frac{4}{3\pi} = 0.4244 \tag{10.127}$$

Fig. 10.35 shows the normalized collector voltage and current waveforms, the normalized waveform of the current flowing through the capacitor C, the third-harmonic and fundamental-frequency sinusoidal current waveforms for idealized optimum Class-E/F$_3$ mode during the entire interval $0 \le \omega t \le 2\pi$. From the collector voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch, and the current consisting of the DC-supply current, third-harmonic, and load sinusoidal currents flows through the switch. However, when the transistor is turned off, all this current flows through the capacitor C. In this case, there is no nonzero voltage and current simultaneously, which means a lack of the power losses that gives an idealized collector efficiency of 100% given by Eq. (10.122).

Hence, the optimum normalized series inductance L and shunt capacitance C can be calculated as

$$\frac{\omega L}{R} = \frac{V_{\mathrm{L}}}{V_{\mathrm{R}}} = 0.961 \tag{10.128}$$

$$\omega CR = \frac{\omega C V_{\mathrm{R}}}{I_0} \Big/ \frac{I_{\mathrm{R}}}{I_0} = 0.209 \tag{10.129}$$

The optimum load resistance R can be obtained from Eqs. (10.122) and (10.126) for the DC-supply voltage V_{cc} and fundamental-frequency output power P_{out} delivered to the load as

$$R = \frac{1}{2}\frac{V_{\mathrm{R}}^2}{P_{\mathrm{out}}} = \frac{2V_{\mathrm{cc}}^2}{P_{\mathrm{out}}} \Big/ \left(\frac{I_{\mathrm{R}}}{I_0}\right)^2 = 0.657\frac{V_{\mathrm{cc}}^2}{P_{\mathrm{out}}} \tag{10.130}$$

From Eqs. (10.128)–(10.130), it follows that the load resistance R is greater by 14% in nominal Class-E/F$_3$ mode compared with a conventional Class-E with shunt capacitance, whereas the series inductance L and shunt capacitance C are approximately the same for both classes for the same V_{cc} and P_{out}.

The phase angle ϕ of the load network at the fundamental seen by the switch, as shown in Fig. 10.34, and required for an idealized optimum (or nominal) Class-E/F$_3$ mode can be determined through the load-network parameters using Eqs. (10.128) and (10.129) as

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) - \tan^{-1}\left(\frac{\omega CR}{1 - \dfrac{\omega L}{R}\omega CR}\right) = 29.2^\circ \tag{10.131}$$

The peak collector voltage $V_{\max}$ and current $I_{\max}$ can be determined from Eqs. (10.113) and (10.116) using Eqs. (10.121) and (10.125)–(10.127) as

$$\frac{V_{\max}}{V_{\mathrm{cc}}} = 3.142 \tag{10.132}$$

$$\frac{I_{\max}}{I_0} = 3.056 \tag{10.133}$$

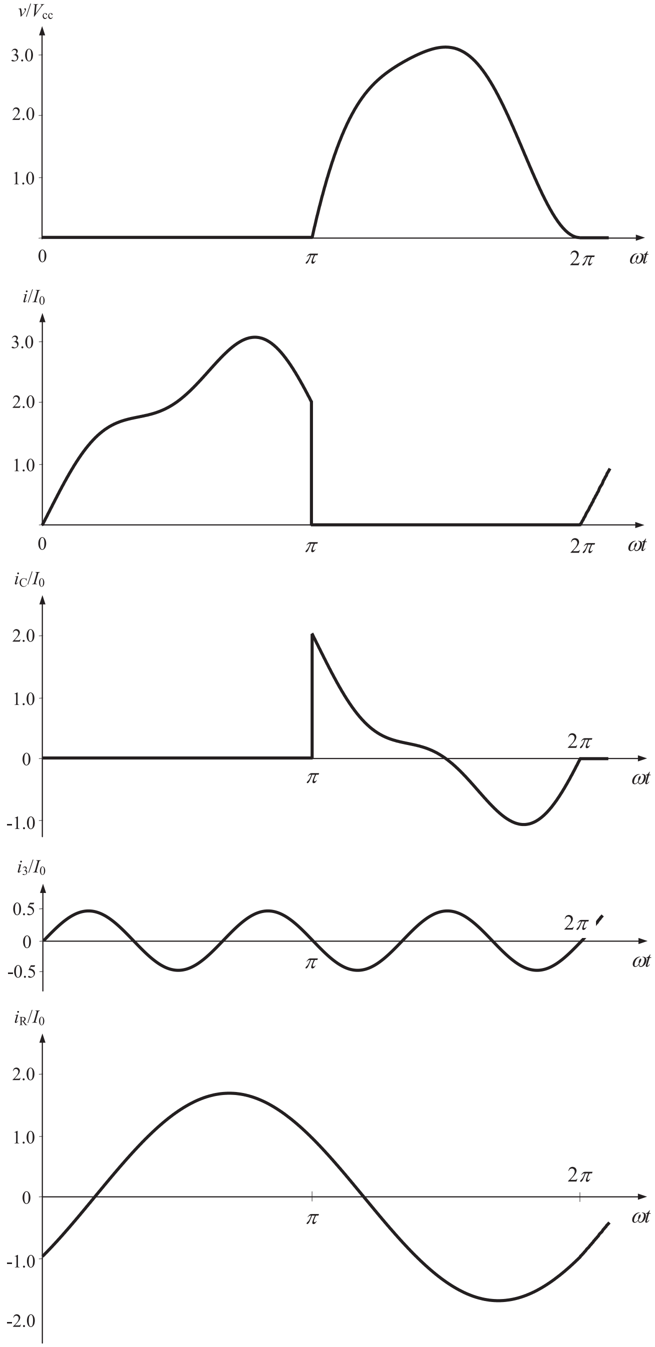
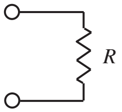
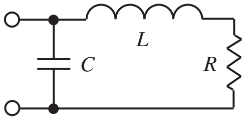
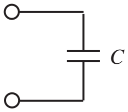
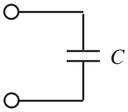
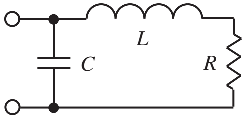
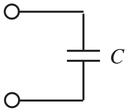


FIG. 10.35

Ideal waveforms for optimum Class-E/F_3 operation mode.

Table 10.3 Optimum impedances at fundamental and harmonics.

High-efficiency mode	**f_0 (fundamental)**	**$2nf_0$ (even harmonics)**	**$(2n+1)f_0$ (odd harmonics)**
Inverse Class-F		Open	Short
Class-E with shunt capacitance			
Class-E/F$_3$			Short

that shows that the voltage peak factor is lower by 13.4% compared with a conventional Class-E with shunt capacitance.

The maximum operating frequency $f_{\max}$ in nominal Class-E/F$_3$ mode is limited by the device output (collector or drain-source) capacitance C_{out}. As a result, from Eqs. (10.129) and (10.130) it follows that

$$f_{\max} = 0.0506 \frac{P_{\text{out}}}{C_{\text{out}} V_{\text{cc}}^2} \tag{10.134}$$

which corresponds to the maximum operating frequency of a Class-E with shunt capacitance.

In Table 10.3, the optimum impedances seen from the device collector at the fundamental and higher-order harmonic components are illustrated by the appropriate circuit configurations. It can be seen that an inverse Class-F mode shows purely resistive impedance at the fundamental, open-circuit conditions at even harmonics, and short-circuit conditions at odd harmonics. As opposed to inverse Class-F mode, Class-E mode with shunt capacitance requires inductive impedance at the fundamental and capacitive reactance at any other harmonic component. As a result, an idealized mixed Class-E/F$_3$ mode provides simultaneously the harmonic impedance conditions typical for both Class-E with a shunt capacitance and inverse Class-F with third-harmonic control.

Fig. 10.36 shows the ADS simulation setup for a nominal Class-E/F$_3$ operation in the time domain, where an input source Vt_PulseDT represents a voltage source with pulse train defined at discrete time steps used in envelope and transient simulators. The active device is represented by a voltage-controlled switch with off-resistance of 1 MΩ and small finite on-resistance, the value of which can generally be varied. The use of a discrete time pulse source, as opposed to a standard pulse source, can guarantee that there is no timing jitter in the pulse edges due to the waveform being sampled asynchronously by a fixed time interval simulation. The simulation time is significantly faster than the period of a square wave.

To provide the circuit simulation in the time domain, the transient simulator is added to the simulation template. The stop time of 80 s is chosen for an operating frequency normalized to unity that is sufficient to reach a steady-state mode. The inductors and capacitors are lossless and the loaded quality

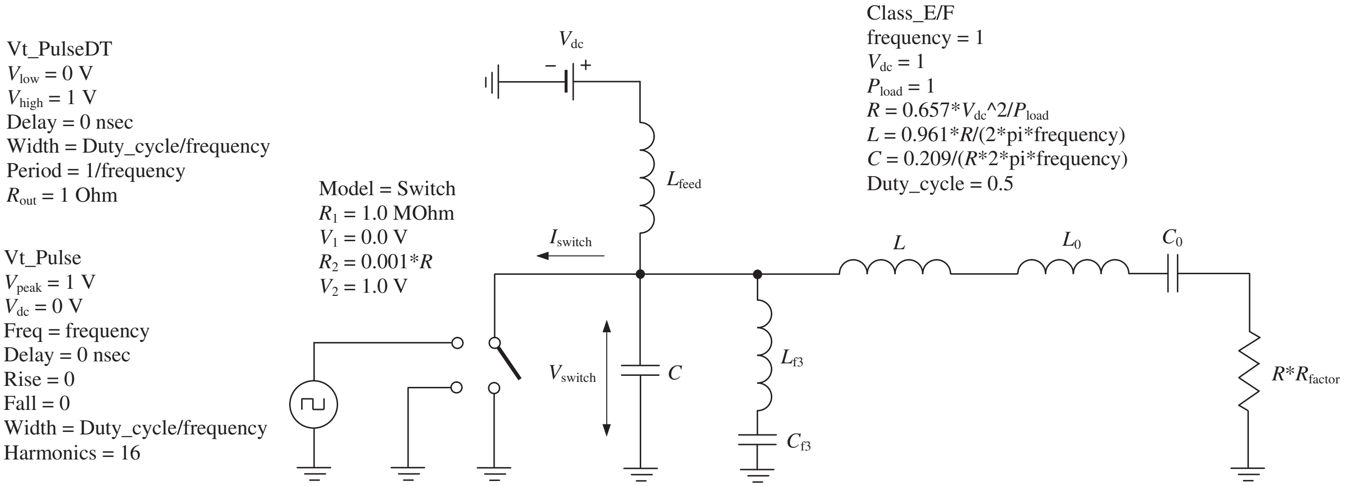

Vt_PulseDT
V_{low} = 0 V
V_{high} = 1 V
Delay = 0 nsec
Width = Duty_cycle/frequency
Period = 1/frequency
R_{out} = 1 Ohm
Vt_Pulse
V_{peak} = 1 V
V_{dc} = 0 V
Freq = frequency
Delay = 0 nsec
Rise = 0
Fall = 0
Width = Duty_cycle/frequency
Harmonics = 16
Model = Switch
R_1 = 1.0 MOhm
V_1 = 0.0 V
R_2 = 0.001*R
V_2 = 1.0 V
V_{dc}
−
+
L_{feed}
I_{switch}
V_{switch}
C
L_{f3}
C_{f3}
Class_E/F
frequency = 1
V_{dc} = 1
P_{load} = 1
R = 0.657*V_{dc}^2/P_{load}
L = 0.961*R/(2*pi*frequency)
C = 0.209/(R*2*pi*frequency)
Duty_cycle = 0.5
L
L_0
C_0
R*R_{factor}

FIG. 10.36

Simulation setup for idealized Class-E/F_3 mode in time domain.

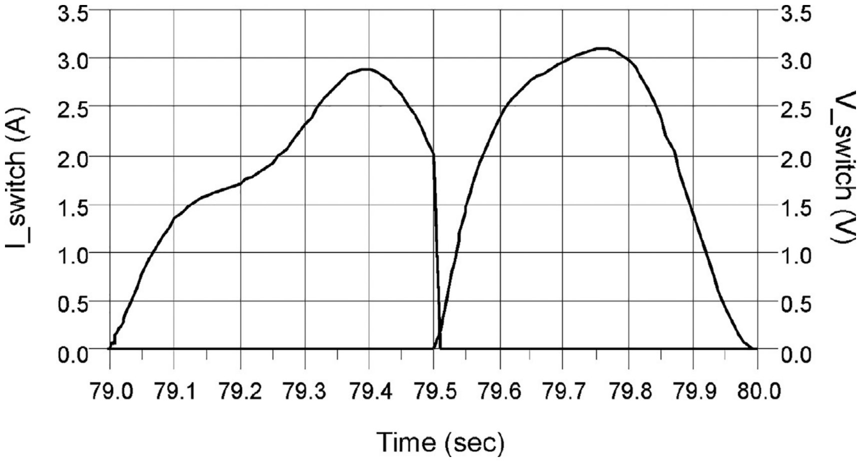


FIG. 10.37

Simulated switch voltage and current waveforms in time domain.

factor Q_L of the series resonant circuit is set as high as 10. The measure equations include the conditions when the switch voltage V_{switch} and its voltage derivative must take zero values at the instant just before the switch is turned on. The efficiency is calculated in the 79th + 80th period since the products of instantaneous current and voltage are integrated over these two periods and divided by two. Since the RF choke inductance L_{feed} should have a finite number in transient simulations, its value was chosen to be 10 times greater than that of a series inductance L. As a result, the value of a load resistance is increased by 22% ($R_{factor} = 1.22$) compared to the nominal case to obtain the optimized switch voltage and current waveforms shown in Fig. 10.37 with efficiency of 99.8%. Similar increase in optimum value of the load resistance for the reduced value of the RF choke inductance is observed in a Class-E mode with finite DC-feed inductance.

The simulation setup shown in Fig. 10.36 can also be used to obtain the nominal Class-E/F$_3$ operation with infinite RF choke in the frequency domain, where an input source Vt_Pulse represents a voltage source with Fourier-series expansion of periodic rectangular wave with different pulse width characterized by a duty cycle used in a harmonic-balance simulator. Generally, using the frequency domain enables the overall simulation procedure to be much faster than that in the time domain and can take a few seconds. However, because the number of harmonic components is not infinite, the simulation waveforms and numerical results for the optimum load network parameters are not so accurate. The harmonic order is set to 100.

In this case, the optimization procedure can be applied with respect to efficiency as an optimization parameter. Since the simulation time is very short, a number of iterations can significantly be increased for better accuracy. Fig. 10.38 shows the normalized (*a*) switch voltage and current waveforms and (*b*) sinusoidal third-harmonic and fundamental-frequency waveforms obtained for the nominal parameters of the Class-E/F$_3$ load network given by Eqs. (10.128)–(10.130) with 50% duty cycle and $R_{factor} = 1$.

Unlike the simulations in the time domain, the frequency-domain simulations are characterized by smoother transitions between the positions when the switch is turned on and the switch is turned off and vice versa. Nevertheless, for $r_{sat}/R = 0.001$, where r_{sat} is the switch saturation resistance, and lossless

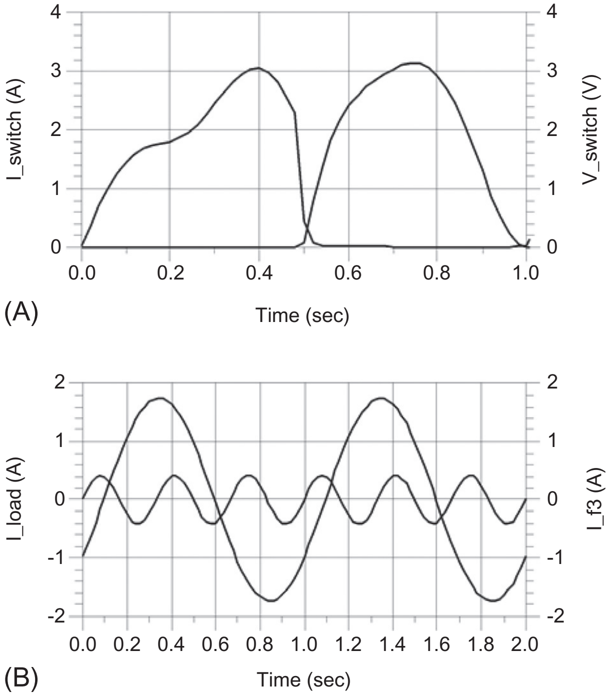


FIG. 10.38

Simulated voltage and current waveforms in frequency domain.

circuit elements except load resistance *R*, the efficiency is equal to 98.2%, and the simulated normalized switch voltage and current waveforms shown in Fig. 10.38 are similar to the same theoretical waveforms shown in Fig. 10.35.

To design a lumped load network which corresponds to Class-E/F$_3$ mode, first it is necessary to choose the optimum parameters from Eqs. (10.128)–(10.130) for the shunt capacitance, series inductance, and load resistance at the fundamental and then add an additional network to provide an open circuit at the second harmonic and a short circuit at the third harmonic. A Class-E/F$_3$ PA using such a lumped load network and based on a MOSFET device IRF510 achieved an output power 36.8 dBm with a drain efficiency of 96% and a power gain of 12 dB at an operating frequency of 4 MHz.[29] It should be noted that the maximum switch voltage is affected by the nonlinearity of the shunt capacitance, when $V_{\max}/V_{\rm dd}$ is increased from 3.0 to 3.8 with increasing $V_{\rm dd}$ up to 100 V.[30] For such a Class-E/F$_3$ PA, high efficiencies of about 95% can be achieved in a nonoptimum operation with zero-voltage and non-zero voltage-derivative switching conditions when the switch turns on with declining voltage having negative derivative.[31]

As an alternative, a Class-E/F$_3$ load network can be represented by a lumped network shown in Fig. 10.39, which consists of two cascaded parallel resonant circuits (L_1C_1 and L_2C_2), tuned to the fundamental ($\omega = \omega_0$) and second harmonic ($\omega = 2\omega_0$), respectively, to provide the open-circuit conditions

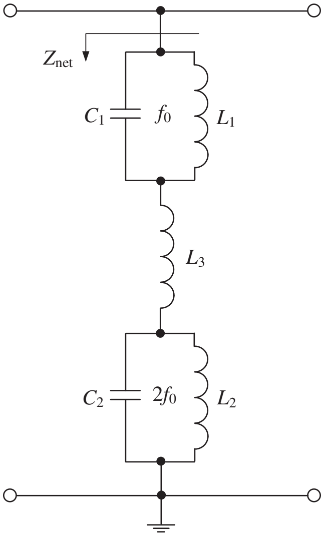


FIG. 10.39

Lumped network for second- and third-harmonic tuning.

for these components, and a series inductor L_3. The network impedance Z_{net} at the input of this lumped network can be written as

$$Z_{net}(\omega) = \frac{j\omega L_1}{1 - \omega^2 L_1 C_1} + j\omega L_3 + \frac{j\omega L_2}{1 - \omega^2 L_2 C_2} \tag{10.135}$$

To provide a short-circuit condition at the third harmonic ($\omega = 3\omega_0$), Eq. (10.135) can be rewritten in the form

$$Z_{net}(3\omega_0) = \frac{j3\omega_0 L_1}{1 - 9\omega_0^2 L_1 C_1} + j3\omega_0 L_3 + \frac{j3\omega_0 L_2}{1 - 9\omega_0^2 L_2 C_2} = 0 \tag{10.136}$$

As a result, the ratios between the network elements for certain values of the inductances L_1 and L_2 can be given by

$$C_1 = \frac{1}{\omega_0^2 L_1} \tag{10.137}$$

$$C_2 = \frac{1}{4\omega_0^2 L_2} \tag{10.138}$$

$$L_3 = 0.125 L_1 + 0.8 L_2 \tag{10.139}$$

Fig. 10.40 shows the simulated transfer characteristic (magnitude S_{21} in decibels versus frequency) for the lumped network shown in Fig. 10.39, where its parameters were calculated according to Eqs. (10.137)–(10.139) for $f_0 = 430\,\text{MHz}$, $L_1 = 60$ nH, and $L_2 = 12.5$ nH as $L_3 = 17.5$ nH, $C_1 = 2.3\,\text{pF}$, and $C_2 = 2.7\,\text{pF}$. The inductor quality factors Q for all three inductors were set to 50. The values of inductances L_1 and L_2 should be properly chosen to provide low impedance (first zero)

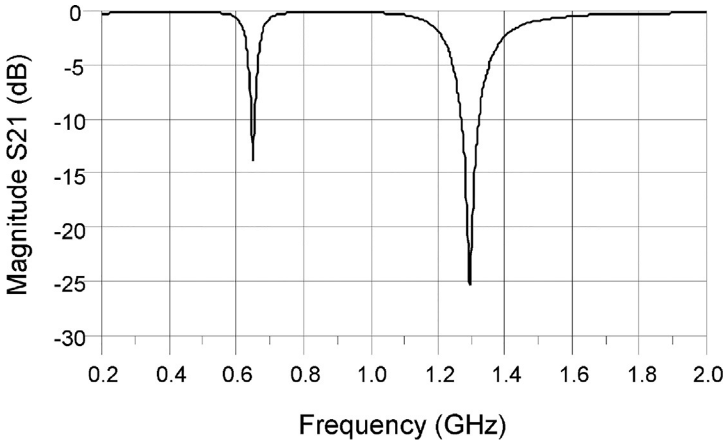


FIG. 10.40

Frequency response of lumped network for Class-E/F_3 mode.

enough far from both first (at fundamental) and second (at the second harmonic) poles, as shown in Fig. 10.40.

The lumped Class-E/F_3 PA based on a 28-V 10-W Cree GaN HEMT power transistor CGH40010 was simulated at an operating frequency of 430 MHz according to the simulation setup shown in Fig. 10.41.[28] In this case, the required optimum load resistance given by Eq. (10.130) is close to 50 Ω, therefore it is enough to use a series high-Q_L resonant circuit including an optimum series inductance given by Eq. (10.128). An additional external shunt capacitance of 0.6 pF is used because the device output capacitance of about 1.3 pF is slightly less than required by Eq. (10.129). Generally, it is necessary to consider the device package parasitics, with the series bondwire and lead inductance as the most important, which can seriously affect the device performance at higher frequencies if the device drain-source capacitance is not optimum according to Eq. (10.129). As a result, for infinite inductor quality factors Q in the load network, an output power of 40.1 dBm, a drain efficiency of 87%, and a *PAE* of 84.5% with a power gain of about 15 dB were simulated for an input power $P_{\text{in}} = 25$ dBm, as shown in Fig. 10.42A. For more practical values of $Q = 50$, an output power of 39.3 dBm is achieved with a drain efficiency of 77.5% and a *PAE* of 74.9%. Fig. 10.42B shows the simulated drain waveform which is very close to the theoretical one shown in Fig. 10.35.

The circuit schematics of a high-efficiency transmission-line Class-E/F_3 PA are shown in Fig. 10.43, where the optimum load resistance R is matched to the standard load impedance $R_L = 50\,\Omega$ at the fundamental frequency.[28] Here, both high impedance at the second harmonic and low impedance at the third harmonic are created at the device output by using a series transmission line TL_1 with an electrical length of 45 degrees, a series transmission line TL_2, the electrical length θ of which depends on the value of the optimum series inductance L, a quarterwave short-circuit transmission line TL_3, and an open-circuit stub TL_4 with an electrical length of 30 degrees.

Fig. 10.44A shows the load network seen by the device multiharmonic current source at fundamental. Here, the combined series transmission line $TL_1 + TL_2$ with the same characteristic impedance Z_1 together with an open-circuit capacitive stub TL_4 with an electrical length of 30 degrees provides an

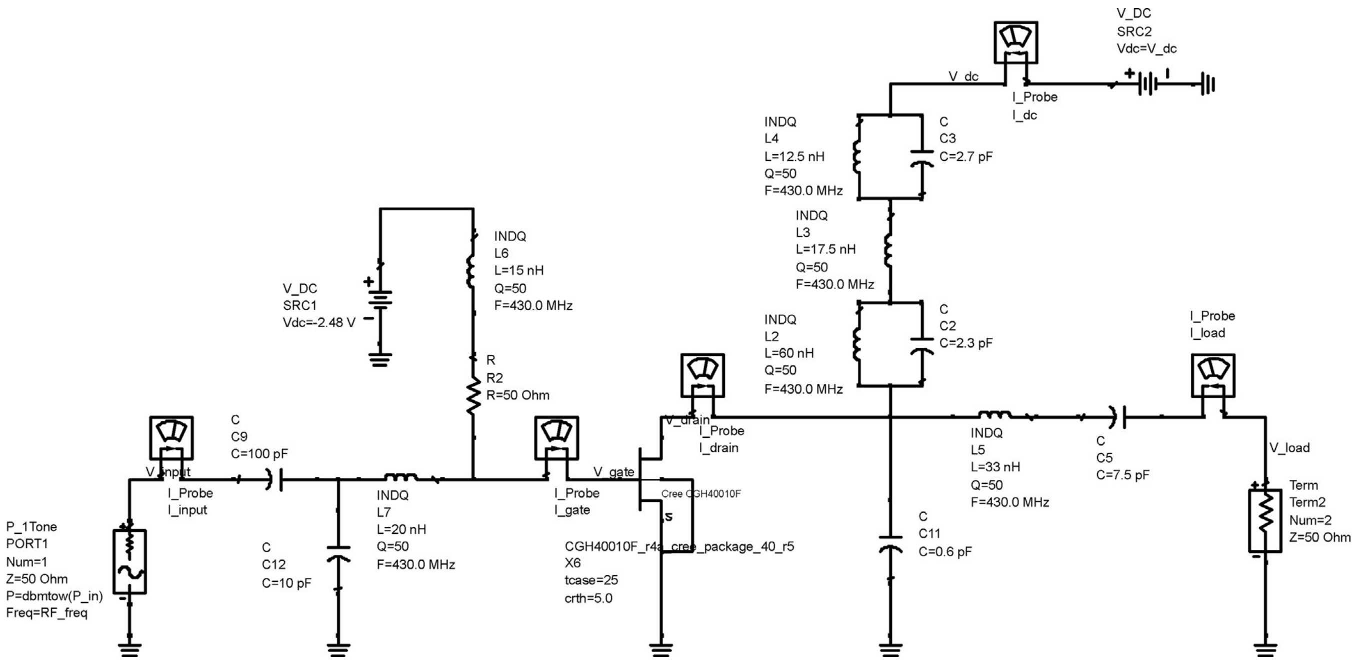

V_DC
SRC2
Vdc=V_dc
V_dc
I_Probe
I_dc
INDQ
L4
L=12.5 nH
Q=50
F=430.0 MHz
C
C3
C=2.7 pF
INDQ
L3
L=17.5 nH
Q=50
F=430.0 MHz
INDQ
L2
L=60 nH
Q=50
F=430.0 MHz
C
C2
C=2.3 pF
I_Probe
I_load
INDQ
L6
L=15 nH
Q=50
F=430.0 MHz
V_DC
SRC1
Vdc=-2.48 V
R
R2
R=50 Ohm
C
C9
C=100 pF
V_input
I_Probe
I_input
V_drain
I_Probe
I_drain
V_gate
I_Probe
I_gate
Cree CGH40010F
INDQ
L7
L=20 nH
Q=50
F=430.0 MHz
INDQ
L5
L=33 nH
Q=50
F=430.0 MHz
C
C5
C=7.5 pF
V_load
Term
Term2
Num=2
Z=50 Ohm
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(P_in)
Freq=RF_freq
C
C12
C=10 pF
CGH40010F_r4a_cree_package_40_r5
X6
tcase=25
crth=5.0
C
C11
C=0.6 pF

FIG. 10.41

Simulation setup for lumped Class-E/F_3 GaN HEMT PA.

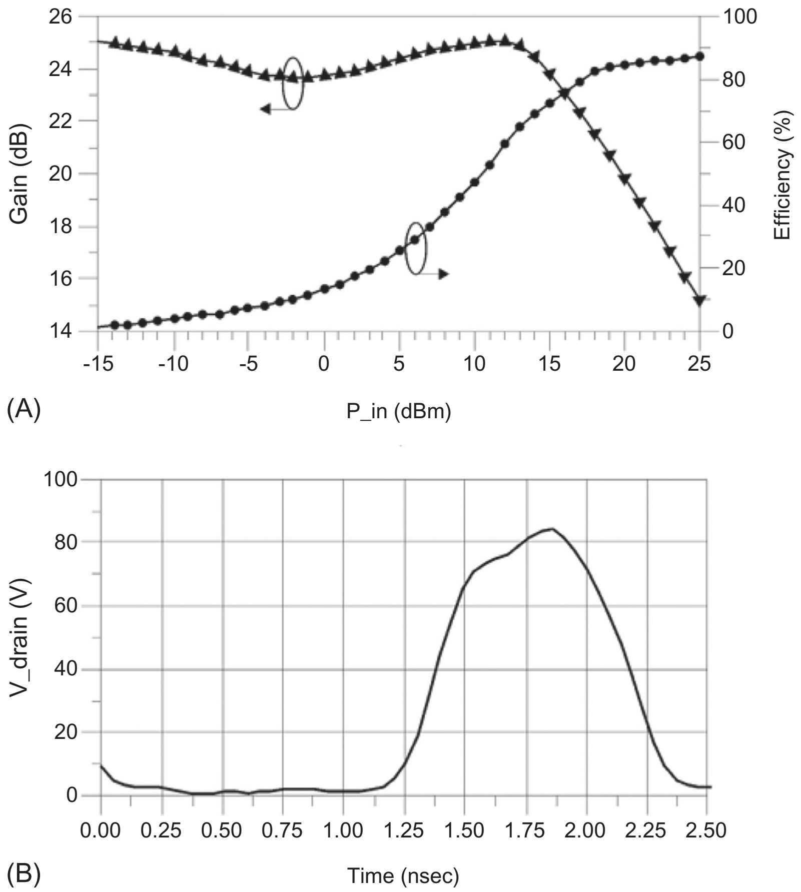


FIG. 10.42

Simulated results of lumped Class-E/F$_3$ GaN HEMT PA.

impedance matching between the optimum load-network impedance seen from the device output $Z_{\text{net}} = R$ and the load resistance R_{L} by proper choice of the transmission-line characteristic impedances Z_1 and Z_2, which can be explicitly calculated for a certain electrical length θ.

The optimum load-network impedance Z_{net} at fundamental can be written as

$$Z_{\text{net}} = Z_1 \frac{R_{\text{L}}(Z_2 - Z_1 \tan 30^\circ \tan\theta_1) + jZ_1 Z_2 \tan\theta_1}{Z_1 Z_2 + j(Z_1 \tan 30^\circ + Z_2 \tan\theta_1) R_{\text{L}}} \tag{10.140}$$

where $\theta_1 = 45$ degrees + θ, Z_1 is the characteristic impedance of the series transmission line, and Z_2 is the characteristic impedance of the open-circuit stub with an electrical length of 30 degrees.

Separating Eq. (10.140) into real and imaginary parts, the following system of two equations with two unknown parameters is obtained:

$$(Z_1 \tan 30^\circ + Z_2 \tan\theta_1)^2 R_{\text{L}}^2 R - (Z_1 Z_2)^2 \left[R_{\text{L}}\left(1 + \tan^2\theta_1\right) - R\right] = 0 \tag{10.141}$$

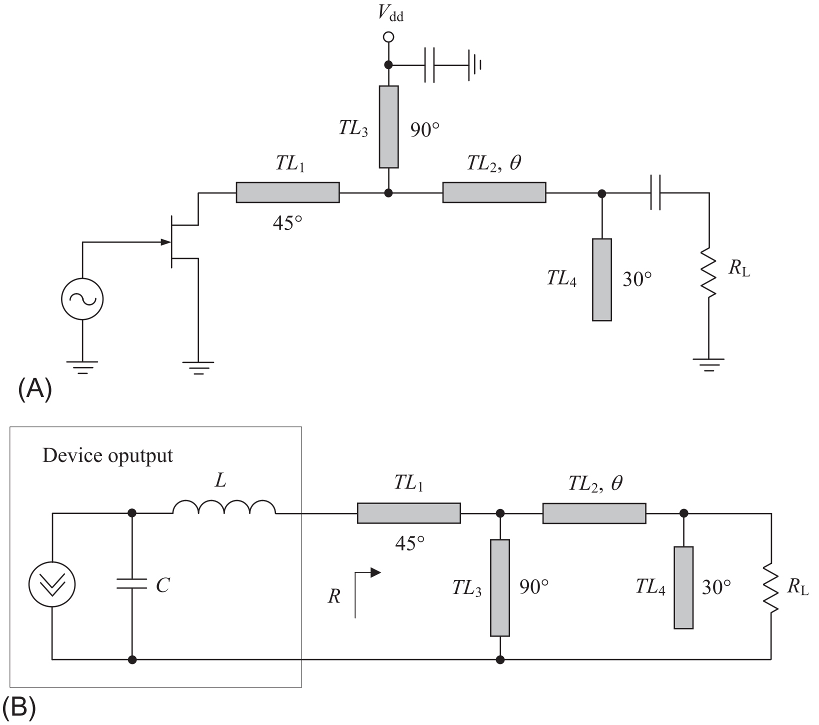

V_{dd}
TL_3
90°
TL_1
TL_2, θ
45°
TL_4
30°
R_L
(A)
Device oputput
L
C
R
TL_1
45°
TL_2, θ
TL_3
90°
TL_4
30°
R_L
(B)

FIG. 10.43

Schematics of transmission-line Class-E/F$_3$ PA.

$$(Z_1Z_2)^2\tan\theta_1 + R_L^2(Z_1\tan 30^\circ + Z_2\tan\theta_1)(Z_2 - Z_1\tan 30^\circ\tan\theta_1) = 0 \tag{10.142}$$

which allows direct calculation of the characteristic impedances Z_1 and Z_2.

This system of two equations can be explicitly solved as a function of the parameter $r = R_L/R$, resulting in

$$\frac{Z_1}{R_L} = \frac{\sqrt{r(1+\tan^2\theta_1) - 1}}{r\tan\theta_1} \tag{10.143}$$

$$\frac{Z_1}{Z_2} = \frac{r-1}{r\tan 30^\circ\tan\theta_1} \tag{10.144}$$

which are reduced for $\theta = 15$ degrees and $\theta_1 = 45$ degrees + $\theta = 60$ degrees to

$$\frac{Z_1}{R_L} = \frac{\sqrt{4r-1}}{\sqrt{3}\,r} \tag{10.145}$$

$$\frac{Z_1}{Z_2} = \frac{r-1}{r} \tag{10.146}$$

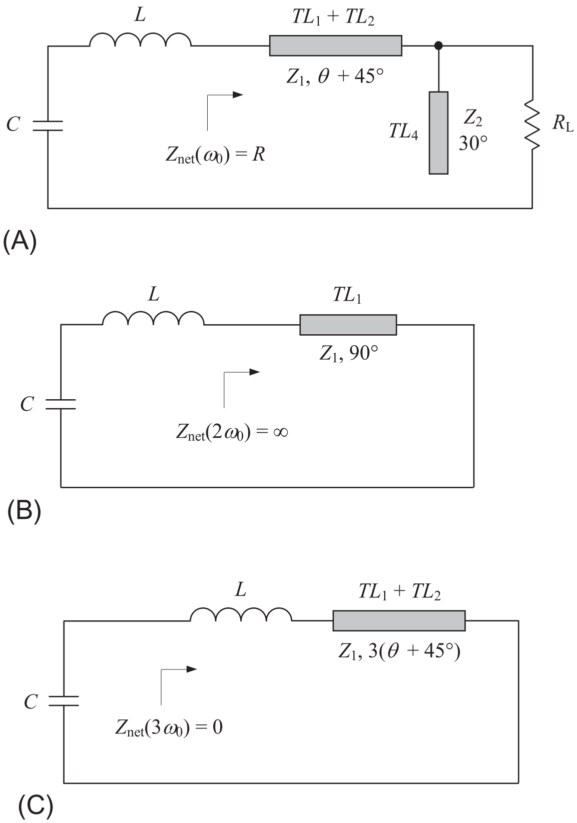


FIG. 10.44

Load networks seen by device output at harmonics.

Consequently, for specified value of the parameter r with the required Class-E/F$_3$ optimum load resistance R and standard load $R_L = 50\,\Omega$, the characteristic impedance Z_1 is calculated from Eq. (10.145) and then the characteristic impedance Z_2 is obtained by Eq. (10.146). Hence, if $R = 20\,\Omega$, resulting in $r = 2.5$, the characteristic impedance of the series transmission line is $Z_1 = 35\,\Omega$ and the characteristic impedance of the open-circuit stub is $Z_2 = 58\,\Omega$.

The load network seen by the device output at the second harmonic is shown in Fig. 10.44B, taking into account the shorting effect of the quarterwave short-circuit stub TL_3. Here, the transmission line TL_1 provides an open-circuit condition for the second harmonic at the device output. Similar load network at the third harmonic is shown in Fig. 10.44C, due to the open-circuit effect of the short-circuited quarterwave line TL_3 and short-circuit effect of the open-circuited harmonic stub TL_4 at the third harmonic. In this case, the combined transmission line $TL_1 + TL_2$ together with the series inductance L_{out} provides a short-circuit condition for the third harmonic at the device output being shorted at its right-hand side. Depending on the actual physical length of the device output electrode, on-board adjusting of the transmission lines TL_1 and TL_2 can easily provide the required open- and short-circuit conditions, as well as an impedance matching at the fundamental frequency, due to their series connection to the device output.

The required electrical length θ of the transmission line TL_2 can be defined from

$$3\omega_0 L + Z_1 \tan 3(\theta + 45^\circ) = 0 \tag{10.147}$$

where the total electrical length of the entire series transmission line $\theta_1 = 45$ degrees + θ is equal to π or 180 degrees at the third harmonic component when $L = 0$. As a result,

$$\theta = \frac{\pi}{12} - \frac{1}{3}\tan^{-1}\frac{3\omega_0 L}{Z_1} \tag{10.148}$$

In this case, by combining Eqs. (10.143) and (10.148), the resulting transcendental equation to implicitly determine the electrical length θ as a single unknown parameter by iterative method can be obtained. Then, the characteristic impedance Z_1 is calculated from Eq. (10.143) that allows the characteristic impedance Z_2 to be defined from Eq. (10.144).

Fig. 10.45 shows the simulated circuit schematic, which approximates a transmission-line Class-E/F_3 PA based on a 28-V, 10-W Cree GaN HEMT power transistor CGH40010 and a transmission-line load network implemented on a 30-mil RO4350 substrate shown in Fig. 10.43A.[28] The input matching circuit provides a complex-conjugate matching with the standard 50-Ω source. The load network was slightly modified by optimizing the parameters of the series transmission line since the device output capacitance C_{out} and series inductance L_{out} formed by drain bondwires and package lead do not match the required exact values of the shunt capacitance C and series inductance L for nominal Class-E/F_3 operation mode. Special stripline models for the device input and output package leads need to be added to the simulation setup to consider their inductances, whose correct values depend on assembling procedure. The maximum output power of 40.8 dBm, power gain of 12.8 dB (linear gain of about 18 dB), drain efficiency of 82.5%, and *PAE* of 78.2% are achieved at an operating frequency of 2.14 GHz with a DC-supply voltage of 28 V and a quiescent current of 40 mA.

An alternative configuration of a Class-E/F PA, whose circuit schematic with lumped elements is shown in Fig. 10.46A, is based on a parallel-circuit Class-E structure, where the series L_0C_0 filter is tuned to the fundamental frequency while the series L_nC_n circuit can be tuned to any odd-harmonic component.[32] The theoretical switch voltage and current waveforms calculated for $n = 3$ are similar to those shown in Fig. 10.35 for the Class-E/F_3 with shunt capacitance and series inductance, with slightly higher peak switch voltage equal to $V_{\text{max}} = 3.279V_{\text{dd}}$.

The optimum normalized series inductance L and shunt capacitance C are obtained by.

$$\frac{\omega L}{R} = 0.975 \tag{10.149}$$

$$\omega CR = 0.551 \tag{10.150}$$

whereas the optimum load resistance R for the DC-supply voltage V_{dd} and fundamental-frequency output power P_{out} delivered to the load can be calculated from.

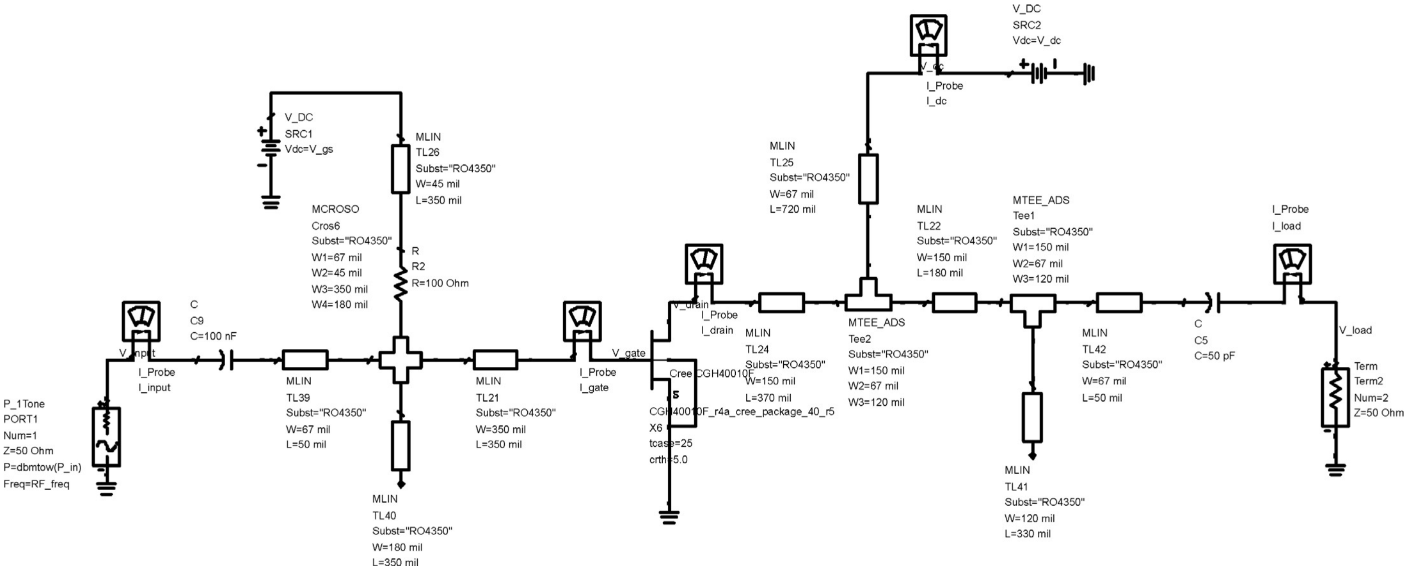

V_DC
SRC2
Vdc=V_dc
V_dc
I_Probe
I_dc
V_DC
SRC1
Vdc=V_gs
MLIN
TL26
Subst="RO4350"
W=45 mil
L=350 mil
MLIN
TL25
Subst="RO4350"
W=67 mil
L=720 mil
MCROSO
Cros6
Subst="RO4350"
W1=67 mil
W2=45 mil
W3=350 mil
W4=180 mil
R
R2
R=100 Ohm
MLIN
TL22
Subst="RO4350"
W=150 mil
L=180 mil
MTEE_ADS
Tee1
Subst="RO4350"
W1=150 mil
W2=67 mil
W3=120 mil
I_Probe
I_load
C
C9
C=100 nF
V_input
I_Probe
I_input
V_drain
I_Probe
I_drain
MLIN
TL24
Subst="RO4350"
W=150 mil
L=370 mil
MTEE_ADS
Tee2
Subst="RO4350"
W1=150 mil
W2=67 mil
W3=120 mil
MLIN
TL42
Subst="RO4350"
W=67 mil
L=50 mil
C
C5
C=50 pF
V_load
MLIN
TL39
Subst="RO4350"
W=67 mil
L=50 mil
MLIN
TL21
Subst="RO4350"
W=350 mil
L=350 mil
I_Probe
I_gate
V_gate
Cree CGH40010F
S
CGH40010F_r4a_cree_package_40_r5
X6
tcase=25
crth=5.0
Term
Term2
Num=2
Z=50 Ohm
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow(P_in)
Freq=RF_freq
MLIN
TL41
Subst="RO4350"
W=120 mil
L=330 mil
MLIN
TL40
Subst="RO4350"
W=180 mil
L=350 mil

FIG. 10.45

Circuit schematic of transmission-line Class-E/F_3 GaN HEMT PA.

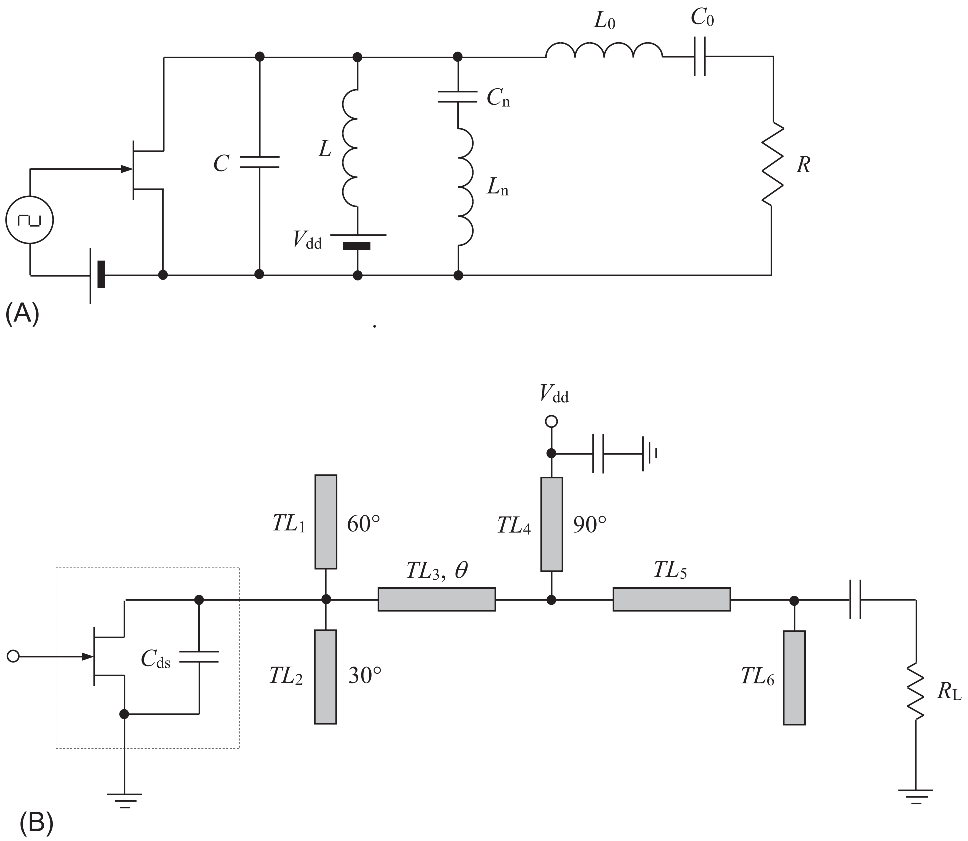


FIG. 10.46

Circuit schematics of (A) lumped and (B) transmission-line parallel-circuit Class-E/F_3 PA.

$$R = 1.256\,\frac{V_{\mathrm{dd}}^2}{P_{\mathrm{out}}} \tag{10.151}$$

Fig. 10.46B shows the circuit schematic of a transmission-line parallel-circuit Class-E/F_3, where C_{ds} is the drain-source capacitance and R_{L} is the standard load usually equal to 50 Ω. Here, a 30 degree open-circuit stub TL_2 provides a short-circuit condition at the third harmonic, a 90 degree short-circuited transmission line TL_4 provides a short-circuit condition at the second harmonic, and the electrical length θ of the series transmission line TL_3 is optimized to resonate with the shunt capacitance C_{ds} at the second harmonic. The output matching with the standard 50-Ω load is provided by an L-type transformer with a series transmission line TL_5 and an open-circuit stub TL_6. At the same time, the load-network parameters are optimized to provide the required optimum inductive impedance at the fundamental frequency. The parallel-circuit Class-E/F_3 PA based on a GaN

HEMT device CGH40010F and fabricated on Rogers 5880 substrate achieved a drain efficiency of 83.9% with an output power of 40.4 dBm and a power gain of 10.4 dB at an operating frequency of 2.4 GHz.[32]

10.4 High-efficiency mixed-mode broadband PA

High-efficiency ultra-broadband PAs are usually designed using GaN HEMT technology and different load-network techniques. Depending on the operating frequency bandwidths and implementation capabilities, different Class-C, Class-E, or Class-F modes based upon a finite number of harmonics can be used to achieve high efficiency of the PA operation. In this case, lower drain voltage peak factors can be obtained by using the conventional Class-F or inverse Class-F lumped or transmission-line load networks. When operating in a Class-F mode with the second- and third-harmonic control, the maximum efficiency >81% can be achieved.[33] A drain efficiency of >70% was measured over the frequency bandwidth from 1.45 to 2.45 GHz with an output power of 40.4–42.2 dBm using a 10-W Cree GaN HEMT device.[34] By combining Class-F and inverse Class-F modes with optimized DC-supply voltages, a wide frequency range from 1.3 to 3.3 GHz was covered achieving the drain efficiencies of 60%–84% with output powers of 10–11 W.[35]

In contrast to the conventional Class-C PAs with a parallel resonant circuit resulting in a sinusoidal collector voltage waveform, the mixed-mode Class-C configuration with a series resonant circuit was widely adopted for most VHF and UHF transistor PAs, which could provide better efficiency performance.[36, 37] By simply optimizing the fundamental-frequency and second-harmonic impedances across the frequency bandwidth from 525 to 1325 MHz, the drain efficiency over 70% and output power over 39 dBm were achieved.[38] Much broader frequency bandwidths can be achieved with resistive harmonic loading and lossy input matching. For example, a broadband lossy matched GaN HEMT monolithic microwave integrated circuit (MMIC) PA achieved the drain efficiency of 44.9%–63.6% and output power of 9–13.6 W over the frequency bandwidth of 0.5–2.5 GHz.[39] A decade bandwidth of 0.4–4.1 GHz with a drain efficiency of 40%–62% was achieved by a GaN HEMT PA with a simplified broadband load network delivering the output power over 40 dBm.[40]

Fig. 10.47 shows the reactance compensation load network with a low-pass matching section which includes the third-harmonic resonant circuit to approximate Class-F mode at higher bandwidth

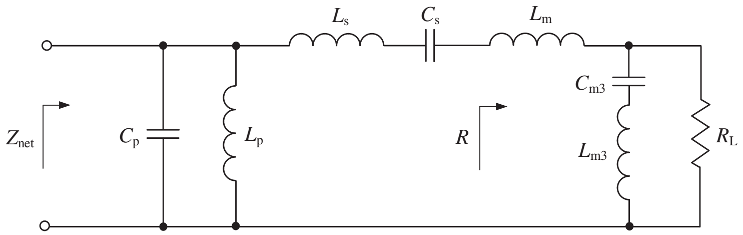


FIG. 10.47

Broadband matching network with third-harmonic trap.

frequencies to increase efficiency at these frequencies. The third-harmonic resonant circuit $L_{\mathrm{m}_3}C_{\mathrm{m}_3}$ provides a capacitive reactance at the fundamental frequency and an open-circuit condition seen by the device output at the third harmonic due to parallel resonant circuit formed by the shunt capacitor C_{p} and equivalent inductor composed of the shunt inductor L_{p} and series $L_{\mathrm{s}}C_{\mathrm{s}}L_{\mathrm{m}}$ circuit having an inductive reactance at the third harmonic.

The reactive part of the input impedance ImZ_{net} should be set to infinite at the third harmonic to approximate Class-F mode at an operating frequency

$$\omega_0 = \frac{1}{\sqrt{L_{\mathrm{p}}C_{\mathrm{p}}}} = \frac{1}{\sqrt{L_{\mathrm{s}}C_{\mathrm{s}}}} \tag{10.152}$$

where the third-harmonic resonant circuit $L_{\mathrm{m}_3}C_{\mathrm{m}_3}$ is tuned to zero, thus resulting in

$$\omega_0 C_{\mathrm{p}} - \frac{L_{\mathrm{p}} + L_{\mathrm{m}} + \frac{8}{9}L_{\mathrm{s}}}{\omega_0 L_{\mathrm{p}}\left(L_{\mathrm{m}} + \frac{8}{9}L_{\mathrm{s}}\right)} = 0 \tag{10.153}$$

For the simplified case of equal loaded quality factors when $Q_{\mathrm{L}} = \omega_0 C_{\mathrm{p}} R = \omega_0 L_{\mathrm{s}}/R = \omega_0 L_{\mathrm{m}}/R$, from Eq. (10.153) it follows that $Q \cong 0.25$, the low value of which allows the high efficiency across a very wide frequency bandwidth to be achieved using mixed-mode operation.

Fig. 10.48A shows the circuit schematic of a high-efficiency ultra-broadband GaN HEMT PA using a 10-W Cree CGH40010F device with an output shunt capacitance of 1.3 pF at $V_{\mathrm{dd}} = 28$ V.[41] The input lossy matching circuit includes a parallel *RC* circuit connected in series to the gate to improve stability at low frequencies and power gain at higher bandwidth frequencies, as well as a 3:1 voltage ferrite-based transformer and a shunt *RL* circuit to provide broadband input matching with minimum return loss. Here, the series resonant circuit is tuned to 1.0 GHz, whereas the third-harmonic circuit is optimized to 6.5 GHz (referring to higher fundamental frequency). As a result, a drain efficiency of 70% ± 5% with an output power of 40.8 ± 1.2 dBm shown in Fig. 10.48B and a power gain of 11.3 ± 1.2 dB was achieved across the frequency bandwidth from 500 MHz to 2.5 GHz.

10.5 Biharmonic Class-E$_{\mathrm{M}}$ PAs

A basic limitation of a Class-E operation mode at higher frequencies is significant efficiency degradation due to the increased switching power losses with increasing values of the turn-off switching time. To minimize this undesirable effect, it is necessary to find a solution without instant jump in an ideal collector current waveform at turn-off to allow efficient operation at frequencies high enough that the switch turn-off transition would occupy a substantial fraction of the waveform period, of 30% and more. However, the Class-E PAs can deliver nonzero output power only if at least one of the switch waveforms, either voltage or current, has a jump under assumption that the circuit comprises an ideal switch and linear passive components.[42] To satisfy the requirements of both jumpless voltage and current waveforms and sinusoidal load waveform with nonzero output power delivered to the load, it is necessary to allow power flow in the system at two or more harmonically related frequencies. This can be done by using nonlinear reactive elements in the load network to convert the fundamental-frequency

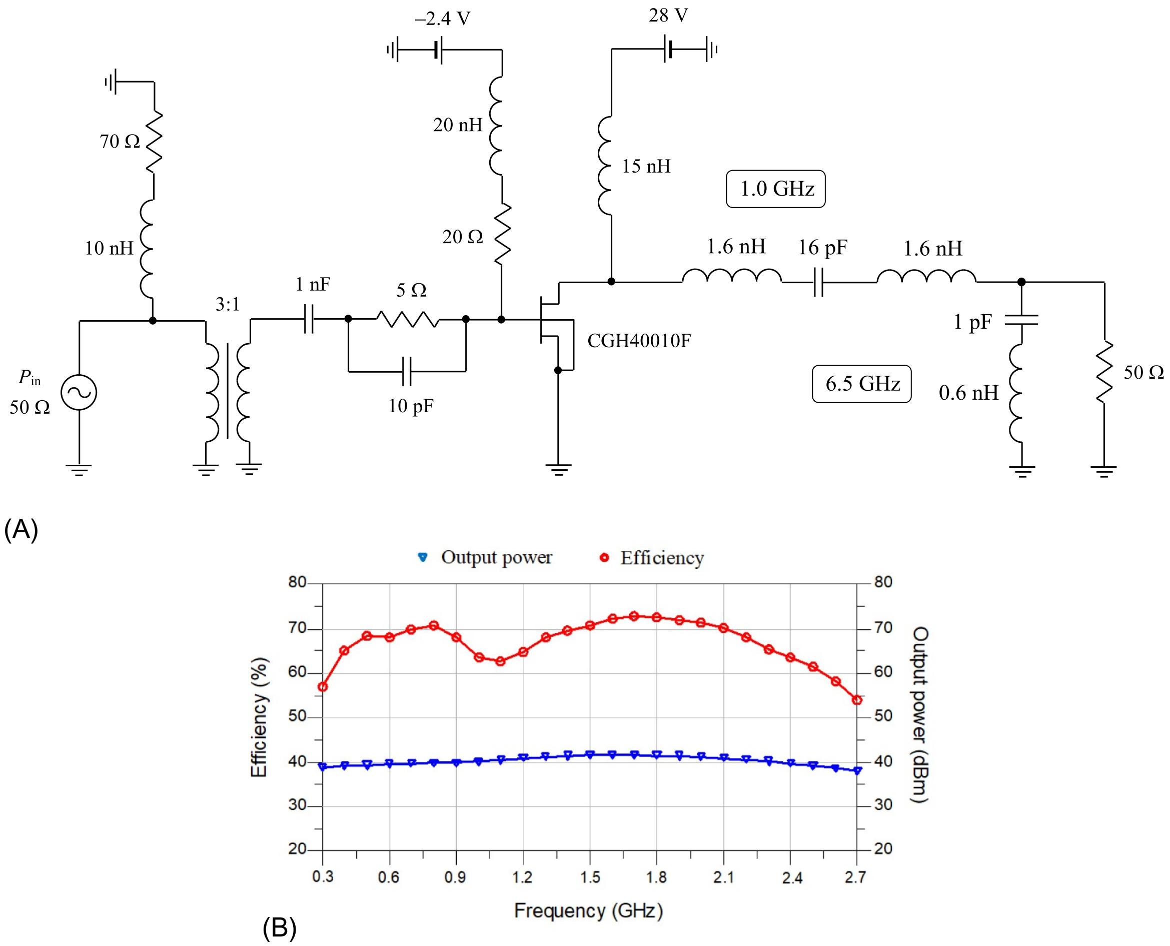

–2.4 V
28 V
70 Ω
10 nH
20 nH
20 Ω
15 nH
1.0 GHz
3:1
1 nF
5 Ω
10 pF
1.6 nH
16 pF
1.6 nH
CGH40010F
1 pF
0.6 nH
6.5 GHz
50 Ω
P_{in}
50 Ω
(A)
Output power
Efficiency
Efficiency (%)
Output power (dBm)
80
70
60
50
40
30
20
0.3
0.6
0.9
1.2
1.5
1.8
2.1
2.4
2.7
Frequency (GHz)
(B)

FIG. 10.48

Schematic and performance of broadband mixed-mode GaN HEMT PA.

power to a desired harmonic frequency or by injecting the harmonic-frequency power into the load network from an external source.

The simplest low-order implementation approach having jumpless switch voltage and current waveforms, called the biharmonic Class-E$_M$ mode and described in Ref. 43 comprises the two-part output stage including

- Main amplifier that consumes DC power equal to approximately 75% of the load power, and converts this power and the power generated by the auxiliary amplifier to power at the output frequency f.
- Smaller auxiliary amplifier (or varactor frequency multiplier), phased locked to the main amplifier, which generates approximately 25% of the load power at the frequency $2f$.

The main amplifier has jumpless switch voltage and current waveforms, while the auxiliary amplifier can be a conventional Class-E PA. If the frequency multiplier is fed from the output of the main amplifier, the load power is reduced by the amount of power converted by the frequency multiplier from frequency f to frequency $2f$ to change the waveform shapes to continuous ones. The higher-order implementations can use harmonic components of order higher than 2, or multiple harmonics. For operation at higher frequencies, the biharmonic Class-E$_M$ PA can be energetically superior to a conventional Class-E PA using the same power device and supplying the same output power at the same operating frequency. That is because it can tolerate slow transistor turn-off with much less efficiency loss. In addition, less input drive is needed for the biharmonic Class-E$_M$ PA because slower switching times are tolerable, considering that switching times are inversely proportional to the square root of the input driving power.

Fig. 10.49 shows the circuit schematic of a biharmonic Class-E$_M$ MOSFET PA designed to operate at 3.5 MHz with second-harmonic power injection from an auxiliary amplifier operating at 7 MHz. The derivation of the ideal drain waveforms of the main amplifier is based on the assumption that the resultant current of the active device, operating as a switch, and its shunt capacitor contains only DC, fundamental, and second-harmonic components written as

$$i(\omega t) = I_0 + I_{1A}\cos\omega t + I_{1B}\sin\omega t + I_{2A}\cos 2\omega t + I_{2B}\sin 2\omega t \tag{10.154}$$

where ω is the angular fundamental frequency, I_{1A} and I_{1B} are the quadrature fundamental current components, and I_{2A} and I_{2B} are the quadrature second-harmonic current components, respectively. The shunt capacitors at the transistor drains can be composed of the device output capacitances and external capacitors.

For a 50% duty ratio when the switch is turned off during $0 < \omega t \le \pi$, the current through the switch $i(\omega t) = 0$, and the current $i_C(\omega t)$ flowing through the capacitor C fully represents the current $i(\omega t)$ given in Eq. (10.154), reproducing the voltage across the switch by charging the capacitor according to

$$v(\omega t) = \frac{1}{\omega C}\int_0^{\omega t} i(\omega t)\, d\omega t \tag{10.155}$$

The optimum conditions for a biharmonic Class-E$_M$ optimum operation with jumpless voltage $v(\omega t)$ and current $i(\omega t)$ waveforms are

$$i(\omega t)|_{\omega t=0} = 0 \tag{10.156}$$

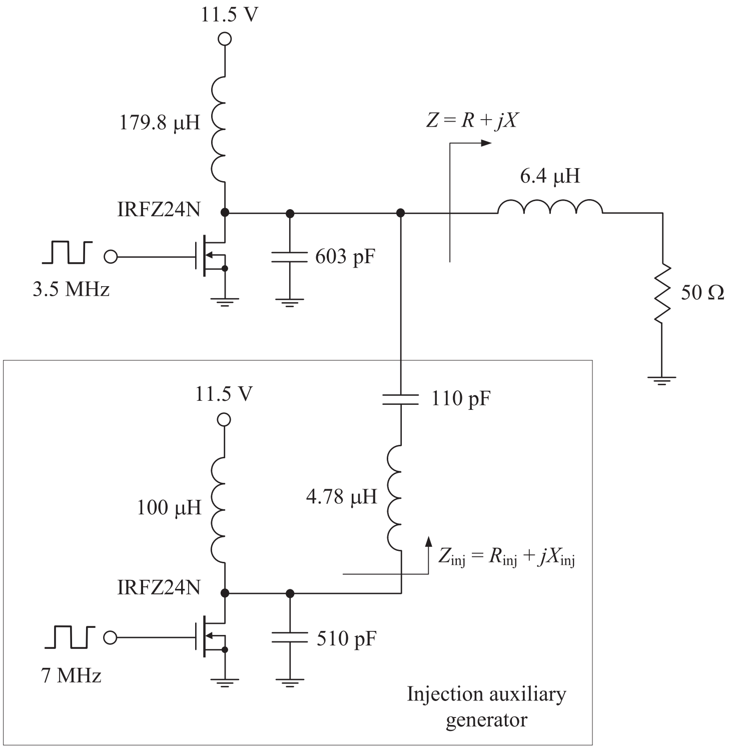

11.5 V
179.8 μH
Z = R + jX
6.4 μH
IRFZ24N
603 pF
3.5 MHz
50 Ω
11.5 V
110 pF
100 μH
4.78 μH
$Z_{\text{inj}} = R_{\text{inj}} + jX_{\text{inj}}$
IRFZ24N
510 pF
7 MHz
Injection auxiliary generator

FIG. 10.49

Biharmonic Class-E_M PA schematic.

$$i(\omega t)|_{\omega t=\pi} = 0 \tag{10.157}$$

$$v(\omega t)|_{\omega t=\pi} = 0 \tag{10.158}$$

$$\left.\frac{v(\omega t)}{d\omega t}\right|_{\omega t=0} = 0 \tag{10.159}$$

Substituting Eq. (10.154) into Eq. (10.155) and applying the boundary conditions given by Eqs. (10.156)–(10.159) yield

$$I_{1A} = 0 \tag{10.160}$$

$$I_{1B} = -\frac{\pi}{2}I_0 \tag{10.161}$$

$$I_{2A} = -I_0 \tag{10.162}$$

$$I_{2B} = \frac{\pi}{4}I_0 \tag{10.163}$$

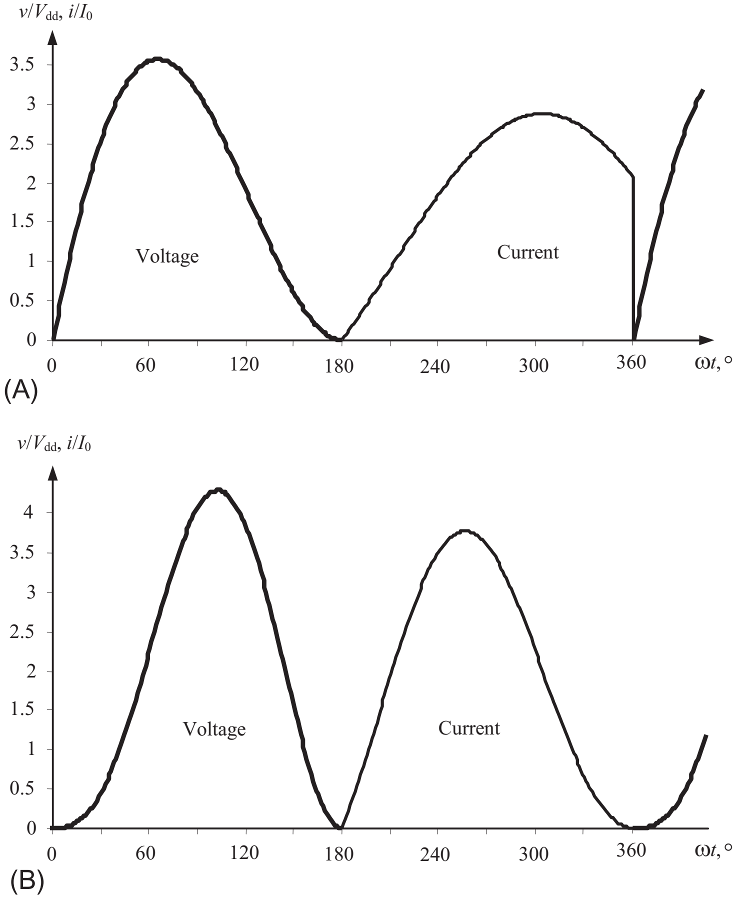


FIG. 10.50

Normalized ideal switch waveforms of (A) Class-E with shunt capacitance and (B) biharmonic Class-E$_M$ with second-harmonic power injection.

As a result, the normalized steady-state ideal switch voltage waveform for a period of $0 \le \omega t < \pi$ and current waveform for a period of $\pi \le \omega t < 2\pi$ are

$$\frac{i(\omega t)}{I_0} = 1 - \frac{\pi}{2}\sin\omega t + \frac{\pi}{4}\sin 2\omega t - \cos 2\omega t \qquad (10.164)$$

$$\frac{v(\omega t)}{V_{dd}} = \frac{2}{\pi}(8\omega t + 4\pi\cos\omega t - \pi\cos 2\omega t - 4\sin 2\omega t - 3\pi) \qquad (10.165)$$

where V_{dd} is the DC supply voltage.

Fig. 10.50B shows the normalized switch voltage and current waveforms for an idealized optimum biharmonic Class-E$_M$ with a second-harmonic power injection. From switch voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch and the current $i(\omega t)$ consisting of the DC, fundamental, and injected second-harmonic components flows through the device. However, when the transistor is turned off, this current flows through the shunt capacitance C. There is no jump in the switch current waveform at the instant of switching off compared to the switch current corresponding to a Class-E with shunt capacitance, the voltage and current waveforms of which are shown in Fig. 10.50A. However, the voltage peak factor is higher in a biharmonic Class-E$_M$ mode exceeding a value of 4. It should be mentioned that injecting a higher-order harmonic component will generally increase the voltage peak factor even more. Also, there is no solution for a biharmonic Class-E$_M$ mode with third-harmonic injection and duty ratio of 50%. The voltage peak factor can exceed a value of 7 for a third-harmonic injection with a duty ratio of 33%. The voltage and current waveforms of the auxiliary amplifier are the usual waveforms corresponding to a switchmode Class-E with shunt capacitance.

In a biharmonic Class-E$_M$ mode, it is assumed that the DC power $P_0 = I_0 V_{dd}$ is equal to approximately 75% of the output load power P_{out} delivered to the load that results in

$$I_0 V_{cc} = \frac{3 P_{out}}{4 V_{dd}} \tag{10.166}$$

The fundamental-frequency load-network impedance of the main amplifier and the second-harmonic injection-port impedance of the auxiliary amplifier can be determined by a Fourier-series analysis of the voltage and current waveforms. As a result, the optimum shunt capacitance C and load-network impedance $Z = R + jX$ for the main amplifier as a function of the DC-supply voltage V_{dd} and output power P_{out} are derived as

$$C = \frac{3\pi}{64}\frac{P_{out}}{\omega V_{dd}^2} \tag{10.167}$$

$$R = \frac{128}{9\pi^2}\frac{V_{dd}^2}{P_{out}} \tag{10.168}$$

$$X = \frac{32\,(3\pi^2 - 32)}{9\pi^3}\frac{V_{dd}^2}{P_{out}} \tag{10.169}$$

while the optimum injection-port impedance $Z_{inj} = R_{inj} + jX_{inj}$ for the auxiliary amplifier can be obtained by

$$R_{inj} = \frac{128}{9\,(\pi^2 + 16)}\frac{V_{dd}^2}{P_{out}} \tag{10.170}$$

$$X_{inj} = -\frac{16\,(3\pi^2 + 16)}{9\pi\,(\pi^2 + 16)}\frac{V_{dd}^2}{P_{out}} \tag{10.171}$$

The measured output power of a second-harmonic Class-E$_M$ PA was 13.2 W with overall PAE of 85.2% at an operating frequency of 3.5 MHz. The injected power at $2f$ necessary to achieve jumpless drain waveforms was measured as 29.8% of the total DC power of the main amplifier instead of the theoretical value of 25% due to the resistive power losses in reactive components, finite loaded quality factors of the series filters, and harmonic power conversions in the nonlinear device capacitances. To achieve simple and accurate design for the Class-E$_M$ PA with higher-order circuits, the numerical design procedure can be applied.[44] The analytical expressions for Class-E$_M$ PA considering the fundamental-frequency and harmonic components in the output currents of the main and auxiliary circuits are given in.[45]

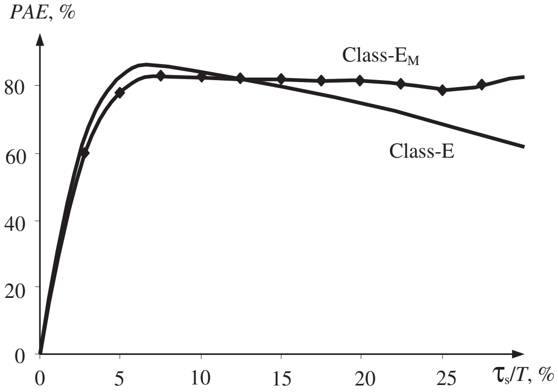


FIG. 10.51

Efficiency versus switching time for Class-E_M and Class-E PAs.

Fig. 10.51 shows the comparison between power-added efficiencies of the second-harmonic Class-E_M and classical Class-E PAs as functions of the normalized transistor switching time τ_s.[43] It is assumed that the switching time is inversely proportional to the input driving power. The plots were simulated for PAs delivering the output power of 3.2 W at an operating frequency of 870 MHz using a pHEMT device with a gate periphery of 0.5 μm × 50 mm in the main amplifier. The peak value of a *PAE* for the biharmonic Class-E_M PA is 3.3% lower than that for the classical Class-E PA. However, a *PAE* for the Class-E_M PA varies by just ±2% for all switching times from 6% to 30% of the period, whereas a *PAE* for the Class-E PA drops monotonically from its peak to 73.5% of its peak value for switching times of 30% of the period.

An analysis of the Class-E_M PA can be simplified and accurate explicit design equations for the load-network parameters can be derived by using an isolation circuit incorporated between the main and auxiliary circuits, thus resulting in a new configuration of the Class-E_M PA shown in Fig. 10.52.[46] Here, both the main and auxiliary circuits consist of a shunt capacitance (C_{s1}, C_{s2}), an RF choke (L_{C1}, L_{C2}), a series resonant circuit (L_1C_1 tuned to the fundamental f_0, L_2C_2 tuned to $2f_0$), and a series reactance (X_1, X_2), respectively. The isolation circuit consists of a series quarterwave transmission line TL_1 and an open-circuit quarterwave stub TL_2, providing a short-circuited termination at the fundamental and odd harmonics with the corresponding open-circuited termination due to TL_1. Thus, the impedance Z_M presented by the auxiliary circuit to the main circuit is sufficiently high with good isolation of the main circuit from auxiliary one at the fundamental and odd harmonics. In this case, an analysis of the main and auxiliary circuits can be done separately. To provide some design flexibility and to extend the maximum operating frequency of the Class-E_M PA, a finite DC-feed inductances L_{C1} and L_{C2} can be used in the main and auxiliary circuits.[47]

In an alternative configuration of the biharmonic Class-E_M PA, one of the harmonics existing at drain of the main stage is filtered, amplified, phase shifted, and injected back to output of the main stage, as shown in Fig. 10.53A.[48] For internal stability of the positive feedback loop created by the harmonic injection circuit, the transistors T_1 and T_2 are biased well below the pinch-off voltage to provide their Class-C operation, and the bandpass filter in the loop is used to surpass all harmonics (except

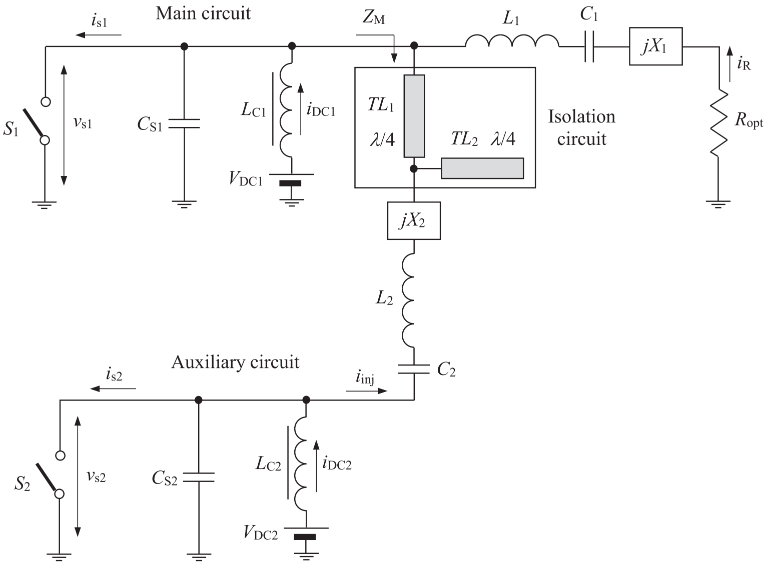


FIG. 10.52

Circuit schematic of Class-E_M PA with isolation circuit.

the second harmonic) with a loop gain lower than 1. Fig. 10.53B shows the chip implementation of Class-E_M PA with a harmonic-injection circuit implemented in a 0.25-μm pHEMT technology with overall size of $3.2 \times 2.0\,mm^2$, where the feedback transmission line *TL* is realized by a 3-mm, 75-Ω microstrip line. As a result, by using the second-harmonic injection scheme delivering a 250-mW power at the second harmonic and consuming a DC-supply power of 370 mW when a drain efficiency of 67.5% for Class-C harmonic-injection circuit is achieved, an output power of 29 dBm with a power gain of 14 dB and a peak *PAE* of 63% was obtained at 2.4 GHz.

10.6 Inverse Class-E PAs

Another approach to the design of the Class-E PA with efficiency of 100% under idealized operation conditions is to use its configuration with shunt inductance.[49] Such a Class-E PA represents an inverse version of a classical Class-E PA with shunt capacitance, where the load-network inductor and capacitor replace each other. In this case, the storage element is a shunt inductor instead of a shunt capacitor, resulting in the inverse collector voltage and current waveforms. The basic circuit of a Class-E PA with shunt inductance as a simplest version of an inverse Class-E mode is shown in Fig. 10.54A, where the load network consists of an inductor L shunting the transistor, a series capacitor C, a series fundamentally tuned L_0C_0 circuit, and a load resistor R. Fig. 10.54B shows the equivalent circuit of such a switch-mode PA where the active device is considered an ideal switch that is driven so as to provide the device switching between its on-state and off-state operation conditions.

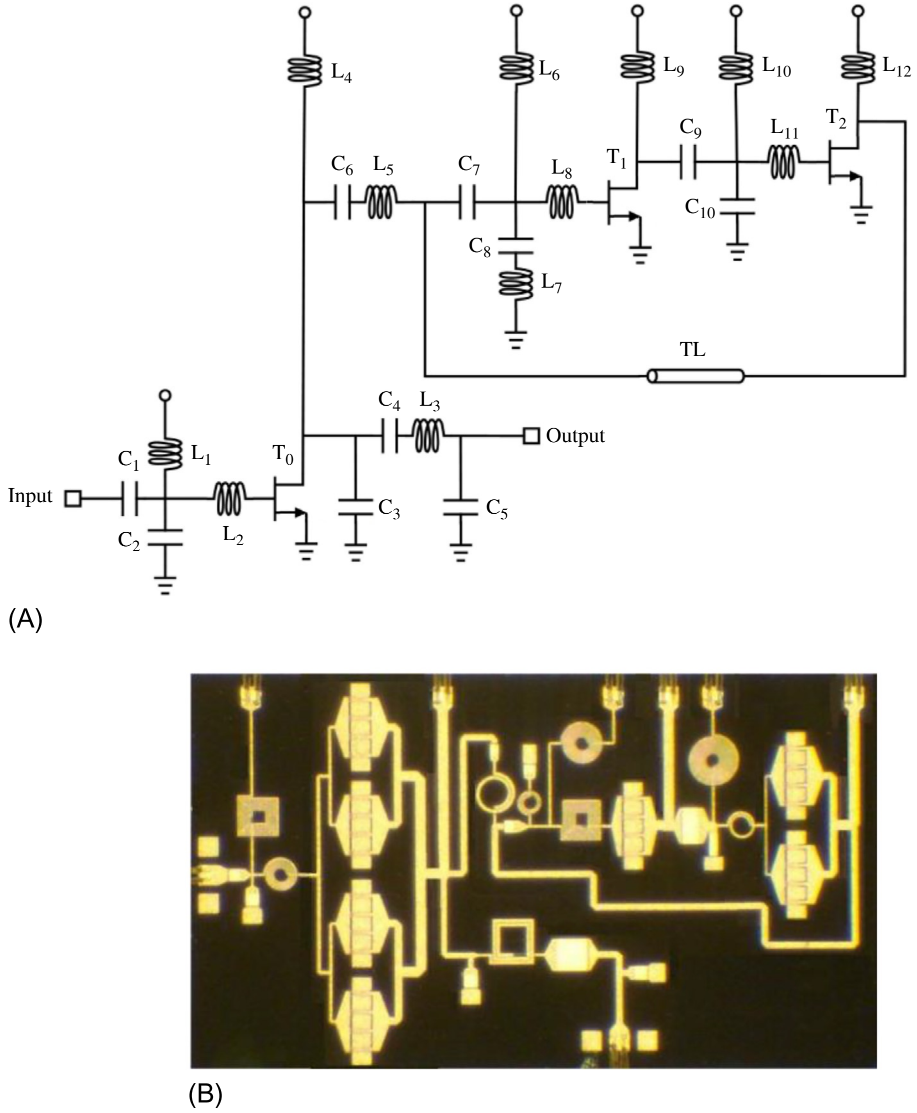

L4
L6
L9
L10
L12
C6
L5
C7
L8
T1
C9
L11
T2
C10
C8
L7
TL
C4
L3
Output
C1
L1
T0
Input
C2
L2
C3
C5
(A)
(B)

FIG. 10.53

Circuit schematic of Class-E_M PA with second-harmonic injection and its chip implementation.[48]

To simplify an analysis of a Class-E PA with shunt inductance, the following several assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.
- The loaded quality factor $Q_L = \omega L_0/R = 1/\omega C_0 R$ of the series resonant L_0C_0 circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal at the switching frequency.

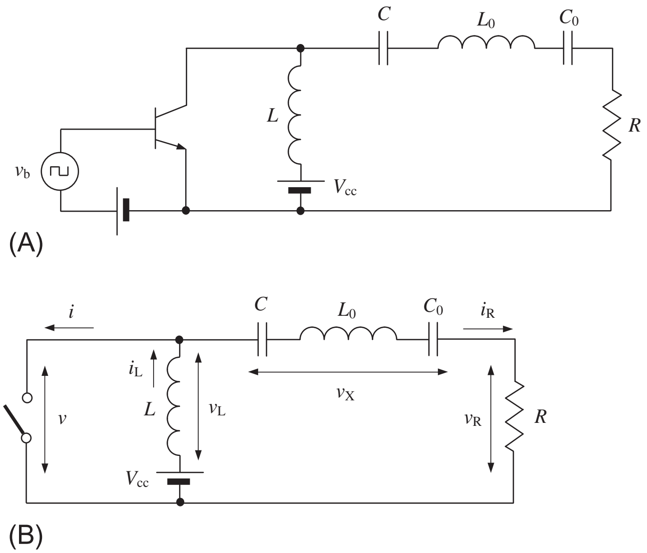


FIG. 10.54

Basic circuits of Class-E PA with shunt inductance.

- There are no losses in the circuit except only in the load R.
- For an optimum operation mode, a 50% duty ratio is used.

In the Class-E mode with shunt inductance similar to the other Class-E modes, it is possible to eliminate power losses during on-to-off transition by providing the following collector current conditions:

$$i(\omega t)\big|_{\omega t=2\pi}=0 \tag{10.172}$$

$$\left.\frac{di(\omega t)}{d\omega t}\right|_{\omega t=2\pi}=0 \tag{10.173}$$

where $i(\omega t)$ is the current flowing through the switch. These conditions are important to provide zero on-to-off switching time without any power dissipation and can be performed by proper choice of the load-network parameters.

For the simplified PA circuit shown in Fig. 10.54B, the relationships between the voltages and currents can be written as

$$i(\omega t)=i_L(\omega t)-i_R(\omega t) \tag{10.174}$$

$$v(\omega t)=V_{cc}-v_L(\omega t) \tag{10.175}$$

where the load current i_R is assumed sinusoidal,

$$i_R(\omega t)=I_R\sin(\omega t+\varphi) \tag{10.176}$$

with the amplitude I_R and initial phase φ.

When the switch is turned off during $0\le\omega t\le\pi$,

$$i(\omega t)=0 \tag{10.177}$$

then from Eqs. (10.174) and (10.176) it follows that

$$i_{\mathrm{L}}(\omega t) = i_{\mathrm{R}}(\omega t) = I_{\mathrm{R}} \sin(\omega t + \varphi) \tag{10.178}$$

At the same time, the voltage across the inductor L can be written as

$$v_{\mathrm{L}}(\omega t) = \omega L \frac{di_{\mathrm{L}}(\omega t)}{d\omega t} = \omega L I_{\mathrm{R}} \cos(\omega t + \varphi) \tag{10.179}$$

from which it follows that the voltage $v(\omega t)$ according to Eq. (10.175) is

$$v(\omega t) = V_{\mathrm{cc}} - \omega L I_{\mathrm{R}} \cos(\omega t + \varphi) \tag{10.180}$$

When the switch is turned on during $\pi \le \omega t \le 2\pi$,

$$v(\omega t) = 0 \tag{10.181}$$

then substituting Eq. (10.181) into Eq. (10.175) yields

$$v_{\mathrm{L}}(\omega t) = V_{\mathrm{cc}} \tag{10.182}$$

By using Eqs. (10.178), (10.179), and (10.182), the current flowing through the inductor L can be obtained as

$$i_{\mathrm{L}}(\omega t) = \frac{V_{\mathrm{cc}}}{\omega L}(\omega t - \pi) - I_{\mathrm{R}} \sin\varphi \tag{10.183}$$

Hence, from Eqs. (10.174), (10.176), and (10.183), it follows that

$$i(\omega t) = \frac{V_{\mathrm{cc}}}{\omega L}(\omega t - \pi) - I_{\mathrm{R}}[\sin(\omega t + \varphi) + \sin\varphi] \tag{10.184}$$

Applying a zero-current switching condition given by Eq. (10.172) to Eq. (10.184) gives

$$I_{\mathrm{R}}(\omega t) = \frac{\pi V_{\mathrm{cc}}}{2\omega L \sin\varphi} \tag{10.185}$$

where $0 < \varphi < \pi$ because $I_{\mathrm{R}} > 0$.

As a result, by substituting Eqs. (10.185) into Eq. (10.184), the steady-state current waveform across the switch can be obtained as

$$i(\omega t) = \frac{V_{\mathrm{cc}}}{\omega L}\left[\omega t - \frac{3\pi}{2} - \frac{\pi}{2\sin\varphi}\sin(\omega t + \varphi)\right] \tag{10.186}$$

Applying a zero current-derivative switching condition given by Eq. (10.173) to Eq. (10.186) gives

$$\tan\varphi = \frac{\pi}{2} \tag{10.187}$$

resulting in the phase angle equal to

$$\varphi = \tan^{-1}\left(\frac{\pi}{2}\right) = 57.518^{\circ} \tag{10.188}$$

From Eq. (10.187), it follows that

$$\sin\varphi = \frac{\pi}{\sqrt{\pi^2 + 4}} \tag{10.189}$$

$$\cos\varphi = \frac{2}{\sqrt{\pi^2 + 4}} \tag{10.190}$$

which allows us to rewrite Eq. (10.186) as

$$i(\omega t) = \frac{V_{cc}}{\omega L}\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{10.191}$$

By using a Fourier-series expansion, the DC-supply current is

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\, d\omega t = \frac{V_{cc}}{\pi\omega L} \tag{10.192}$$

whereas the fundamental-current amplitude can be obtained using Eqs. (10.185), (10.189), and (10.192) as

$$I_R = \frac{\pi\sqrt{\pi^2+4}}{2} I_0 = 5.8499 I_0 \tag{10.193}$$

As a result, the normalized steady-state collector current waveform for $\pi \le \omega t \le 2\pi$ and the normalized voltage waveform for $0 \le \omega t \le \pi$ are

$$\frac{i(\omega t)}{I_0} = \pi\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{10.194}$$

$$\frac{v(\omega t)}{V_{cc}} = \frac{\pi}{2}\sin\omega t - \cos\omega t + 1 \tag{10.195}$$

From the voltage and current waveforms shown in Fig. 10.55, it follows that, when the switch is turned off, the switch current $i(\omega t)$ is zero, and the inductor current i_L is determined by the sinusoidal load current i_R. However, when the switch is turned on, the switch voltage $v(\omega t)$ is zero and the DC-supply voltage V_{cc} produces the linearly increasing current i_L. The difference between the inductor current i_L and the load current i_R flows through the switch.

The peak collector current I_{max} and voltage V_{max} can be determined by differentiating the corresponding waveforms given by Eqs. (10.194) and (10.195) and setting the results equal to zero, thus resulting in

$$I_{max} = \pi(\pi - 2\varphi) I_0 = 3.562 I_0 \tag{10.196}$$

$$V_{max} = \left(\frac{\sqrt{\pi^2+4}}{2} + 1\right) V_{cc} = 2.8621\, V_{cc} \tag{10.197}$$

Under the assumption of a sinusoidal load current, the load voltage is also sinusoidal,

$$v_R(\omega t) = V_R \sin(\omega t + \varphi) \tag{10.198}$$

where $V_R = I_R R$ is the voltage amplitude across the load resistor.

The voltage v_X across the elements of the series resonant circuit is not sinusoidal. Consequently, its fundamental component across the capacitance C is obtained due to an assumed high Q_L-factor as

$$v_C(\omega t) = -V_C \cos(\omega t + \varphi) \tag{10.199}$$

where $V_C = I_R/\omega C$ is the voltage amplitude on the capacitor.

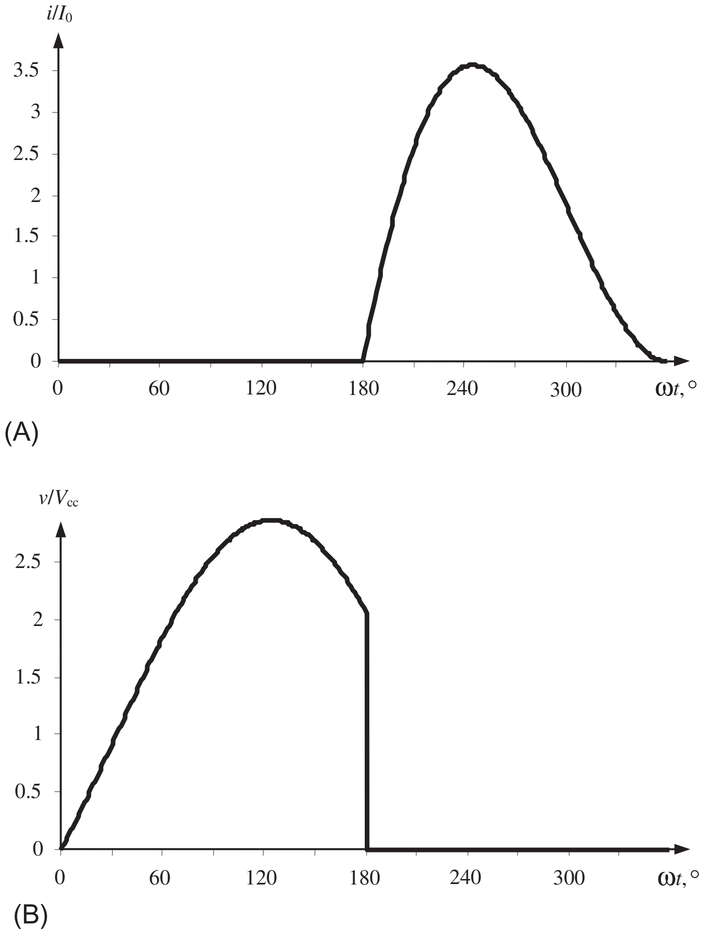


FIG. 10.55

Normalized switch voltage and current waveforms for inverse Class-E mode.

As a result, the phase shift between the fundamental components of the capacitor and load-resistor voltages can be defined by

$$\tan\psi \;=\; -\frac{V_{\mathrm{C}}}{V_{\mathrm{R}}} = -\frac{1}{\omega RC} \tag{10.200}$$

Using Eq. (10.195) for the idealized collector voltage waveform and applying a Fourier-series expansion yields

$$V_{\mathrm{R}} = \frac{1}{\pi}\int_{0}^{2\pi} v(\omega t)\sin(\omega t+\varphi)d\omega t = \frac{4V_{\mathrm{cc}}}{\pi\sqrt{\pi^2+4}} = 0.3419V_{\mathrm{cc}} \tag{10.201}$$

$$V_C = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t+\varphi)d\omega t = \frac{(\pi^2+12)V_{cc}}{4\sqrt{\pi^2+4}} = 1.4681V_{cc} \tag{10.202}$$

Substituting Eqs. (10.192) and (10.193) into Eqs. (10.201) and (10.202) results in

$$V_R = \frac{8}{\pi(\pi^2+4)}\omega L I_R \tag{10.203}$$

$$V_C = \frac{\pi^2+12}{2(\pi^2+4)}\omega L I_R \tag{10.204}$$

Hence, by using Eq. (10.200), the optimum series inductance L and shunt capacitance C can be calculated as.

$$\frac{\omega L}{R} = \frac{\pi(\pi^2+4)}{8} = 5.4466 \tag{10.205}$$

$$\omega CR = \frac{16}{\pi(\pi^2+12)} = 0.2329 \tag{10.206}$$

with an optimum phase angle ψ equal to

$$\psi = -\tan^{-1}\left[\frac{\pi(\pi^2+12)}{16}\right] = -76.891° \tag{10.207}$$

The optimum phase angle ϕ of the entire load network with a shunt inductor L and a series capacitor C is calculated by using Eqs. (10.205) and (10.206) as equal to.

$$\phi = -35.945\ \text{degrees} \tag{10.208}$$

which indicates that the input impedance of such a load network is capacitive.

The optimum load resistance R can be found using Eq. (10.201) by

$$R = \frac{8}{\pi^2(\pi^2+4)}\frac{V_{cc}^2}{P_{out}} = 0.05844\frac{V_{cc}^2}{P_{out}} \tag{10.209}$$

The high-Q_L assumption for the series resonant L_0C_0 circuit can lead to considerable errors if its value is substantially small in real circuits.[50] For example, for a 50% duty ratio, the values of the optimum shunt inductance L, collector current peak factor, and second-harmonic current component increase rapidly for $Q_L < 5$.

Fig. 10.56 shows an alternative inverse Class-E load-network configuration with a series inductor L, a shunt capacitor C, and a parallel resonant L_0C_0 circuit tuned to the fundamental

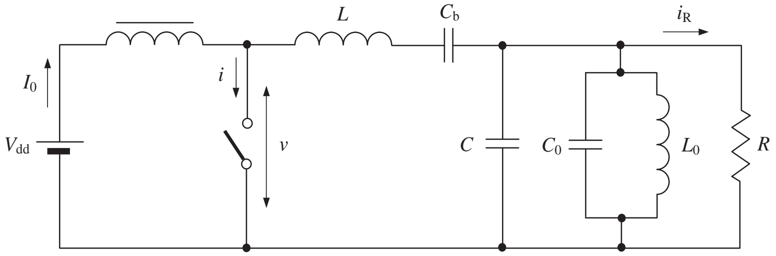


FIG. 10.56

Equivalent circuit of inverse Class-E PA with series inductance.

frequency.[51] Here, the RF choke is necessary to supply the DC current I_0 and the blocking capacitor C_b is required to decouple the parallel resonant circuit from the DC path. Such an inverse Class-E with series inductance and shunt capacitance is dual to a classical Class-E with shunt capacitance and series inductance. In this case, the series resonant L_0C_0 circuit is replaced by its parallel equivalent configuration. However, it is characterized by the same switch voltage and current waveforms, as shown in Fig. 10.55 for an inverse Class-E configuration with shunt inductance and series capacitance.

The optimum series inductance L, shunt capacitance C, and load resistance R of the Class-E load network with series inductance and shunt capacitance can be calculated as

$$\frac{\omega L}{R} = \frac{8}{\pi(\pi^2+4)} = 0.1836 \tag{10.210}$$

$$\omega CR = \frac{\pi(\pi^2-4)}{16} = 1.1525 \tag{10.211}$$

$$R = \frac{\pi^2+4}{8}\frac{V_{\mathrm{dd}}^2}{P_{\mathrm{out}}} = 1.7337\frac{V_{\mathrm{dd}}^2}{P_{\mathrm{out}}} \tag{10.212}$$

where V_{dd} is the drain supply voltage and P_{out} is the fundamental-frequency output power delivered to the load.[52, 53]

The previous analysis was based on the assumption of a zero output capacitance of the active device. However, at high frequencies and for high-power applications, this capacitance cannot be considered negligible and should be considered. In this case, the PA could operate in a switching mode with both shunt and series capacitances when the required idealized operations conditions are realized with zero-current and zero current-derivative switching conditions. At the same time, to compensate for the capacitor nonzero discharging process, it is necessary to provide a zero voltage-derivative condition. Therefore, the theoretical analysis illustrates the infeasibility of a zero-current switching Class-E mode to approach 100% collector efficiency with nonzero device output capacitance.[54] Moreover, the collector efficiency will drop drastically if the output device capacitance is significant. This means that, in the frequency domain, the harmonic impedance conditions should be different, being inductive at the fundamental frequency and capacitive for higher-order harmonics, which can be achieved only with zero-voltage switching conditions.

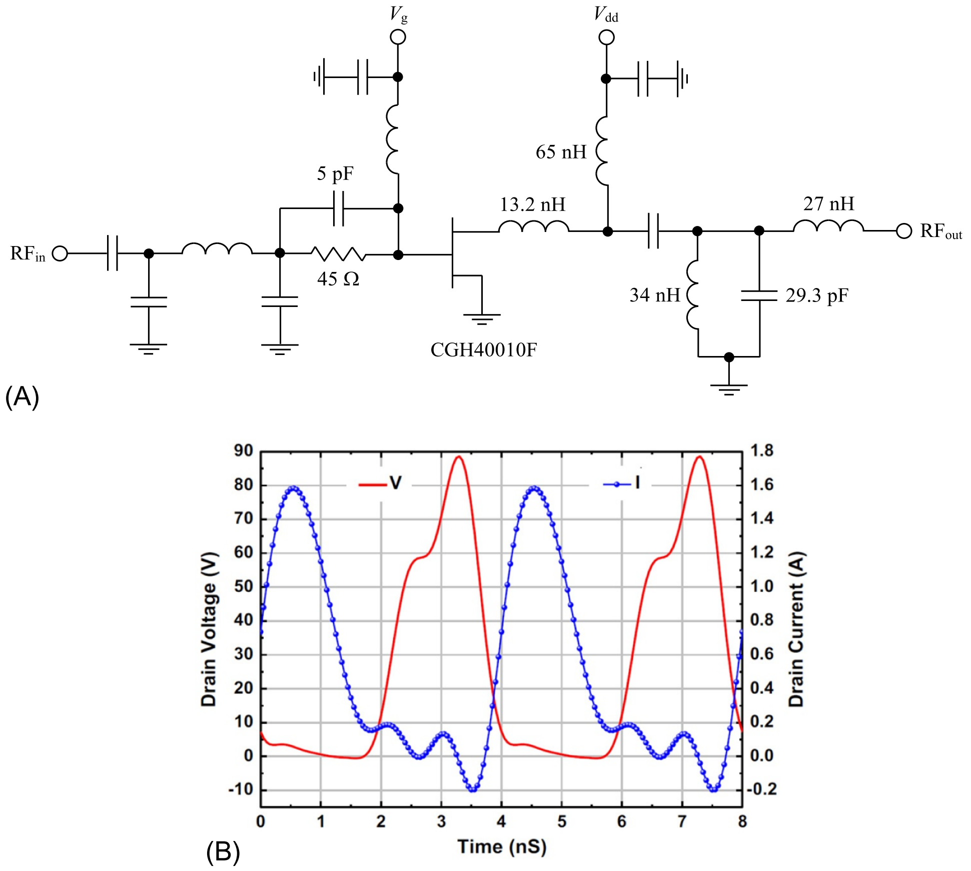
However, there is a class of the pHEMT or GaN HEMT devices, the output capacitance of which is sufficiently small and can be used for a low- or medium-power high-frequency Class-E PA application. The typical value of the drain-source capacitance for a 0.5-μm pHEMT device with a total gate width of 8 × 75 μm is of about 0.25 pF, and, as a first approximation, it increases linearly with total gate width.[53] The simulation results at an operating frequency of 2.5 GHz show that, for the same device parameters when using output capacitance as a variable, the drain efficiency is just slightly affected when its value is $<$0.7 pF. However, the drain efficiency reduces significantly as the drain-source capacitance increases above 0.7 pF. Consequently, there is a limitation in the device size, above which it is not possible to achieve high drain efficiency. To estimate the maximum achievable output power, it is necessary to consider typical pHEMT DC current density of 300 mA/mm for reliable operation. The measurements results of a hybrid single-stage PA using a pHEMT device with the gate width of 6 × 50 μm and standard surface-mounted components in an inverse Class-E mode with series inductance exhibited an output power of 18 dBm with a power gain of 18 dB and a drain efficiency of 95% at an operating frequency of 870 MHz and a DC-supply voltage of 2 V.[51]

To provide an additional harmonic control in an inverse Class-E, a third-harmonic tank can be included in series to the series inductance.[55] In this case, the drain current waveform can be flattened and the power capability of a Class-F_3/E PA can be maximized. The test results show that, when using a an IRF510 MOSFET, a drain efficiency of 88% can be achieved with an output power of 40 dBm at an operating frequency of 4 MHz.

It should be mentioned that the inverse Class-E PA at subnominal condition with only zero-current switching condition is characterized by lower switch voltage peak factor and lower switch voltage jump at the off-to-on instant.[56] However, its tolerance ability is not as good as that of the Class-E PA at nominal condition. In this case, the variation of the circuit parameters should be limited to ±10%, and the parasitic shunt capacitance should be $<$10% of the smallest capacitance of all circuit elements. At the same time, the out-of-nominal conditions can enhance the degree of the design freedom when the design equations corresponding to zero-current switching condition can be obtained for any load resistance with the given peak switch voltage.[57] To reduce the effect of the parasitic shunt capacitance mainly represented by the device drain-source capacitance, the compensating shunt inductance can be used.[58, 59]

Another approach to reduce the effect of the parasitic shunt capacitance is to use a finite DC-feed inductance which is resonated with the shunt capacitance at the fundamental frequency. At microwaves, the shunt inductance can be replaced by a short-length short-circuited microstrip line. Fig. 10.57A shows the circuit schematic of an inverse Class-E PA based on a 10-W GaN HEMT device intended to operate at 250 MHz, with the simulated drain voltage and current waveforms shown in Fig. 10.57B.[60] The measured output power of 40 dBm with a drain efficiency of 80.1% and a *PAE* of 78.9% was obtained with an input power of 22 dBm at a DC-supply voltage of 28 V.

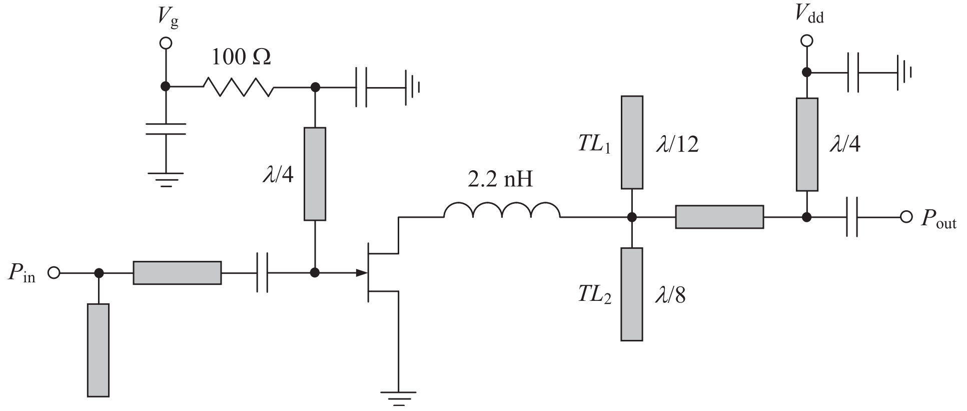
Fig. 10.58 shows the circuit schematic of a transmission-line inverse Class-E PA, where the shunt capacitor C shown in Fig. 10.56 is replaced by two shunt open-circuit stubs to provide the second- and third-harmonic short-circuit terminations, thus dispensing with the need for a parallel-tuned L_0C_0 circuit.[61, 62] The electrical lengths of the open-circuit stubs are 45 degrees and 30 degrees at the fundamental frequency f_0, representing an overall capacitive reactance, and they are equivalent to 90 degrees



V_g
V_{dd}
5 pF
65 nH
13.2 nH
27 nH
RF_{in}
RF_{out}
45 Ω
34 nH
29.3 pF
CGH40010F
(A)
V
I
Drain Voltage (V)
Drain Current (A)
90
80
70
60
50
40
30
20
10
0
-10
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0
1
2
3
4
5
6
7
8
Time (nS)
(B)

FIG. 10.57

Circuit schematic of inverse Class-E PA with finite DC-feed inductance and its drain voltage and current waveforms.



V_g
100 Ω
$\lambda/4$
P_{in}
2.2 nH
TL_1
$\lambda/12$
TL_2
$\lambda/8$
V_{dd}
$\lambda/4$
P_{out}

FIG. 10.58

Circuit schematic of transmission-line inverse Class-E PA.

at $2f_0$ and $3f_0$, respectively. As a result, for a 0.3-μm GaAs MESFET with a gate width of 1200 μm, an output power of 22 dBm with a drain efficiency of 69% was obtained at an operating frequency of 2.3 GHz with a DC-supply voltage of 3 V.

10.7 Harmonic tuning using load-pull techniques

Generally, the transistor in the PA is operated as a nonlinear active device under large-signal conditions, resulting in a significant number of harmonic components. Because the second harmonic is the largest harmonic component, it was found experimentally that just providing the proper source and load second-harmonic terminating impedances at the input and output ports of the transistor, respectively, can significantly improve the PA efficiency At microwave frequencies, the special network based on three coupled bars positioned between two ground planes was used to realize a wide range of impedance matching at the fundamental frequency, while simultaneously presenting reactive impedance at the second harmonic, thus decoupling the second-harmonic signal from a 50-Ω load.[63]

To maximize the PA efficiency, the optimum impedances at the harmonic components must be provided at the transistor output port. Those impedances must be measured or simulated very accurately at microwave frequencies, considering the device parasitic elements and difficulties in accurately defining the values of the device equivalent circuit parameters under large-signal operation. Since it is necessary to realize zero or infinite harmonic impedance conditions seen by the internal device multiharmonic current source required for ideal conventional Class-F or inverse Class-F modes, the corresponding optimum reactances at the harmonics must be presented at the device external output port which can then be translated to those internal required for a switchmode operation. Once the optimum impedances at the device output at the second and third harmonics are established by accurate measurements or simulations, the next step is to properly design the load network using lumped or transmission-line elements to achieve those impedances.

Fig. 10.59 shows the circuit configuration of a high-efficiency MESFET PA using a harmonic-reaction technique based on the effect of the second-harmonic injection.[64] Unlike the balanced PA, this configuration includes a second-harmonic path between the output ports of the devices. The fundamental-frequency output paths and second-harmonic path are designed to provide independent matching of the device output impedances: conjugate impedance matching with a 50-Ω load at the fundamental frequency and optimum reactance matching at the second harmonic for maximum drain efficiency. Because the second-harmonic path has well-matched impedance characteristics, each MESFET device mutually injects without reflection a second-harmonic component into the other MESFET device through the second-harmonic path. However, it should be noted that a high-efficiency operation is possible only if both devices are driven with phase-coherent and equal-amplitude input signals. As a result, an output power of 5 W with a *PAE* of 70% and a drain efficiency of 75% was obtained at an operating frequency of 2 GHz and a supply voltage of 7 V.

Fig. 10.60A shows the circuit schematic of a single-ended *X*-band MESFET PA designed to provide simultaneously the optimum load impedance at the fundamental frequency and zero impedance at the second harmonic at the device output.[65] The load network includes the series parasitic drain lead inductor, whose value was optimized to provide the proper reactance to the device. An open-circuit stub with electrical length of 45 degrees at the fundamental was used for the second-harmonic short circuit. Since it presents a capacitive reactance at the fundamental frequency, it becomes a part of the output

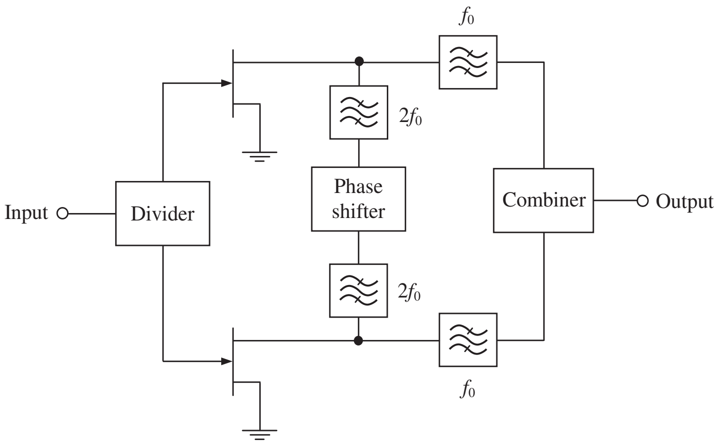

f_0
$2f_0$
Input
Divider
Phase shifter
Combiner
Output
$2f_0$
f_0

FIG. 10.59

Circuit configuration of harmonic-reaction amplifier.

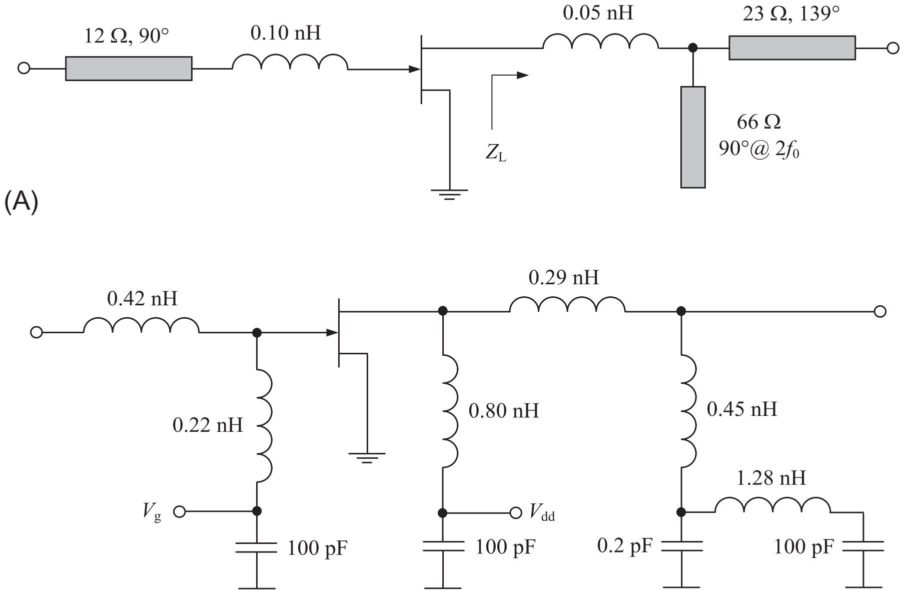

12 Ω, 90°
0.10 nH
0.05 nH
23 Ω, 139°
Z_L
66 Ω
90°@ $2f_0$
(A)
0.42 nH
0.29 nH
0.22 nH
0.80 nH
0.45 nH
1.28 nH
V_g
V_{dd}
100 pF
100 pF
0.2 pF
100 pF
(B)

FIG. 10.60

Circuit schematics of Class-B PA with harmonic tuning.

matching circuit as a shunt capacitor. An output power of 450 mW and a maximum *PAE* of 61% with a drain efficiency of 76% were obtained at an operating frequency of 10 GHz, using a GaAs MESFET device with a gate geometry of 0.5 μm × 1200 μm. The same PA without second-harmonic tuning circuit had demonstrated a *PAE* of only 50%. Fig. 10.60B shows the circuit schematic of an *X*-band 0.5-W MESFET PA with the same device geometry having a load network with lumped elements tuned to optimally terminate the second and third harmonics.[66] As a result, the measured efficiency of the PA with optimal harmonic tuning achieved 49.3%, while the maximum efficiency reduced to 44.5% when the device was tuned to the fundamental only.

Generally, the second-harmonic-tuned PA design strategy can be based on the control of the harmonic terminations at both input and output device ports, so as to properly shape the gate and drain voltage waveforms at 1-dB gain-compression point.[67] In this case, input matching circuit is responsible for assuring the fundamental conjugate-matching condition and shaping the device input waveform, thus controlling the generation of properly phase-related drain-current harmonic components. The load network is responsible for shaping the device output voltage waveform and delivering maximum output power to the load at the fundamental frequency. For an integrated PA structure, the input and output matching circuits can be designed using high-dielectric substrates to be implemented into a small-size package. In this case, the input matching circuit includes two quarterwave transmission lines to transform the standard 50-Ω source to the device input impedance and open-circuit stubs to provide a second-harmonic reflection phase of around 180 degrees (short) at the gate. The output matching circuit comprises three transmission-line transformers with different characteristic impedances to transform the fundamental-frequency low optimum impedance at the device drain with the standard 50-Ω load and to provide the second-harmonic impedance close to open-circuit condition. As a result, a drain efficiency of 68% was achieved for a 100-W GaN HEMT PA (package cavity size is 14.3 mm × 15.2 mm) with a DC-supply voltage of 40 V at an operating frequency of 4 GHz.[68]

Fig. 10.61 shows the circuit schematic of a load network with distributed harmonic control, which was designed to operate in the frequency range of 1.8 to 2.3 GHz and provide a support of multiband and multistandard operation.[69] The load network is composed of two separate blocks: a fundamental matching circuit and a second-harmonic inductive termination circuit. In this case, the fundamental matching circuit consisting of three series transmission lines TL_1, TL_2, and TL_3 of different characteristic impedances and electrical lengths is relatively simple because the optimum impedance remains relatively constant over the required frequency range. Therefore, the fundamental matching impedance was optimized for a center bandwidth frequency of 2.14 GHz. Since the optimum second-harmonic termination Z_{net} varies significantly over the required frequency range, a distributed topology with multiple discrete harmonic terminations was designed and optimized for $f_1 = 1.85$ GHz, $f_2 = 1.96$ GHz, and $f_3 = 2.14$ GHz. As a result, drain efficiencies over 60% were achieved between 1.77 and 2.17 GHz for a 45-W GaN HEMT PA. Note that generally high efficiency can be achieved over a range of second-harmonic termination phase, and, as the second-harmonic termination is swept from capacitive to inductive, the optimal fundamental impedance sweeps from inductive to capacitive.[70]

One popular and effective way to measure the fundamental optimum equivalent device output impedance is to use the passive or active load-pull measurement system.[71, 72] The objective of the active

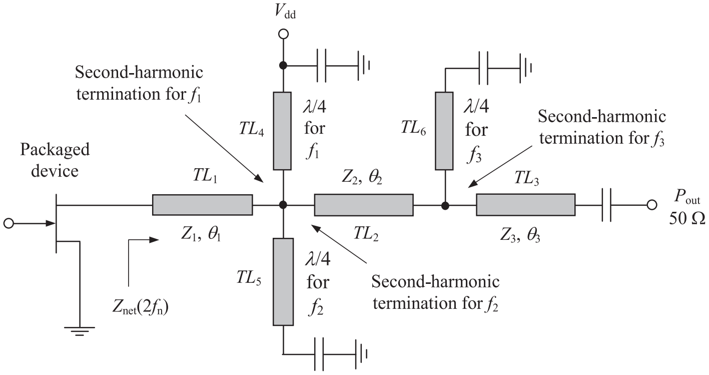


FIG. 10.61

Circuit schematic of load network with distributed second-harmonic control.

load-pull measurement technique is to find the best output load in terms of the optimum value of the load reflection coefficient $\Gamma_L(f_0)$ presented to the transistor output at the fundamental frequency, such that the power gain and PAE are optimized. Although cumbersome and labor intensive, such an experimental technique can provide accurate information regarding the nonlinear operation of the active device. It should be mentioned that the transistor large-signal S-parameters measured at the certain bias condition and output power provide insufficient information for the design of strongly driven PAs with strongly nonlinear behavior of the active device. Therefore, when the transistor is operated in a nonlinear mode, measurement techniques are required that reproduce large-signal operation in the form of the input and output impedances or a nonlinear active device model valid for all used bias conditions and frequency ranges.

Fig. 10.62 shows the basic components of an active load-pull measurement system based on two six-port reflectometers.[73] At the input of the device under test (DUT), the six-port reflectometer SP_1 provides a measurement of the large-signal reflection coefficient $\Gamma_{in}(f_0)$ and the input power $P_{in}(f_0)$ absorbed by the DUT. At the output of the DUT, the measurements of the large-signal reflection coefficient $\Gamma_L(nf_0)$ and the output power $P_L(nf_0)$ for $n = 1, 2$ are achieved by the six-port reflectometer SP_2. The evaluation of $\Gamma_L(nf_0)$ and $P_L(nf_0)$ at a particular frequency requires that the power at that frequency be extracted from the output spectrum by means of splitting and filtering circuits inserted between all detection ports and the power sensors. Performing a fundamental load-pulling consists of varying the load $\Gamma_L(f_0)$ over the entire Smith chart with RF and DC measurements for each load, while the load $\Gamma_L(2f_0)$ is maintained constant and near 50 Ω. However, the fundamental load-pull technique does not include the effects of harmonic loading. The second harmonic load-pull characterization is based on varying the load $\Gamma_L(2f_0)$, while maintaining the load $\Gamma_L(f_0)$ at a desired value. As a result, it was found that the best performance in terms of power gain and PAE is obtained for purely reactive second-harmonic loads, since this allows the elimination of the resistive power losses. For a specific case of the MESFET PA designed to operate at 3.5 GHz, an improvement of PAE by about 8% was achieved by using a second-harmonic active load-pull characterization technique. The active load-pull

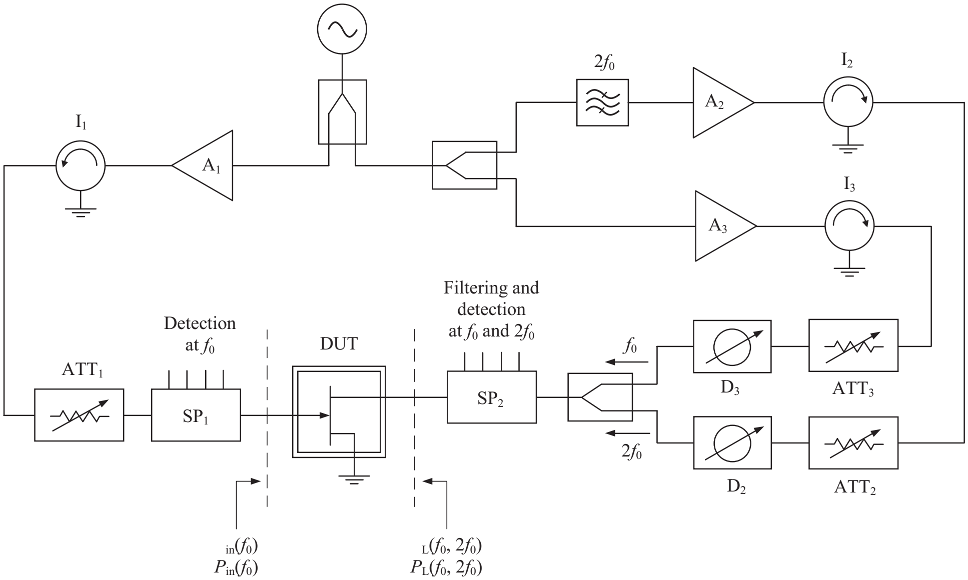

$2f_0$
I_2
I_1
A_2
A_1
I_3
A_3
Filtering and detection at f_0 and $2f_0$
Detection at f_0
DUT
f_0
ATT_1
SP_2
SP_1
D_3
ATT_3
$2f_0$
D_2
ATT_2
$_{in}(f_0)$
$P_{in}(f_0)$
$_L(f_0, 2f_0)$
$P_L(f_0, 2f_0)$

FIG. 10.62

Harmonic active load-pull measurement system schematic.

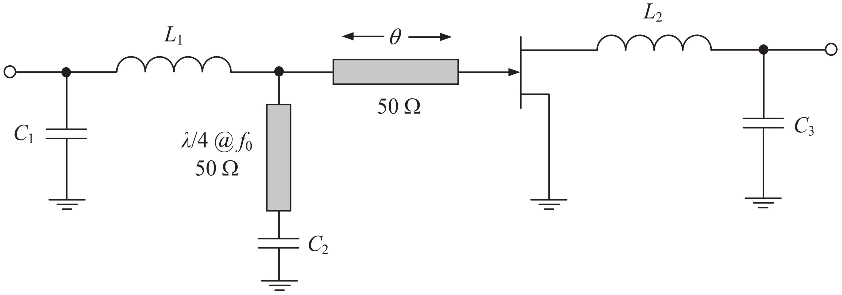

L_2
L_1
θ
$50\ \Omega$
C_1
$\lambda/4$ @ f_0
$50\ \Omega$
C_3
C_2

FIG. 10.63

Circuit schematic of Class-AB PA with source-harmonic tuning.

system based on a six-port reflectometer can also be used to optimize both linearity and output power or *PAE* for modulated signal.[74]

In addition to harmonic loading at the device output, the harmonic tuning at the device input can also be effective. For Class-AB PAs, both the linearity and efficiency can be improved by proper suppression of even-order harmonic components at the device input. Fig. 10.63 shows an example of the circuit schematic of a microwave MESFET PA with a source second-harmonic tuning designed to operate in a Class-AB mode.[75] To terminate even harmonics at the device input, a quarterwave shunt

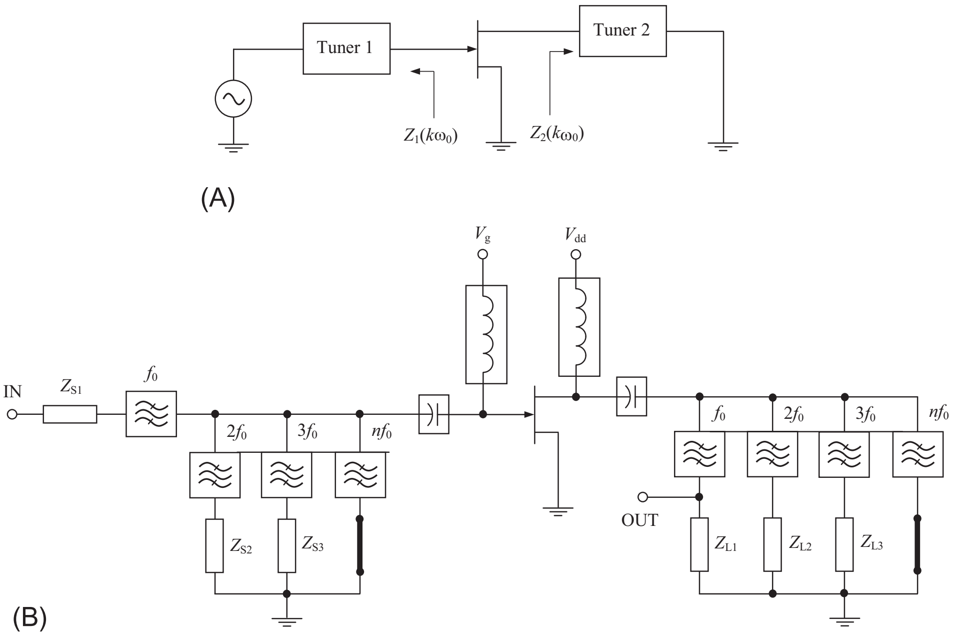


FIG. 10.64

Circuit topologies for multiharmonic load-pull design procedure.

transmission line was short-circuited at its far end using a large-value capacitance C_2. The series transmission line with varying electrical length θ is necessary to provide a symmetrical gate-voltage waveform by compensating for the phase of terminating second-harmonic component, taking into account the device input gate-source capacitance and parasitic series gate inductance. The results of nonlinear circuit simulations demonstrated a linear (at 1-dB gain compression point) output power of 37.4 dBm at an operating frequency of 6 GHz with a *PAE* improved by 7% by using a source-harmonic tuning. It should be noted that changes in the source second-harmonic impedance can vary *PAE* significantly, from 30% to 80% for a 5-GHz 28.4-dBm MESFET PA.[76]

A systematic procedure of multiharmonic load-pull simulation using the harmonic-balance method includes two basic steps: finding the optimal loading at each harmonic component and checking the power levels of higher harmonics.[77] An impedance-sampling method can be used to find the optimal harmonic loading. Generally, only one impedance component $Z_i(k\omega_0)$ at *k*th harmonic and *i*th external port is sampled at the defined impedance plane, while the others are kept constant at each step. For a specific case of the MESFET PA with input and output tuners, as shown in Fig. 10.64A, the design procedure steps are as follows:

1. Start load-pull simulation by sampling the impedance at the fundamental frequency $Z_i(\omega_0)$ and find the optimal load $Z_{i_{opt}}(w_0)$.
2. Fix $Z_i(\omega_0)$ at $Z_{i_{opt}}(w_0)$ and check the output spectrum to observe the effects of higher harmonic loads on the PA response.

3. Perform load-pull simulation by sampling the *k*th harmonic impedance $Z_i(k\omega_0)$ and find the optimal load $Z_{i_{opt}}(kw_0)$.
4. Fix $Z_i(k\omega_0)$ at $Z_{i_{opt}}(kw_0)$ and check the output spectrum to observe the effects of higher harmonic loads on the PA response.

It should be noted that, if checking the output power spectrum shows that the power at higher harmonics is sufficiently small, then the design procedure is stopped.

For a 900-MHz PA using a GaAs MESFET device with a gate periphery of 0.7 μm × 600 μm biased at 3 V with a quiescent current of approximately 10% of total DC drain current, it was shown that, for a sinusoidal driving signal, the best PAEs are achieved at load phase angles close to ±180 degrees for a second harmonic, corresponding to a short-circuit condition, and at load phase angles close to zero at the third harmonic, corresponding to an open-circuit condition that approximates a Class-F mode.[78] The simulation results demonstrated a strong dependence of efficiency with the second-harmonic termination, while the effect of the third harmonic is much weaker. The effect of the fourth- and fifth-harmonic terminations, stronger in the former case and weaker in the latter case, results in an efficiency variation of approximately 2.5%. It is necessary to minimize the resistive losses in harmonic terminations, intended to be purely reactive, that could be changed from reactive to resistive if the second- and higher-order harmonic terminations are excessively lossy.

The properly phased input and output voltage-harmonic components using a multiharmonic terminating scheme shown in Fig. 10.64B can be achieved by choosing the optimum impedances for each harmonic component.[79, 80] For example, in a Class-F mode these output impedances can be purely resistive (low at even harmonics and high at odd harmonics), since the drain (collector) current second harmonic is always in-phase and the drain (collector) current third harmonic is always out-of-phase with respect to the fundamental component for conduction angles ranging from 180 degrees (Class-B biasing) to 0 degree (Class-C biasing). Under slightly overdriven device operation when the drain current waveform represents a truncated half-sinusoid, the third harmonic becomes out-of-phase also for Class-AB biasing with conduction angles >180 degrees. The same result can be obtained by using a driver stage in a Class-F mode. However, in an inverse Class-F mode, the drain current second harmonic must be 180 degrees out-of-phase with respect to the fundamental-frequency component which can be realized by reactive input termination of the second harmonic providing the required phase shift. Fortunately, the main contribution to the harmonic-generating mechanism at the device input is given by its nonlinear input gate-source capacitance acting in a required reverse direction by generating the second- and third-harmonic components with proper phasing. As a result, optimum half-sinusoidal drain-voltage waveform corresponding to an inverse Class-F mode can be achieved by optimizing the input and output impedances at the second and third harmonics simultaneously.

Generally, it is very difficult to provide accurate source- and load-pull measurements at high microwave and millimeter-wave frequencies where de-embedding of waveguide transitions and parasitic discontinuities lead to significant measurement errors. It can be done accurately enough by using on-wafer measurements for an active device with limited output power capability at the fundamental frequency. At the same time, the *S*-parameters of tuner structures can be accurately predicted using both linear and electromagnetic circuit simulators. The determination of the optimum impedances at the

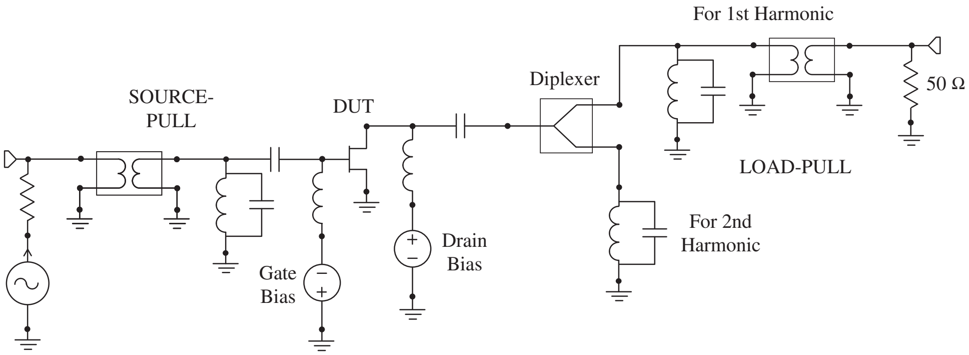


FIG. 10.65

Schematic of source- and load-pull simulation setup.

second harmonic can be provided by computer source- and load-pull analysis. In this case, it is no problem to isolate the fundamental and second-harmonic paths to determine their optimum impedances. Fig. 10.65 shows the schematic of a source- and load-pull simulation setup for a *V*-band InP HEMT PA, where the ideal output duplexer separates the fundamental from the second-harmonic component.[81] By changing the ideal transformer turns ratio and the reactive component values, the output power, PAE, power gain, and stability circle contours can be simulated for various bias voltages and operating frequencies around center-band frequency of 60 GHz. The optimum second-harmonic termination resulted in a theoretical 6% improvement in *PAE* at 3-dB gain-compression point under Class-AB bias. However, in practice, a smaller improvement is expected because low-loss reactive harmonic loading at 120 GHz is difficult to physically implement without degrading the fundamental load match at 60 GHz.

By considering reactive parasitic elements in the transistor, an optimum load condition in the GHz-band can be predicted with the MHz-band evaluation method when, for example, the active load-pull system is easily constructed by using a commercial arbitrary waveform generator and oscilloscope.[82] Fig. 10.66A shows the basic load configuration of a high-efficiency PA where the transistor is modeled by the nonlinear current source, intrinsic nonlinear capacitances and external package parasitic elements. In this case, the reactive elements can be ignored in the MHz-band, and the optimum load impedance for the transistor without parasitic elements can be estimated in the MHz-band by using a simple active load-pull system with harmonics tuning shown in Fig. 10.66B and then translated to the GHz-band by considering the measured reactive parasitics. In the MHz-band, the time-domain voltage and current waveforms in the transistor can be directly measured when a voltage signal is applied from the output side by properly adjusting of the amplitudes and phases of the fundamental and harmonic signals to provide maximum efficiency, resulting in the corresponding impedance conditions for the fundamental and harmonics calculated based on the Fourier-transform technique. The intrinsic nonlinear capacitive elements can be identified based on the frequency- and bias-dependent *S*-parameter measurements.[83]

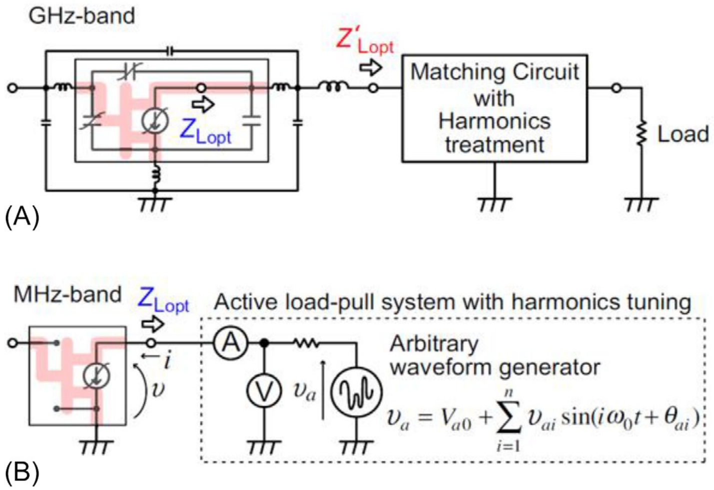

GHz-band
Z'_{Lopt}
Z_{Lopt}
Matching Circuit with Harmonics treatment
Load
(A)
MHz-band
Z_{Lopt}
Active load-pull system with harmonics tuning
i
v
A
V
v_a
Arbitrary waveform generator
$v_a = V_{a0} + \sum_{i=1}^{n} v_{ai} \sin(i\omega_0 t + \theta_{ai})$
(B)

FIG. 10.66

Circuit configuration of high-efficiency PA and active load-pull system with harmonics tuning.[82]

The measured drain voltage and current waveforms, together with the load impedance conditions up to fifth harmonic, are shown in Fig. 10.67, where the fundamental frequency was set to 20 MHz.[82] Here, a Class-F operation with a pure resistive load at the fundamental, low impedance at the second and fourth harmonics, and high impedance at the third and fifth harmonics is shown in Fig. 10.67A. When a capacitive reactance is added to the resistive load at the fundamental, the adjusted harmonic impedance conditions (inductive for the second, third, and fifth harmonics and capacitive for the fourth harmonic) are shown in Fig. 10.67B. Similarly, when an inductive reactance is added to the resistive load, the adjusted harmonic impedance conditions (capacitive for the second, third, and fifth harmonics and inductive for the fourth harmonic) are shown in Fig. 10.67C. The maximum drain efficiency in all three cases is achieved with minimal overlapping of the voltage and current waveforms that corresponds to minimum power losses. In these measurements a minimum voltage of about 0.3 V was observed due to on-resistance and series parasitic resistance of the HEMT device.

Fig. 10.68A shows the fabricated PA using a 0.25-μm pHEMT device having a gate width of $2 \times 100\,\mu$m with the quarterwave open-circuit harmonic stubs making the short-circuited impedance conditions for each harmonic on the microstrip line when every required harmonic reactance is provided by shifting the position of the corresponding stub and the impedance matching at the fundamental is realized at the end of the microstrip line after the harmonic-tuning circuit.[82] The drain voltage and current waveforms with the harmonic impedance conditions measured at 1.88 GHz using a 20-MHz active load-pull system are shown in Fig. 10.68B, where an efficiency reduction of 6% was observed,

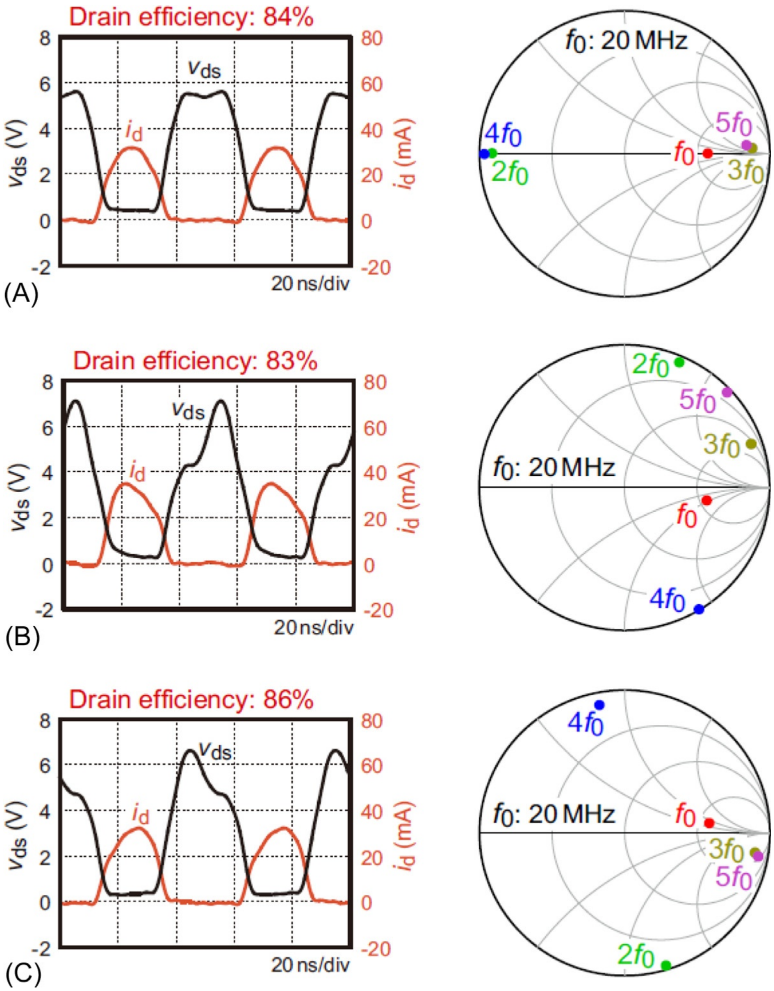


FIG. 10.67

Measured drain voltage and current waveforms and load impedance conditions: (A) Class-F operation, (B) capacitive element added at fundamental, and (C) inductive element added at fundamental.[82]

as compared to the drain efficiency given in Fig. 10.67C. It should be mentioned that, if impact of the second harmonic at the input due to the nonlinear contribution of the device gate-source capacitance can be enough sufficient when the PA is designed to operate in a Class-F mode, then the performance in an inverse Class-F (Class-F^{-1}) mode is practically immune to any change in the second-harmonic impedance at the input of the transistor.[84]

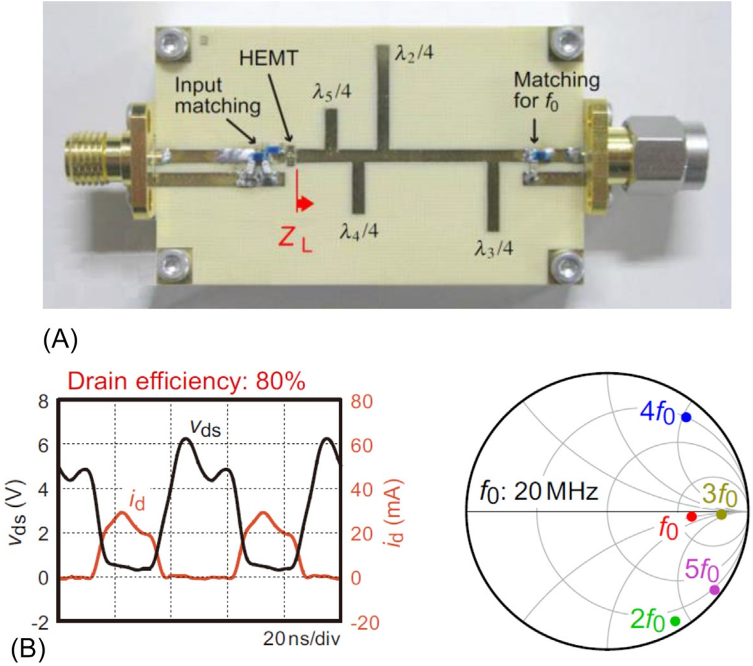


FIG. 10.68

(A) Fabricated HEMT PA and (B) Measured drain voltage and current waveforms and load impedances at 1.88 GHz.[82]

10.8 Outphasing PAs

The outphasing modulation technique was invented in the mid-1930s in order to improve both the efficiency and linearity of AM-broadcast transmitters.[85] Substantially later in 1970s, its application was extended up to microwave frequencies under the name LINC (*linear amplification using nonlinear components*).[86] An outphasing transmitter is operated as a linear PA system for amplitude-modulated signals having a linear transfer function over a wide range of the input signal levels by combining the outputs of two nonlinear PAs that are driven with signals of constant amplitude but different time-varying phases corresponding to the envelope of the input signal.

A simple outphasing PA system is shown in Fig. 10.69A.[87] The signal component separator (SCS) generates from the input amplitude-modulated signal two sinewave signals of constant envelopes with different phases $+\phi(t)$ and $-\phi(t)$. These two signals are then separately amplified by the identical nonlinear PAs and combined to produce the output amplitude-modulated signal. The peak output power is obtained with $\phi = 90$ degrees when currents from PAs with equal amplitudes $I_L = I_1 = I_2$ are added in phase, similar to a push–pull operation. Zero output power corresponds to the signal with $\phi = 0$ degrees when equal currents from PAs cancel each other, resulting in $I_L = 0$. Intermediate values of phase in between 0 degrees $< \phi < 90$ degrees produce intermediate values of the output voltage amplitude. As

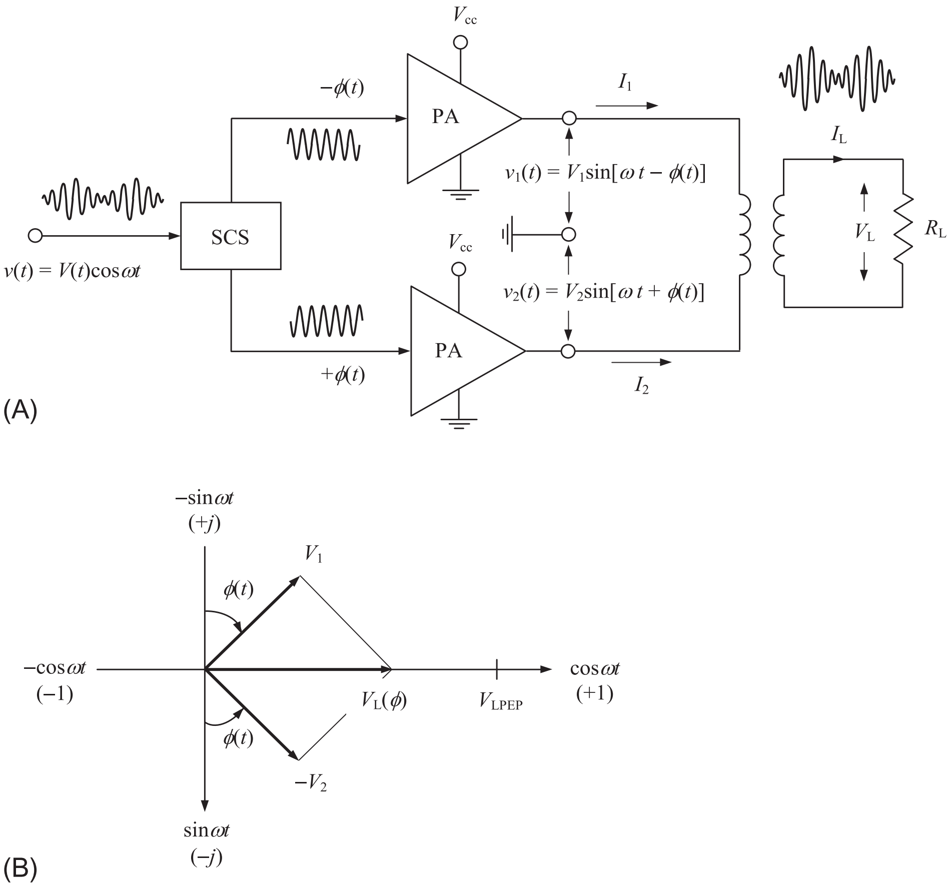

V_{cc}
$-\phi(t)$
PA
I_1
I_L
$v(t) = V(t)\cos\omega t$
SCS
$v_1(t) = V_1\sin[\omega t - \phi(t)]$
V_{cc}
V_L
R_L
$v_2(t) = V_2\sin[\omega t + \phi(t)]$
PA
$+\phi(t)$
I_2
(A)
$-\sin\omega t$
$(+j)$
V_1
$\phi(t)$
$-\cos\omega t$
(-1)
$V_L(\phi)$
V_{LPEP}
$\cos\omega t$
$(+1)$
$\phi(t)$
$-V_2$
$\sin\omega t$
$(-j)$
(B)

FIG. 10.69

Simple outphasing PA system.

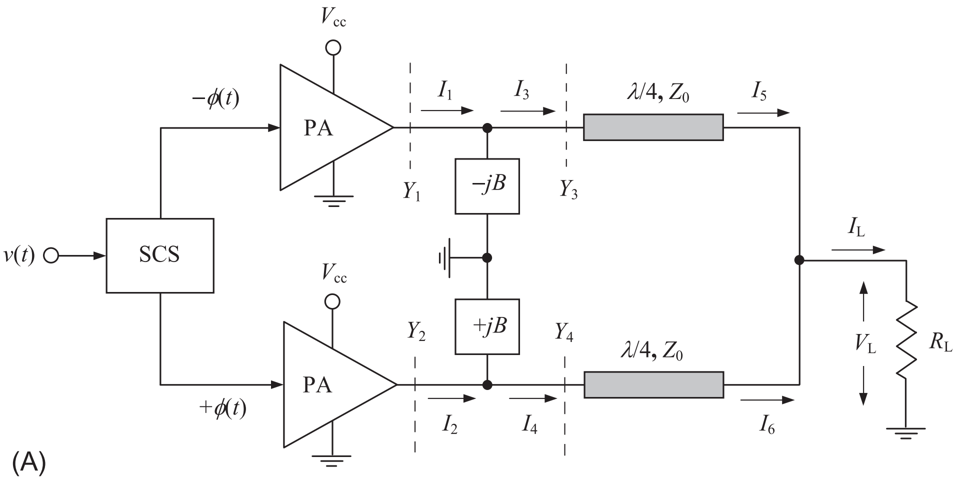
shown in Fig. 10.69B, the time-varying phase ϕ can be written using the vector sum of the output voltages V_1 and V_2 by

$$\phi = \sin^{-1}\left(\frac{V_L}{V_{L_{PEP}}}\right) \tag{10.213}$$

where $V_L = I_L R_L$ is the output voltage amplitude across the load resistance R_L and V_{LPEP} is the maximum output voltage amplitude at peak envelope power.

The instantaneous collector efficiency of a simple outphasing system with Class-B PAs can be calculated from

$$\eta = \frac{\pi}{4}\frac{V_L}{V_{L_{PEP}}} \tag{10.214}$$



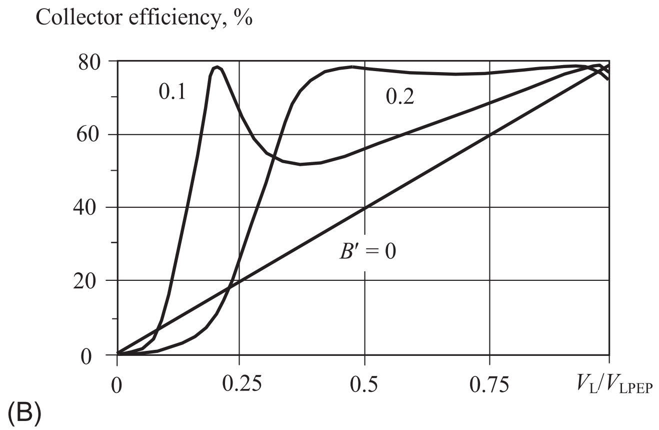


FIG. 10.70

Chireix outphasing PA system and instantaneous efficiencies.

having maximum value of 78.5% in saturation when $V_L = V_{L_{PEP}}$ with $\phi = 90$ degrees and zero value when $V_L = 0$ with $\phi = 0$ degree. Thus, the efficiency of a simple PA outphasing system is the same as that of an ideal Class-B PA, reducing linearly with the output voltage amplitude. In this case, to accurately perform the required signal component separation, it is necessary to use a digital signal processing (DSP) technique.[88]

The efficiency at lower output voltages can be significantly improved by using a lossless Chireix outphasing PA system shown in Fig. 10.70A, which includes additional series quarterwave transmission lines and shunt reactances. Phasor analysis of the load network for the time-varying phase ϕ with an impedance-transforming quarterwave transmission line results in

$$Y_3 = \frac{2R_\mathrm{L}}{Z_0^2}\frac{V_\mathrm{L}}{V_\mathrm{LPEP}}(\sin\phi + j\cos\phi) \tag{10.215}$$

$$Y_4 = \frac{2R_\mathrm{L}}{Z_0^2}\frac{V_\mathrm{L}}{V_\mathrm{LPEP}}(\sin\phi - j\cos\phi) \tag{10.216}$$

where Z_0 is the characteristic impedance of the transmission lines.[87] From Eqs. (10.215) and (10.216), it follows that the admittances Y_3 and Y_4 are purely resistive for $\phi = 90$ degrees only, corresponding to the case of in-phase output currents. However, for most values of phase ϕ, the PAs have highly reactive loads that become completely reactive when $\phi = 0$ degree with 180 degrees out-of-phase output currents. The effect of the reactive loads can be partially compensated by adding the corresponding shunt susceptances —B and $+B$, respectively. In this case, the reactive parts of the admittances $Y_1 = Y_3 - jB$ and $Y_2 = Y_4 + jB$ can be zeroed at one specific output voltage amplitude by setting

$$B = \frac{2R_\mathrm{L}}{Z_0^2}\frac{V_\mathrm{L}}{V_\mathrm{LPEP}}\sqrt{1 - \left(\frac{V_\mathrm{L}}{V_\mathrm{LPEP}}\right)^2} \tag{10.217}$$

which can be obtained by substituting Eq. (10.213) into Eqs. (10.215) and (10.216). As a result, for the case of a purely resistive load, the instantaneous collector efficiency of a Chireix outphasing system with ideal Class-B PAs can reach the maximum value of

$$\eta = \frac{\pi}{4} \tag{10.218}$$

The instantaneous efficiencies of the Chireix outphasing system for different values of the normalized shunt susceptance $B' = BZ_0^2/2R_\mathrm{L}$ are shown in Fig. 10.70B, from which it follows that the selection of a proper value of B increases efficiency at a specified medium level of the output voltage amplitude, however it is degraded at low and high amplitudes. Using a value $B' = 0.2$ can provide high efficiency over the upper 6 dB of the output voltage range. The case when $B' = 0$ corresponds to the collector efficiency variations of an ideal Class-B PA. An improvement in the average efficiency calculated over a wide range of output voltages for various amplitude-modulated signals of up to a factor of two over that of an ideal Class-B PA can be achieved by properly selecting the shunt susceptances in the outphasing PA system. The steep efficiency drop at low output power can be explained by the fact that the loading conditions of the active devices become almost entirely reactive that is very harmful for efficiency. On the whole, to design such an outphasing system, it is necessary to consider simultaneously such factors as a complexity of the SCS circuit and sensitivity of the PAs to the wide range of load impedances.

In a practical LINC transmitter, there are three main mechanisms that degrade the overall performance: power gain and phase imbalance between two RF amplifying paths and different nonlinear characteristics of both PAs.[89] For example, if the gain imbalance between paths is about 1%, the output rejection may reduce to 45 dB and even further to only 28 dB, depending on the relative level of the input modulating signal amplitude. On the other hand, a phase error between amplifying paths as low as 2 degrees diminishes the undesired response rejection to only 33 dB at best case. At the same time, the effect of the imbalance of the PA nonlinearities is less meaningful. In terms of the Chireix PA parameters, it is very important to minimize the combiner impedance mismatching, especially at microwave frequencies where the Chireix outphasing combiner should consist of two shunt stubs of equal and opposite reactances and two series quarterwave transmission lines.[90] To provide high amplitude and phase accuracy of the LINC system, a DSP-based architecture can be developed where the compensation of the amplitude and phase imbalances can be accomplished using calibration Schemes.[91] For a Chireix outphasing system with a transmission-line combiner, an average efficiency of 30% with an *ACLR* of −45 dBc was achieved for a single-carrier wideband code division multiple access (WCDMA) signal in a frequency range of 2.11–2.17 GHz, measured at a channel output power of 20 W.[92] Independent control of the branch PAs by two in-phase/quadrature modulators enables optimum outphasing and input power leveling that can result in significant improvements in power gain, efficiency, especially for low output power levels, and linearity.[93]

Further efficiency improvement can potentially be achieved by using high-efficiency PAs operating in different switching modes or their approximations. For example, a drain efficiency of an 800-MHz outphasing system based on the voltage-mode Class-D amplifiers implemented in a 0.18-µm SiGe BiCMOS process and transmission-line Chireix combiner was improved for a CDMA IS-95 signal with a $PAR = 5.5$ dB from 38.6% to 48% at an output power of 15.4 dBm.[94] Applying a single-carrier WCDMA signal, a drain efficiency of 51% with an output power of 21.6 dBm was measured for a 1.92-GHz outphasing system based on the voltage-mode Class-D amplifiers and integrated lumped Chireix combiner fully implemented in a 0.13-µm CMOS process.[95]

Using a push–pull configuration with a rat-race balun for each saturated Class-B PAs based on 0.25-µm pHEMT devices in an outphasing system with a Chireix microstrip combiner had contributed to a system efficiency of 42.2% with a channel power of 31.2 dBm (−7 dB backoff) for a single-carrier 2.14-GHz WCDMA signal, which is more than two times better than for the Wilkinson combiner system.[96] Note that the Chireix combiner when used with ideal sources leads to a linear LINC system. However, for 10-W GaN HEMT PAs operating in a Class-F mode, more than 4-dB expansion in gain and 14 degrees compression in phase are obtained in a Chireix outphasing system due to load-pulling effect.[97] In an outphasing system using an asymmetric Chireix transmission-line combiner with different electrical lengths and additional input phase adjustment where PAs are based on two 15-W LDMOSFET transistors operating in an inverse Class-F mode, a drain efficiency of 48% at 6-dB output power backoff was achieved at an operating frequency of 2.14 GHz.[98]

Fig. 10.71A shows the asymmetric architecture for the outphasing of two Class-E PAs, where the transmission lines TL_1 and TL_2 have electrical lengths of $\theta + \delta$ and θ - δ, respectively.[99, 100] In this case, the transmission lines TL_1 and TL_2 rotate the impedance loci on the Smith chart to center them on the line at 65 degrees, which corresponds to the maximum efficiency of both Class-E PAs when $\theta = 147.5$ degrees. As a result of centering the impedance loci, the amplitudes of the PA outputs ideally vary identically with difference in phase between the drive signals. The phases of the output signals are nearly the same over most of the amplitude range of $\Delta\phi$. The value of a differential line length δ can be chosen to alter the instantaneous efficiency characteristics to optimize the average efficiency for a given signal. The circuit schematic of a lumped MOSFET prototype of the Chireix outphasing system with asymmetric combiner operating at 1.82 MHz is shown in Fig. 10.71B. Here, two identical Class-E PAs using IRF510 MOSFETs and achieving a drain efficiency of 95% with an output power of 14 W each were implemented using lumped shunt capacitors and series lumped inductors. The asymmetric Chireix combiner represents a lumped low-pass T-network replacing the transmission lines TL_1

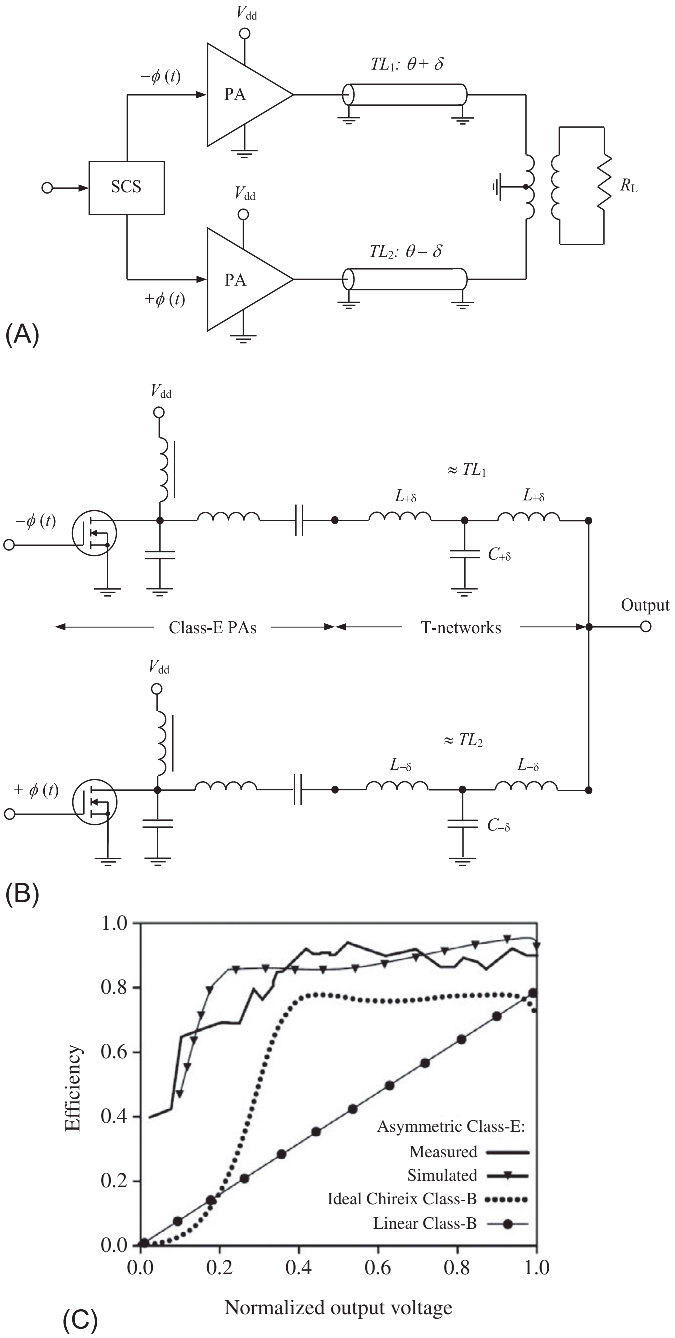

V_{dd}
$-\phi(t)$
PA
TL_1: $\theta+\delta$
SCS
V_{dd}
R_L
TL_2: $\theta-\delta$
PA
$+\phi(t)$
(A)
V_{dd}
$\approx TL_1$
$L_{+\delta}$
$L_{+\delta}$
$-\phi(t)$
$C_{+\delta}$
Output
Class-E PAs
T-networks
V_{dd}
$\approx TL_2$
$L_{-\delta}$
$L_{-\delta}$
$+\phi(t)$
$C_{-\delta}$
(B)
Efficiency
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.2
0.4
0.6
0.8
1.0
Normalized output voltage
Asymmetric Class-E:
Measured
Simulated
Ideal Chireix Class-B
Linear Class-B
(C)

FIG. 10.71

Asymmetric Chireix outphasing systems with Class-E PAs.

and TL_2, where the values of the LC elements can be determined analytically using a single-frequency equivalence between the lumped and distributed circuits.

The transmission matrix $[ABCD]_{\text{TL}}$ for a transmission line with electrical lengths of $\theta \pm \delta$ and the transmission matrix $[ABCD]_{\text{LC}}$ for a low-pass T-type lumped circuit, consisting of a shunt capacitor and two series inductors, are written as

$$[ABCD]_{\text{TL}} = \begin{bmatrix} \cos(\theta \pm \delta) & jZ_0 \sin(\theta \pm \delta) \\ j\dfrac{\sin(\theta \pm \delta)}{Z_0} & \cos(\theta \pm \delta) \end{bmatrix} \tag{10.219}$$

$$[ABCD]_{\text{LC}} = \begin{bmatrix} 1 & j\omega L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1-\omega^2 LC & j\omega L(2-\omega^2 LC) \\ j\omega C & 1-\omega^2 LC \end{bmatrix} \tag{10.220}$$

Equating the corresponding elements of both matrices yields the simple equations to determine the corresponding parameters of the lumped T-network through the transmission-line parameters as

$$C_{\pm\delta} = \frac{\sin(\theta \pm \delta)}{\omega Z_0} \tag{10.221}$$

$$L_{\pm\delta} = \frac{Z_0}{\omega} \tan \frac{\theta \pm \delta}{2} \tag{10.222}$$

where Z_0 is the transmission-line characteristic impedance.

Fig. 10.71C shows the simulated and measured results of a Class-E outphasing efficiency versus normalized output voltage for $\theta = 147.5$ degrees and $\delta = 17.4$ degrees, from which it follows that a drain efficiency of 85% or better for amplitude range of 15 dB from 0.8 W to full output power of 27.5 W in simulation and for amplitude range of 10 dB in measurement is maintained. In contrast, the efficiency for outphasing with ideal Class-B PAs is no better than 78.5%. The value of the difference δ in a transmission-line length (or its equivalent lumped T-network) does not appear to be critical and high efficiency is obtained for δ equals to 10 degrees, 18.4 degrees, 22 degrees, and 48 degrees.

The Class-E/F_2 topology with a second-harmonic tank connected in series to the device drain can be selected when it is necessary to provide an efficient operation over a very wide range of resistive loads. Fig. 10.72A shows the simplified circuit schematic of an outphasing amplifier with lumped Chireix combiner and L-type low-pass LC output impedance transformer using a pair of the Class-E/F_2 PAs based on GaN HEMT CGH35030F devices.[101] Based on these PAs, an outphasing scheme in the 700-MHz band was implemented, with an efficiency >60% up to an output power below 5% (−13 dB) of its peak value of 47 W, as shown in Fig. 10.72B. Besides, the frequency bandwidth of around 17 MHz was obtained where the efficiency remains >50% at 13-dB of power backoff. For a 10-MHz LTE signal with a peak *PAR* of 12.2 dB, an average drain efficiency of 46.6% and a *PAE* of 42.9% were measured at 700 MHz.

The schematic of a CMOS outphasing system with a transformer-based power combiner intended for broadband operation is shown n Fig. 10.73A.[102] Here, the series resonators of both Class-E PAs are shifted to the secondary side of the combiner, in series with the transformer leakage inductance defined as $L_{\text{leak}} = L_{\text{p}}(1-k^2)/k^2$, where k is the transformer voltage coupling coefficient. The leakage inductance is merged with the resonator inductance and inductance of the wideband two-section output matching circuit. To achieve a transformation ratio equal to 1, the primary inductance L_{p} and secondary inductance L_{s} must relate to each other as $L_{\text{p}}/L_{\text{s}} = 1/k$. The compensation susceptance of the transistor M_2 is

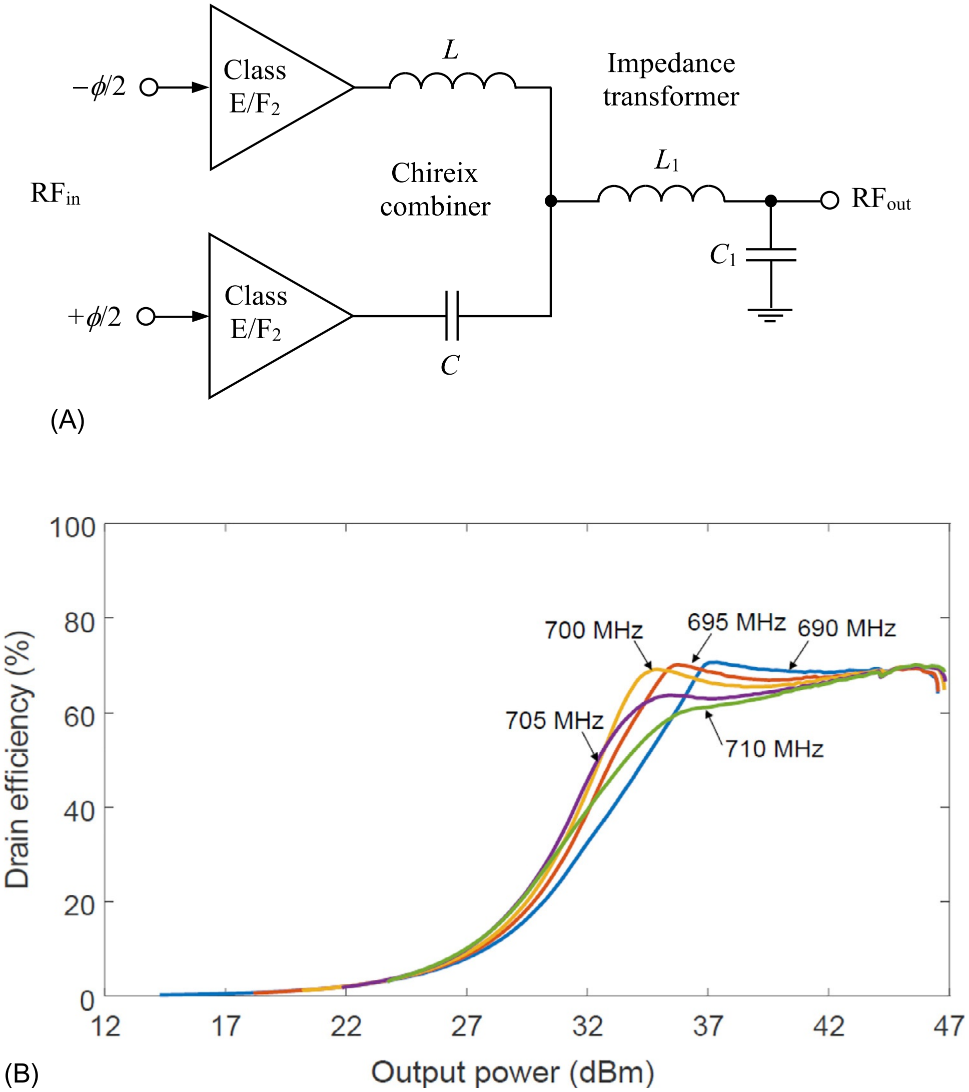


FIG. 10.72

Chireix outphasing systems with Class-E/F_2 PAs.[101]

created by changing the value of the DC-feed inductance to a larger value. The primary transformer winding serves as a DC-feed inductance for the transistor M_1 and a compensation susceptance. The resonator at the secondary side has a low loaded quality factor to enable a high-bandwidth operation. For a larger bandwidth, the inductance L_p must be small and coupling coefficient k must be close to 1. As a result, such a Chireix outphasing system with a combining circuit implemented on a three-layer PCB and two 65-nm CMOS Class-E PAs achieved a peak power over 30 dBm and a drain efficiency

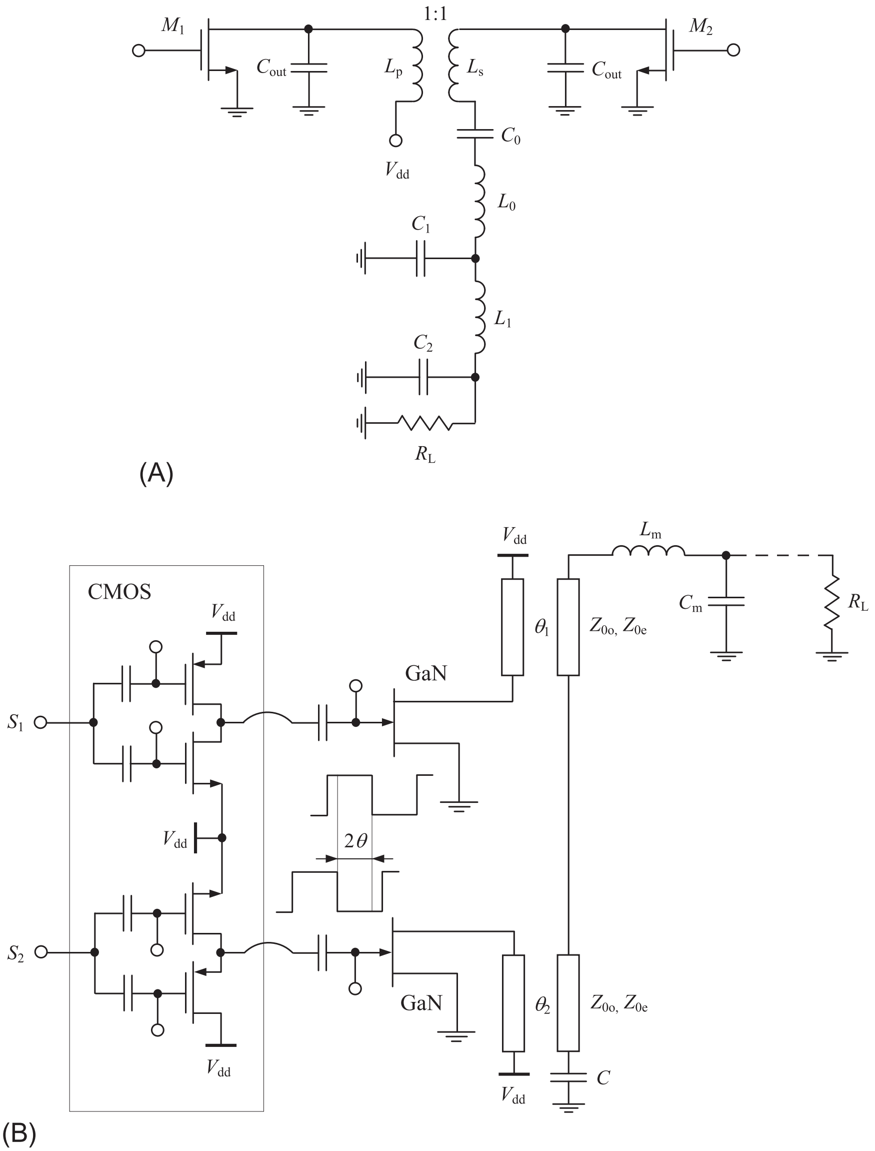

M_1
1:1
M_2
C_{out}
L_p
L_s
C_{out}
C_0
V_{dd}
L_0
C_1
L_1
C_2
R_L
(A)
V_{dd}
L_m
CMOS
V_{dd}
C_m
R_L
θ_1
Z_{0o}, Z_{0e}
GaN
S_1
V_{dd}
2θ
S_2
GaN
θ_2
Z_{0o}, Z_{0e}
C
V_{dd}
V_{dd}
(B)

FIG. 10.73

CMOS Chireix outphasing systems with Class-E PAs.

over 46.4% at 6-dB power backoff across the frequency range of 600–800 MHz at a DC-supply voltage of 3.6 V. By extending such a Chireix outphasing system with a combining circuit implemented on a PCB substrate and two 65-nm CMOS Class-E PAs to higher frequencies, a drain efficiency over 65% with an output power of 20.1 dBm at an operating frequency of 1.8 GHz using a DC-supply voltage of 1.25 V was achieved, with a drain efficiency of 37% at 12-dB power backoff.[103]

Because the lumped-element combining circuit is difficult to implement for high powers at microwave frequencies, coupled lines can be used to combine the outputs like in a Marchand balun. Fig. 10.73B shows the circuit schematic of a two-stage Chireix outphasing system where the push–pull drivers are fabricated in a standard 65-nm CMOS technology and the Class-E PAs are based on a 28-V GaN HEMT technology.[104] The CMOS drivers are ac-coupled to overcome the negative bias voltage required for GaN HEMT devices. The electrical lengths of the coupled lines with odd-mode characteristic impedance $Z_{0_\mathrm{o}} = 1/Y_{0_\mathrm{o}}$ and even-mode characteristic impedance $Z_{0_\mathrm{e}} = 1/Y_{0_\mathrm{e}}$ are unequal and the terminating capacitance is defined as

$$C = \frac{Y_{0_\mathrm{o}} + Y_{0_\mathrm{e}}}{2\omega} \cot\theta_2 \tag{10.223}$$

that tunes out the leakage inductance of the coupled-line transformer. A fourth-order Butterworth matching filter transforms the 50-Ω antenna impedance to the required Class-E load and sets the bandwidth property. As a result, a drain efficiency of 65.1% and a total system efficiency of 51.6% with an output power of 19 W were measured for a single-carrier WCDMA signal with a *PAR* of 7.5 dB at 1.95 GHz. Besides, a peak drain efficiency over 60% can be achieved in a frequency range of 1800–2050 MHz at 6-dB power backoff.

In a package-integrated outphasing PA system based on two Class-E GaN HEMT PAs and a Chireix combiner with two bondwire-based lumped transformers including compensating elements, an output power of 70.6 W with a peak drain efficiency of 73% at an operating frequency of 2.3 GHz was achieved at a DC-supply voltage of 28 V.[105] After applying a WCDMA signal with a *PAR* of 9.6 dB, an average drain efficiency of 53.5% and a total efficiency of 43.5% were measured with $ACLR_1$ of −49 dBc and $ACLR_2$ of −56 dBc after memoryless digital predistortion. At the same time, a drain efficiency over 50% was obtained across the frequency ranges exceeding 260, 160, and 80 MHz at 6-, 8-, and 10-dB power backoff, respectively.

The basic advantage of a Chireix combining technique is the fact that the combiner is ideally lossless, and that the real components of the effective load admittances seen by the individual PAs vary with outphasing so as to minimize PA losses when output power reduces. However, the reactive portions of the effective load admittances are only zero for at most two outphasing angles and become large outside of a limited power range. This limits efficiency due both to loss associated with added reactive currents and to degradation of the PA performance with reactive loading. In this case, multistage technique applied to a conventional Chireix outphasing system can overcome the loss and reactive loading problems, providing an ideally lossless power combining with nearly resistive loading of the individual PAs over a very wide output power range when high average efficiencies are achieved even for large peak-to-average power ratios.[106]

Fig. 10.74A shows the simplified four-stage outphasing architecture, where the PAs are modeled as ideal voltage sources. The lossless power combiner has four input ports and one output port connecting to the load, and it comprises reactive elements having specified reactances at the operating frequency. The system behavior can be described based on the relationships between the source voltages and input currents of the network of Fig. 10.74A according to

$$\begin{bmatrix} I_\mathrm{A} \\ I_\mathrm{B} \\ I_\mathrm{C} \\ I_\mathrm{D} \end{bmatrix} = \frac{1}{X_1} \begin{bmatrix} \gamma + j(1-\beta) & -\gamma + j\beta & \gamma & -\gamma \\ -\gamma + j\beta & \gamma - j(\beta+1) & -\gamma & \gamma \\ \gamma & -\gamma & \gamma + j(\beta+1) & -\gamma - j\beta \\ -\gamma & \gamma & -\gamma - j\beta & \gamma + j(\beta-1) \end{bmatrix} \begin{bmatrix} V_\mathrm{A} \\ V_\mathrm{B} \\ V_\mathrm{C} \\ V_\mathrm{D} \end{bmatrix} \tag{10.224}$$

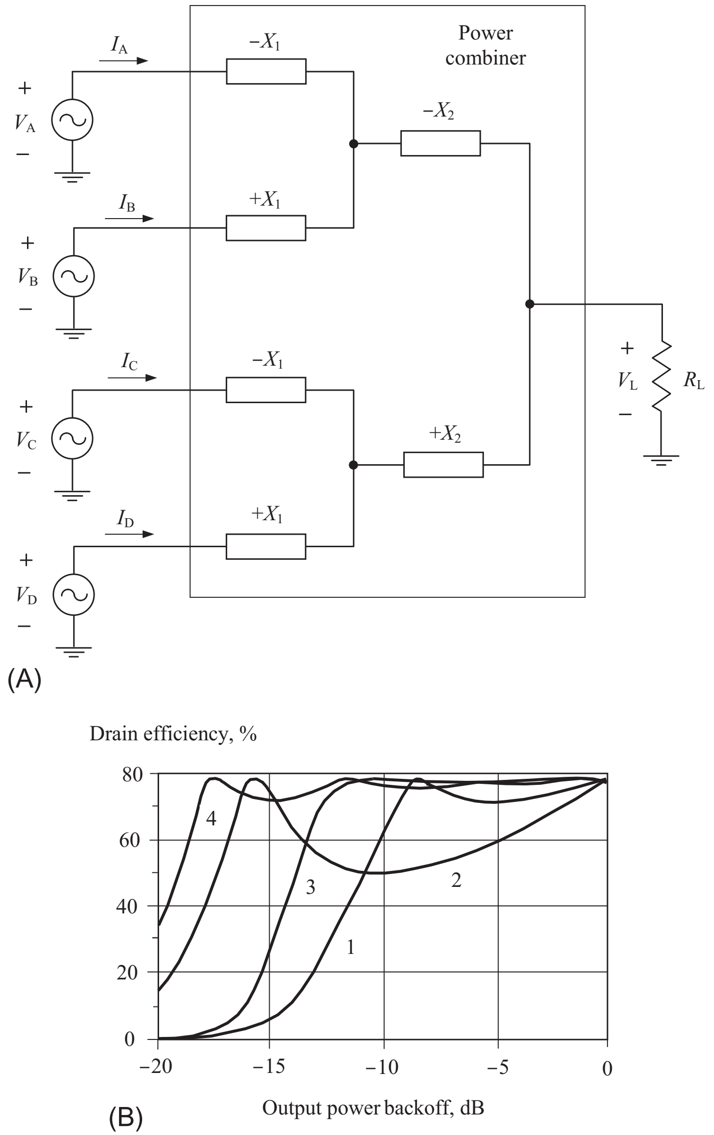

Power combiner
I_A
I_B
I_C
I_D
V_A
V_B
V_C
V_D
$-X_1$
$+X_1$
$-X_1$
$+X_1$
$-X_2$
$+X_2$
V_L
R_L
(A)
Drain efficiency, %
80
60
40
20
0
−20
−15
−10
−5
0
4
3
2
1
Output power backoff, dB
(B)

FIG. 10.74

Four-stage outphasing architecture and instantaneous efficiencies.

where $\gamma = R_L/X_1$, $\beta = X_2/X_1$, and voltage amplitudes are equal having different control angles used for outphasing. In this case, $+X_1$ and $+X_2$ represent inductive reactances due to inductances and $-X_1$ and $-X_2$ represent capacitive reactances due to capacitances. The effective admittance at a combiner input port is the complex ratio of current to voltage at the port with all sources active. The effective admittances represent the admittances seen by the sources when they are operating under outphasing control. A key advantage of this outphasing system is that susceptive portion of admittance loading the PAs is substantially smaller than with a conventional Chireix combining.

The drain efficiency of a multistage outphasing system using ideal saturated Class-B PAs can be obtained by

$$\eta = \frac{\pi}{4} \frac{\sum_{j=1}^{N} \mathrm{Re}\left(Y_{\mathrm{eff},j}\right)}{\sum_{j=1}^{N} \left|Y_{\mathrm{eff},j}\right|} \tag{10.225}$$

where $Y_{\mathrm{eff},j}$ is the effective admittance at a corresponding combiner input port seen by the jth source and N is the number of ports. For example, for the output probability density function (PDF) representing a WLAN signal with a *PAR* of 9.01 dB, the average drain efficiency remains almost constant for much larger range of backoff output powers for a four-stage outphasing architecture (curves 3 and 4) compared with a conventional Chireix outphasing architecture (curves 1 and 2), as shown in Fig. 10.74B, with average drain efficiencies of 38% and 46.1% corresponding to curves 1 and 2 and average drain efficiencies of 56.9% and 69% corresponding to curves 3 and 4, respectively.[106]

Fig. 10.75A shows the implementation of a Chireix outphasing system, where each of two outphased sources is constructed of a pair of the PAs designed to operate in a Class-E/F$_{\mathrm{odd}}$ mode at 27.12 MHz with output powers up to 750 W using ARF521 power MOSFETs. The two pairs of PAs are outphased using a Chireix combiner having $X_c = 13.6\,\Omega$ and supply a load resistance $R_L = 13\,\Omega$. For the four-stage outphasing system shown in Fig. 10.73A, the power combiner is used with a load resistance of 50 Ω and reactance values $X_1 = 35\,\Omega$ and $X_2 = 48.78\,\Omega$. The drain efficiency versus output power for both the four-stage combining system and conventional Chireix system is shown in Fig. 10.75B, where the four-stage outphasing architecture (curve 2) demonstrates superior performance at low power levels compared with a conventional Chireix system (curve 1), with more than 12% higher efficiency at 300-W output at 10-dB power backoff and more than 20% higher efficiency at 12.5-dB power backoff. The difference in efficiency arises both due to the higher reactive currents in the conventional Chireix architecture and because the greater reactive loading on the Chireix PAs at low power levels causes them to lose zero-voltage switching, resulting in a substantial capacitive discharge loss. At the same time, the four-stage outphasing system is advantageous in that it maintains desirable switching conditions down to far lower power levels than is possible in a conventional Chireix system and is effective in controlling the system output power.[107]

In a practical implementation, a four-stage outphasing system with a lumped-element combiner and four microstrip inverse Class-F PAs achieves a peak CW (continuous wave) drain efficiency of 68.9%, with efficiency >55% over a 5.5-dB power range at 2.14 GHz. It provides an average drain efficiency of 57% at an output power of 42 dBm with an *ACLR* of −36.6 dBc for a 5-MHz WCDMA signal with a *PAR* of 3.47 dB.[108] Here, the inductive branch impedances are synthesized from the series *LC* combinations in order to provide DC blocking, and capacitive branch impedances use both series and parallel capacitor combinations to facilitate tuning and so that all branches have the same physical length.

Fig. 10.76A shows the diagram of a four-way power combining transmission-line network, where Z_1 and Z_2 are the characteristic impedances of the branch transmission lines, respectively, and each transmission-line pair has a base length l_{base} with a specified offset (Δ_1 or Δ_2) from that base length.[109, 110] Although an arbitrary base length is possible, the base length is chosen here to be a quarter- or half-wavelength, as this allows for symmetric length increments $\pm\Delta_{1,2}$ and simplifies the combiner

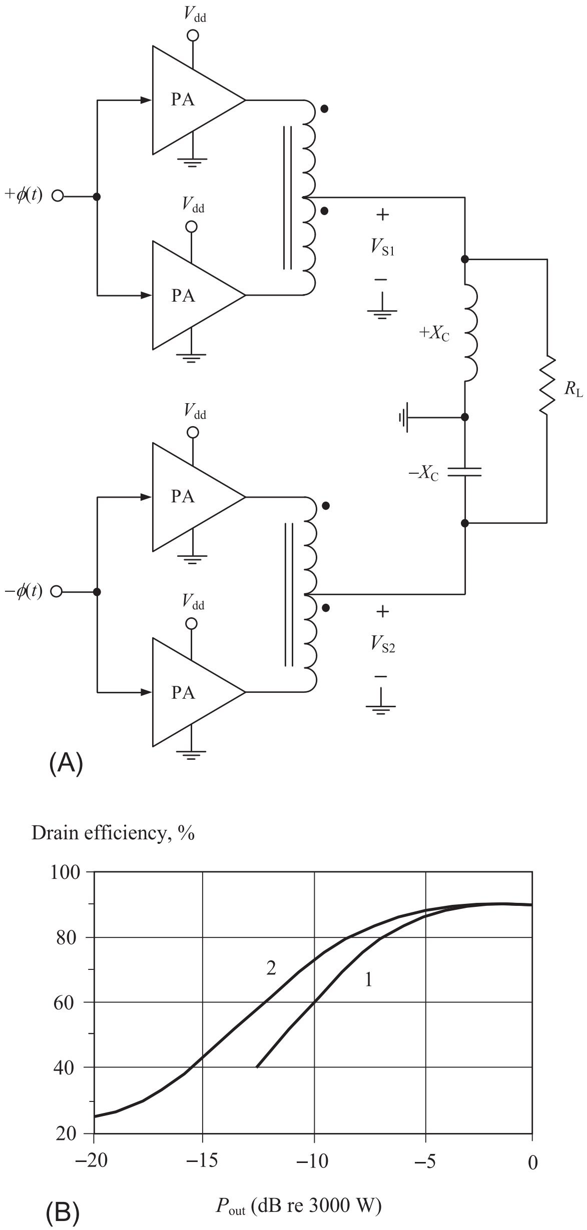
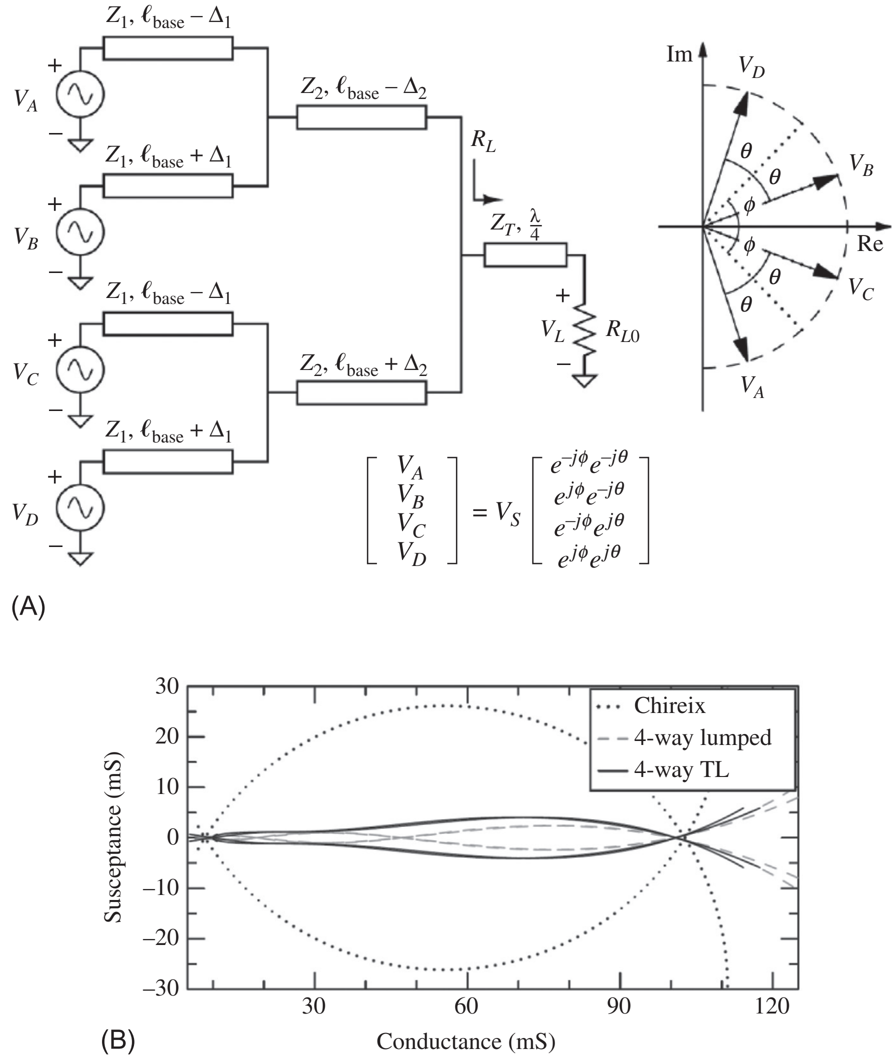

V_{dd}
PA
$+\phi(t)$
V_{dd}
PA
$+$
V_{S1}
$-$
$+X_C$
R_L
V_{dd}
$-X_C$
PA
$-\phi(t)$
V_{dd}
PA
$+$
V_{S2}
$-$
(A)
Drain efficiency, %
100
80
60
40
20
2
1
−20
−15
−10
−5
0
P_{out} (dB re 3000 W)
(B)

FIG. 10.75

Chireix outphasing PA system and instantaneous efficiencies.


$Z_1, \ell_{\text{base}} - \Delta_1$
$Z_1, \ell_{\text{base}} + \Delta_1$
$Z_1, \ell_{\text{base}} - \Delta_1$
$Z_1, \ell_{\text{base}} + \Delta_1$
$Z_2, \ell_{\text{base}} - \Delta_2$
$Z_2, \ell_{\text{base}} + \Delta_2$
V_A
V_B
V_C
V_D
R_L
$Z_T, \frac{\lambda}{4}$
V_L
R_{L0}
Im
Re
V_D
V_B
V_C
V_A
θ
ϕ
(A)
Chireix
4-way lumped
4-way TL
Susceptance (mS)
Conductance (mS)
30
20
10
0
−10
−20
−30
30
60
90
120
(B)

$$\begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = V_S \begin{bmatrix} e^{-j\phi}e^{-j\theta} \\ e^{j\phi}e^{-j\theta} \\ e^{-j\phi}e^{j\theta} \\ e^{j\phi}e^{j\theta} \end{bmatrix}$$

FIG. 10.76

Diagram of four-way power combining transmission-line network and loading conditions.[109]

analysis. The convenient approach for determining the loading characteristics is to describe the transmission-line combiner with a multiport admittance matrix relating the combiner input-port voltages to its respective input-port currents. In the case of the four-way combiner, this reduces to a four-port admittance matrix relating the four input-port voltages $V_A - V_D$ to the respective input-port currents, with the corresponding phase relationship among these four inputs. Control of the output power delivered by the combiner to the load can be achieved either by adjusting the signal amplitudes of the combiner inputs, by controlling the phase shift between the PAs, or by a combination of both of these methods. To minimize the reactive loading through selection of an optimal susceptance control behavior, the outphasing angles θ and ϕ are chosen such that the peak imaginary part of the load admittance is minimized over a specified output power operating range. A comparison of the theoretical effective loading conditions for Chireix combining, lumped-element four-way, and transmission-line four-way combining for the design example with a 10:1 operating power range and $Z_1 = Z_2 = 3R_L$, is shown Fig. 10.76B, when minimum sensitivity to loading reactance is provided by four-way combining. An experimental transmission-line four-way outphasing amplifier system operating at 2.14 GHz could demonstrate >60% drain efficiency for an output power range of 6.2 dB and 54.5% average modulated efficiency for a WCDMA signal with a *PAR* of 9.15 dB at an output power of 41.1 dBm.

A significant performance improvement can be achieved with post-optimization of the combiner element values, especially when it is necessary to increase the operating frequency bandwidth and efficiency. Fig. 10.77A shows the optimized circuit schematic of a transmission-line outphasing

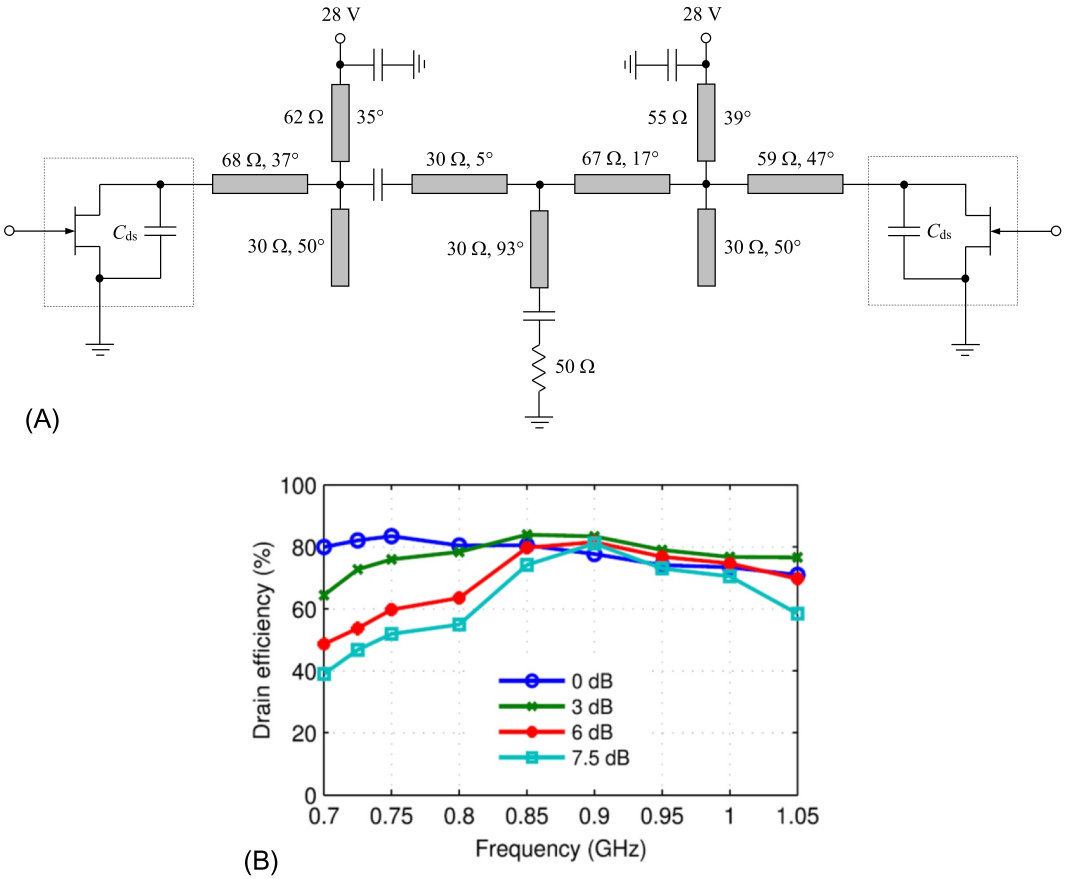

28 V
28 V
62 Ω
35°
55 Ω
39°
68 Ω, 37°
30 Ω, 5°
67 Ω, 17°
59 Ω, 47°
C_{ds}
C_{ds}
30 Ω, 50°
30 Ω, 93°
30 Ω, 50°
50 Ω
(A)
100
80
60
40
20
0
Drain efficiency (%)
0.7
0.75
0.8
0.85
0.9
0.95
1
1.05
Frequency (GHz)
0 dB
3 dB
6 dB
7.5 dB
(B)

FIG. 10.77

Broadband outphasing PA and drain efficiency.

combiner including second-harmonic control circuitry of the broadband high-efficiency outphasing PA using two GaN HEMT CGH60015DE devices with the drain-source capacitances of 1.3 pF, where the characteristic impedances and electrical lengths circuit parameters are given at 850 MHz.[111] As a result, a two-stage CMOS GaN outphasing PA could provide drain efficiencies over 60% at 6-dB power backoff and over 52% at 7.5-dB power backoff across the frequency band of 750–1050 MHz, as shown in Fig. 10.76B. In this case, the peak output power remains fairly flat versus frequency, where the variation across the entire frequency band within ±0.18 dB around 44 dBm is achieved.

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CHAPTER

High-efficiency Doherty power amplifiers

11

This chapter describes the historical aspect of the Doherty approach to the power amplifier (PA) design and modern trends in Doherty amplifier (DA) design techniques using multistage and asymmetric multiway architectures. To increase efficiency over the power-backoff range, the switchmode Class-E, conventional Class-F, or inverse Class-F operation mode by controlling the second and third harmonics can be used in the load network. The DA with a series connected load, inverted, balanced, push-pull, and dual Doherty architectures are also described and discussed. Finally, examples of the integrated and monolithic DAs for sub-6-GHz and millimeter-wave applications, digitally driven Doherty technique, and broadband capability of the conventional and inverted DAs are given.

11.1 Historic aspect, operational principle, and basic structures

A new PA technique for amplitude-modulated (AM) radio frequency (RF) signals was introduced by William H. Doherty in broadcasting in the mid-1930s as a more efficient alternative to both conventional amplitude-modulation techniques and Chireix outphasing.[1, 2] This new technique achieves plate circuit efficiencies of up to 60%–65% independent of modulation by means of a combined action of the variation of load distribution of the vacuum tubes, and the variation of the circuit impedance over the modulation cycle. When Doherty joined the radio development department of the Bell Telephone Laboratories in June 1929, he was engaged in the development of high-power radio transmitters for transoceanic radiotelephony and broadcasting. As a result, in 1936 he invented a means to greatly improve the efficiency of RF PAs, quickly termed the "Doherty amplifier." It was first used in a 50-kW transmitter with audio-frequency feedback providing a resulting distortion level from less than 1% at lower frequencies to a few percent at high audio frequencies. In this case, the PA was operated at an efficiency of 60% representing a reduction of nearly one-half in the all-day power consumption, as compared with the power required in the conventional type of linear PA operating at 33% efficiency.[3] The IRE Morris Liebmann Memorial Award was voted to Doherty in May 1937 for his improvement in the efficiency of RF PAs.[4] By 1940 the DAs had been incorporated in 35 commercial radio stations worldwide, at powers up to 50 kW.

In subsequent years, the DAs continued to be used in a number of medium- and high-power low-frequency (LF) and medium-frequency (MF) vacuum-tube AM transmitters.[5, 6] In August 1953, a 1-MW vacuum-tube transmitter in which the outputs of two 500-kW DAs were joined in a bridge-type combiner began regular operation in the long-wave band in Europe. The DAs had also been considered for use in solid-state MF and high-frequency (HF) systems, as well as in high-power ultrahigh-frequency (UHF) transmitters.[7–9] The practical implementation of a classic triode-based Doherty

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scheme was restricted by its substantial nonlinearity for both linear amplification of AM signals and grid-type signal modulation that required complicated envelope correction and feedback linearization circuits. At the same time, the DAs using tetrode transmitting tubes could improve their overall performance when the modulation was applied to the screen grids of both the carrier and peaking tubes, while the control grids of both tubes are fed by an essentially constant level of RF excitation.[10] This resulted in the peaking tube being modulated upward during positive half of the modulating cycle and the carrier tube being modulated downward during negative half of the modulating cycle.

The DA still remains in use in high-power AM transmitters, but for lower-power AM transmitters, the vacuum-tube amplifiers in general were eclipsed in the 1980s by solid-state PAs due to their advantages of smaller size and cost, lower operating voltages, higher reliability and greater physical ruggedness, insensitivity to mechanical shock and vibration, and possibility to use fully automated manufacturing processes and high level of integration. However, the transistor (bipolar or field-effect) as a three-electrode solid-state device is characterized by significant nonlinearity of its transfer characteristic and intrinsic capacitances that requires complicated linearization schemes, which was difficult to realize in analog domain at that time. Interest in the Doherty configuration has been later revived due to significant progress in radio communication systems based on complex digital modulation schemes such as WiMAX in OFDM (orthogonal frequency division multiplexing) systems, CDMA2000, WCDMA, or LTE (long-term evolution) enhancement to the UMTS wireless standard, where the sum of several constant-envelope signals creates an aggregate AM signal with high peak-to-average power ratio (*PAR*) and digital linearization techniques can be applied to reduce the DA distortion. DAs of different architectures have found widespread application in cellular base station transmitters operating at GHz frequencies. Recent developments of the Doherty concept make it one of the most attractive candidates for realizing energy-efficient wireless systems into the future.[11, 12]

11.1.1 Basic structures

Generally a DA system combines the outputs of two (or more) linear RF PAs through an impedance-inverting network composed of the lumped elements or represented by a quarterwave transmission line. The two fundamental forms of the DA are shown in Fig. 11.1, with a shunt connected load in Fig. 11.1A and with a series connected load in Fig. 11.1B.[2] In the former case, the load impedance used is $R_L = R/2$, which is the same as would be used if the tubes were to be connected in parallel in the conventional type of PA, where R is the load impedance seen by each tube at maximum output power. In the latter case, as long as the right-hand or peaking tube does not conduct, the impedance-inverting network provides zero impedance being terminated as open circuit, and the left-hand or carrier tube operates into a load impedance $R_L = 2R$. However, when the peaking tube is permitted to conduct, each tube is operating into the impedance R at the peak of modulation and delivering twice the carrier power (or power of the transmitted unmodulated signal), so that the total instantaneous output is the required value of four times the carrier power. The shunt connection appears to be more advantageous for most practical applications because the load circuit is grounded, while the load is neither grounded nor balanced to ground in the series arrangement.

The ideal anode voltage and current behavior in the carrier and peaking tubes as the amplitude of the grid excitation is varied is shown in Fig. 11.1C. Here, for the classic DA with equal-power tubes, the transition voltage is half the peak-envelope point (PEP), and the total output power of the amplifier comes from the carrier tube for input amplitudes less or equal to the transition point. The region

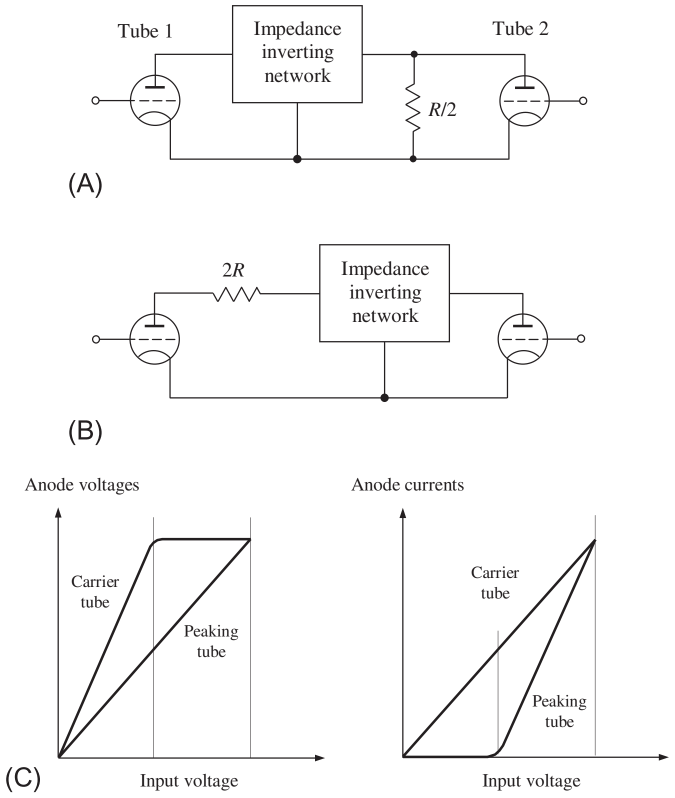

Tube 1
Impedance inverting network
Tube 2
R/2
(A)
2R
Impedance inverting network
(B)
Anode voltages
Carrier tube
Peaking tube
Input voltage
Anode currents
Carrier tube
Peaking tube
Input voltage
(C)

FIG. 11.1

Doherty fundamental load-network structures and their ideal voltage and current behavior.

between the transition-point and PEP values represents the load modulation region and the voltage on the carrier tube remains constant at the PEP level. At the same time, the voltage across the peaking tube continues to rise linearly, with its current commencing and rising twice as fast as the current in the carrier tube to reach its PEP value at maximum output power. Thus at low output power levels, the carrier amplifier operates linearly, reaching saturation that corresponds to maximum efficiency at some transition voltage below the system peak-output voltage. However, at higher output power levels, the carrier amplifier remains saturated, while the peaking amplifier operates linearly.

The corresponding shapes of the envelopes of anode currents and voltages during complete load variation are shown in Fig. 11.2.[2] In a simple case of a sinusoidal-modulating signal $v_{\mathrm{m}}(t) = V_{\mathrm{m}} \cos \Omega t$, where V_{m} is the modulating amplitude and Ω is the modulating frequency, the average output power P_{avr} for the modulated signal with a time-varying amplitude $V = V_0 + v_{\mathrm{m}}(t) = V_0(1 + m \cos \Omega t)$, where V_0 is the carrier amplitude and $m = V_{\mathrm{m}}/V_0$ is the modulation index, can be written as

$$P_{\mathrm{avr}} = \frac{V_0^2}{4\pi R_{\mathrm{L}}} \int_0^{2\pi} (1 + m \cos \Omega t)^2 d\Omega t = P_0 \left(1 + \frac{m^2}{2}\right), \tag{11.1}$$

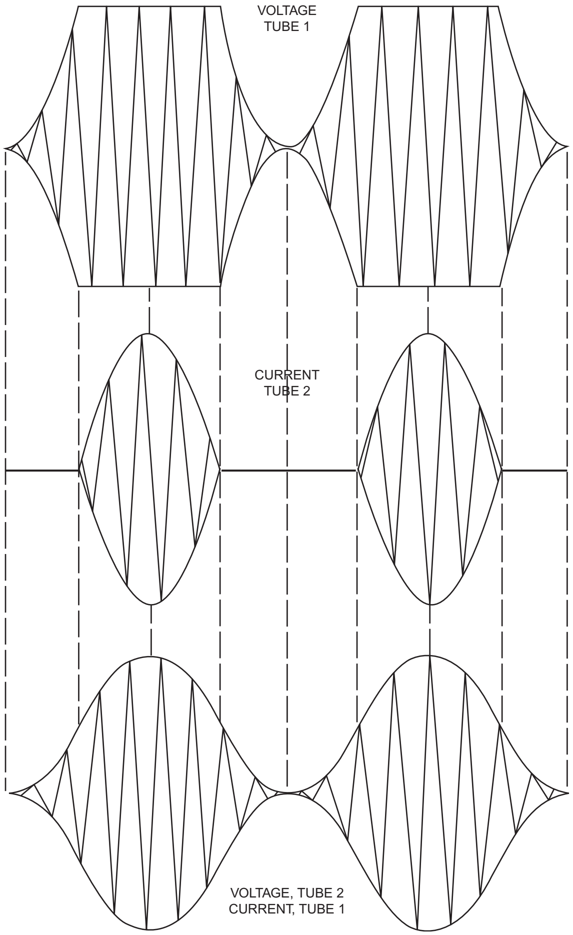


FIG. 11.2

Envelopes of anode currents and voltages during load variation.

where $P_0 = V_0^2/2R_L$ is the carrier power without modulation and m denotes the ratio of the variation of the modulated carrier amplitude to the unmodulated carrier amplitude. Because the average anode current in the carrier amplifier remains constant for all cycle of load variation but the duration of anode current in the peaking amplifier increases gradually with the amplitude, the average efficiency through the modulation cycle is then derived to be

$$\eta_{\text{avr}} = \eta_0 \frac{1 + \dfrac{m^2}{2}}{1 + \dfrac{2mq}{\pi}}, \tag{11.2}$$

where η_0 is the efficiency for zero modulation and q is the variable factor that ranges from approximately 0.7 for zero modulation to 0.93 for full modulation.[1]

Fig. 11.3A shows the DA schematic, where the anodes of the carrier and peaking tubes are connected together by a Π-type 90 degrees lumped network, which introduces a lagging phase shift of 90 degrees from the anode of the carrier tube to the anode of the peaking tube.[2, 10] Such a 90-degree lumped network is used due to its impedance-inverting characteristics. This means that if the terminating impedance at the point in the network where the peaking tube is located is reduced, then the impedance seen by the carrier tube will increase. In this case, as the load network of the high-power transmitter was approximately 35 Ω, the 90-degree lumped network was set to provide an impedance at the carrier tube of approximately 140 Ω. As a result, the series inductance and two shunt capacitors are each selected to provide a characteristic impedance equal to $\sqrt{35 \times 140} = 70\,\Omega$. To compensate for the output phase shift of 90 degrees, the input to the grid of the peaking tube is delayed by 90 degrees by similar means. If the input excitation is applied to the grid of the peaking tube, a Π-type lumped network consisting of the series capacitor and two shunt inductances is added between the grids of the carrier and peaking tubes to compensate for the output phase shift of 90 degrees, as shown in Fig. 11.3B.

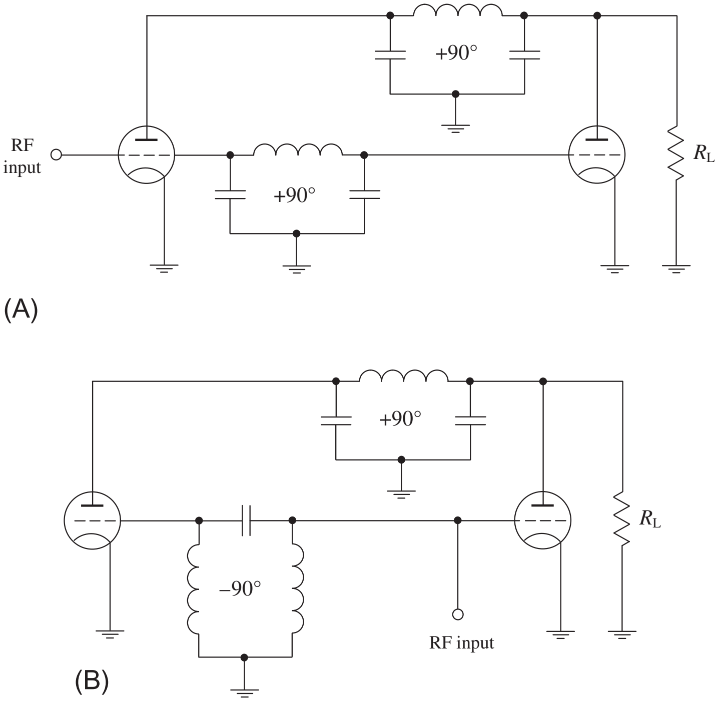


FIG. 11.3

Doherty amplifier basic schematics with lumped elements.

The simplified two-stage transmission-line Doherty power-amplifier architecture shown in Fig. 11.4A incorporates the carrier and peaking PAs, separated by a quarterwave transmission line in the carrier amplifier path.[13, 14] Such a section of line, known as a quarterwave transformer, has the ability to invert impedances according to

$$Z_0 = \sqrt{Z_{\text{in}} Z_{\text{out}}}, \tag{11.3}$$

where Z_0 is the characteristic impedance of the transmission line. This property can be seen more clearly by rewriting Eq. (11.3) as

$$Z_{\text{out}} = \frac{Z_0^2}{Z_{\text{in}}}, \tag{11.4}$$

from which it follows that the output impedance Z_{out} increases inversely with the input impedance Z_{in} for constant Z_0. The quarterwave transmission line at the input of the peaking amplifier is required to compensate for the 90 degrees phase shift caused by the quarterwave transmission line at the output of the carrier amplifier. The output quarterwave line with $Z_0 = \sqrt{25 \times 50} = 35\,\Omega$ is required to match the standard load impedance of $50\,\Omega$ when both carrier and peaking amplifiers deliver maximum power, each of which designed in a 50-Ω environment.

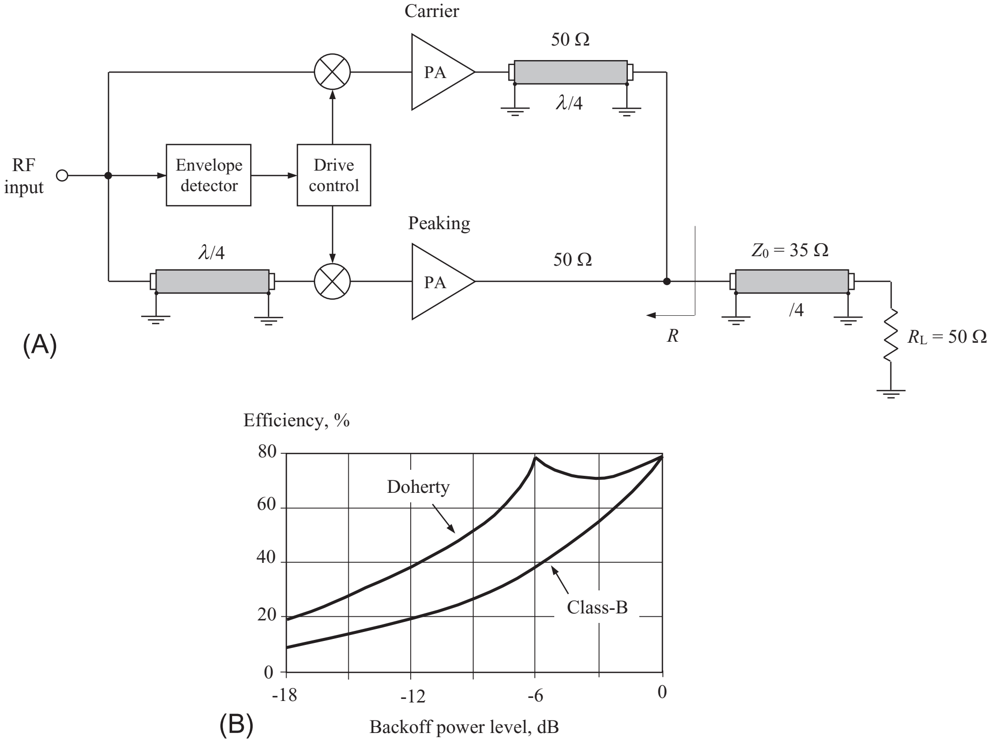

Carrier
PA
50 Ω
λ/4
RF
input
Envelope
detector
Drive
control
Peaking
λ/4
PA
50 Ω
$Z_0 = 35$ Ω
/4
R
$R_L = 50$ Ω
(A)
Efficiency, %
80
60
40
20
0
Doherty
Class-B
-18
-12
-6
0
Backoff power level, dB
(B)

FIG. 11.4

Doherty amplifier architecture with quarterwave lines and collector efficiencies.

An input drive controller is used to turn on the peaking amplifier (bias control) when the carrier amplifier starts to saturate because it is assumed that the carrier and peaking amplifiers are biased in Class-B for idealized system analysis. However, in practice, the carrier amplifier is biased in a Class-B mode, whereas the peaking amplifier is biased in a Class-C mode. At a backoff power level of $-6\,\text{dB}$, the saturated output power of the carrier amplifier is four times lower than the peak output power P_{PEP}. This indicates that its collector (or drain) efficiency, when operated in an ideal Class-B mode, is twice than that of a conventional Class-B PA, achieving a maximum efficiency of 78.5%, as shown in Fig. 11.4B.

11.1.2 Operation principle

The basic operation principle of a conventional Doherty power-amplifier architecture shown in Fig. 11.5A can be analyzed for low, medium, and peak output power regions separately.[14]

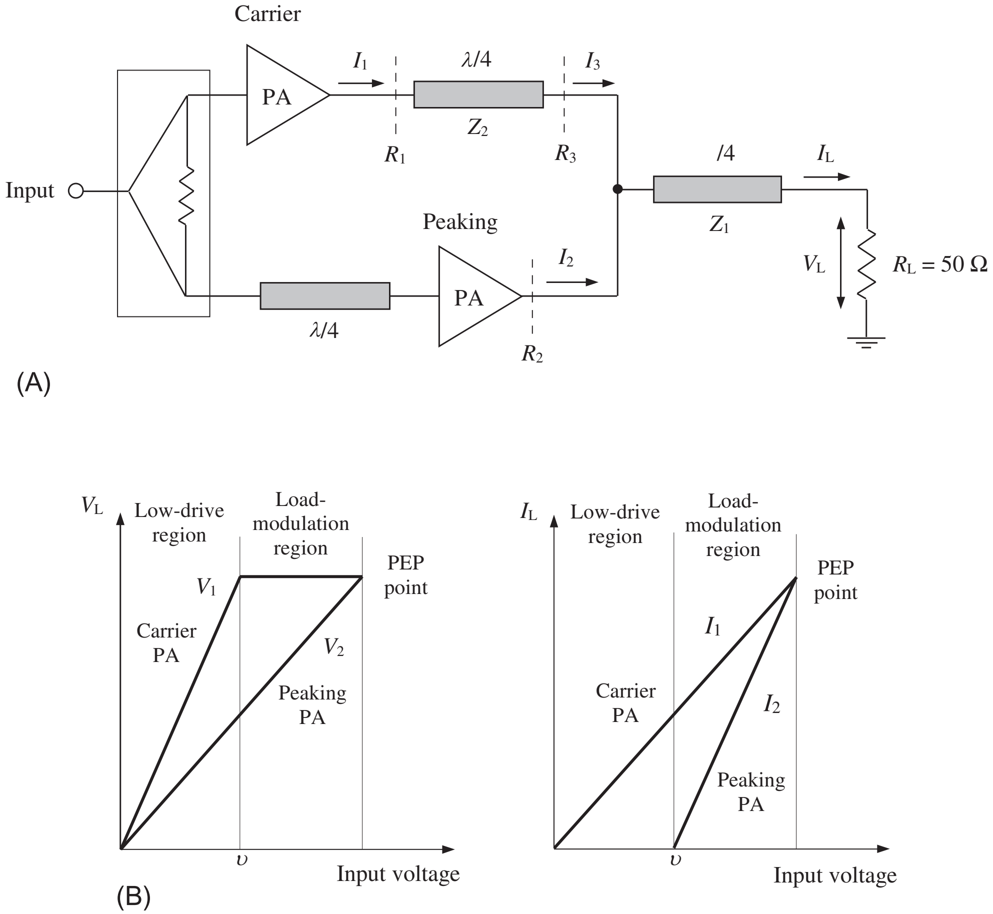

Carrier
PA
I_1
$\lambda/4$
I_3
Z_2
R_1
R_3
Input
/4
I_L
Z_1
Peaking
I_2
V_L
$R_L = 50\ \Omega$
PA
$\lambda/4$
R_2
(A)
V_L
Low-drive region
Load-modulation region
PEP point
V_1
Carrier PA
V_2
Peaking PA
υ
Input voltage
(B)
I_L
Low-drive region
Load-modulation region
PEP point
I_1
Carrier PA
I_2
Peaking PA
υ
Input voltage

FIG. 11.5

Basic two-stage Doherty amplifier architecture and its operation principle.

Fig. 11.5B shows the current and voltage behavior for ideal transistors and lossless matching circuits, where V_L is the load voltage and I_L is the load current. The condition of power conservation for a lossless output transmission line is written as

$$I_3 = I_1\sqrt{\frac{R_1}{R_3}}, \tag{11.5}$$

whereas the current division ratio β is defined by

$$\beta = \frac{I_3}{I_2 + I_3}. \tag{11.6}$$

As a result, the overall output power P_{out} is the sum of the carrier (main) amplifier output power $P_1 = \beta P_{out}$ and peaking (auxiliary) amplifier output power $P_2 = (1-\beta)P_{out}$. The impedance seen at the output of the transmission line in the carrier-amplifier path is

$$R_3 = \frac{I_2 + I_3}{I_3}\frac{Z_1^2}{R_L} = \frac{Z_1^2}{\beta R_L}, \tag{11.7}$$

and the impedance seen by the peaking PA is

$$R_2 = \frac{I_2 + I_3}{I_2}\frac{Z_1^2}{R_L} = \frac{Z_1^2}{(1-\beta)R_L}. \tag{11.8}$$

At peak output power P_{PEP} when both carrier and peaking amplifiers are saturated, the resultant collector efficiency is equal to the maximum achievable efficiency $\eta = \pi/4 \approx 78.5\%$ for an ideal Class-B operation. For the conventional Doherty PA architecture shown in Fig. 11.5A with the current (β) and power (α) division ratios $\beta = \alpha = 0.5$ when both carrier and peaking amplifiers produce equal output powers, their load impedances are equal to $R_1 = R_3 = R_2 = Z_2 = 2Z_1^2/R_L$. If the characteristic impedance of the output transmission line is chosen to be $Z_1 = 35\,\Omega$, then $R_1 = R_3 = R_2 = Z_2 = R_L = 50\,\Omega$.

At lower power levels in a low-drive region, the peaking amplifier is turned off because the instantaneous amplitude of the input signal is insufficient to overcome the negative Class-C bias and appears as an open circuit, whereas the carrier amplifier operates in the active region. In this case, the load impedance seen by the carrier amplifier is

$$R_1 = \left(\frac{Z_2}{Z_1}\right)^2 R_L, \tag{11.9}$$

resulting in $R_1 = 2R_L = 100\,\Omega$ when $Z_1 = 35\,\Omega$ and $Z_2 = R_L = 50\,\Omega$. Because the output power of the carrier amplifier in saturation is four times less than the peak output power $P_{PEP,}$ the collector efficiency of the carrier amplifier in an ideal Class-B mode will be twice than that of a conventional Class-B PA, achieving a maximum of 78.5% at backoff power level of −6 dB, as shown in Fig. 11.4B.

At medium power levels in a load-modulation region, the carrier amplifier is saturated, whereas the peaking amplifier is turned on and operates in the active region. Because the output voltage of the carrier amplifier $V_1 = I_1 R_1$ is constant under saturation conditions, from Eq. (11.5) it follows that the current I_3 is constant in the medium power region as well. The collector efficiency of the carrier amplifier remains at its maximum value, whereas the collector efficiency of the peaking amplifier increases up to its maximum value for Class-B operation at peak output power P_{PEP}. As a result, the DA architecture achieves maximum efficiency at both the transition −6 dB backoff point and the peak output power, and remains relatively high in between, as seen from Fig. 11.4B.

For high-quality signal transmission, it is important to obtain in vacuum-tube PAs a linear relation between grid exciting voltage and output anode voltage. The high impedance used for the carrier tube over the lower half of the modulation envelope causes the dynamic characteristic to be quite straight in this region. To obtain linearity from the point where curvature begins on the carrier tube, up to point representing the peaks of modulation, is a matter involving both the point, at which the peaking tube comes into operation, and the rate, at which its contribution increases with drive. For securing a satisfactory adjustment, there are two variables: the bias on the carrier tube and the amplitude of the excitation on this tube, whose careful selection may allow the PA to operate with low distortion.[2] Besides, in a low-power region, linearity of the DA is entirely determined by the carrier amplifier that should be highly linear even though the load impedance is high. In a high-power region, linearity can be improved by the harmonic cancellation from the carrier and peaking amplifiers using appropriate gate bias voltages. For example, in terms of gain characteristics of each amplifier using LDMOSFET devices, a late gain expansion of the Class-C biased peaking amplifier compensates the gain compression of the Class-AB biased carrier amplifier, and thus improving the third-order intermodulation (IM_3) level.[15]

In the mid-1990s, it was found that by using existing microwave design techniques and by implementing a few modifications, a microwave version of the DA could be realized.[16] In this case, an efficiency of 61% was achieved at 1-dB gain compression point and this level of efficiency was maintained through a 5.5-dB reduction in output power at an operating frequency of 1.37 GHz. A few years later, the possibility of achieving high-efficiency performance of a microwave monolithic DA was demonstrated in the *Ku*-band and *K*-band frequencies using pHEMT and InP DHBT technologies.[17, 18] The first fully integrated millimeter-wave DA monolithic microwave integrated circuit (MMIC) with a chip size of 2 mm^2 operating in a frequency range of 38–46 GHz was developed using a 0.15-μm GaAs HEMT process.[19] By using modern high-voltage HBT and GaN HEMT technologies, a high average efficiency of 55% and greater can be achieved for multicarrier WCDMA/LTE signals using a high-power two-way symmetrical DA.[20, 21]

11.1.3 Offset lines

At high frequencies, it is necessary to take into account that the transistor input impedance is varied with bias voltage and that the transistor output reactance should be compensated to provide the required open-circuit condition by using so-called offset lines with optimized electrical lengths.[15, 22] Fig. 11.6 shows the basic schematic diagram of a fully matched microwave DA with offset lines in the output circuit and phase-compensating circuits in the input circuit required to reduce amplitude modulation/phase modulation (AM/PM) variations because the output power level can change significantly with phase variations between the carrier and peaking paths.[22, 23] At high frequencies, it is enough to use an input phase-compensating transmission line (offset line) at the input of the peaking amplifier. Because of different biasing of the carrier (Class-AB) and peaking (Class-C) amplifiers, an offset line at the input of the peaking amplifier can be used to optimize linearity and efficiency for multicarrier applications.[24] To closer approximate ideal DA performance, an adaptive power-dependent input power distribution between the carrier and peaking amplifiers can be provided so as to deliver more power to the carrier amplifier in the low-power region and to the peaking amplifier in the high-power region,

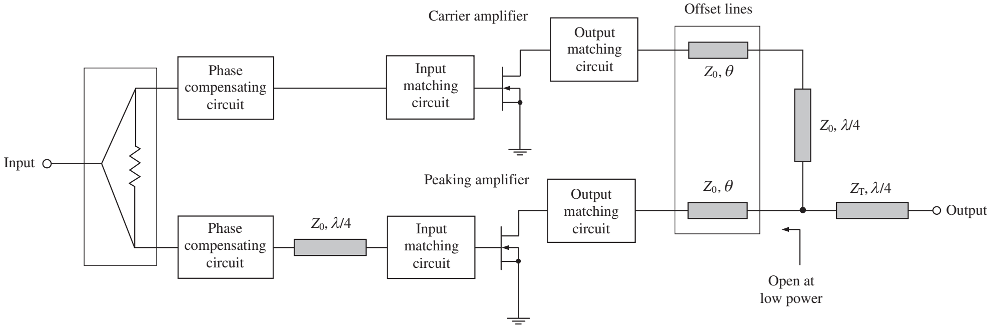


FIG. 11.6

Block diagram of microstrip LDMOSFET Doherty amplifier.

which can result in a linearity improvement of 5–7 dB over a wide range of output powers and an increased efficiency up to 5% for WCDMA signals at 2.4 GHz.[25]

The additional offset lines with the characteristic impedance of 50 Ω and fixed electrical lengths θ_c and θ_p are connected after the matching circuits of the carrier and peaking amplifiers, as shown in Fig. 11.7A. In a low-power region, the phase adjustments of the offset lines cause the peaking amplifier to be open-circuited and the load impedance seen by the carrier amplifier is doubled to 100 Ω due to an impedance-transforming property of a 50-Ω quarterwave transmission line, assuming that the matching circuit in conjunction with the offset line provides the required impedance transformation to the optimum high impedance Z_{opt} seen by the device output at the 6-dB power backoff, as shown in Fig. 11.7B. At the same time, the offset line in the peaking path is adjusted to provide high impedance (ideally infinite) from the matching-circuit impedance $Z_{\text{match\_off}}$ so that it prevents power leakage to the peaking path when the peaking transistor is turned off. In real device, the effect of the knee voltage should be considered due to nonzero value of the device on-resistance, which may be smaller or larger depending on the transistor implementation technology. To maximize efficiency at the 6-dB backoff power, the carrier amplifier with nonzero knee voltage should have a load impedance larger than 100 Ω, or larger than $2Z_0$ if $Z_0 \neq 50\,\Omega$, otherwise the carrier amplifier does not reach the saturation region where maximum efficiency can be achieved.[26] In this case, the offset-line length θ_c of the carrier amplifier is optimized to increase the load impedance, while the offset-line length θ_p of the peaking amplifier is adjusted to block the output power leakage, and the phase-compensating line with electrical length of $90° + (\theta_c - \theta_p)$ is used at the input of the peaking amplifier.

11.1.4 Linearity

Generally the nonideal power gain and phase performance in a high-power nonlinear region can cause a significant linearity problem for transmitting signals with a nonconstant envelope in wireless communication transmitters. To solve this problem, an improved DA architecture can be used by employing an envelope tracking technique to control the gate bias voltage of the peaking amplifier in accordance with the input signal envelope. Such an approach can also provide a higher efficiency with a lower bias voltage for higher output powers. This ensures both high efficiency and good linearity requirements over a wide range of output powers. Fig. 11.8A shows the block diagram of a 2.14-GHz LDMOSFET

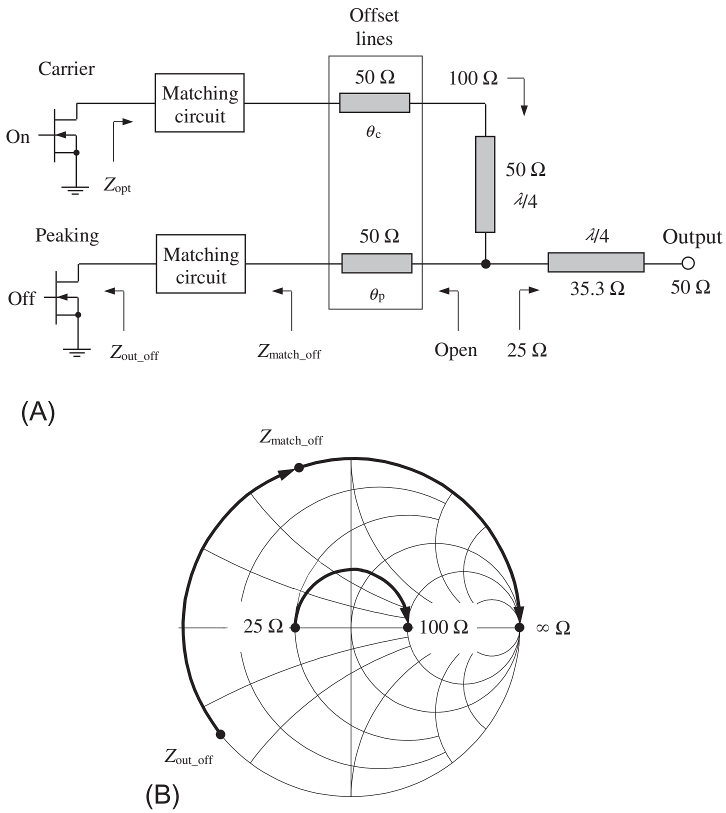

Offset lines
Carrier
On
Matching circuit
50 Ω
θ_c
100 Ω
50 Ω
λ/4
Z_{opt}
Peaking
Off
Matching circuit
50 Ω
θ_p
λ/4
Output
35.3 Ω
50 Ω
Z_{out_off}
Z_{match_off}
Open
25 Ω
(A)
Z_{match_off}
25 Ω
100 Ω
∞ Ω
Z_{out_off}
(B)

FIG. 11.7

Load-network schematic and impedances.

microstrip Doherty PA for WCDMA applications with adaptive gate bias control.[27] For the same average output powers of 32.7 dBm, such a two-stage Doherty PA demonstrates an improvement in a power-added efficiency (*PAE*) of 15.2% at an adjacent channel leakage power ratio (*ACLR*) of −30 dBc compared with its Class-AB counterpart. This is because the quiescent current in a Doherty structure is maintained constant only for the carrier amplifier, whereas the bias point of the peaking amplifier is varied according to the input signal envelope. However, it should be noted that the wider the modulation bandwidth of the transmitting signal, the more problematic to implement such a technique in practice to achieve significant linearity improvement.

The linearity of the PA can be improved by using digital signal processing to provide more accurate gate-bias control alongside the digital predistortion (DPD) needed for the simultaneous correction of the gain and phase characteristics in a high-power region. Fig. 11.8B shows the block schematic of an 840-MHz MESFET Doherty PA for CDMA applications with the digital signal processor (DSP) implemented externally on a board controlled by a personal computer.[28] In this case, the DSP generates both the baseband in-phase (*I*) and quadrature (*Q*) signals, which are upconverted to form an RF signal using

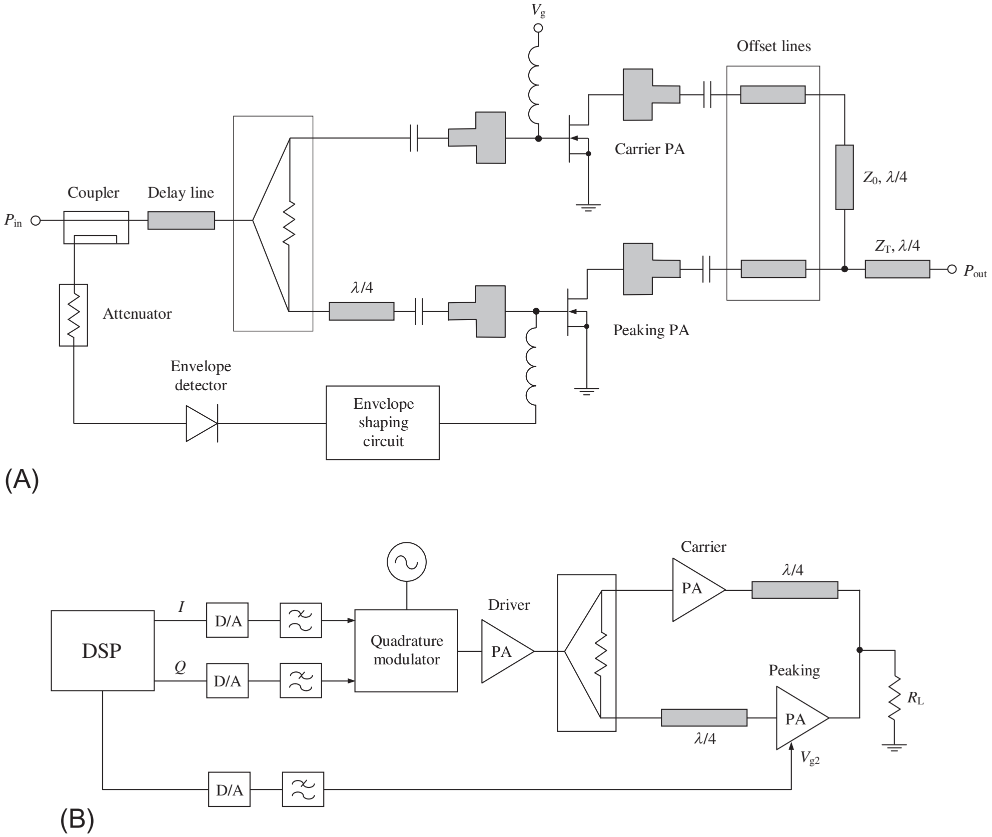

V_g
Offset lines
Carrier PA
Z_0, λ/4
Coupler
Delay line
P_{in}
Z_T, λ/4
P_{out}
λ/4
Attenuator
Peaking PA
Envelope detector
Envelope shaping circuit
(A)
Carrier
PA
λ/4
Driver
I
D/A
DSP
Quadrature modulator
PA
Q
D/A
Peaking
PA
R_L
λ/4
V_{g2}
D/A
(B)

FIG. 11.8

Block diagrams of Doherty amplifier architectures with adaptive control.

the quadrature modulator. The DSP unit also generates the voltage signal V_{g2}, which is applied to the peaking amplifier as the gate bias. This results in an efficiency improvement by the dynamic gate biasing of the peaking amplifier according to the instantaneous envelope of the input signal. At the same time, the phase performance is corrected by the phase predistortion at baseband level based on the dynamic gate bias-voltage values from the gain correction, thus resulting in a linearity improvement. An overall improvement of *PAE* of 3%–5% and an *ACLR* of approximately 10 dB at an average output power of 23 dBm can be achieved by using such a DSP technique. Besides, a simple bias-switching technique can be used in Doherty-type amplifiers, so that they can satisfy the linearity requirements of the PAs for CDMA handset applications over the entire dynamic power range.[29] In addition to bias-switching technique, a dual-mode matching approach can be used to optimally design a dual-mode DA operated simultaneously in HPSK (hybrid phase shift keying) mode and OFDM 64-QAM (quadrature amplitude modulation) mode for mobile terminals.[30]

11.1.5 Series-connected load

In comparison with the shunt-connected load type, the series-connected load combines the output powers of the carrier and peaking amplifiers in a manner similar to that of the push-pull amplifiers, having the same capability to suppress even harmonic components in the output signal spectrum. Fig. 11.9 shows the block diagram of a DA with a series-connected load, where the input and output baluns are implemented with the lumped inductances and capacitors.[31] The lumped-element balun can be designed for an arbitrary unbalanced-load value by proper selecting its element values. In this case, an unbalanced load of 50 Ω and a balanced port load of 100 Ω were chosen. At low-power levels when the peaking amplifier is turned off, one balanced port of the balun connected to the open-circuited quarterwave transmission line is shorted that results in a load of 100 Ω for the carrier amplifier. At high power level when the peaking amplifier becomes active, both the carrier and the peaking amplifiers are operated in a near push-pull mode. For such a GaN HEMT DA operating at 1.8 GHz, high efficiencies of 31% and 56% were achieved at 24- and 31-dBm saturated output powers, respectively.

In some cases, by inserting a short-length transmission line, the output impedance of the peaking amplifier can be transformed from the capacitive to a near-short impedance. As a result, the quarter-wave impedance-inverting line can be removed. Fig. 11.10A shows the circuit schematic of a 1.9-GHz GaN HEMT DA without an impedance-transforming network, which was designed in the form of a series-connected-load configuration using an output-combining balun.[32] Here, a microstrip Wilkinson power divider is used for input power splitting, and the matching circuits and balun with a transformation ratio 2:1 are implemented using lumped-element components. Therefore the load impedance presented to the carrier amplifier varies from 100 Ω at low-power level to 50 Ω at saturation level. The circuit schematics of the carrier and peaking amplifiers are shown in Fig. 11.10B and C, respectively. A two-section output matching circuit for the carrier amplifier is required to provide the two impedance conditions, matching at high-power level and impedance-transforming at low-power level. At the same time the single-section output matching circuit for the peaking amplifier provides a near-zero condition. As a result, a *PAE* above 48% at a saturated output power of greater than 31 dBm at a DC-supply voltage of 20 V was obtained over a wide frequency range from 1.67 to 1.97 GHz.

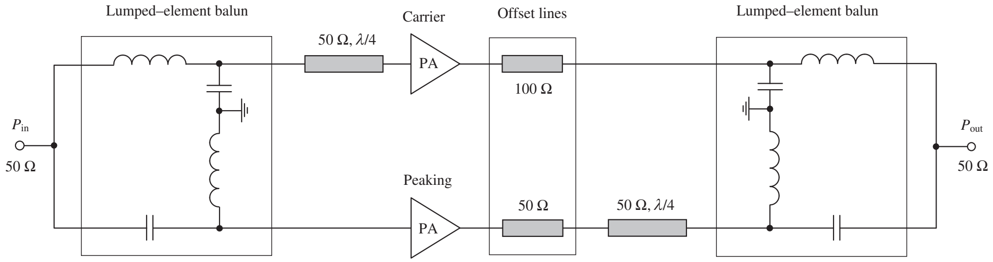


FIG. 11.9

Block diagram of Doherty amplifier with series-connected load.

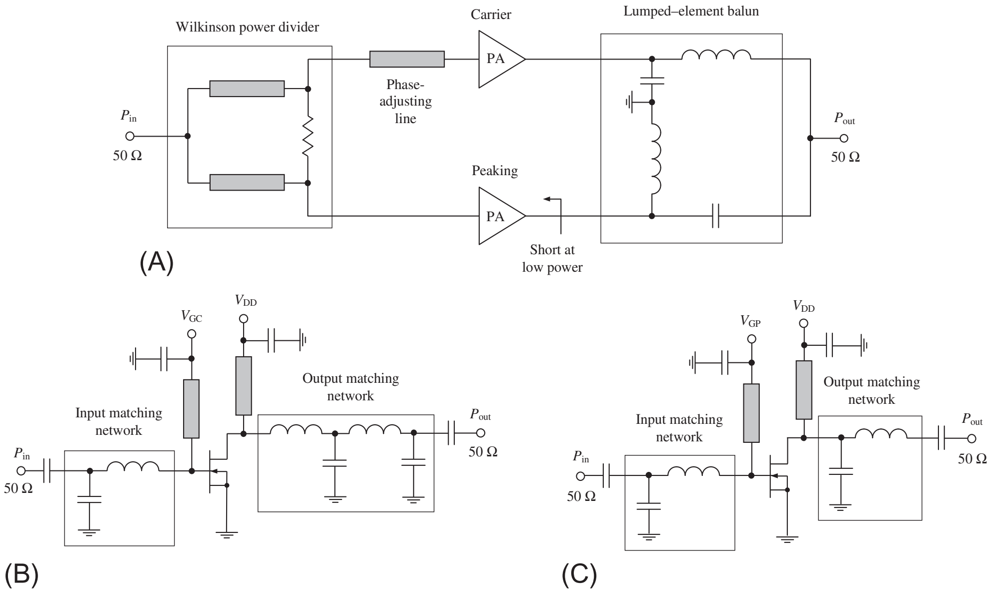

Wilkinson power divider
Carrier
Lumped–element balun
PA
Phase-
adjusting
line
P_{in}
50 Ω
P_{out}
50 Ω
Peaking
PA
Short at
low power
(A)
V_{DD}
V_{GC}
Output matching
network
Input matching
network
P_{out}
50 Ω
P_{in}
50 Ω
(B)
V_{DD}
V_{GP}
Output matching
network
Input matching
network
P_{out}
50 Ω
P_{in}
50 Ω
(C)

FIG. 11.10

Schematics of Doherty amplifier without quarterwave impedance inverter.

11.2 Carrier and peaking amplifiers with harmonic control

Further efficiency improvement of the vacuum-tube DAs can be achieved by creating biharmonic modes at the input and load networks of the carrier and peaking amplifiers. Specifically, additional parallel resonant circuits tuned to the third harmonic were used, that have resulted in an efficiency of over 80%.[33] Ideally, an infinite number of odd-harmonic resonators results in an idealized Class-F mode with a square voltage waveform and a half-sinusoidal current waveform, whereas an infinite number of even-harmonic resonators results in an idealized inverse Class-F mode with a half-sinusoidal voltage waveform and a square current waveform at the device output terminal. However, in practice at microwave frequencies, it is enough to control the second- and third-harmonic components to provide a high operation efficiency of the PA, and it is preferable to use short- and open-circuit stubs instead of lumped capacitors in the load network.

Fig. 11.11A shows the block schematic of a fully matched microwave DA, including the harmonic-control circuits used in front of the output matching circuits and offset lines.[34] To approximate a Class-F operation mode, the harmonic-control circuit includes both arm shunt stubs for a better harmonic trap and a series tuning line to compensate for the output device parasitic elements, as shown in Fig. 11.11B. Despite the fact that the DA with harmonic control provides worse linearity than the conventional DA in terms of AM/AM and AM/PM performance, applying a digital feedback predistortion linearizer allows the *ACLR* to be significantly improved. For example, the *ACLR* of a 2.14-GHz Class-F two-stage GaN HEMT DA with an average output power of 36 dBm and a drain efficiency of 52.4% was

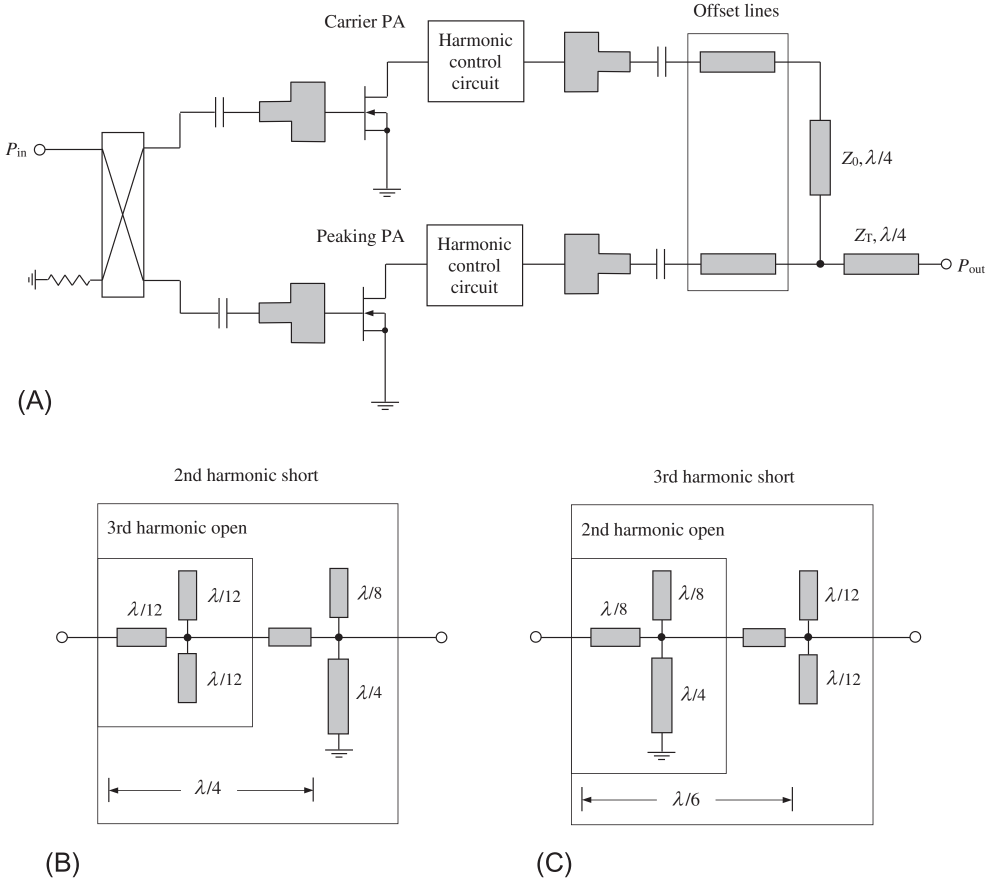

Carrier PA
Harmonic control circuit
Offset lines
$Z_0, \lambda/4$
P_{in}
Peaking PA
Harmonic control circuit
$Z_T, \lambda/4$
P_{out}
(A)
2nd harmonic short
3rd harmonic open
$\lambda/12$
$\lambda/12$
$\lambda/8$
$\lambda/12$
$\lambda/4$
$\lambda/4$
3rd harmonic short
2nd harmonic open
$\lambda/8$
$\lambda/8$
$\lambda/12$
$\lambda/4$
$\lambda/12$
$\lambda/6$
(B)
(C)

FIG. 11.11

Block diagram of Doherty amplifier with harmonic-control circuits.

improved by more than 20 dB.[34] The inverse Class-F two-stage LDMOSFET DA using the harmonic-control circuits shown in Fig. 11.11C is capable of providing a drain efficiency of 54.7% at an average output power of 32 dBm for a 1-GHz forward-link WCDMA signal.[35]

In some cases, a Class-F design strategy can be applied to the carrier amplifier only, whereas the peaking amplifier operates in a conventional Class-C mode.[36] Fig. 11.12 shows the simplified circuit schematic of a Class-F/Class-C DA, in which the drain bias supplies are connected to the corresponding device drain terminals through the short-circuited quarterwave transmission lines providing inherent even-harmonic suppression.[37, 38] In this case, the drain current of the Class-B biased carrier FET contains the DC, fundamental-frequency, and even-harmonic components. However, the drain current of the Class-C biased peaking FET is ideally purely sinusoidal because its odd-harmonic components are shunted by the short-circuited bias-feed quarterwave line connected to the carrier FET, thus resulting in no harmonics appearing at the peaking FET output. However, the effect of output parasitics of the

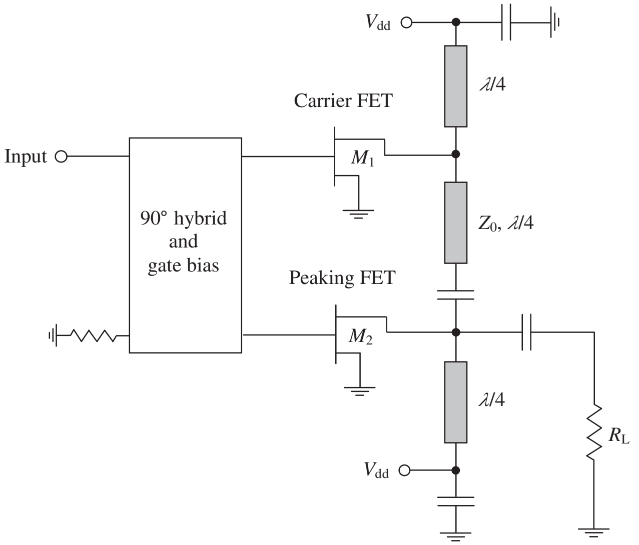


FIG. 11.12

Schematic of Class-F/Class-C Doherty amplifier.

carrier FET reduces the quality of the odd-harmonic short-circuit termination at the peaking FET, resulting in PA performance degradation when measured efficiency was slightly above 60% in saturation at an operating frequency of 770 MHz for a DC-supply voltage of 3.5 V.

The test board of a highly efficient 2.14-GHz 2.5-W transmission-line two-stage GaN HEMT DA with an input branch-line coupler operating in an inverse Class-F mode and implemented in a 30-mil RO4350 substrate is shown in Fig. 11.13A.[11] The load networks of the carrier and peaking amplifiers having the same structure provide the load matching at the fundamental frequency and the corresponding second- and third-harmonic control. Here, high impedance at the second harmonic and low impedance at the third harmonic are created at the output of each device using a short-length series microstrip line short-circuited at the second and third harmonics by a quarterwave short-circuited transmission line (RF grounded by a bypass capacitor) and an open-circuit stub with an electrical length of 30 degrees, respectively.[39] The exact electrical lengths of the microstrip lines depend on the values of the device output shunt capacitance and series inductance. As a result, the drain efficiency at maximum output power and 6-dB backoff point exceeded 65% using two 5-W NPTB00004 GaN HEMT devices. Higher peak efficiencies (over 70%) with much more compact PCB board implementation shown in Fig. 11.13B can be achieved by using two 10-W CGH40010P GaN HEMT devices when both the carrier and peaking PA are based on an inverse Class-F mode according to Fig. 4.41 (Chapter 4), with an average drain efficiency over 50% at an average output power of 5 W for a single-carrier WCDMA signal with a *PAR* of 6.5 dB.

Efficiency enhancement of a DA using GaAs heterostructure FET (HFET) devices can also be provided with a combination of Class-F and inverse Class-F schemes for the carrier and peaking amplifiers, respectively, and an efficiency of 45% can be achieved at 10-dB backoff at 2.1 GHz.[40] At the same time, a peak output power of 44 dBm with a peak drain efficiency of 86.7% can be achieved

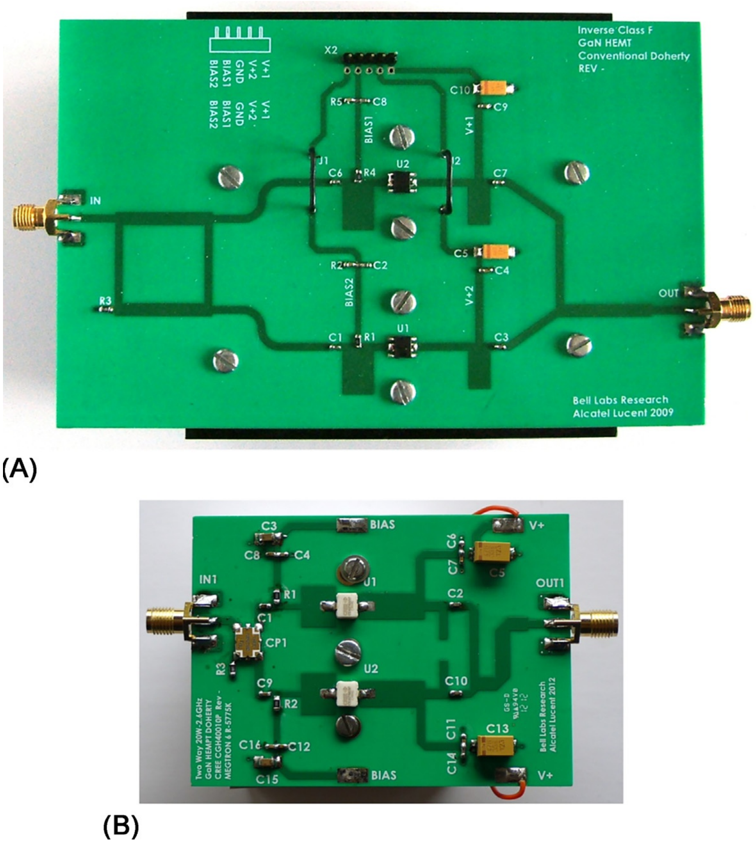

(A)
Inverse Class F
GaN HEMT
Conventional Doherty
REV -
Bell Labs Research
Alcatel Lucent 2009
IN
OUT
(B)
IN1
OUT1
BIAS
V+
Two Way 20W-2.6GHz
GaN HEMPT DOHERTY
Bell Labs Research
Alcatel Lucent 2012

FIG. 11.13

Test boards of inverse Class-F GaN HEMT Doherty amplifiers.

at 2.4 GHz when the carrier amplifier is operated in an inverse Class-F mode and peaking amplifier is designed to operate in a Class-F mode using GaN HEMT devices in an asymmetric Doherty structure.[41] In this case, for a single-carrier 10-MHz LTE signal with a *PAR* of 6.6 dB, an average output power of 37.3 dBm with a drain efficiency of 68% and an *ACLR* of −30.5 dBc before digital linearization was measured.

A high efficiency of the DA can also be achieved using a Class-E mode when the device output shunt capacitance can be considered as an internal element of the Class-E load network.[42] If the device shunt capacitance is larger than the nominal Class-E capacitance, an additional compensation circuit with a series capacitor and a shunt inductance needs to be added to the device output. For example, such a configuration was used in the design of a 2.14-GHz Class-E Doherty PA using 25-W GaN HEMT devices in the carrier and peaking amplifiers, resulting in a *PAE* of 44.8% at an average output power of 37 dBm for a single-carrier WCDMA signal.[43] The symmetric Doherty configuration using packaged devices in the carrier and peaking amplifiers can also be designed in a Class-E mode when the device output capacitance is used to compose a Π-section Class-E load network.[44] In this case, the ideal high-Q series resonant circuit required for the Class-E mode is replaced by a low-pass matching circuit with the series inductance, implemented as a microstrip line on a ceramic substrate, and a shunt ceramic chip capacitor.

At higher operating frequencies and output power levels when low-value device input and output impedances are realized, it is necessary to implement the prematching sections inside the device package to eliminate the effect of long package bondwires and to simplify the external impedance matching with standard 50-Ω source and load. In this case, the input prematching circuit can include an *RC* network to improve the operation stability and the output prematching circuit can provide an optimum second-harmonic reflection phase for high-efficiency operation using thin ceramic substrates with high dielectric permittivity. As a result, a symmetrical 3.5-GHz DA based on two 200-W GaN HEMT devices achieved a drain efficiency of 64.6% at peak output power and a drain efficiency of 51.7% at an output power of 49.2 dBm (83 W) with a power gain of 13.5 dB and an *ACLR* of −50.6 dBc for a single-carrier 20-MHz LTE signal with a *PAR* of 7.5 dB by applying a DPD system.[45]

11.3 Balanced, push-pull, and dual Doherty amplifiers

To increase the overall output power of the DA system, two individual two-stage conventional DAs can be connected in a push-pull configuration using the coaxial-line baluns at both input and output ports to provide balanced-to-unbalanced impedance transformation by combining the outputs of the DAs.[46] The output power capability can further be improved by using two-push-pull PAs in a Doherty configuration. However, at high-power applications, coaxial cables tend to lose their sustainability because of significant effect of the connecting parasitics when output device impedances are very low. In this case, it is preferable to use broadside coupled lines which are placed at $\lambda/8$ phase length (fundamental frequency) from the internal transistor drain.[47] Because broadside coupled lines do not propagate even-harmonic signals, this will act as an open circuit for the second-harmonic signal coming from the transistor, which in turn can improve an operating efficiency due to the even-harmonic short-circuit termination. Such a planar compact configuration of the push-pull DA contributes to bandwidth extension as well when a drain efficiency above 40% with an average output power of 115 W was achieved across the frequency bandwidth of 522–762 MHz using two balanced 350-W LDMOSFET devices operating at a DC-supply voltage of 50 V. Further bandwidth extension can be provided using an additional wideband balun with high impedance ratio at the output instead of a single-ended multistep microstrip transformer. In this case, a drain efficiency of approximately 40% with an average output power of 220 W is achieved across the frequency bandwidth of 470–790 MHz using two balanced 650-W LDMOSFET devices.[48]

Fig. 11.14 shows the balanced configuration using 90-degree hybrid branch-line couplers to split input power and to combine output powers from two identical conventional DAs.[49] In this case, to achieve higher efficiency up to 6-dB backoff output power, a combined design technique based on uneven power divider and asymmetrical devices with optimized size ratio can be used.[50] However, better linearity and higher power capability can be achieved with a balanced structure which combines two identical DAs. To match each individual Doherty structure with the output coupler having 50-Ω inputs, it is necessary to choose the characteristic impedances of the series impedance-transforming quarterwave transmission lines equal to $50/\sqrt{2} = 35\,\Omega$. The balanced DA where the peaking amplifier of the top two-stage Doherty structure and the carrier amplifier of the bottom two-stage Doherty

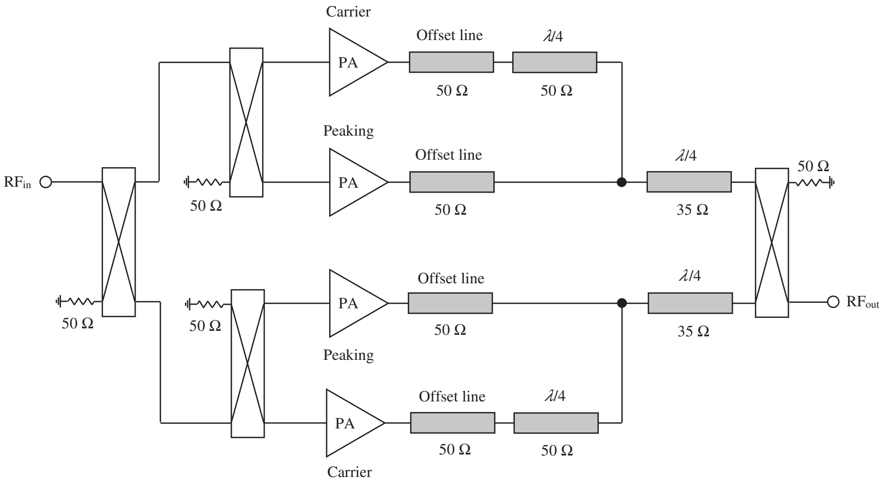


FIG. 11.14

Balanced Doherty amplifier architecture.

structure are interchanged since they have equal 90-degree phase shifts at their outputs can provide better frequency flatness and circuit stability.[51]

The distributed DA uses two individual dual-fed distributed amplifiers where these two distributed amplifiers are coupled in the conventional DA configuration with a 90-degree hybrid at the input and a quarterwave transmission line at the output.[52] By interleaving one peaking amplifier and one carrier amplifier, the input hybrid can be replaced with a quarterwave transmission line, thus resulting in an interleaved four-way DA where two carrier amplifiers and two peaking amplifiers are separated by the input and output quarterwave transmission lines that reduces the overall system size.[52, 53] A distributed Doherty architecture can also represent a single-ended dual-fed distributed structure without the need for a two-way input divider and output combiner when the individual identical two-stage conventional DAs are separated by a $\lambda/2$ at the operating frequency using half-wavelength 50-Ω microstrip lines.[54] However, in this case, both individual DAs should be matched to a 100-Ω output and an additional output impedance transformer must be used.

Fig. 11.15A shows the dual DA architecture where it is enough to use the quarterwave 50-Ω transmission lines only, one in the input circuit to provide a 90-degree phase shift and two in the output circuit to provide a parallel in-phase connection of two individual DAs.[55] This is because the input of each output quarterwave transmission line is 25 Ω, which is then transformed to 100 Ω by a quarterwave 50-Ω transmission line. Finally a parallel connection of two 100-Ω output impedances results in the required 50-Ω output. To provide a high impedance of the peaking amplifiers when they are turned off and to compensate for the effect of their output matching elements and phase delays, offset lines are used in each carrier and peaking amplifying path. In addition, such a parallel dual Doherty architecture can provide high efficiencies at very low power levels since three of the four identical amplifiers can be switched off providing high impedance at the corresponding ends of the output 50-Ω lines, as shown in Fig. 11.15B. As a result, the remaining single PA operates in a 50-Ω environment, providing an efficient and linear operating condition at low output power levels.

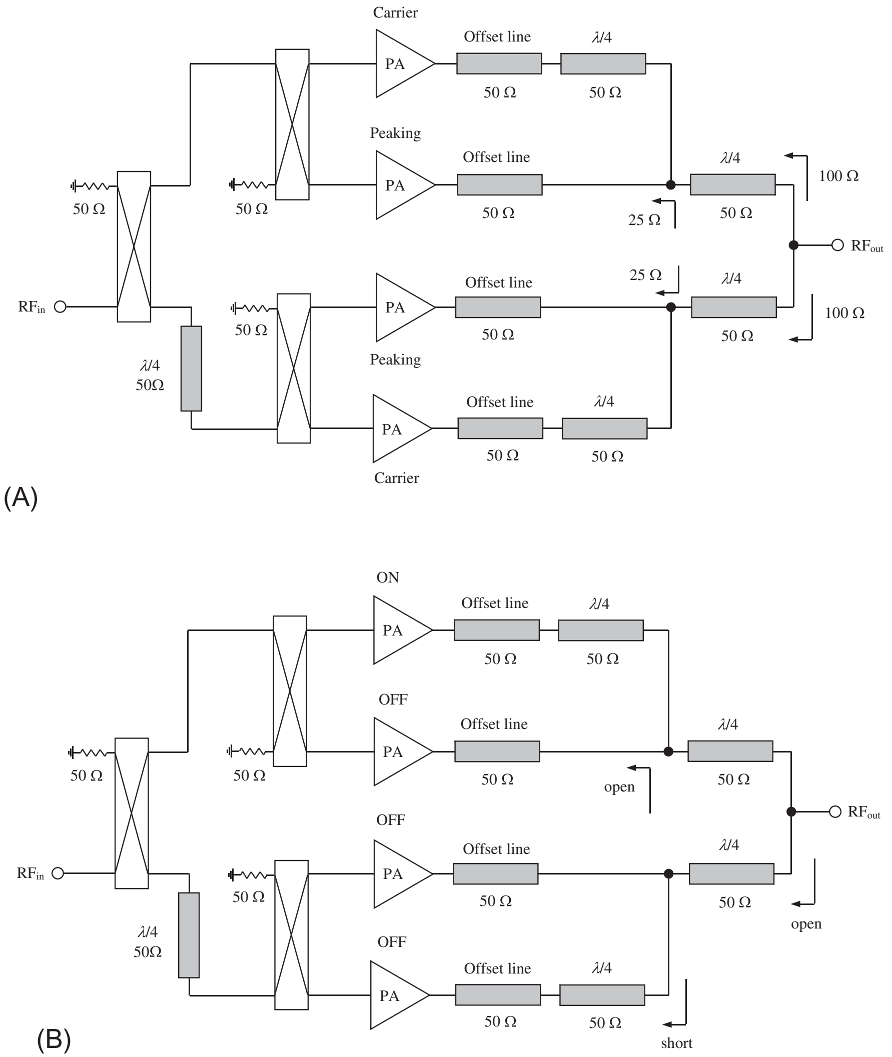

Carrier
PA
Offset line
50 Ω
λ/4
50 Ω
Peaking
PA
Offset line
50 Ω
25 Ω
λ/4
50 Ω
100 Ω
RFout
50 Ω
50 Ω
RFin
PA
Offset line
50 Ω
25 Ω
λ/4
50 Ω
100 Ω
50 Ω
λ/4
50Ω
Peaking
PA
Offset line
50 Ω
λ/4
50 Ω
Carrier
(A)
ON
PA
Offset line
50 Ω
λ/4
50 Ω
OFF
PA
Offset line
50 Ω
open
λ/4
50 Ω
RFout
50 Ω
50 Ω
RFin
OFF
PA
Offset line
50 Ω
λ/4
50 Ω
open
50 Ω
λ/4
50Ω
OFF
PA
Offset line
50 Ω
λ/4
50 Ω
short
(B)

FIG. 11.15

Dual Doherty amplifier architecture.

Fig. 11.16 shows the simulated continuous-wave (CW) drain efficiency versus output power for the dual DA shown in Fig. 11.15A (*curve 1*) and for the switched-path PA shown in Fig. 11.15B (*curve 2*). In this case, for the switched-path GaN HEMT PA based on four 5-W GaN HEMT (NPTB00004) devices and designed in an inverse Class-F mode when only the top transistor is turned on, the drain efficiency of 28.5% at an output power of 30 dBm can be achieved at an operating frequency of 2.14 GHz. This efficiency is 7.5% higher than that for a dual DA (*curve 1*). This means that the PA configuration shown in Fig. 11.15B can operate as a dual DA at high output power levels and as a single PA at low output power levels, thus providing a significant DC-power saving capability.

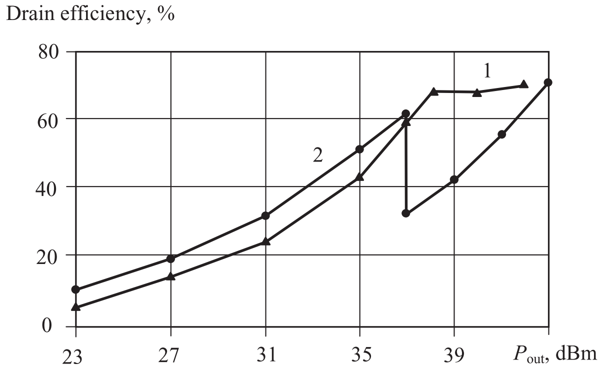


FIG. 11.16

Simulated drain efficiencies versus output power.

11.4 Asymmetric Doherty amplifiers

There is a possibility to extend the region of high efficiency over a wider range of output powers if the carrier and peaking amplifiers are designed to operate with different output powers: smaller for the carrier amplifier and larger for the peaking amplifier. For instance, for a power division ratio $\alpha = P_{\text{carrier}}/P_{\text{peaking}} = 0.25$, the transition point with maximum drain efficiency corresponds to the back-off power level of -12 dB from peak output power.[14] At peak output power when the carrier and peaking amplifiers shown in Fig. 11.5A are saturated, it follows from consideration of their output powers that $R_1 = Z_2 = R_3 = 3R_2$. As a result, $I_2 = 3I_3$ and $\beta = 0.25$. The output impedances R_2 and R_3 as functions of the load resistance R_L and characteristic impedance Z_1 can be obtained from Eqs. (11.7) and (11.8). For example, if one can choose the characteristic impedance of the output transmission line and load resistance equal to $Z_1 = 15\,\Omega$ and $R_L = 50\,\Omega$, respectively, then the characteristic impedance of the quarterwave transformer and load impedance for the carrier amplifier are $Z_2 = R_1 = 18\,\Omega$, while the output impedance of the peaking amplifier is $R_2 = R_1/3 = 6\,\Omega$.

As from Eqs. (11.7) and (11.8), it follows that

$$R_1 = \frac{Z_2^2}{\beta R_3}, \tag{11.10}$$

hence, at lower power levels when the peaking amplifier is turned off, the output impedance R_1 is four times higher than that at peak output power where $R_1 = Z_2 = R_3$. In this case, the power ratio between the peaking and carrier amplifiers should be 3:1. The scaling ratio of 4:1 was chosen for GaAs HBT devices with total emitter areas of 3360 and 840 μm^2 for the peaking and carrier amplifiers, respectively, to implement the extended Doherty technique into the monolithic PA developed for CDMA handset applications. As a result, the *PAE* of 45% and 23% were measured at the highest output power of 25 dBm and at 10-dB backoff level, respectively.[56] Note that the conventional Class-AB PAs designed for the same application normally have the power-added efficiency of about four times lower at this backoff power. To optimize linearity and efficiency of the asymmetric DA, it is very important to optimize the biasing conditions for the carrier and peaking amplifiers.[57]

For the packaged devices when it is difficult to choose the proper power ratio between the devices, it is convenient to use the identical PAs that can compose ideally the N-way Doherty architecture where one carrier amplifier is in parallel with $(N-1)$ numbers of the peaking amplifiers. This is the simplest hybrid approach to acquire an $(N-1)$ times larger-sized peaking amplifier compared with the carrier amplifier for an asymmetric two-way DA configuration.[58] Fig. 11.17A shows the schematic diagram of an N-way DA with a parallel connection of one carrier amplifier and $(N-1)$ identical peaking amplifiers. The ideal drain efficiencies of the N-way DA architectures with peak values at −6, −9.5, −12, and −14 dB power backoff points according to $P_{\text{backoff}} = 20\log_{10}N$ for the two-, three-, four-, and five-way structures, respectively, and the conventional Class-B PA are shown in Fig. 11.17B.

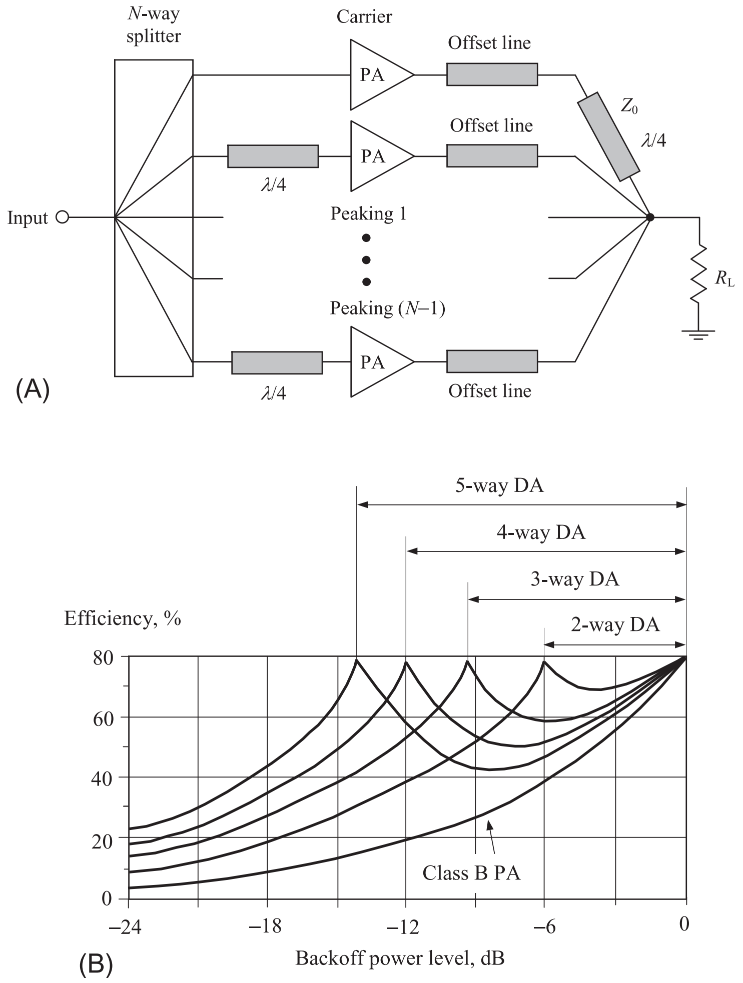

N-way splitter
Carrier
PA
Offset line
Z0
λ/4
Offset line
PA
λ/4
Input
Peaking 1
Peaking (N–1)
RL
PA
λ/4
Offset line
(A)
5-way DA
4-way DA
3-way DA
2-way DA
Efficiency, %
80
60
40
20
0
Class B PA
–24
–18
–12
–6
0
Backoff power level, dB
(B)

FIG. 11.17

Asymmetric *N*-way Doherty amplifier and efficiencies.

Generally the *N*-way DA is composed of the *N*-way power splitter, identical fully matched carrier and $(N-1)$ peaking amplifiers, *N* offset lines, and an output combiner representing a quarterwave impedance transformer. The characteristic impedance of a quarterwave transmission line for converting the load of the carrier amplifier is $Z_0 = R_0/\sqrt{\alpha}$ and the common load resistance is $R_L = R_0/(\alpha+1)$, where R_0 is the matched load for both carrier and peaking amplifiers, usually equal to 50 Ω.[59] For asymmetric two- and three-way DAs with optimized individual bias conditions and load matching for the carrier and peaking amplifiers, applying an uneven drive results in more linear operation and produces more power than an even drive.[60, 61] For example, a three-way DA based on Class-F load networks and fabricated using 10-W GaN HEMT devices achieved a *PAE* of 45.9% and an *ACLR* of −49.2 dBc for a single-carrier WCDMA signal with a *PAR* of 10 dB at 2.14 GHz using a digital feedback predistortion technique.[62]

For a high-PA with a very low output impedance, the width of the matching microstrip line is wide being comparable with its length and the overall size of the matching circuit, including an offset line to create an open-circuit condition when the peaking amplifier is turned off and a quarterwave transforming line, becomes sufficiently large and it is very difficult to physically connect the output of the peaking amplifier directly to the carrier amplifier path. Therefore for convenience of implementation, the classical *N*-way DA configuration can be modified by including an additional half-wave line at the output of each peaking amplifier. Fig. 11.18A shows the block schematic of a three-way asymmetric DA configuration, where the output combiner includes one quarterwave microstrip line in a carrier path, two quarterwave microstrip lines in each peaking path, and one combining quarterwave microstrip line. Here, each amplifying path includes the packaged device of the same die size, input and output matching circuits using microstrip lines. Offset lines are necessary to provide open-circuit conditions at their ends for peaking amplifiers when they are turned off. Then, two quarterwave microstrip lines with different widths required for the corresponding impedance transformation translate this open-circuit condition in each peaking path to open circuit seen by the carrier path at output power levels lower than −9 dBc at a common node in the output combiner. For example, for identical carrier and peaking amplifiers having optimum load impedance $Z_0 = 5\,\Omega$ each and $Z_2 = R_L = 50\,\Omega$, where R_L is the standard 50-Ω load impedance, $Z_1 = \sqrt{Z_0 Z_2} = 15.8\,\Omega$ and $Z_3 = \sqrt{Z_2 R_L}/\sqrt{3} = 28.9\,\Omega$. There may be different combinations of the characteristic impedances between quarterwave microstrip lines in the output combiner. The quarterwave microstrip line in the input path of the carrier amplifier is used to compensate for the delay provided by the output combiner.

The test board of a modified three-way DA based on three dual-path GaN HEMT devices in metal-ceramic flange packages, each including a pair of 180-W GaN HEMT dies with internal input matching, was fabricated on a 20-mil RO4350 substrate. The input three-way divider, input and output matching circuits, offset lines, output combiner, and gate and drain bias circuits (having bypass capacitors on their ends) are fully based on microstrip lines of different electrical lengths and characteristic impedances. Special care was taken for device implementation process to minimize the output lead inductances of the packaged GaN HEMT device. As a result, the measured output power at 1-dB gain compression point P_{1dB} of 60 dBm and peak efficiency of 80% with a power gain of approximately 15 dB were achieved at a DC-supply voltage of 55 V within the frequency range of 2.11–2.17 GHz. Fig. 11.18B shows the plots of the drain efficiency and power gain versus output power, with a drain efficiency of approximately 70% at approximately 8.5 dB power backoff.[63] For a single-carrier 20-MHz LTE signal with a *PAR* of 8 dB, an average power of 52 dBm was obtained with a drain efficiency of approximately 65%. In this case, a power gain of approximately 15 dB was achieved in a

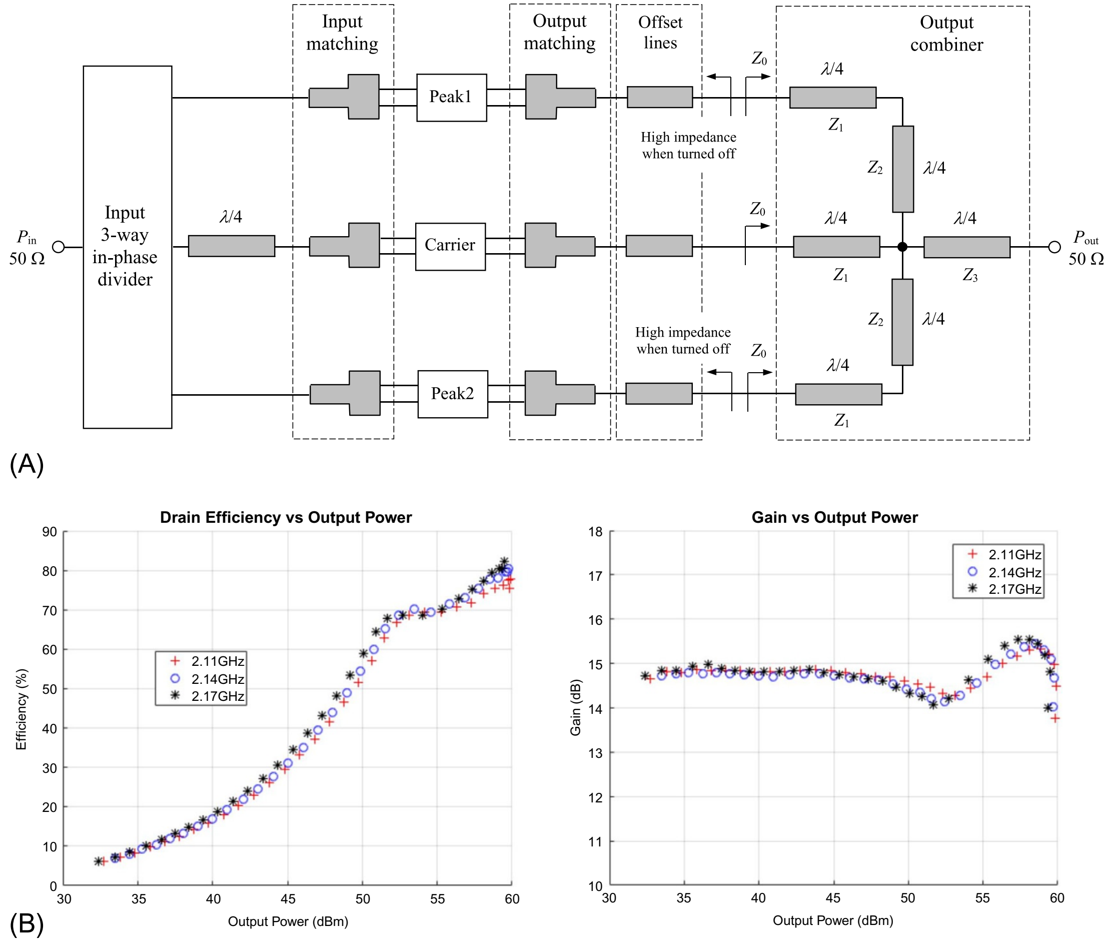

Input matching
Output matching
Offset lines
Output combiner
Z_0
$\lambda/4$
Peak1
Z_1
High impedance when turned off
Z_2
$\lambda/4$
P_{in}
50 Ω
Input 3-way in-phase divider
$\lambda/4$
Carrier
Z_0
$\lambda/4$
$\lambda/4$
Z_1
Z_3
P_{out}
50 Ω
Z_2
$\lambda/4$
High impedance when turned off
Z_0
$\lambda/4$
Peak2
Z_1
(A)
Drain Efficiency vs Output Power
Efficiency (%)
Output Power (dBm)
2.11GHz
2.14GHz
2.17GHz
0
10
20
30
40
50
60
70
80
90
30
35
40
45
50
55
60
Gain vs Output Power
Gain (dB)
Output Power (dBm)
2.11GHz
2.14GHz
2.17GHz
10
11
12
13
14
15
16
17
18
30
35
40
45
50
55
60
(B)

FIG. 11.18

Block schematic and performance of high-power three-way Doherty amplifier.

linear operating region having 2-dB flatness over the entire output power range up to 60 dBm when its value reduces by just 1 dB compared with its value in linear region.

To predict the wideband Doherty performance and optimize the input and output transmission lines of the carrier and peaking amplifying paths required for optimum impedance transformation and phase compensation, nonlinear behavioral models can be generated for both carrier and peaking amplifiers. As a result of the circuit optimization, accurate load-pull testing and practical implementation of an asymmetric two-way DA based on Qorvo 0.25-μm GaN HEMT QPD2094 and QPD2195 devices, an average power of 85 W with a peak power of 470–570 W and relatively flat average efficiency of 45%–49% was achieved across the frequency band of 1.8–2.2 GHz for a single-carrier 20-MHz WCDMA signal with a *PAR* of 10 dB.[64]

11.5 Multistage Doherty amplifiers

Generally an asymmetric Doherty architecture exhibits a significant drop in efficiency in the region between the efficiency peaking points, especially for large power ratios between the carrier and peaking amplifiers. However, it is possible to use more than two PAs to prevent significant deterioration of efficiency at backoff output power levels. This can be provided by the so-called multistage DAs, the operation of which is analogous to that of the conventional two-stage DA as having a low-power region when only the carrier amplifier is turned on and a high-power region when all peaking amplifiers are turned on.[14] In this case, unlike the asymmetric DA when all peaking amplifiers are turned off simultaneously, the peaking amplifiers in a multistage DA are turned off consecutively at the corresponding peak efficiency points, beginning from $(N-1)$ peaking amplifier.

The basic multistage Doherty PA architecture shown in Fig. 11.19A comprises more than one peaking amplifier, with the quarterwave transmission lines to combine their output powers.[65] The characteristic impedances of each output quarterwave transmission line depend on the levels of backoff power and can be calculated from

$$Z_i = R_L \prod_{j=1}^{i} \gamma_j, \tag{11.11}$$

$$\prod_{j=k}^{(i+k)/2} \gamma_{(2j-k)} = 10^{(B_i/20)}, \tag{11.12}$$

where $i = 1, 2, \ldots, N-1$, $k = 1$ (for odd i) or 2 (for even i), N is the total number of amplifier stages, and B_i is the backoff level (positive value in decibels) from the maximum output power of the system, at which the efficiency peaks. The maximum level of backoff B_{N-1} is set by the carrier amplifier, while the number of efficiency peaking points is directly proportional to the number of amplifier stages used in the design.

Fig. 11.20 shows the theoretical instantaneous drain efficiencies of the multistage DA architectures for two, three, and four stages, having maximum efficiencies at the transition points of −6, −12, and −18 dB backoff output power levels, respectively. From Fig. 11.20, it follows that the multistage architecture provides higher efficiencies at backoff levels between the efficiency peaking points compared with an asymmetric Doherty architecture and significantly higher efficiency at all backoff output power levels compared with the conventional Class-B PAs. For the most practical case of a three-stage DA, the block schematic of which is shown in Fig. 11.19B, the characteristic impedances of each output quarterwave transmission line can be obtained from Eqs. (11.11) and (11.12) as

$$Z_1 = \gamma_1 R_L, \tag{11.13}$$

$$Z_2 = \gamma_1 \gamma_2 R_L, \tag{11.14}$$

where $\gamma_1 = 10^{(B_1/20)}$, $\gamma_2 = 10^{(B_2/20)}$, $B_1 = 6$, and $B_2 = 12$ for peak efficiencies at −6 and −12 dB backoff points, respectively, resulting in $Z_1 = 30\,\Omega$ and $Z_2 = 120\,\Omega$ for $R_L = 15\,\Omega$.

For a 1.95-GHz WCDMA application, a three-stage DA structure using GaAs MESFET devices with the device periphery ratio of 1:2:4 and microstrip power combining elements could provide a *PAE* of 48.5% and a power gain of 12 dB at $P_{1dB} = 33$ dBm. The peak power-added efficiencies of 42% and 27% were measured at −6 and −12 dB backoff levels, respectively.[65] Efficiencies at backoff

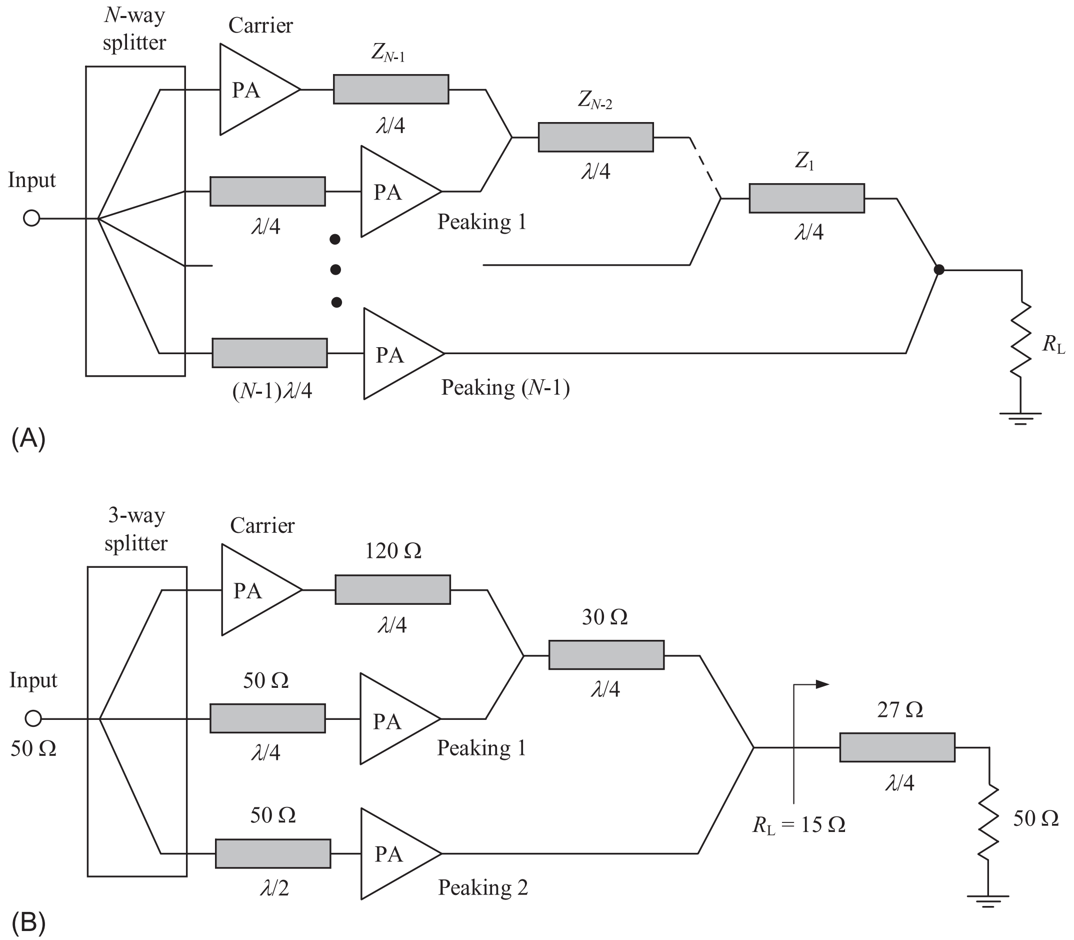

N-way splitter
Carrier
PA
Z_{N-1}
λ/4
Z_{N-2}
λ/4
Z_1
λ/4
Input
PA
λ/4
Peaking 1
PA
(N-1)λ/4
Peaking (N-1)
R_L
(A)
3-way splitter
Carrier
PA
120 Ω
λ/4
30 Ω
λ/4
Input
50 Ω
50 Ω
λ/4
PA
Peaking 1
50 Ω
λ/2
PA
Peaking 2
R_L = 15 Ω
27 Ω
λ/4
50 Ω
(B)

FIG. 11.19

Multistage Doherty amplifier architectures.

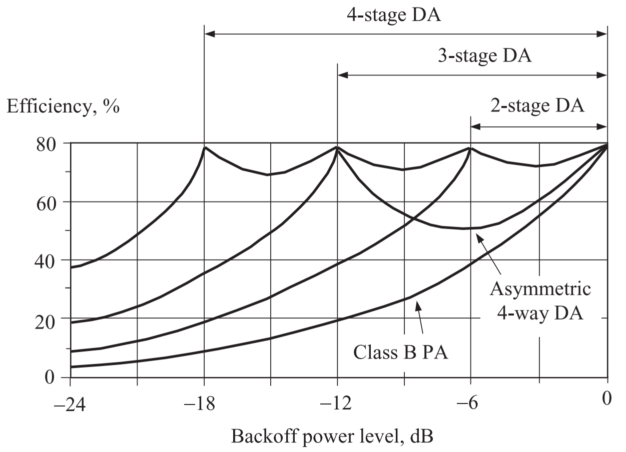


FIG. 11.20

Theoretical efficiencies of different Doherty amplifier architectures.

points can be increased by optimizing the input drive conditions for the peaking amplifiers.[66] Moreover, further efficiency improvement of a three-stage DA at the maximum output power and backoff points can be achieved by using the highly effective GaN HEMT devices and applying DPD technique for linearization. In this case, the drain efficiency at −12 dB output power backoff point can be increased to be higher than 60%.[67]

A typical problem associated with the conventional three-stage DA is that the load-line modulation of the carrier stage stops at a certain power level, leaving the carrier amplifier in deep saturation and leading, consequently, to a significant degradation of its linear performance. In addition, when the carrier and peaking amplifiers have equal configurations with the same device periphery sizes, similar performance is obtained with regards to the symmetrical two-stage DA, with the efficiency peaking points at −3.5 and −6 dB backoff output powers. These problems can be partially solved by using a modified three-stage DA architecture with a parallel combination of one carrier and one DA used as a peaking amplifier, as shown in Fig. 11.21A.[68] In this case, a novel way of combining enables high instantaneous efficiencies at −6 and −9.5 dB backoff output powers with a single device size.

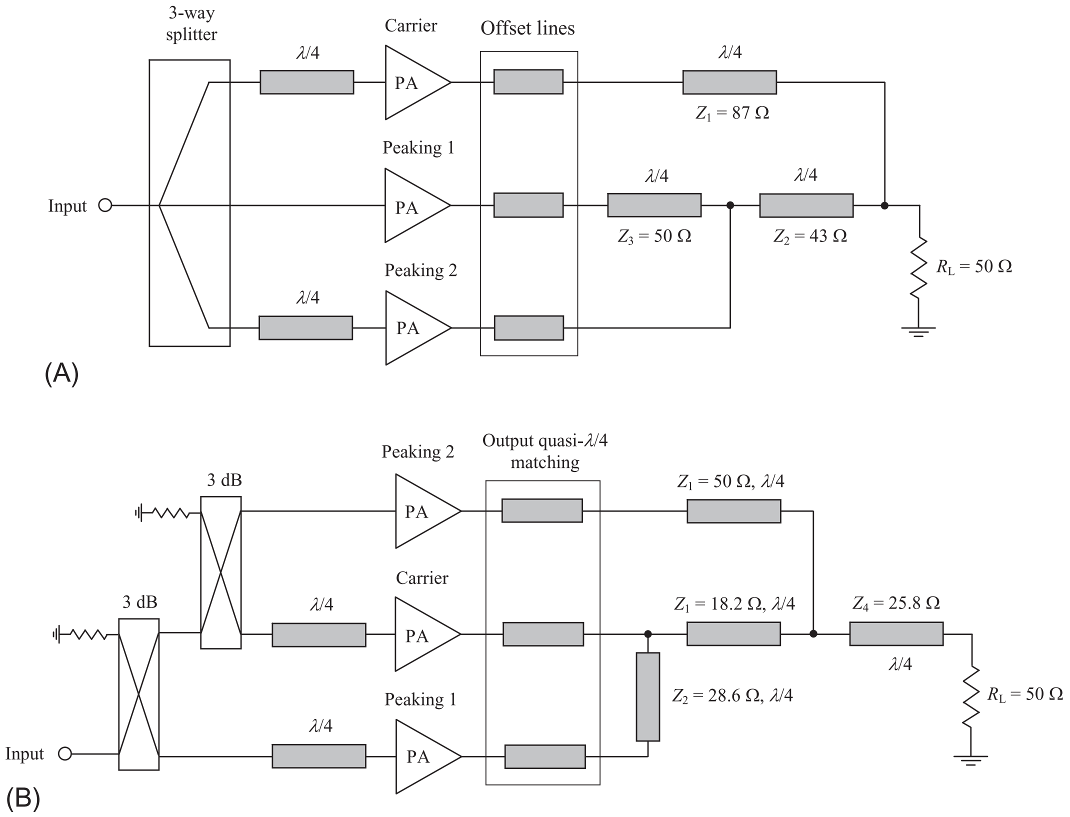

3-way splitter
Carrier
Offset lines
λ/4
PA
λ/4
Z₁ = 87 Ω
Peaking 1
Input
λ/4
λ/4
Z₃ = 50 Ω
Z₂ = 43 Ω
R_L = 50 Ω
Peaking 2
λ/4
(A)
Peaking 2
Output quasi-λ/4 matching
3 dB
Z₁ = 50 Ω, λ/4
Carrier
3 dB
λ/4
Z₁ = 18.2 Ω, λ/4
Z₄ = 25.8 Ω
λ/4
Z₂ = 28.6 Ω, λ/4
R_L = 50 Ω
Peaking 1
λ/4
Input
(B)

FIG. 11.21

Modified three-stage Doherty amplifier architectures.

The characteristic impedances of the transforming quarterwave transmission lines are calculated as $Z_1 = \sqrt{3}R_L$, $Z_2 = (\sqrt{3}/2)R_L$, and $Z_3 = R_L$, where R_L is the load resistance.[69, 70]

Fig. 11.21B shows the schematic of the other modified classical three-stage Doherty architecture with power ratio of 1:1.75:1 and half-wave electrical lengths from intrinsic drains of the carrier and second peaking devices to corresponding combining points for convenience of practical implementation.[71] By using 28-V LDMOSFET devices having a peak power of 150 W for peaking amplifiers and 260 W for carrier amplifier, an average output power of 49 dBm with a drain efficiency >55% and a power gain >15.5 dB was achieved in the frequency range of 1805–1880 MHz for a single-carrier 20-MHz WCDMA signal with a *PAR* of 9.9 dB. After applying a DPD technique, the linearity was improved from −29 to −60 dBc.

To split or combine the output powers at microwaves in a 50-Ω environment, the branch-line 90-degree microstrip-line hybrid combiners with equal power split, as shown in Fig. 11.22A, are the most popular. In this case, the characteristic impedances of the transverse branches should be of 50 Ω, whereas the longitudinal branches must have the characteristic impedance of $50/\sqrt{2} = 35.3\,\Omega$. In practice, because of the quarterwave transmission-line requirements, the bandwidth of such a balanced PA based on two quadrature branch-line hybrids is limited to 10%–20%.

However, if one pair of terminating resistors has different values compared with the other pair, the resulting branch-line hybrid can operate as a directional coupler and an impedance transformer simultaneously.[72] In this case, the design values of the branch- and main-line characteristic impedances for a branch-line hybrid coupler shown in Fig. 11.22B, related to the input source impedance Z_{0S} and output load impedances Z_{0L}, can be calculated from

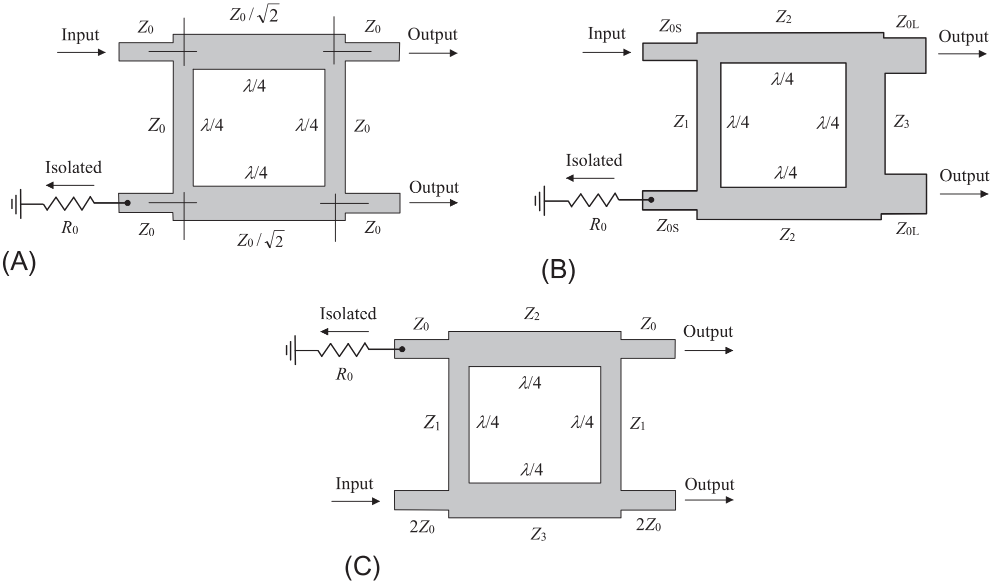

Input
Z_0
$Z_0/\sqrt{2}$
Z_0
Output
$\lambda/4$
Z_0
$\lambda/4$
$\lambda/4$
Z_0
Isolated
$\lambda/4$
Output
R_0
Z_0
$Z_0/\sqrt{2}$
Z_0
(A)
Input
Z_{0S}
Z_2
Z_{0L}
Output
$\lambda/4$
Z_1
$\lambda/4$
$\lambda/4$
Z_3
Isolated
$\lambda/4$
Output
R_0
Z_{0S}
Z_2
Z_{0L}
(B)
Isolated
Z_0
Z_2
Z_0
Output
R_0
$\lambda/4$
Z_1
$\lambda/4$
$\lambda/4$
Z_1
$\lambda/4$
Input
Output
$2Z_0$
Z_3
$2Z_0$
(C)

FIG. 11.22

Schematics of branch-line microstrip hybrid couplers with different coupling and impedances.

$$Z_1 = \frac{Z_{0S}}{K}, \tag{11.15}$$

$$Z_2 = \sqrt{\frac{Z_{0S}Z_{0L}}{1+K^2}}, \tag{11.16}$$

$$Z_3 = \frac{Z_1 Z_{0L}}{Z_{0S}}, \tag{11.17}$$

where K is the voltage-split ratio between the output ports, and $R_0 = Z_{0S}$.[73] Such a branch-line hybrid coupler with a 2:1 (50- to 25-Ω) impedance transformation ratio can provide an approximately 20% frequency bandwidth with a ±0.25-dB amplitude imbalance. However, for a fixed directivity, the frequency bandwidth of the branch-line impedance-transforming hybrid coupler increases as the output-to-input impedance ratio is reduced.[72] In this case, for a 50- to 25-Ω coupler with 3-dB coupling, the characteristic impedances of the corresponding branch line are $Z_1 = 42\,\Omega$, $Z_2 = 22.7\,\Omega$, and $Z_3 = 21\,\Omega$. Wider bandwidth performance of the branch-line coupler with arbitrary coupling levels can be achieved if an additional transforming quarterwave line is connected to each port of the coupler.[74]

An example of the branch-line hybrid coupler with a 1:2 power split with different port impedances is shown in Fig. 11.22C, where the impedances of the input and through ports are equal to $2Z_0$ and the impedances of the isolated and coupled ports are equal to Z_0. In this case, the design values of the branch- and main-line characteristic impedances can be obtained by

$$Z_1 = \sqrt{2}\,Z_0 K, \tag{11.18}$$

$$Z_2 = \sqrt{\frac{Z_0 Z_1}{Z_1^2 + 2Z_0^2}}, \tag{11.19}$$

$$Z_3 = 2Z_2, \tag{11.20}$$

where Z_0 is the system impedance usually equal to 50 Ω.[75]

In some case, it is important to provide an unequal power split for more than two PAs or amplifying stages with different output powers and input impedances. By combining two branch-line impedance-transforming hybrid couplers with different power split ratio, a three-way impedance-transforming power divider can be obtained, as shown in Fig. 11.23A. Here, the power division ratio of 1:2:4 is used, corresponding to the same devise size ratio and providing the proportional impedances of 7, 15, and 30 Ω to simplify the input matching conditions for three PAs in a three-stage Doherty configuration intended to operate in a frequency bandwidth of 3.6–3.8 GHz. In this case, to provide an impedance of 7 Ω seen by the coupled output port of the top branch-line hybrid, an additional quarterwave line is required for a 15- to 7-Ω impedance transformation. As shown in Fig. 11.23B, the forward transmission ratio to three output ports from the input port corresponding to the power split ratio of 1:2:4 is defined as −8.5, −5.4, and −2.4 dB, respectively.

Fig. 11.24 shows the theoretical instantaneous drain efficiencies of the multistage (three and four stages) and four-way asymmetric DA architectures for different power (or device size) ratios, with peak efficiencies ranging from −12 dB power backoff levels. From Fig. 11.24, it follows that the four-way or any asymmetric multiway Doherty architecture provides significantly lower efficiency between the corresponding peak efficiency points. However, for a multistage Doherty configuration, the peak efficiency points at lower power backoff levels can be achieved using an optimum device size ratio.

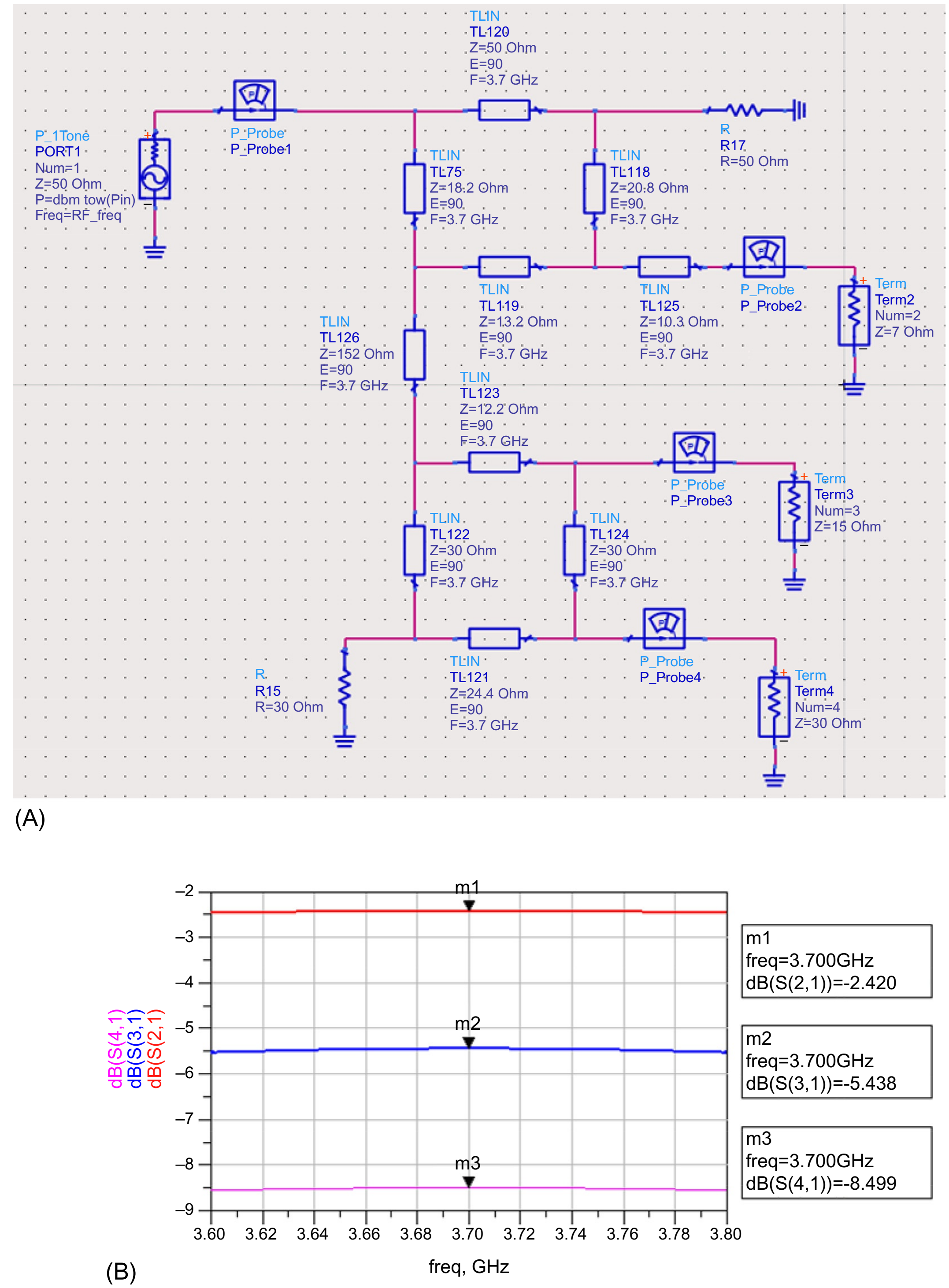

TLIN
TL120
Z=50 Ohm
E=90
F=3.7 GHz
P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbm tow(Pin)
Freq=RF_freq
P_Probe
P_Probe1
TLIN
TL75
Z=18.2 Ohm
E=90
F=3.7 GHz
TLIN
TL118
Z=20.8 Ohm
E=90
F=3.7 GHz
R
R17
R=50 Ohm
TLIN
TL119
Z=13.2 Ohm
E=90
F=3.7 GHz
TLIN
TL125
Z=10.3 Ohm
E=90
F=3.7 GHz
P_Probe
P_Probe2
Term
Term2
Num=2
Z=7 Ohm
TLIN
TL126
Z=152 Ohm
E=90
F=3.7 GHz
TLIN
TL123
Z=12.2 Ohm
E=90
F=3.7 GHz
P_Probe
P_Probe3
Term
Term3
Num=3
Z=15 Ohm
TLIN
TL122
Z=30 Ohm
E=90
F=3.7 GHz
TLIN
TL124
Z=30 Ohm
E=90
F=3.7 GHz
R
R15
R=30 Ohm
TLIN
TL121
Z=24.4 Ohm
E=90
F=3.7 GHz
P_Probe
P_Probe4
Term
Term4
Num=4
Z=30 Ohm
(A)
m1
m2
m3
dB(S(4,1))
dB(S(3,1))
dB(S(2,1))
−2
−3
−4
−5
−6
−7
−8
−9
3.60
3.62
3.64
3.66
3.68
3.70
3.72
3.74
3.76
3.78
3.80
freq, GHz
m1
freq=3.700GHz
dB(S(2,1))=-2.420
m2
freq=3.700GHz
dB(S(3,1))=-5.438
m3
freq=3.700GHz
dB(S(4,1))=-8.499
(B)

FIG. 11.23

Three-way impedance-transforming power divider with power division ratio of 1:2:4.

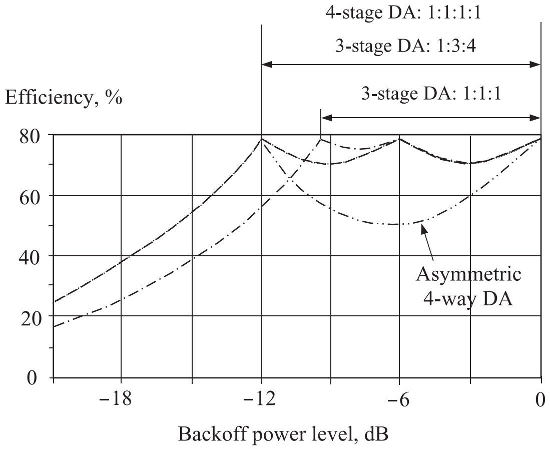


FIG. 11.24

Theoretical efficiencies of different Doherty amplifier architectures.

For example, a peak efficiency at the lowest backoff point of −12 dB is achieved for a device periphery ratio of 1:3:4 in a three-stage DA, whereas the lowest backoff of approximately −9.5 dB corresponds to the peak efficiency for an equal device periphery size of 1:1:1 in the modified three-stage DAs shown in Fig. 11.21A.[65, 70]

In a classical four-stage Doherty PA with corresponding peak efficiencies at −6, −12, and −18 dB backoff output power points, the maximum ratio between the characteristic impedances of the quarter-wave transmission lines is equal to 16.[65] For example, for $R_L = 6\,\Omega$, the characteristic impedances of the consecutive quarterwave transmission lines are $Z_1 = 12\,\Omega$, $Z_2 = 48\,\Omega$, and $Z_3 = 192\,\Omega$, respectively. These values are difficult to correctly implement using microstrip lines on a single substrate with a fixed thickness and dielectric permittivity. In a four-stage Doherty configuration with the device size ratio of 1:1:1:1 shown in Fig. 11.25, where two conventional two-stage DAs are combined in a final four-stage Doherty configuration, the maximum ratio between the transmission-line characteristic impedances is $50\,\Omega/25\,\Omega = 2$ only.[76]

Fig. 11.24 also shows the three efficiency peaking points provided by a four-stage DA with the device size ratio of 1:1:1:1 where the gate bias voltages for the second and third peaking amplifiers are the same. Furthermore, the optimization of these gate bias voltages can change the efficiency profile between the peak power and −6 dB backoff points and contribute to linearity improvement. Because of the device input and output parasitics such as the gate-source and drain-source capacitances, additional input offset lines are implemented at the input of the peaking amplifiers and identical output offset lines that introduce the compensating inductive reactances are connected in series to each output circuit. This is a very practical version of a four-stage DA, capable of achieving high output powers with high drain efficiency and having three commercially available 90-degree hybrid couplers at the input and four quarterwave microstrip lines at the output.

Fig. 11.26 shows the test board of a four-stage GaN HEMT Doherty PA based on four 25-W Cree CGH40025F devices and fabricated using a 30-mil RO4350 substrate.[11] The carrier and peaking amplifiers are designed to operate in an inverse Class-F mode with the second- and third-harmonic control

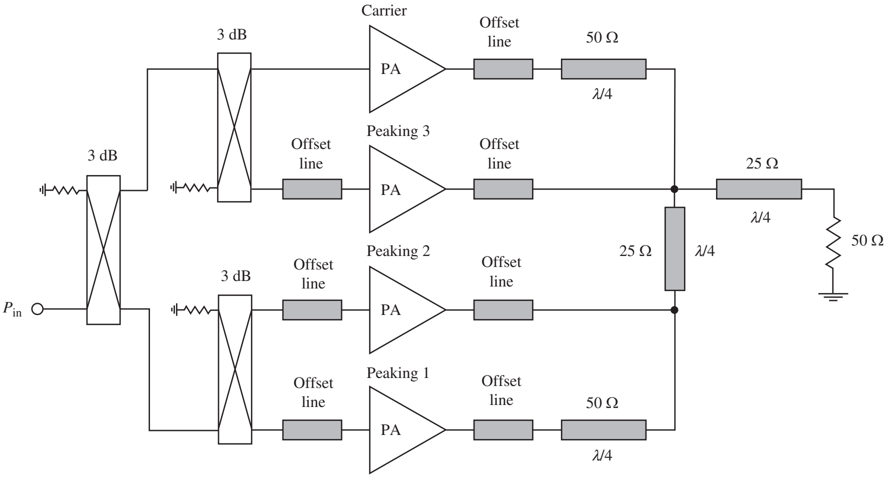

Carrier
3 dB
Offset line
50 Ω
λ/4
PA
Peaking 3
Offset line
Offset line
25 Ω
3 dB
λ/4
50 Ω
25 Ω
λ/4
Peaking 2
Offset line
Offset line
3 dB
P_{in}
Peaking 1
Offset line
Offset line
50 Ω
λ/4

FIG. 11.25

Four-stage Doherty amplifier architecture with equal-size devices.

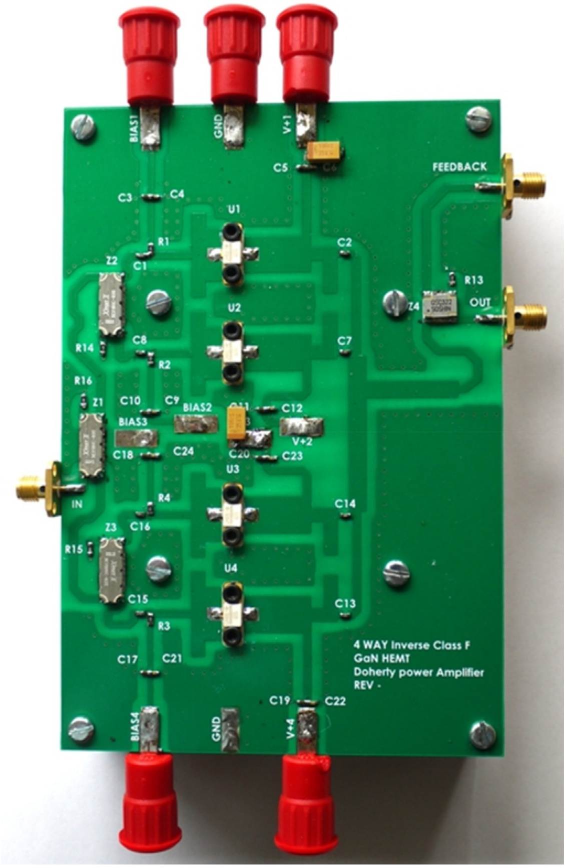

BIAS1
GND
V+1
FEEDBACK
OUT
IN
BIAS4
GND
V+4
4 WAY Inverse Class F
GaN HEMT
Doherty power Amplifier
REV -

FIG. 11.26

Test board of 2.14 GHz 100-W four-stage Doherty GaN HEMT amplifier.

by using a transmission-line load-network technique according to Fig. 4.42 in Chapter 4. The input dividing network includes three 90-degree hybrid couplers, while a 30-dB directional coupler required to sampling output power for linearization loop needs to be connected to the output port. The simulated optimized drain efficiency and power gain versus output power for this architecture is shown in Fig. 11.27A, from which it follows that high drain efficiency over 80% at saturation and more than 60% over 10-dB output power backoff level can be achieved with optimum gate bias voltages for each transistor. In a CW operation mode when all transistors are biased with the same gate voltage of −3.4 V, an output power of 50 dBm (100 W) and a drain efficiency of 77% were achieved at a DC-supply voltage of 34 V. For a single-carrier 2.14-GHz WCDMA signal with a *PAR* of 6.5 dB, a drain efficiency of 61% was measured at an average output power of 43 dBm (20 W) with an *ACLR* of −31 dBc.

The four-stage LDMOSFET Doherty PA based on four 75-W NXP BLF6G22LS-75 devices was fabricated using a 30-mil RO4350 substrate based on the similar circuit schematic shown in Fig. 11.25. The carrier and peaking amplifiers are designed to operate in an inverse Class-F mode with the second- and third-harmonic control by using a transmission-line load-network technique according to Fig. 4.46

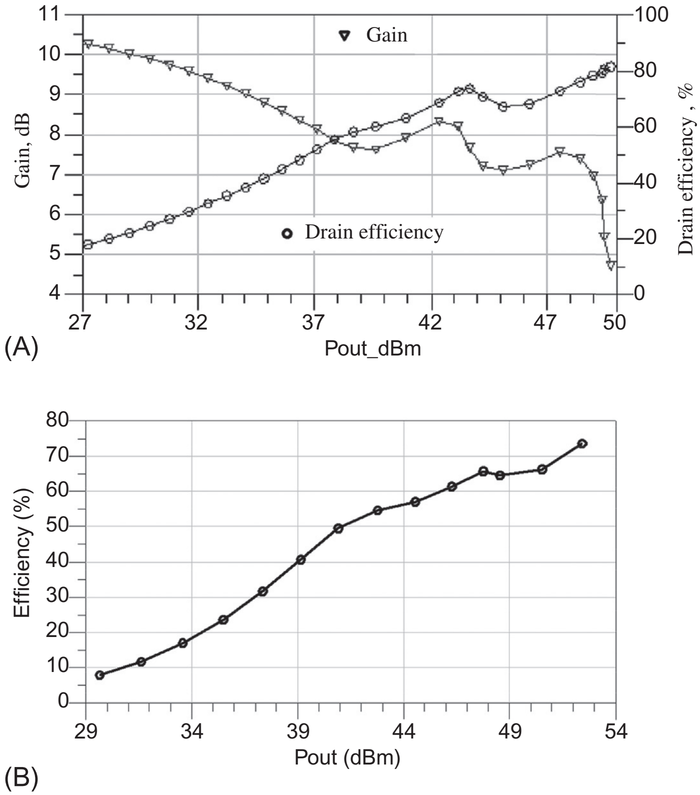
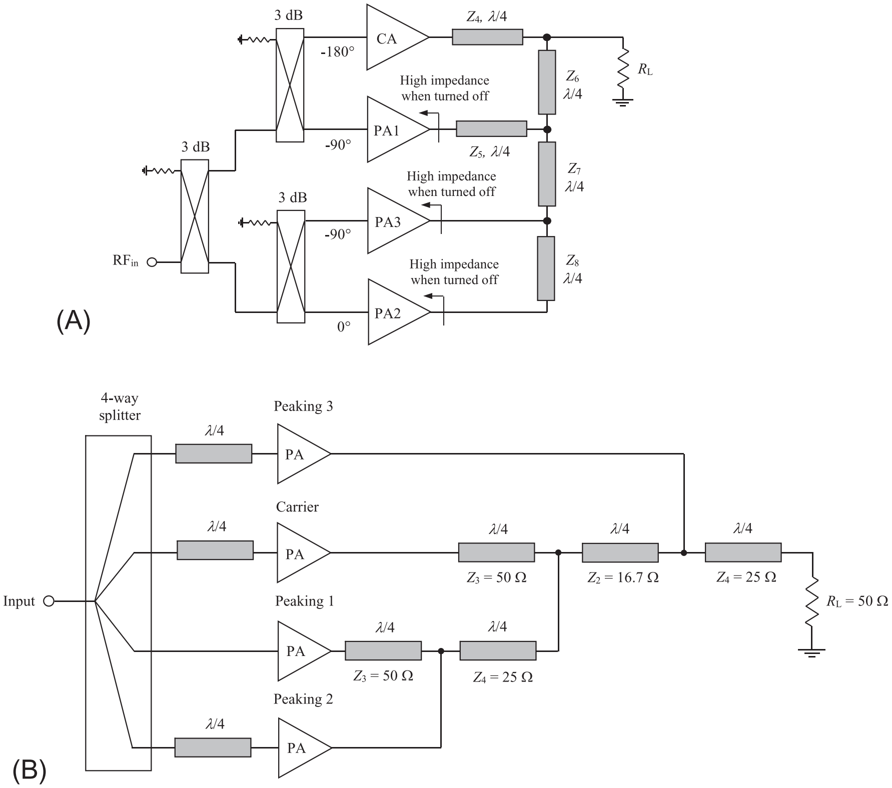


FIG. 11.27

Comparative measured performance of (A) 100-W GaN HEMT and (B) 300-W LDMOSFET four-stage Doherty amplifiers.

in Chapter 4. The input dividing network includes three 90-degree hybrid couplers. Fig. 11.27B shows the simulated drain efficiency performance versus output power when the peak power of 52.7 dBm with a drain efficiency of 72.5% was achieved at an operating frequency of 2.14 GHz using a DC-supply voltage of 28 V, with a high efficiency exceeding 50% down to 41 dBm (~12 dB power backoff). The measured drain efficiency of 52% was obtained at an average output power of 47 dBm (50 W) with a power gain of 12 dB for a single-carrier 5-MHz WCDMA signal with a *PAR* of 6.5 dB.

Fig. 11.28A shows the schematic of the modified four-stage Doherty configuration with the device size ratio of 1:1:1:1, where one carrier and three peaking amplifiers are combined in a four-stage Doherty configuration providing the maximum backoff peak efficiency point of −12 dBc.[77] Here, the input power dividing circuit includes also three quadrature couplers to split equally input power over the carries and peaking amplifiers and to provide the required phase shifts between the carrier and peaking amplifiers, but with extended number of the quarterwave lines in the load network. Another modification of the four-stage DA with equal-size devices using a four-way equal-power input splitter and three quarterwave lines for the corresponding phase compensation is shown in Fig. 11.28B.[78] As an alternative, the input circuit can also be based on three quadrature couplers,



3 dB
CA
-180°
Z_4, $\lambda/4$
Z_6
$\lambda/4$
R_L
High impedance
when turned off
PA1
-90°
Z_5, $\lambda/4$
3 dB
Z_7
$\lambda/4$
High impedance
when turned off
3 dB
PA3
-90°
RF$_{in}$
High impedance
when turned off
Z_8
$\lambda/4$
PA2
0°
(A)
4-way
splitter
Peaking 3
$\lambda/4$
PA
Carrier
$\lambda/4$
PA
$\lambda/4$
$Z_3 = 50\ \Omega$
$\lambda/4$
$Z_2 = 16.7\ \Omega$
$\lambda/4$
$Z_4 = 25\ \Omega$
Input
$R_L = 50\ \Omega$
Peaking 1
PA
$\lambda/4$
$Z_3 = 50\ \Omega$
$\lambda/4$
$Z_4 = 25\ \Omega$
Peaking 2
$\lambda/4$
PA
(B)

FIG. 11.28

Modified four-stage Doherty amplifier architectures.

but with an additional quarterwave line connected to the carrier amplifier to provide the corresponding phase compensation. For convenience of the practical implementation, both the second and third peaking amplifiers were supplemented by two series quarterwave line with different characteristic impedances at their outputs, thus resulting in nine quarterwave lines in total in the load network. As a result, an average output power of 50.2 dBm with a drain efficiency over 59% was measured within the frequency bandwidth of 925–960 MHz using two balanced 50-V LDMOSFET devices at a concurrent transmission of a 26-MHz LTE and GSM signals with a *PAR* of 8 dB.[78]

11.6 Inverted Doherty amplifiers

Fig. 11.29 shows the schematic diagram of an inverted DA configuration with an impedance inverter based on a quarterwave line connected to the output of the peaking amplifier. Such architecture can be very helpful if it is easier in a low-power region to provide a short circuit rather than an open circuit at the output of the peaking amplifier, which depends on the characteristic of the transistor. The quarterwave line can be implemented in a compact form suitable for use in mobile applications.[79] In this case, at low-power levels, a quarterwave line is used to transform very low output impedance after the offset line to high impedance seen from the load junction. In particular, by taking into account the device package parasitic elements of the peaking amplifier, an optimized output matching circuit and a proper offset line are designed to provide the maximum output power from the carrier device.[80] At a high-power level, for the matched phase difference between identical carrier and peaking amplifiers, the load impedances seen by each amplifier after the offset lines are identical, and the impedance-transforming quarterwave line is used to match the parallel-connected carrier and peaking amplifiers with a 50-Ω load. By applying a four-carrier WCDMA signal, a *PAE* of 32% with an *ACLR* of -30 dBc at an average output power level as high as 46.3 dBm was achieved for an inverted 2.14-GHz LDMOSFET DA. This provides a 9.5% improvement in efficiency and 1-dB improvement in the output power under the same *ACLR* conditions as for the balanced Class-AB operation using the same devices.[81] For a 64-QAM modulated signal with a 24-MHz channel bandwidth, a *PAE* higher than 31% with a 0.5-dB output power flatness at 27 dBm was achieved across a frequency bandwidth of 2.4–2.5 GHz with an *ACLR* better than -40 dBc.[82]

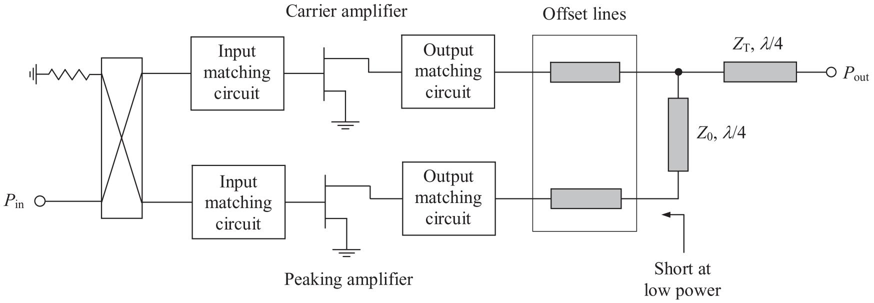
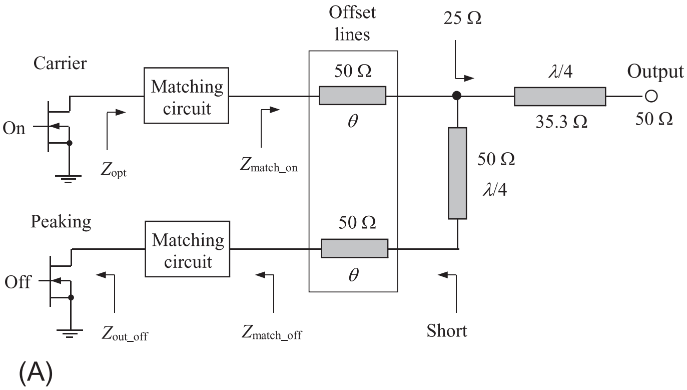


FIG. 11.29

Schematic diagram of inverted Doherty amplifier.

To better understand the operation principle of an inverted DA, consider separately the load network shown in Fig. 11.30A, where the peaking amplifier is turned off. In a low-power region, the phase adjustment of the offset line with an electrical length θ causes the peaking amplifier to be short-circuited (ideally equal to 0 Ω), and the matching circuit in conjunction with offset line provides the required impedance transformation from 25 Ω to the optimum high impedance Z_{opt} seen by the carrier device output at the 6-dB power backoff, as shown in Fig. 11.30B, where the optimum inductive impedance Z_{opt} at fundamental corresponds to a Class-E mode. In this case, the short circuit at the end of the quarterwave line operating as an impedance inverter transforms to the open circuit at its input so that it prevents power leakage to the peaking path when the peaking transistor is turned off. In a high-power region, both the carrier and peaking amplifiers are operated in a 50-Ω environment in parallel, and the output quarterwave line with the characteristic impedance of 35.3 Ω transforms the obtained 25 Ω to the required 50-Ω load.

In a Doherty configuration, both the Class-AB carrier and Class-C peaking amplifiers are not fully isolated from each other. This can result in a serious problem to robustly design the optimum load impedance shift presented to both transistors for high efficiency and low distortion.[83] From the load-pull



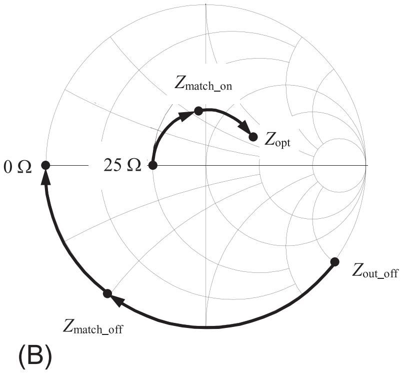


FIG. 11.30

Load-network schematic and impedances.

measurements for a unit-cell 28-V GaAs HJFET device, it was observed that, to obtain high efficiency and low distortion, the carrier amplifier load impedance should change from the maximum efficiency point to the maximum output power point at Class-AB, while the peaking amplifier load impedance should vary from the small-signal gain point to the maximum output power point in Class-C.[84] In this case, the load impedance corresponding to the maximum efficiency point is lower than the load impedance corresponding to the maximum output power point. An inverted Doherty architecture can be suitable to realize the carrier amplifier load impedance variation from lower impedance to higher impedance in accordance with the increase of the input power level. The external input and output matching circuits are necessary to optimize the load impedance shift presented to both the carrier and peaking amplifiers as a function of the input power level. As a result, a drain efficiency of 42% at an output power of 49 dBm (around the 6-dB backoff point) was achieved for a two-carrier WCDMA signal of 2.135 and 2.145 GHz with an IM_3 of -37 dBc.

To improve efficiency of the inverted DA at significant power backoff, an asymmetric configuration is useful for implementation. In this case, the most convenient configurations represent a three- or four-way inverted DA when the devices of the same size are used, with one in a carrier amplifier and two or three in a peaking amplifier, each having a quarterwave line connected to the output of the corresponding amplifier to transform a short-circuit impedance condition at the amplifier output to an open-circuit impedance condition seen by the carrier path.[85, 86] Fig. 11.31 shows the block schematic of an inverted high-power three-way DA where the carrier and peaking amplifiers are matched to 25 Ω at a high input power level, while the load impedance for the carrier amplifier is 8.3 Ω at low input power level, and a quarterwave transmission line at each output of the peaking amplifier is used to minimize power leakage from the carrier amplifier when both peaking amplifiers are turned off.[87] In this case, by using three 200-W Cree GaN HEMT devices, a saturated output power of 600 W and peak drain efficiency more than 57% over the frequency range of 1.9–2.2 GHz were achieved for a pulsed signal with 10% duty ratio. At the same time, an average output power of 49.5 dBm with a drain efficiency of 40% at 1.92 and 2.025 GHz was measured for a single-carrier 10-MHz LTE signal with an *ACLR* lower than -47 dBc after DPD linearization. Similarly, a three-way DA based on high-power LDMOSFET

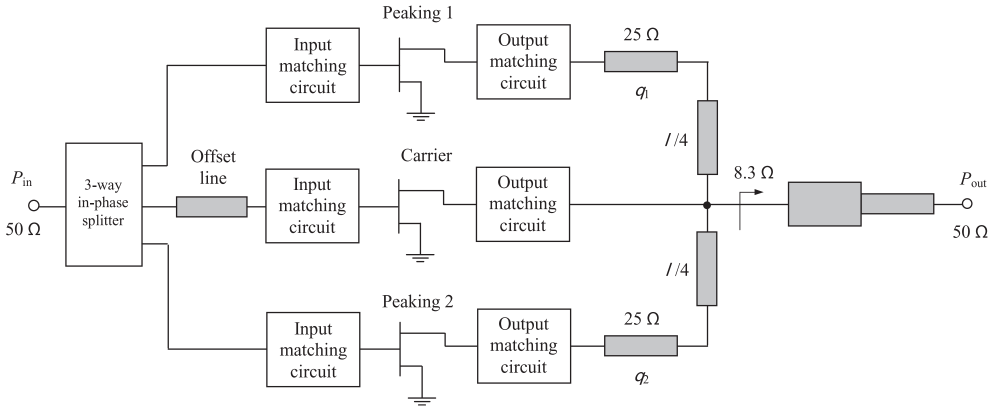


FIG. 11.31

Block schematic of high-power three-way inverted Doherty amplifier.

devices achieved greater than 45% efficiency with a power gain over 15 dB and an *ACLR* better than −55 dBc after DPD linearization at an average output power of 48.7 dBm for a single-carrier WCDMA signal with a *PAR* of 6.5 dB across the frequency band of 2110–2170 MHz.[88]

Fig. 11.32 shows the three-stage inverted DA configuration, where the quarterwave transmission lines are added to the outputs of the carrier and two peaking amplifiers to provide a proper load modulation ratio to obtain three efficiency peaking points.[89] Here the offset lines are necessary to provide short-circuit impedance conditions at their outputs. The half-wave transmission line in the input path of the carrier amplifier is used to compensate for the delay provided by the output load network. The characteristic impedances of the quarterwave transmission lines are optimized to provide a high efficiency over wide output power backoff range. If the device size ratio of the carrier, first peaking, and second peaking amplifiers is $1{:}m_1{:}m_2$, respectively, the characteristic impedances of the quarterwave transmission lines at the full power loading condition can be obtained by

$$Z_T = Z_1\sqrt{\frac{1}{1+m_1+m_2}}, \tag{11.21}$$

$$Z_4 = Z_1\frac{Z_3}{Z_2}\sqrt{\frac{1}{m_1}}, \tag{11.22}$$

$$Z_5 = Z_1\frac{Z_3}{Z_2}\sqrt{\frac{1}{m_2}}, \tag{11.23}$$

assuming the same 50-Ω loading conditions for the standard load and the carrier and peaking amplifiers at full loading conditions. As a result, for the same device sizes for the carrier and peaking amplifiers when $m_1 = m_2 = 1$, $Z_2 = Z_3 = 50\,\Omega$, and $Z_1 = 70\,\Omega$, from Eqs. (11.21) to (11.23), it follows that

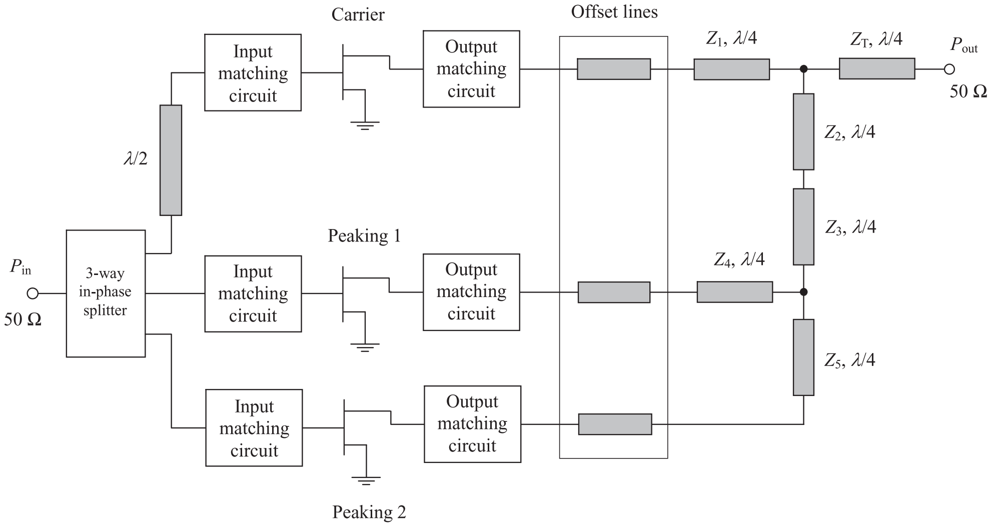

Carrier
Offset lines
Z_1, λ/4
Z_T, λ/4
P_{out}
50 Ω
Input matching circuit
Output matching circuit
λ/2
Z_2, λ/4
Z_3, λ/4
Peaking 1
Z_4, λ/4
P_{in}
50 Ω
3-way in-phase splitter
Input matching circuit
Output matching circuit
Z_5, λ/4
Input matching circuit
Output matching circuit
Peaking 2

FIG. 11.32

Schematic diagram of three-stage inverted Doherty amplifier.

$Z_T = 40.4\,\Omega$ and $Z_4 = Z_5 = 70\,\Omega$, respectively. In this case, the drain efficiency for a single-carrier 2.14-GHz WCDMA signal with a *PAR* of 10.5 dB can be improved by 5% over wide range of output powers.

Fig. 11.33A shows the block schematic of a modified inverted three-stage Doherty configuration with the device size ratio of 1:1:1, where it is enough to use only three quarterwave transmission lines in the output power combiner. Here the input in-phase three-way divider includes a half-wave transmission line in the carrier amplifying path and a quarterwave transmission line in the first peaking amplifying path for phase compensation. Both carrier and peaking PAs include the input matching circuits, whose configurations fully depend on the corresponding device impedances for particular applications to match to 50-Ω source. The offset lines are necessary to provide low impedances at their outputs for peaking amplifiers when they are turned off. The carrier amplifier is turned on only to provide

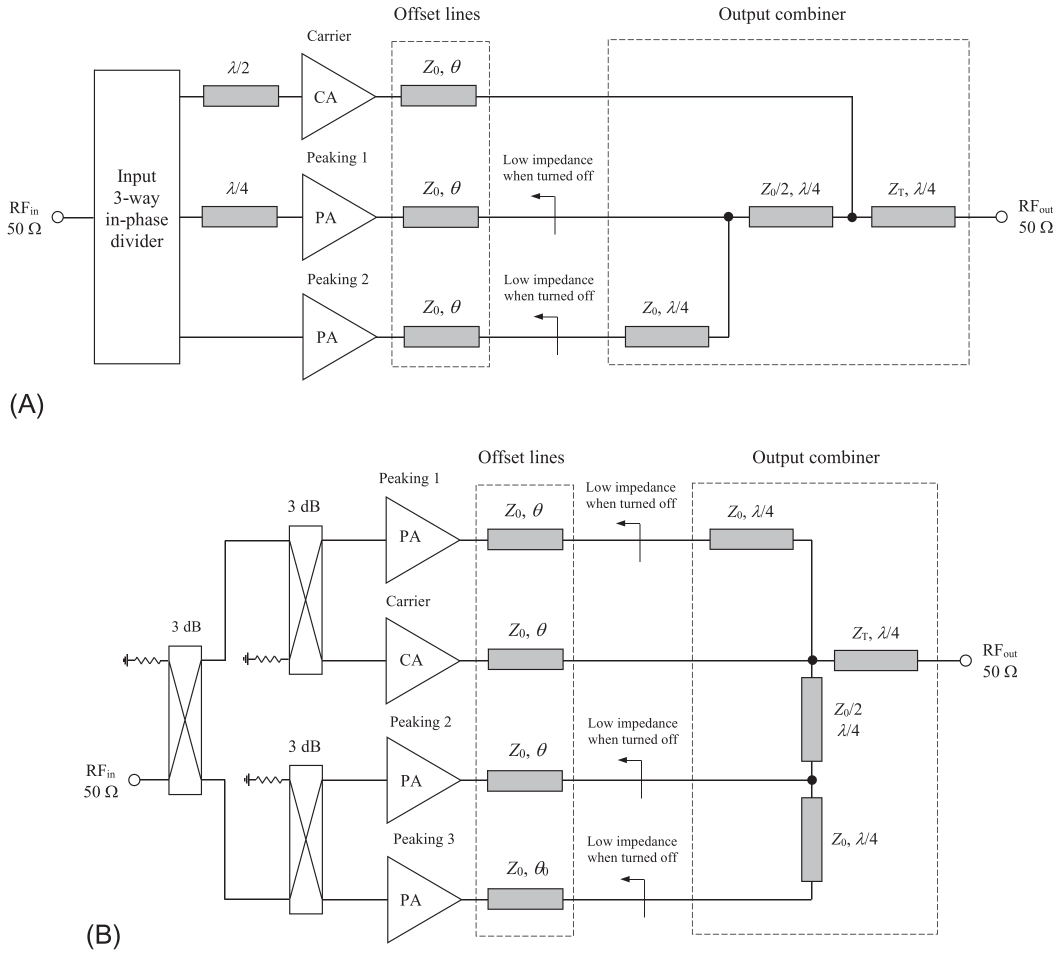

Offset lines
Output combiner
Carrier
λ/2
CA
Z_0, θ
Input 3-way in-phase divider
Peaking 1
λ/4
PA
Low impedance when turned off
$Z_0/2$, λ/4
Z_T, λ/4
RF_{in} 50 Ω
RF_{out} 50 Ω
Peaking 2
Z_0, λ/4
(A)
Offset lines
Output combiner
Peaking 1
3 dB
PA
Z_0, θ
Low impedance when turned off
Z_0, λ/4
Carrier
3 dB
CA
Z_T, λ/4
RF_{out} 50 Ω
$Z_0/2$ λ/4
Peaking 2
3 dB
RF_{in} 50 Ω
Peaking 3
Z_0, θ_0
Z_0, λ/4
(B)

FIG. 11.33

Modified three- and four-stage inverted Doherty amplifier architectures.

efficiency peak at maximum power backoff when both peaking amplifiers are turned off, and both carrier and first peaking amplifiers are turned on to provide an intermediate efficiency peak. In this case, the output matching circuit of the carrier amplifier in conjunction with the offset line should provide the impedance transformation when the high impedance is seen by the current source of the carrier transistor. If necessary, a half-wave transmission line in the carrier path can be moved from the input to the output combiner for convenience of practical implementation.

Fig. 11.33B shows the block schematic of an inverted four-stage Doherty configuration with the device size ratio of 1:1:1:1 where three 90-degree directional couplers are used at the input to equally split the input signal over four amplifying paths.[90] When all three peaking amplifiers are turned off, an efficiency peak occurs at −12 dBc power backoff, similar to the conventional four-stage DA shown in Fig. 11.25. An efficiency peak at power level between the maximum power and −6 dB power backoff can be achieved by turning on the third peaking amplifier when both carrier and remaining two peaking amplifiers are turned on. In a 50-Ω environment, the output impedance transformer with the characteristic impedance of $Z_T = 5\sqrt{2Z_0}/2$ can represent either a single quarterwave line or multisection line depending on the output power (the higher output power, the larger impedance transformation ratio) and frequency bandwidth requirements. Besides, a good compromise between efficiency and linearity can be achieved because, in this case, the carrier amplifier ideally sees higher impedance, whereas the first peaking amplifier sees lower impedance at −6 dB backoff when the second- and third-peaking amplifiers are turned off.

11.7 Integrated and monolithic Doherty amplifiers

At microwave and millimeter-wave frequencies, the transmission-line DA is usually implemented into the MMIC by using a pHEMT, GaN HEMT, or CMOS process. For example, a fully integrated *Ku*-band MMIC DA using a 0.25-μm pHEMT technology achieved a two-tone PAE of 40% at 17 GHz, whereas a single-tone *PAE* of 38.5% at 1-dB gain compression point was measured for a 20-GHz MMIC DA implemented in a 0.15-μm pHEMT process for use in digital satellite communication (DSC) systems.[17, 91] By using a 0.13-μm RF CMOS technology, a transmission-line MMIC DA based on cascode configuration of the carrier and peaking amplifiers achieved a saturation output power of 7.8 dBm from a DC-supply voltage of 1.6 V at an operating frequency of 60 GHz for use in wireless personal area network (WPAN) transceivers.[92] However, the efforts to directly apply the Doherty technique to the design of PA integrated circuits with a high level of integration at lower frequencies face difficulties because the physical size of the quarterwave transmission lines is too large in this case. For example, for an FR4 substrate with effective dielectric permittivity of $\varepsilon_r = 3.48$, the geometrical lengths of the quarterwave transmission lines are 48, 19, and 8.7 mm at the operating frequencies of 900 MHz, 2.4 GHz, and 5.2 GHz, respectively. Therefore, one of the acceptable solutions for the fabrication of small-size DA MMICs intended to operate in cellular transmitter systems is to replace each quarterwave line in the input combining circuit and output impedance transformer by its low-pass Π-type lumped-distributed equivalent with a short-length series transmission line and two shunt capacitors connected to its both ends.[93, 94] Additionally, simple and small-size second-harmonic termination circuits can be realized with integrated metal-insulator-metal (MIM) capacitors and bondwires at the end of the carrier and peaking amplifier collectors.[93] High substrate loss can be minimized and high level of integration to implement the DA in a CMOS process can be provided if the branch-line coupler and quarterwave impedance transformer are fully substituted by their lumped equivalents.[95]

11.7.1 Equivalent circuits with lumped elements and transmission lines

For integrated and MMIC applications, the overall size of the quadrature branch-line hybrids with quarterwave transmission lines is too large. Therefore it is attractive to replace each quarterwave branch line with the combination of a short-length transmission line and two shunt capacitors providing similar bandwidth properties. In this case, consider the admittance matrix $[Y_a]$ for a quarterwave transmission line shown in Fig. 11.34A and the admittance matrix $[Y_b]$ for a Π-type circuit consisting of a short-length transmission line with the two shunt capacitors shown in Fig. 11.34B, which are respectively given by

$$[Y_\mathrm{a}] = \frac{1}{jZ_0}\begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix}, \tag{11.24}$$

$$[Y_\mathrm{b}] = \frac{1}{jZ\sin\theta}\begin{bmatrix} \cos\theta - \omega CZ\sin\theta & -1 \\ -1 & \cos\theta - \omega CZ\sin\theta \end{bmatrix}, \tag{11.25}$$

where Z_0 is the characteristic impedance of a quarterwave transmission line, Z and θ are the characteristic impedance and electrical length of a shortened transmission line, respectively, and C is the shunt capacitance. By equating the corresponding Y-parameters in Eqs. (11.24) and (11.25), the simple analytical ratios between the circuit parameters can be obtained as

$$Z = \frac{Z_0}{\sin\theta}, \tag{11.26}$$

$$C = \frac{\cos\theta}{\omega Z_0}, \tag{11.27}$$

from which it follows that the length of the transmission line can be made much shorter by increasing its characteristic impedance Z. For example, when choosing the electrical length of $\theta = 45°$, the characteristic impedance of the transmission line increases by a factor of $\sqrt{2}$.

The circuit schematic of a reduced-size branch-line quadrature hybrid coupler is shown in Fig. 11.34C.[96] Compared with the conventional branch-line hybrid coupler with the characteristic

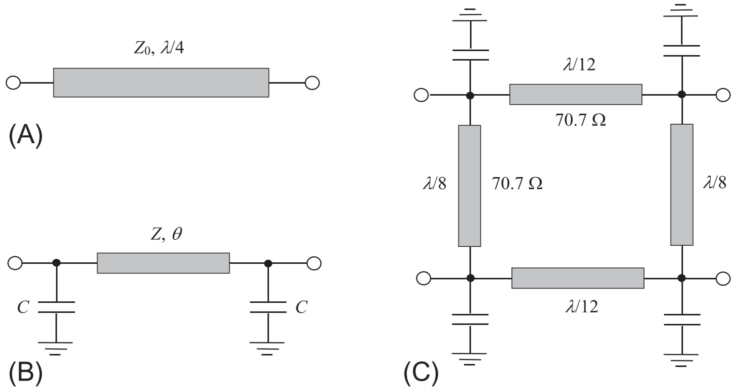


FIG. 11.34

Reduced-size branch-line quadrature hybrid.

impedances of its branch and main lines of Z_0 and $Z_0/\sqrt{2}$, respectively, the circuit parameters of the reduced-size branch-line hybrid coupler are obtained by

$$\theta_1 = \sin^{-1}\left(\frac{Z_0}{Z}\right), \tag{11.28}$$

$$\theta_2 = \sin^{-1}\left(\frac{Z_0}{Z\sqrt{2}}\right), \tag{11.29}$$

$$\omega C Z_0 = \sqrt{1-\left(\frac{Z_0}{Z}\right)^2} + \sqrt{2-\left(\frac{Z_0}{Z}\right)^2}, \tag{11.30}$$

where θ_1 and θ_2 are the electrical lengths of the shunt branch line and series main line, respectively. For a particular case of the standard characteristic impedance $Z_0 = 50\,\Omega$, the characteristic impedance and electrical lengths of the transmission lines are defined as $Z = Z_0\sqrt{2}$, $\theta_1 = 45°$, and $\theta_2 = 30°$, as shown in Fig. 11.34C. The experimental results for a 25-GHz reduced-size branch-line quadrature hybrid coupler show that its bandwidth performance is slightly narrower than that of the conventional quarterwave hybrid coupler, but its overall size is more than 80% smaller.

In a general case, when the electrical length of the series transmission line differs from 90 degrees, as shown in Fig. 11.35A, the electrical length and characteristic impedance of the shortened transmission line and the shunt capacitances of its Π-type low-pass equivalent, as shown in Fig. 11.35B, can be obtained from the following system of two trigonometric equations:

$$Z_T = Z_0 \frac{\sin\theta}{\sin\theta_T}, \tag{11.31}$$

$$C_T = \frac{\cos\theta_T - \cos\theta}{\omega Z_T \sin\theta_T}. \tag{11.32}$$

Note that the derivation process can be simplified if the characteristic impedance Z_T can be set in advanced based on the width limitation of the microstrip line to be implemented. Similar ratios between the parameters of the series transmission line and a T-type low-pass equivalent circuit consisting of a

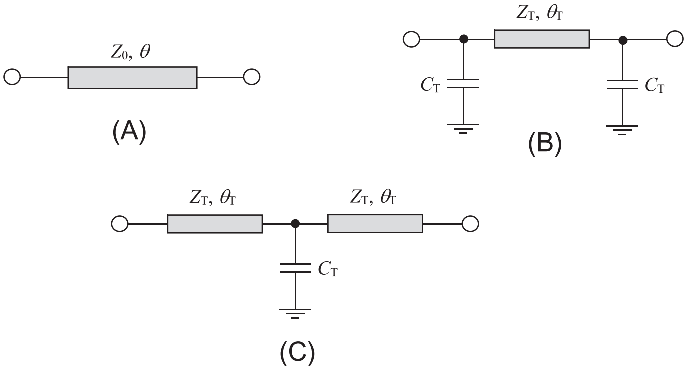


FIG. 11.35

Transmission line and its mixed lumped-distributed equivalents.

shunt capacitance and two shortened series transmission lines with higher characteristic impedances, as shown in Fig. 11.35C.

In a classical DA with a Wilkinson power divider to split input signal between the carrier and peaking amplifying paths, an additional quarterwave transmission line at the input of the peaking amplifier is required to compensate for the 90-degree phase shift caused by the quarterwave transmission line at the output of the carrier amplifier. However, generally its electrical length may differ from 90 degrees because the input reactances of the carrier and peaking devices vary depending on the gate bias voltage. Similarly, due to the presence of additional offset lines at the outputs of the carrier and peaking devices, the overall length of the output impedance inverter will be longer than a quarter wavelength. In this case, by equating the *ABCD*-matrices of the transmission line with the characteristic impedance Z_0 and electrical length of θ, as shown in Fig. 11.36A, and a Π-type low-pass lumped circuit consisting of a series inductance L and two shunt capacitors C, as shown in Fig. 11.36B, according to

$$\begin{bmatrix} \cos\theta & jZ_0\omega L \\ j\sin\theta/Z_0 & \cos\theta \end{bmatrix} = \begin{bmatrix} 1-\omega^2 LC & j\omega L \\ j\omega C(2-\omega^2 LC) & 1-\omega^2 LC \end{bmatrix}, \tag{11.33}$$

the ratio of the circuit parameters corresponding to the transmission line and its Π-type low-pass lumped equivalent can be obtained as a function of electrical length θ by

$$\omega L = Z_0 \sin\theta, \tag{11.34}$$

$$\omega C = \frac{1-\cos\theta}{Z_0\sin\theta}. \tag{11.35}$$

Similarly, by considering the *ABCD*-matrices of the transmission line and a T-type low-pass lumped circuit consisting of a shunt capacitance C and two series inductances L, as shown in Fig. 11.36C, and equating the corresponding elements of both matrices, the ratio between the circuit elements can be written as

$$\omega L = \frac{Z_0(1-\cos\theta)}{\sin\theta}, \tag{11.36}$$

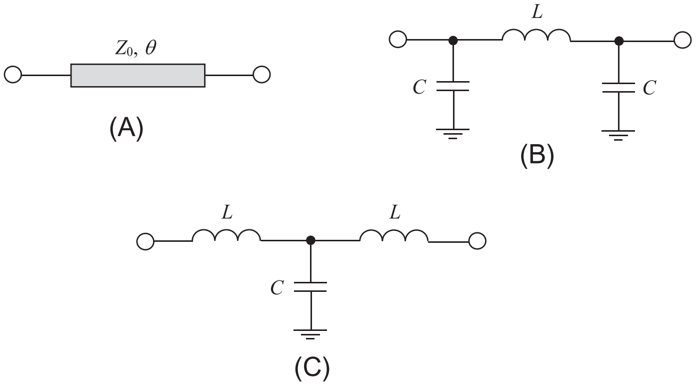


FIG. 11.36

Transmission line and its lumped equivalents.

$$\omega C = \frac{\sin\theta}{Z_0}. \tag{11.37}$$

For a quarterwave transmission line with $\theta = 90°$, Eqs. (11.34) and (11.35), and Eqs. (11.36) and (11.37) become identical and can be rewritten in a general form as

$$Z_0 \omega C = \frac{Z_0}{\omega L} = 1, \tag{11.38}$$

where Z_0 is the characteristic impedance of the quarterwave transmission line.

To further reduce the MMIC size, the transmission lines can be fully replaced by the lumped planar inductors. The lumped-element equivalent circuit of a transmission-line branch-line hybrid coupler is shown in Fig. 11.37A.[97] This circuit has also some additional advantages when each its section can work as a separate impedance transformer, a low-pass filter, and a phase shifter. The circuit can be diced into four separate sections and cascaded for the desired transmission characteristics. The circuit analysis indicates that various types of networks fulfill the conditions required for an ideal hybrid. Therefore greater design flexibility in the choice of the hybrid structure and performance is possible. Several possible single-section two-branch hybrid options are shown in Fig. 11.37.[98] In this case, it should be noted that not only a low-pass section but also a high-pass section can be respectively used. In the latter case, the high-pass *LC* section is considered an equivalent single-frequency replacement for a 270-degree transmission line.[99] Fig. 11.37C and D illustrate the use of both low-pass and high-pass sections simultaneously whereas only high-pass sections compose the hybrid shown in Fig. 11.37E. The performance of the hybrid couplers shown in Fig. 11.37B and E are very similar to those of the classical single-section branch-line hybrid coupler. The bandwidth performances of the hybrid couplers shown in Fig. 11.37C and D are narrower because the power balance between their output ports is much narrower. Broader bandwidth and lower output impedances can be provided with a two-section three-branch lumped-element hybrid coupler. Similarly, the input in-phase transmission-line two-way Wilkinson divider can be replaced by its lumped equivalent, where a Π-type low-pass *LC* circuit is used in its each branch.

11.7.2 Integrated Doherty amplifiers

Fig. 11.38 shows an example of the simplified schematic of a two-stage lumped DA, where the output quarterwave transmission line connected to the carrier amplifier output and operated as an impedance transformer and the input phase-shifting quarterwave transmission line connected to the peaking amplifier input are replaced by equivalent Π-type low-pass 90 degrees and high-pass 270 degrees lumped circuits included into the carrier amplifying path, respectively. In addition, the output quarterwave transformer is replaced by an L-type high-pass matching section, whereas the two L-type low-pass matching circuits are used to provide the input matching of the carrier and peaking amplifiers. At the carrier amplifier input path, the right-hand shunt capacitor as a part of the equivalent Π-type high-pass phase shifter and the shunt capacitor as a part of the input L-type low-pass matching circuit can be combined into a single shunt inductor (or it may be a capacitor depending on the values of the shunt inductance of the phase shifter and shunt capacitance of the L-type matching circuit).

In handset monolithic applications, the transmission-line quarterwave impedance transformer and offset line are implemented with lumped elements, representing the equivalent Π-type low- and

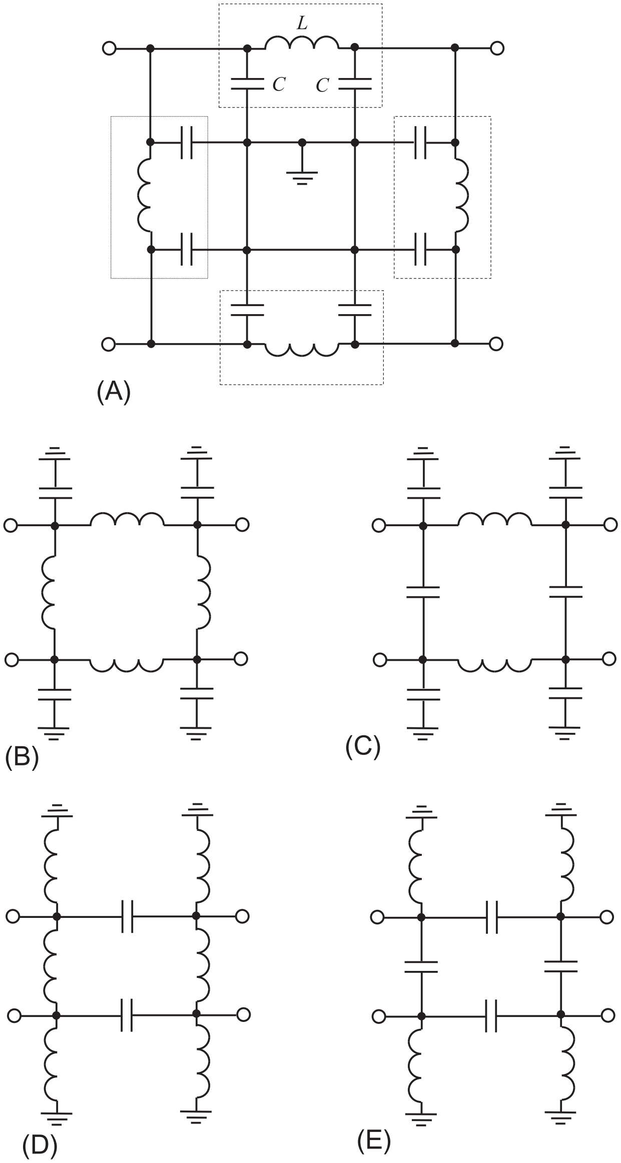


FIG. 11.37

Equivalent circuits of lumped *LC*-type hybrid coupler.

high-pass *LC* networks, respectively, as shown in Fig. 11.39A.[100] In this case, the load-network parameters are optimized to provide an open-circuit condition at the output of the peaking branch over broadband frequency range when the peaking amplifier is turned off. To simplify the load-network structure, the values of the inductances L_1 and L_2 are chosen so as to merge them with the corresponding

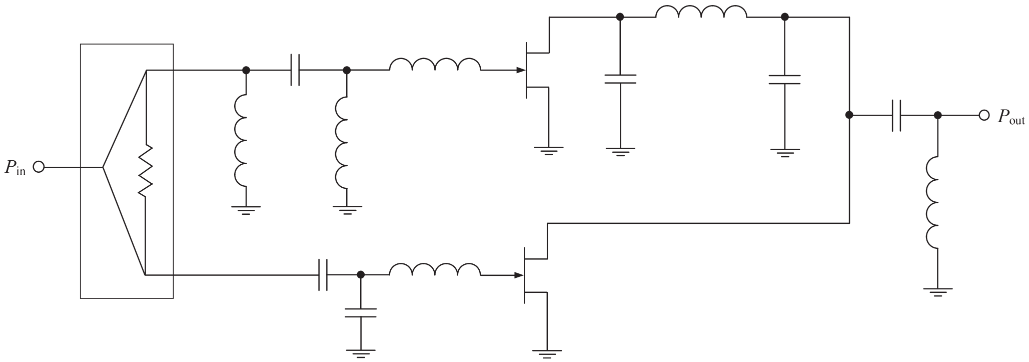


FIG. 11.38

Circuit schematic of lumped Doherty amplifier.

capacitances C_1 and C_2. Fig. 11.39B shows the circuit schematic of a 2-μm GaAs HBT DA, where all components are fully integrated on a chip. In this case, the inductors are implemented using bondwires and slab inductors, the input dividing circuits are broadband based on low-Q matching networks, and the second- and third-harmonic impedances are controlled for high efficiency across the bandwidth. The open-circuit conditions are achieved by optimizing all load-network elements, including drain bondwires and device output capacitances. For a 8.75-MHz 16-QAM m-WiMAX application with a 9.6-dB crest factor, such a lumped DA exhibits a *PAE* above 27% and an output power over 23.6 dBm across 2.2–2.8 GHz using a DPD technique. Similar DA with broadband lumped networks could provide a *PAE* over 30% at an output power of 28 dBm across 1.6–2.1 GHz for a 10-MHz LTE signal with a *PAR* of 7.5 dB.[101]

To minimize size and cost and to simplify the design complexity of a high-power integrated DA implemented in standard discrete package, a Π- or T-type low-pass *LC* circuit to equivalently replace the quarterwave transmission line can be used. An example of the discrete package implementation of an integrated DA with a T-type input phase shifter in a peaking amplifying path and a T-type impedance transformer in a carrier amplifying path using multiple series bondwires and shunt MIM capacitances is shown in Fig. 11.40A.[102] To increase the output power, an integrated solution based on four 10-W MMIC DA cells combined in parallel achieves a drain efficiency of 39.8% at an average output power of 7.5 W with an *ACLR* of −50 dBc using a DPD technique for a two-carrier 2.14-GHz WCDMA signal with a *PAR* of 7.6 dB.[103] Alternatively, it is convenient to use a Π-type low-pass *LC* circuit where the shunt capacitances are represented by the device drain-source capacitances and a series inductance is formed by the bondwire connected between the drain terminals of the carrier and peaking devices.[104] In this case, the input splitter can be similarly designed using the device gate-source capacitances and bondwire connected between the device gates including a DC-blocking capacitor, as shown in Fig. 11.40B. As a result, a maximum power gain of 15.9 ± 0.2 dB and an average drain efficiency of 47% ± 1% at 6-dB backoff from the peak output power of 50 dBm were achieved for a 10-MHz LTE signal with a *PAR* of 7.2 dB across the frequency bandwidth of 1.805–2.17 GHz using a silicon LDMOS technology in a compact package of $50 \times 50\,\text{mm}^2$.[105] To increase the frequency bandwidth, a two-stage high-pass filter to connect the carrier and peaking device outputs with an additional output matching was used, resulting in a drain efficiency over 36% with an output power higher than 41.4 dBm

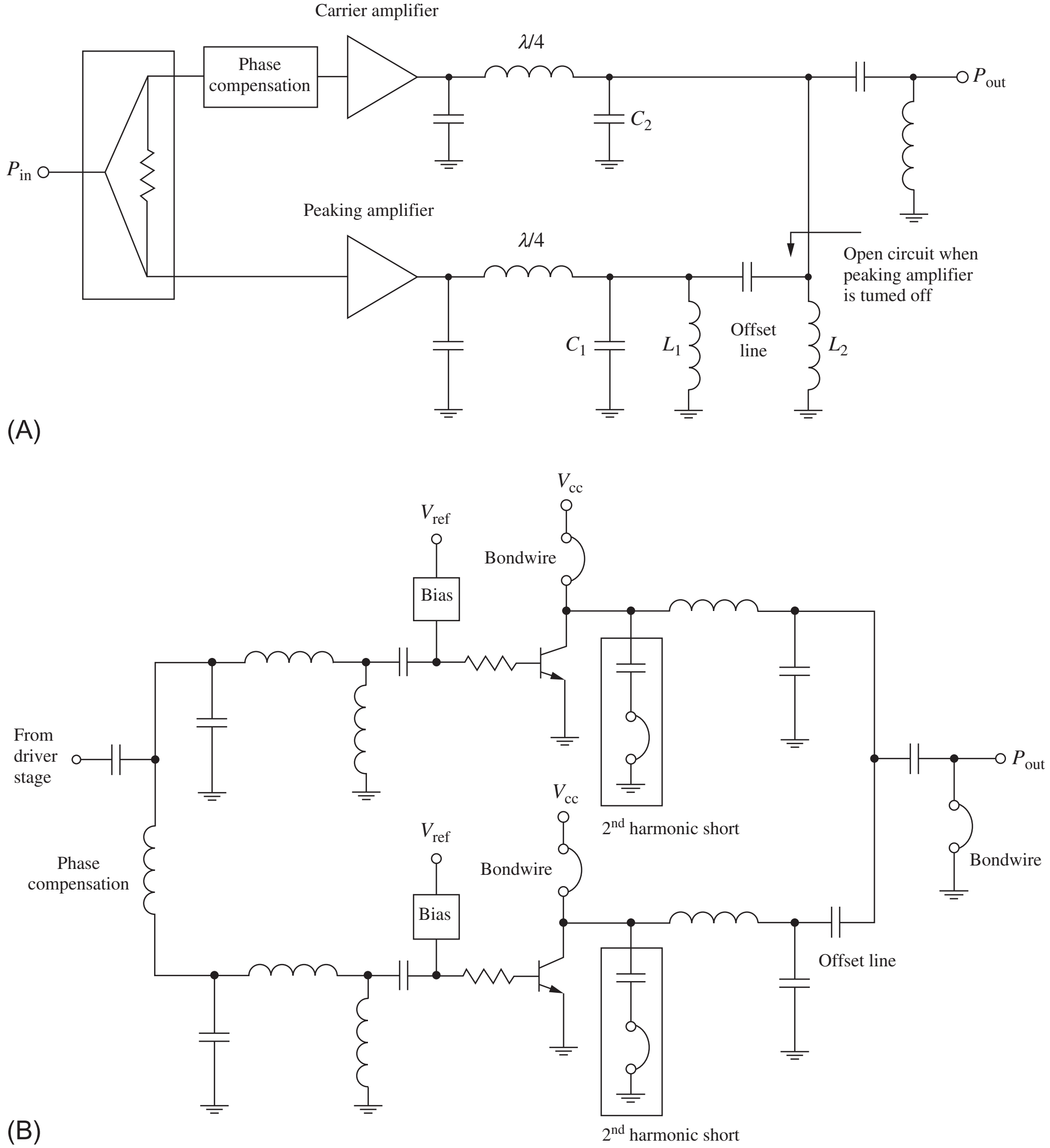

Carrier amplifier
Phase compensation
λ/4
C_2
P_{out}
P_{in}
Peaking amplifier
λ/4
Open circuit when peaking amplifier is turned off
C_1
L_1
Offset line
L_2
(A)
V_{cc}
V_{ref}
Bondwire
Bias
From driver stage
P_{out}
V_{cc}
2nd harmonic short
V_{ref}
Bondwire
Bondwire
Phase compensation
Bias
Offset line
(B)
2nd harmonic short

FIG. 11.39

Schematics of Doherty amplifiers for handset applications.

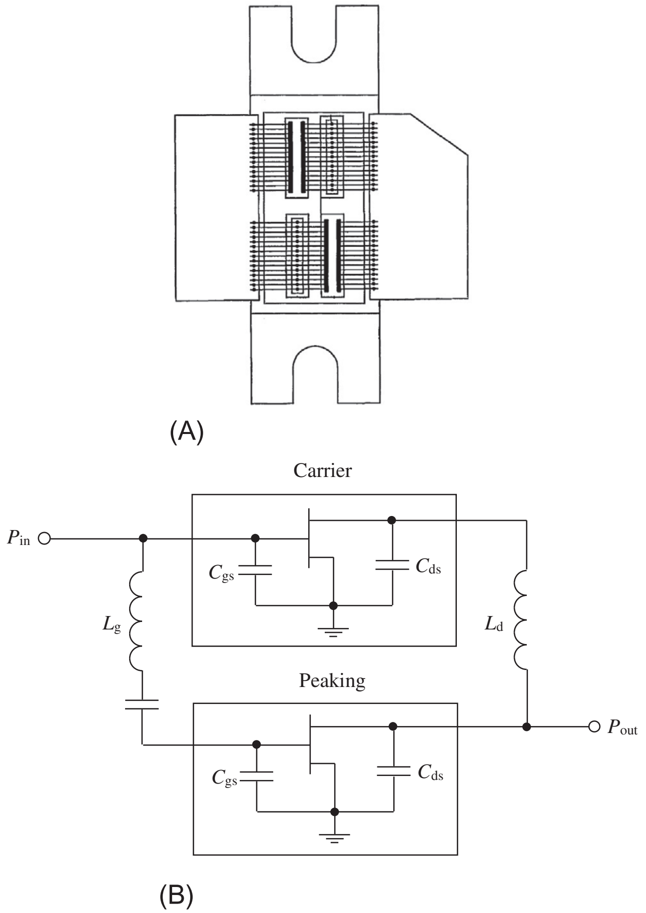


FIG. 11.40

Package integration and basic schematic of lumped Doherty amplifier.

in a frequency bandwidth of 1.8–3.2 GHz for a single-input integrated DA based on a 0.25-μm 50-V GaN HEMT technology.[106]

For massive-MIMO and small-cell applications required in 4/5G communication infrastructure systems, it is necessary to further minimize size and cost of the integrated DAs by providing higher integration capability. In this case, an integrated DA can be fully implemented on a ceramic substrate with discrete GaN HEMT dies, although its cost is sufficiently high despite the small size.[107] As an alternative, the input, interstage, and load networks can be implemented on separate GaAs Integrated Passive Device (IPD) substrates in a single package together with four discrete GaN HEMT dies.[108]

Fig. 11.41A shows the block diagram of a package-integrated DA with two-stage MMIC based on a GaN HEMT technology and two IPDs, one for the input splitter and the other for the load network including Doherty combiner and output matching for symmetric version and PCB-based input splitter

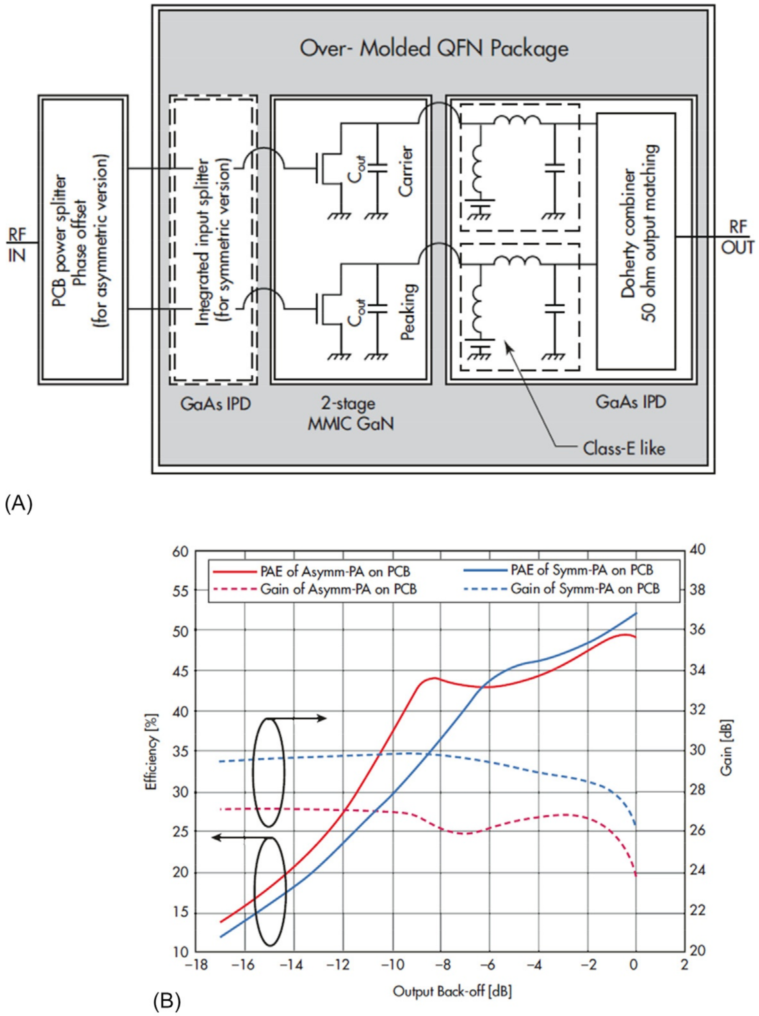

Over- Molded QFN Package
RF IN
PCB power splitter
Phase offset
(for asymmetric version)
Integrated input splitter
(for symmetric version)
GaAs IPD
C_{out}
Carrier
C_{out}
Peaking
2-stage
MMIC GaN
Doherty combiner
50 ohm output matching
GaAs IPD
Class-E like
RF OUT
(A)
PAE of Asymm-PA on PCB
Gain of Asymm-PA on PCB
PAE of Symm-PA on PCB
Gain of Symm-PA on PCB
Efficiency [%]
Gain [dB]
Output Back-off [dB]
60
55
50
45
40
35
30
25
20
15
10
40
38
36
34
32
30
28
26
24
22
20
−18
−16
−14
−12
−10
−8
−6
−4
−2
0
2
(B)

FIG. 11.41

Block diagram and performance of package-integrated inverted Doherty amplifier.[109]

and phase offset circuit for asymmetric version with the device size ratio of 1:2.[109] Both versions use a second-harmonic input short in the final stage to maximize efficiency, in conjunction with the parallel-circuit Class-E load networks for carrier and peaking PAs followed by the output combiner corresponding to the inverted Doherty structure. A 20-W asymmetric and 26-W symmetric DAs operating in a frequency band of 3.4–3.6 GHz were implemented into a small plastic package of $7 \times 7\,\mathrm{mm}^2$. In a CW mode, the saturated output power $P_{3\mathrm{dB}}$ achieves 44.3 dBm with a maximum *PAE* of 52% and a PAE of 44% at 6-dB power backoff for symmetric version, whereas the saturated output power

P_{3dB} achieves 43 dBm with a maximum *PAE* of 49% and a PAE of 44% at 8-dB power backoff for asymmetric version, as shown in Fig. 11.41B. For a single-carrier 20-MHz LTE signal with a *PAR* of 7.2 dB, a *PAE* of 43% with a power gain of 26 dB was measured at an average output power of 35 dBm for asymmetric integrated inverted DA. In a dual-input integrated symmetric DA with two GaAs IPDs for the input and load networks implemented in a plastic package of 8 × 8 mm^2, a *PAE* of 36% at 8-dB backoff from maximum output power of 44 dBm (3.5-dB gain compression) using bias adjustment between the carrier and peaking devices and a small-signal gain of 12.5 dB were measured within the frequency range of 5.5–6.5 GHz.[110]

In view of a high DC-supply voltage (up to 50 V) and a high peak output power (several tens of watt), it makes sense to use thin laminate substrate to implement the load network, thus further reducing cost too. Fig. 11.42 shows an example of the possible implementation of the integrated DA where the carrier and peaking devices are located on separate active die using GaN HEMT technology, the IPD is used for input circuit including lumped Wilkinson power divider and phase shifter where the quarter-wave transmission lines are replaced by the Π-type low-pass *LC* circuits, and the low-cost laminate substrate is used to implement the output matching circuit. An input IPD comprises the combined MIM series capacitor C_1+C_2, series spiral inductors L_1 and L_2, the combined shunt MIM capacitors C_1+C_4 and C_2+C_3 grounded through substrate vias, the ballast resistor R_0, the blocking series MIM capacitor C_b, the series spiral inductor L_3 and the combined shunt MIM capacitor C_3+C_5 grounded through substrate via. The series bondwire inductors L_4 and L_5 represent the corresponding parts of the input low-pass matching sections directly connected to the gates of the carrier and peaking devices, respectively. The bondwire inductor L_0 directly connects the drains of the carrier and peaking devices as a part of the impedance inverter, as it was proposed in Ref. 111. The magnetic coupling between the bondwire inductances L_0 and L_6 is minimized due to their orthogonal orientation to each other.

The bondwire inductor L_6 connected to the drain of the peaking device operates as a series inductor of the output low-pass matching section of a two-section output matching network. A two-section output matching circuit consists of the chip capacitor C_6 (grounded through substrate via) as a shunt element of the low-pass L-type matching section, and the series chip capacitor C_7 and shunt inductor L_7 (grounded through the substrate via) as elements of the high-pass L-type matching section. The combination of the low-pass and high-pass matching sections in a single matching network which is implemented on a laminate substrate operates as an impedance-transforming bandpass filter to suppress the low- and HF intermodulation and harmonic components simultaneously. To improve the quality factors of the inductor and to reduce the insertion loss in the output matching network, the shunt inductor L_7 and choke inductor L_{ch} are implemented as short microstrip lines. As an example, using the laminate substrate with a dielectric permittivity of 3.5 and thickness of 0.5 mm, the lengths of the microstrip lines L_{ch} and L_7 using two 20-W GaN HEMT devices for symmetric Doherty structure (or 10- and 30-W devices for 1:3 asymmetric Doherty configuration) are equal to 3 and 2 mm, respectively, whereas the width of these microstrip lines are of 0.2 mm at 3.5 GHz.

Fig. 11.43 shows the modified implementation of the integrated DA, which is used when the bondwire L_0 is too long and cannot physically be implemented as a single bondwire between two device drains. In this case, a narrow microstrip line implemented on the laminate substrate can be used, whose length and width can be adjusted depending on the required overall inductance value for L_0. Each device drain from active GaN die is connected by short bondwire to the corresponding end of this microstrip line.

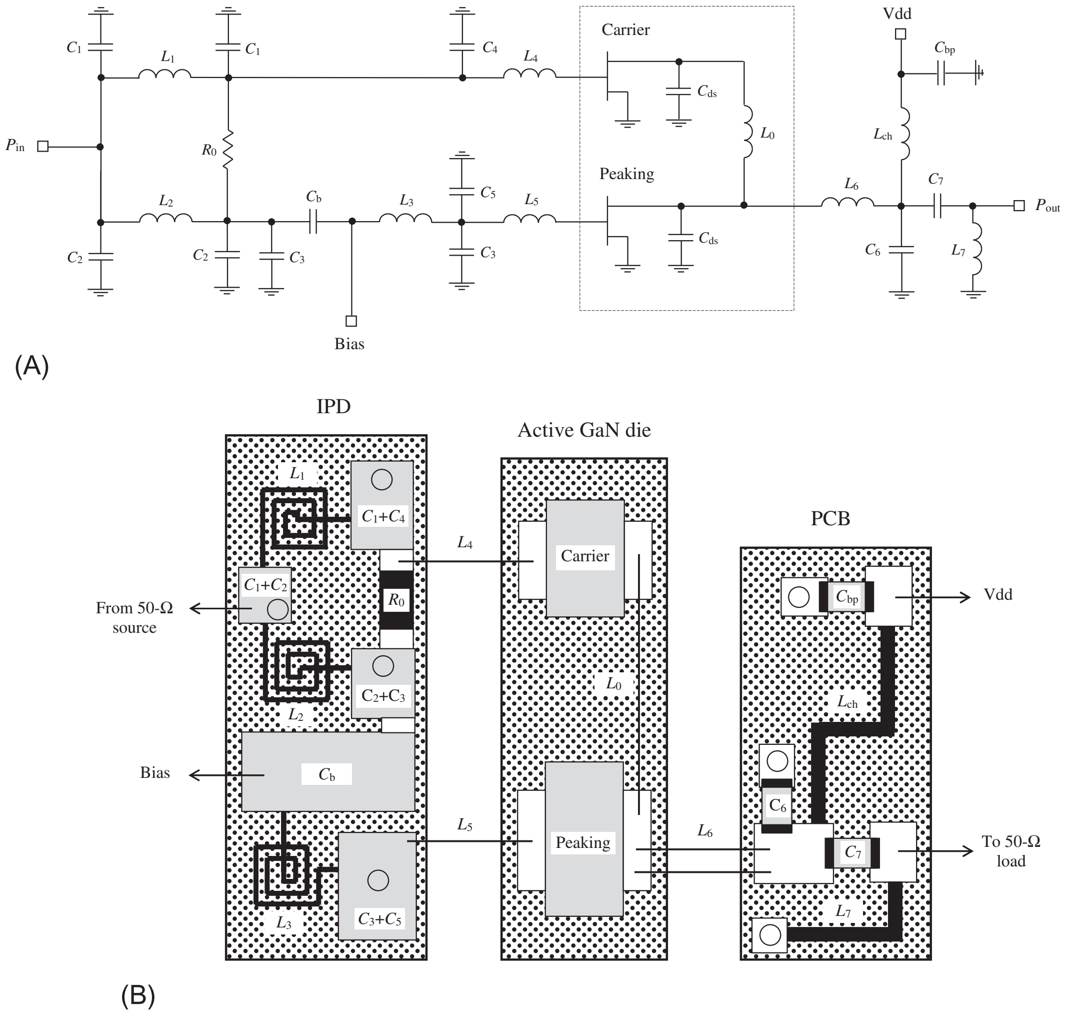

(A)
Carrier
Peaking
Vdd
C_{bp}
C_1
L_1
C_4
L_4
C_{ds}
L_0
L_{ch}
P_{in}
R_0
L_2
C_b
L_3
C_5
L_5
L_6
C_7
P_{out}
C_2
C_3
C_6
L_7
Bias
(B)
IPD
Active GaN die
PCB
C_1+C_4
C_1+C_2
C_2+C_3
C_3+C_5
From 50-Ω source
To 50-Ω load

FIG. 11.42

Schematics of integrated Doherty amplifier for sub-6-GHz cellular systems.

Fig. 11.44 shows an example of the possible implementation of the integrated inverted DA where the impedance inverter in the peaking amplifying path consists of two equal grounded shunt capacitors C_6 and transmission line TL_1. The impedance transformation at the output of the carrier device is provided by the drain-source capacitance C_{ds} and bondwire inductor L_7 and at the output of the peaking device (at high-power region when the transistor is turned on) by the drain-source capacitances C_{ds} and bondwire inductor L_6 (capacitances C_{ds} are different if the carrier and peaking devices have different number of cells), both representing an L-type low-pass LC matching section. The output impedance

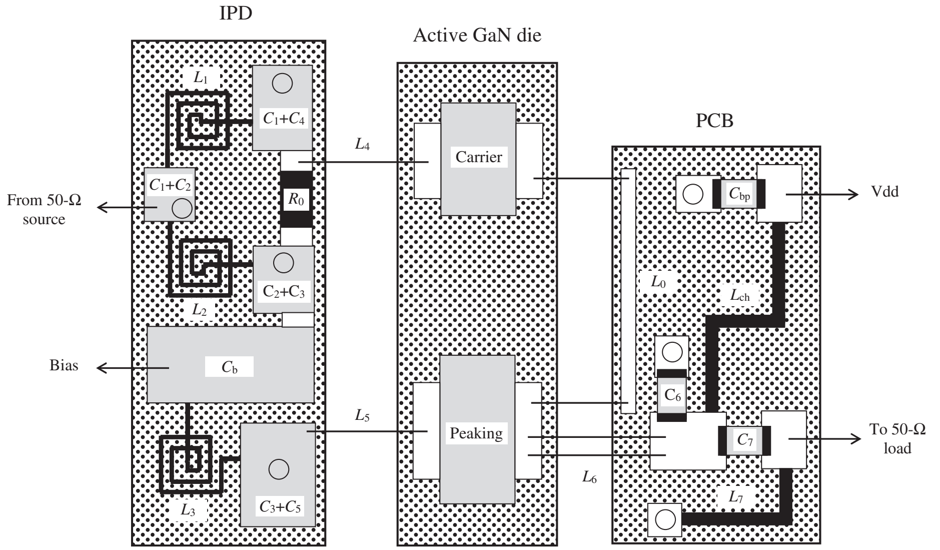

IPD
Active GaN die
PCB
L_1
C_1+C_4
L_4
Carrier
From 50-Ω source
C_1+C_2
R_0
C_{bp}
Vdd
L_2
C_2+C_3
L_0
L_{ch}
Bias
C_b
C_6
L_5
Peaking
C_7
To 50-Ω load
L_6
L_7
L_3
C_3+C_5

FIG. 11.43

Block schematic of modified integrated Doherty amplifier.

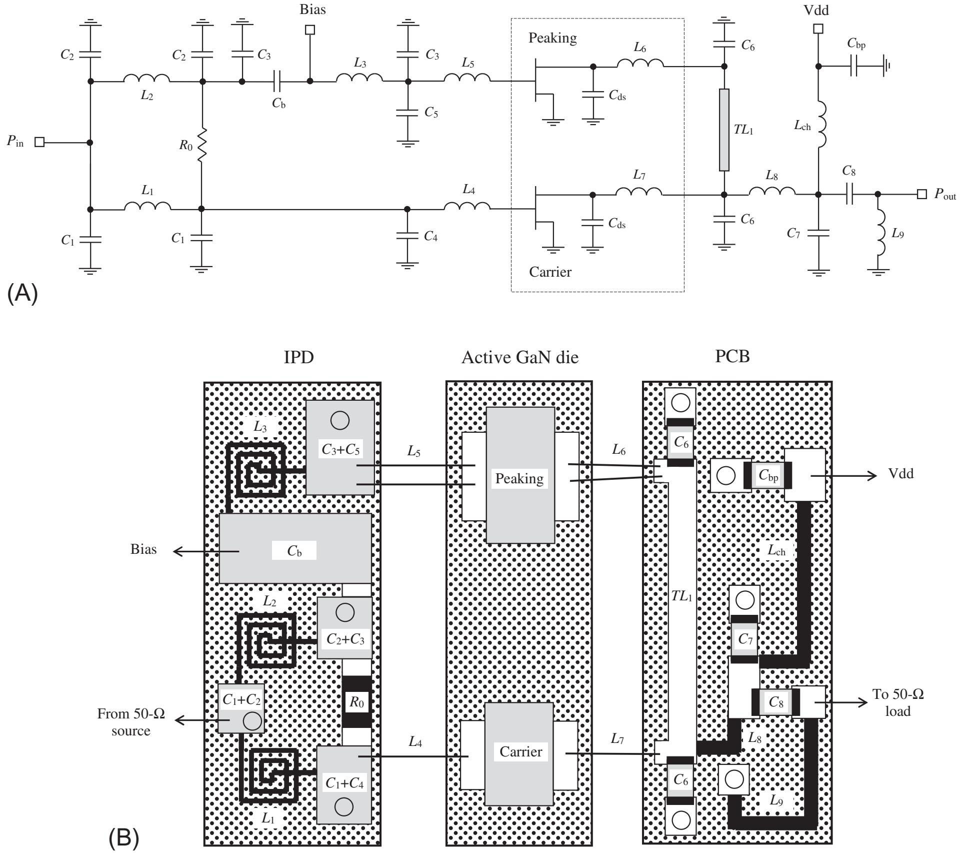

Bias
Vdd
Peaking
C_2
C_2
C_3
C_6
C_{bp}
L_6
L_2
C_b
L_3
C_3
L_5
C_{ds}
P_{in}
R_0
C_5
TL_1
L_{ch}
L_1
L_4
L_7
L_8
C_8
P_{out}
C_1
C_1
C_4
C_{ds}
C_6
C_7
L_9
Carrier
(A)
IPD
Active GaN die
PCB
L_3
C_3+C_5
L_5
L_6
C_6
Peaking
C_{bp}
Vdd
Bias
C_b
L_{ch}
TL_1
L_2
C_2+C_3
C_7
From 50-Ω source
C_1+C_2
R_0
C_8
To 50-Ω load
L_4
L_7
L_8
Carrier
C_6
C_1+C_4
L_1
L_9
(B)

FIG. 11.44

Schematics of integrated inverted Doherty amplifier for sub-6-GHz cellular systems.

transformation is provided by a two-section matching circuit representing a band-pass filter with the first low-pass matching section L_8C_7 to suppress harmonic and intermodulation components above operating bandwidth and the second high-pass matching section C_8L_9 to suppress the modulation, intermodulation, and subharmonic components below operating bandwidth. The choke inductor L_{ch} and bypass capacitor C_{bp} are used to connect the RF amplifying path with DC-feed power supply, and the value of the inductor L_{ch} can be adjusted by varying the value of the shunt capacitor C_7 to optimize the size of the output matching network. Both the impedance inverter and output matching network are implemented on a laminate substrate. In addition to lumped Wilkinson divider ($L_1C_1L_1$-$C_2L_2C_2$-R_0) and the phase compensation line ($C_3L_3C_3$) implemented on IPD, the two input low-pass matching sections (C_4L_4 for carrier device and C_5L_5 for peaking device) are used where L_4 and L_5 are implemented by bonding wires connecting the corresponding device gate to external input circuit. The capacitor C_b is a DC-blocking capacitor to isolate the DC-bias circuit for the peaking device from RF input path.

By removing a 3-dB input hybrid splitter, the conventional DA can be rearranged to more compact structure called a “series-type” Doherty architecture, where the subcircuit of the peaking amplifier and impedance transformer are connected to the output of the carrier amplifier in series rather than in parallel configuration.[112, 113] In this case, the impedance transformers in both carrier and peaking amplifying paths are composed of a high-pass lumped-element T-network each. The shunt inductor in a high-pass T-network can be implemented using a high-impedance microstrip line instead of a lumped inductor. Besides, a high-pass T-network helps to prevent occasional LF oscillations. Such a series-type MMIC DA with optimum device sizes based on a 2-μm InGaP GaAs HBT technology to use in a handset application achieved a *PAE* of 18% and 42.8% at output powers of 16 and 28 dBm, respectively, for a single-carrier 1.9-GHz CDMA signal.

Fig. 11.45A shows the block schematic of consecutive integrated DA based on a multichip module (MCM) which includes the input matching networks (IMNs), *N* cells for the carrier and peaking devices, where the *N*th cell of the carrier device is used to couple the output power from the carrier device output to the peaking device input, and the series transmission line for the phase compensation between the carrier and peaking amplifying paths.[114] The power division ratio can be changed by using different combinations of the cells. Here, the external input quarterwave transmission line is required to match the input impedance of the MCM with the source impedance, the impedance inverter required for the inverted Doherty structure is connected between the peaking device output and common junction point, and the output impedance transformation is provided by a two-stepped transmission line. As a result, only a small part of the output power coupled from the carrier amplifying path flows to the input of the peaking device, thus increasing the power gain of a DA. Because the input of the peaking device and the output of the carrier device are significantly isolated from each other in this case, the operation conditions remain stable.

Fig. 11.45B shows potential improvement in a power gain for the high-power consecutive Doherty structure with two 180-W GaN HEMT devices operating in a frequency bandwidth of 3.4–3.6 GHz compared with the conventional DA with the same devices where ideally half an input power flows to the peaking amplifying path. Different characteristic impedance of the impedance inverter can be used for the asymmetric operation of the consecutive integrated DA when the number of cells of the peaking device is greater than that for the carrier device. The high-gain multistage-stage DA architecture using consecutive configuration can be arranged to improve efficiency at significant power backoff.

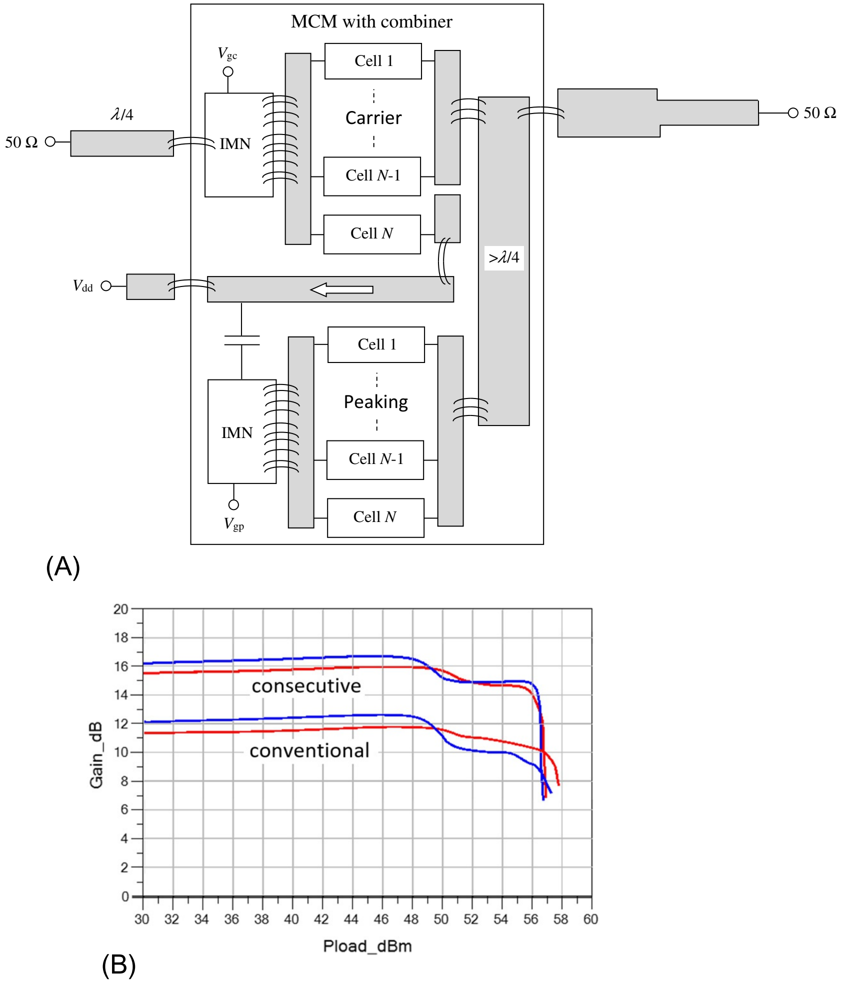

MCM with combiner
V_{gc}
Cell 1
Carrier
Cell N-1
Cell N
$\lambda/4$
50 Ω
IMN
50 Ω
>$\lambda/4$
V_{dd}
Cell 1
Peaking
Cell N-1
Cell N
IMN
V_{gp}
(A)
Gain_dB
20
18
16
14
12
10
8
6
4
2
0
consecutive
conventional
30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60
Pload_dBm
(B)

FIG. 11.45

Block schematic and performance of integrated consecutive Doherty amplifier.

Fig. 11.46 shows the circuit schematic of a three-stage integrated DA where a Wilkinson-type asymmetric input splitter and an output combiner based on lumped low-pass prototype impedance inverters absorb the device gate-source and drain-source capacitances, respectively.[115] With a device size ratio of 1:4:4, the measured results show the capability to achieve a power gain of 12 ± 1 dB and a *PAE* of 45%–55% at 12-dB backoff power level from peak output power of 47 dBm across the frequency bandwidth of 1.8–2.2 GHz using a compact package of $3 \times 5\,\text{mm}^2$ suitable for small-cell applications.

Similarly, a four-stage DA based on two basic 50-W two-stage structures with a device size ratio of 1:1:1:1 and implemented in a dual-path package, as shown in Fig. 11.47, achieved a power gain of 13.4 ± 0.2 dB with an average drain efficiency of 47 ± 1 dB at 8-dB backoff from peak output power

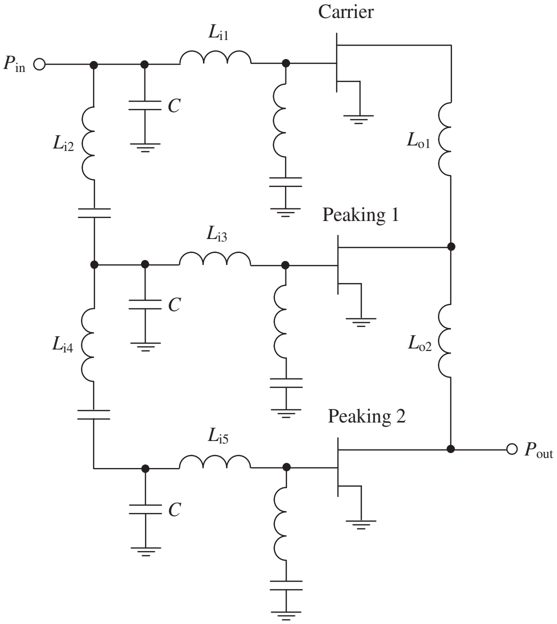

Carrier
L_{i1}
P_{in}
C
L_{i2}
L_{o1}
Peaking 1
L_{i3}
C
L_{i4}
L_{o2}
Peaking 2
L_{i5}
P_{out}
C

FIG. 11.46

Circuit schematic of three-stage integrated Doherty amplifier.

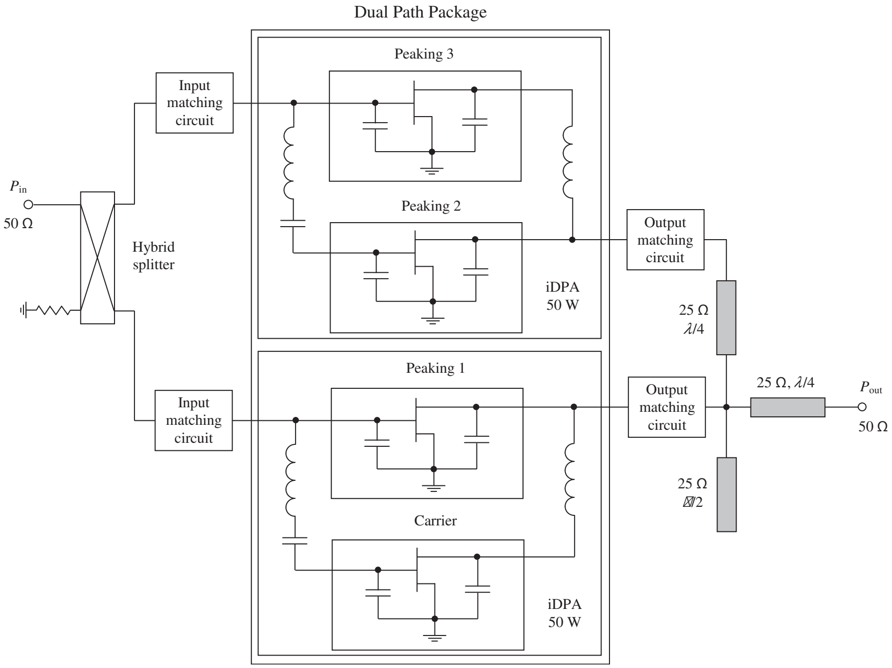

Dual Path Package
Peaking 3
Input matching circuit
P_{in}
50 Ω
Hybrid splitter
Peaking 2
Output matching circuit
iDPA 50 W
25 Ω λ/4
Peaking 1
Input matching circuit
Output matching circuit
25 Ω, λ/4
P_{out}
50 Ω
25 Ω ⊠/2
Carrier
iDPA 50 W

FIG. 11.47

Block schematic of four-stage integrated Doherty amplifier.

of 100 W across the frequency range of 1.805–2.17 GHz for a 20-MHz LTE signal with a *PAR* of 7.2 dB.[116] The half-wave 25-Ω open-circuit stub in the load network is used for bandwidth extension due to effect of reactance compensation.

11.7.3 Monolithic Doherty amplifiers

The transmission-line conventional DA can easily be monolithically implemented using a GaAs HBT, pHEMT, GaN HEMT, or CMOS process. Fig. 11.48 shows the first implementation of a fully integrated *Ku*-band MMIC DA using a 0.25-μm pHEMT technology which achieved a two-tone *PAE* of 40% with an output power of approximately 24 dBm and a corresponding IM_3 of −24 dBc at 17 GHz.[17] Here, two 10-finger 600-μm gate width devices are used for the carrier and peaking amplifiers, low-pass input matching circuits are used to maximize power gain, and a shunt microstrip line is used to resonate the device drain-source capacitances and to provide the drain bias. The input 3-dB hybrid is realized with a Lange coupler and the quarterwave microstrip line is approximated with a capacitively loaded line of higher characteristic impedance. The 50-Ω load is transformed to the desired load network impedance of 25 Ω with an output low-pass matching section. At the same time, a

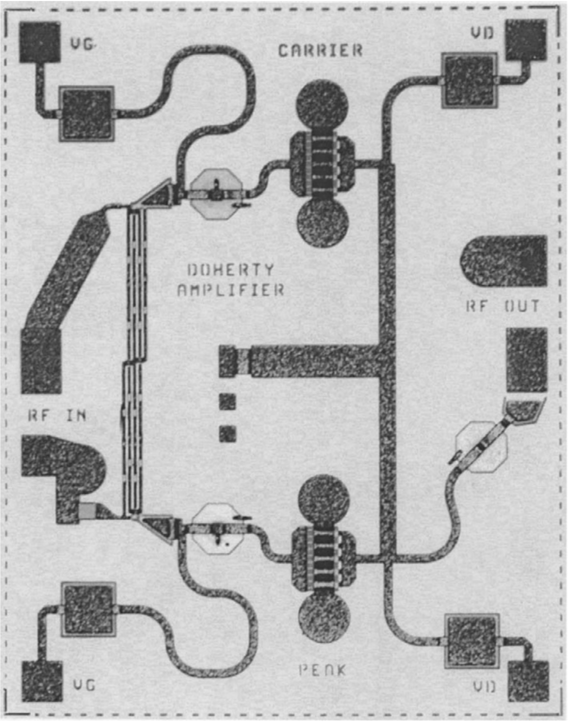


FIG. 11.48

Photo of microwave Doherty amplifier MMIC.[17]

single-tone *PAE* of 38.5% at $P_{1dB} = 23.5$ dBm was measured for a 20-GHz MMIC DA implemented in a 0.15-μm pHEMT process.[117]

Fig. 11.49A shows the test chip of a wideband monolithic GaN HEMT asymmetric Doherty PA, where the input network consists of a lumped-element low-pass Wilkinson power divider and phase shifter, while the load network represents a T-line impedance inverter with optimized characteristic impedances and electrical lengths of microstrip lines.[118] The input matching and stability of operation is provided with a series resistor at the input of the carrier device and with two shunt *LR* circuits connected at the inputs of the carrier and peaking devices, respectively. The Doherty PA was implemented in a 0.25-μm GaN HEMT process, having a 100-μm thick SiC substrate, a relative permittivity of 9.7, a maximum drain current density of 900 mA/mm, and a maximum power density of 5–7 W/mm, with a total chip size of $2.1 \times 1.5\,\text{mm}^2$. To obtain the highest possible output power with model verified device sizes, the total gate widths of the carrier and peaking devices were chosen as $4 \times 100\,\mu\text{m}$ and $10 \times 100\,\mu\text{m}$, respectively. As a result, a drain efficiency above 35%, as shown in Fig. 11.49B, and

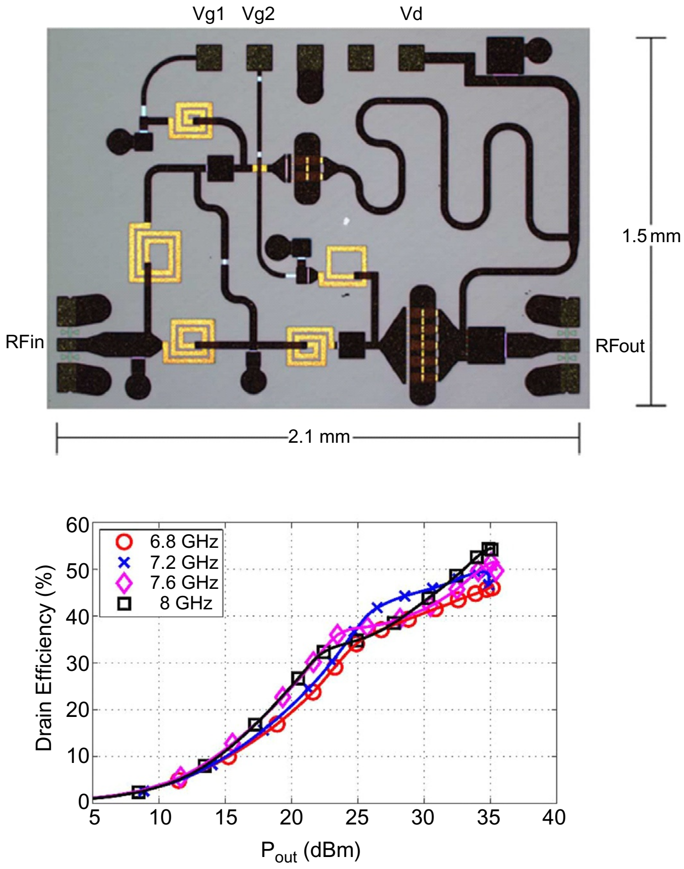


FIG. 11.49

Test chip and performance of wideband monolithic GaN HEMT Doherty amplifier.[118]

a *PAE* over 30% at 9-dB power backoff within the frequency range of 6.7–7.8 GHz and a maximum output power of 35 ± 0.5 dBm from 6.6 to 8.5 GHz were achieved.

Wider frequency bandwidth with high efficiency can be achieved by optimizing the gate and drain bias voltages and IMN. Fig. 11.50 shows the circuit schematic of a monolithic DA providing high-efficiency operation across a frequency bandwidth of 5.8–8.5 GHz based on a 0.25-μm GaN HEMT MMIC process with the sizes of 10 × 100 μm for both carrier and peaking devices.[119] Here the input splitter is realized using a Lange coupler, the input matching circuits represent the two-section structures with low- and high-pass matching sections, and the output matching network was designed to transform the 50-Ω impedance to the desired load impedance of 68 Ω over the entire bandwidth using a quarterwave line. The combining network operating as a quarterwave inverter also provides a possibility for separate drain biasing for carrier and peaking devices. As a result, a *PAE* over 31% was measured across a frequency bandwidth of 5.8–8.8 GHz at 9-dB power backoff from the saturated output power of approximately 36 dBm with a drain bias voltage for carrier device of 12.5 V and for peaking device of 28 V, respectively, with a total chip size of 2.9 × 2.9 mm^2.

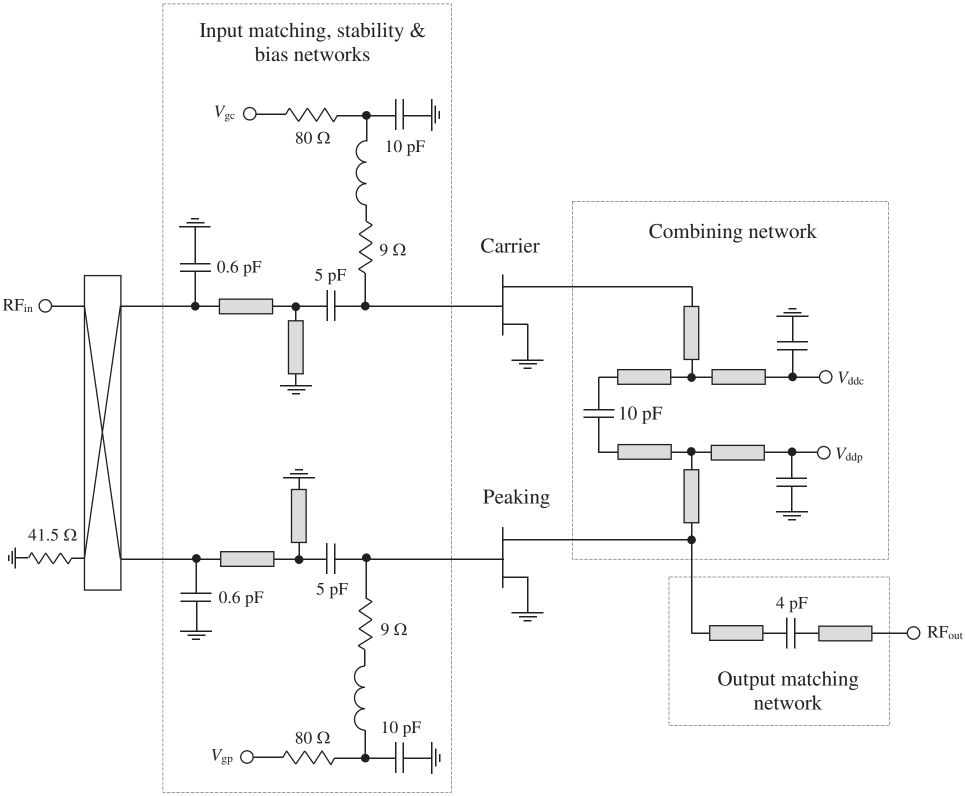

Input matching, stability &
bias networks
V_{gc}
80 Ω
10 pF
9 Ω
0.6 pF
5 pF
Carrier
Combining network
RF_{in}
V_{ddc}
10 pF
V_{ddp}
Peaking
41.5 Ω
0.6 pF
5 pF
9 Ω
4 pF
RF_{out}
Output matching
network
80 Ω
10 pF
V_{gp}

FIG. 11.50

Schematic of monolithic GaN HEMT Doherty amplifier with wide bandwidth.

For a symmetric 10-GHz MMIC Doherty PA using Class-E approximation in both the carrier and peaking amplifiers that are based on 140-nm GaN HEMTs of a 1-mm gate width each, the simulated two-tone results demonstrated a *PAE* of 40.4% at peak output power of 25.6 dBm and a *PAE* of 24% at 6-dB backoff.[120] To improve linearity of a microwave DA, the input divider can be implemented without coupler by using an unequal-power reactive divider, as shown in Fig. 11.51.[121] In this case, the input divider changes the ratio of power delivered to each device as input power increases due to increased difference in the device gate-source capacitances over input drive under different biasing conditions. The increased gate-source capacitance of the peaking amplifier reduces the load impedance presented to the input divider at the peaking amplifier port and therefore, as input power increases, more power is delivered to the peaking amplifier to relax saturated conditions for the carrier amplifier. To simplify the output network, both the carrier and peaking amplifiers were matched to 100 Ω for parallel combining. The fabricated MMIC of a DA based on 0.15-μm GaN HEMT on SiC process demonstrated a saturated output power over 36 dBm and a peak *PAE* of 47% at 10 GHz, with a power gain greater than 9 dB up to 25 dBm of input power and a *PAE* of 41% at 6-dB output power backoff at a supply voltage of 20 V.[121]

To increase power gain of a DA at very high frequencies, especially for *K*-band applications, the complete structure of a DA should include a high-gain driver. In this case, the solution with drivers in the carrier and peaking amplifying paths provide higher *PAE* than an approach with a single driver for a final DA stage.[122] To achieve better linearity performance, the peaking device can be biased in Class-AB or Class-B, while the peaking driver biased in Class-C is responsible for correctly turning on the peaking branch. To preserve stability of operation across the entire frequency range, it was necessary to insert shunt resistors in parallel to the DC-bypass capacitors at drain and gate of each stage and to proper dimension the drain-feed stub lengths of the power stage. The cascaded DA was implemented in a commercially available 0.15-μm pHEMT process with dimensions of $1.43 \times 3\,\text{mm}^2$ and achieved an output power of 30.9 dBm with a *PAE* of 38% at saturation and 20% at 6-dB output power backoff with a power gain of 12.5 dB at 24 GHz in CW operation conditions. However, better performance at *K*-band for a two-stage cascaded DA can be achieved using a 0.15-μm GaN on SiC HEMT technology when the measured results could demonstrate over 5 W of saturated output power with a *PAE* of 48% at $P_{1\text{dB}}$ and a *PAE* of 25% at 8 dB power backoff from $P_{1\text{dB}}$ with a power gain of 16 dB.[123] The inverted asymmetric DA with the same circuit structures but different values of their components for carrier and

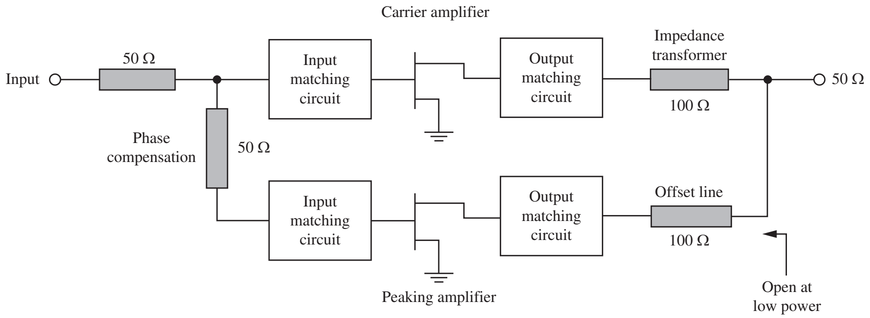


FIG. 11.51

Block schematic of 10-GHz monolithic GaN HEMT Doherty amplifier.

peaking amplifiers including the driver stages and second-harmonic tuning circuits close to the gates of the output devices achieved the saturated output power above 32 dBm over 24–28 GHz with a peak *PAE* of 21.7% and a PAE above 20% at 6-dB power backoff with a power gain of 15 dB at 26 GHz, implemented using a 0.15-μm GaN HEMT process with a chip size of 2.5 × 2.0 mm^2.[124] The saturated output power of 35.6 dBm with a peak *PAE* of 25.5%, a *PAE* of 22.7% and 19.5% at 6-dB and 8-dB backoff, respectively, and a power gain of approximately 15 dB were measured at 28.5 GHz for a symmetric 0.15-μm GaN HEMT DA consisting of the two-stage carrier and peaking PAs, being implemented in a chip size of 2.7 × 1.6 mm^2.[125, 126]

Fig. 11.52A shows the test chip of a monolithic DA with driver stages based on a 100-nm AlGaN/GaN HEMT technology, which could achieve a peak *PAE* of 37%, a saturated output power of 35 dBm, and a linear power gain of 25 dB at 20 GHz, as shown in Fig. 11.52B, occupying an area of 2.1 × 4.0 mm^2.[127] In this technology, a transition frequency f_T of 80 GHz for small-gate devices, saturated drain current densities above 1.6 A/mm and a peak transconductance above 500 mS/mm were

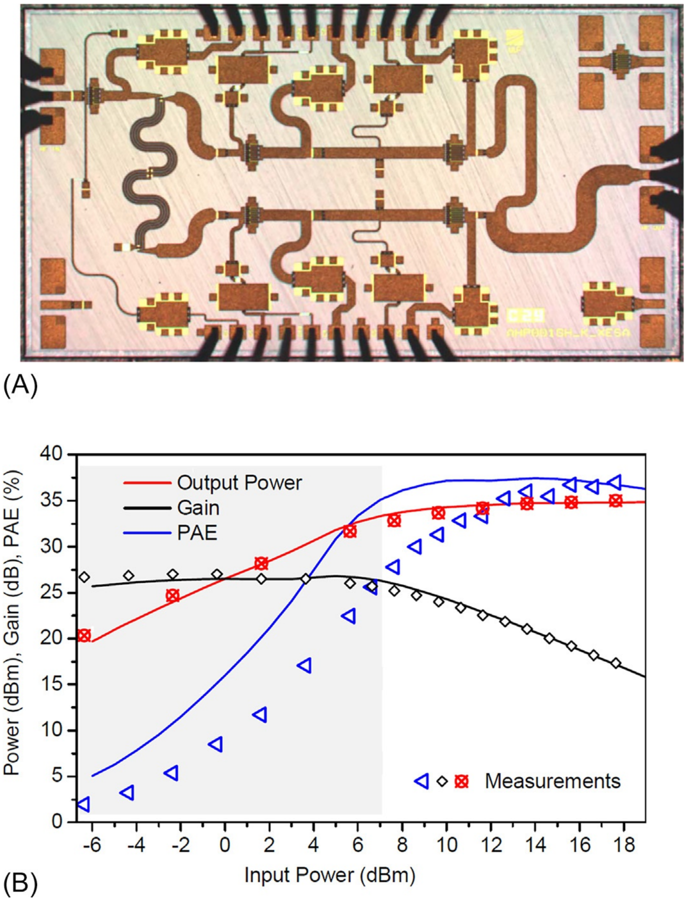


FIG. 11.52

Test chip and performance of 20-GHz GaN HEMT Doherty amplifier.[127]

provided, with a SiC substrate thinned down to 75 μm. The device periphery of driving devices of 8 × 75 μm was selected as a compromise between the linearity, power gain, and the capability to fully drive the final 8 × 100 μm devices. The carrier and peaking amplifying paths are supplied with the quadrature RF signal via a quarterwave Lange coupler, having a meander structure for more compact implementation. Potential LF instabilities induced by the gate biasing network were damped by *RC* networks with only slight performance degradation.

Fig. 11.53A shows the circuit schematic of a monolithic DA operating at sub-6 GHz for 5G cellular systems using a 0.25-μm GaN HEMT process where a compact impedance inverter and output

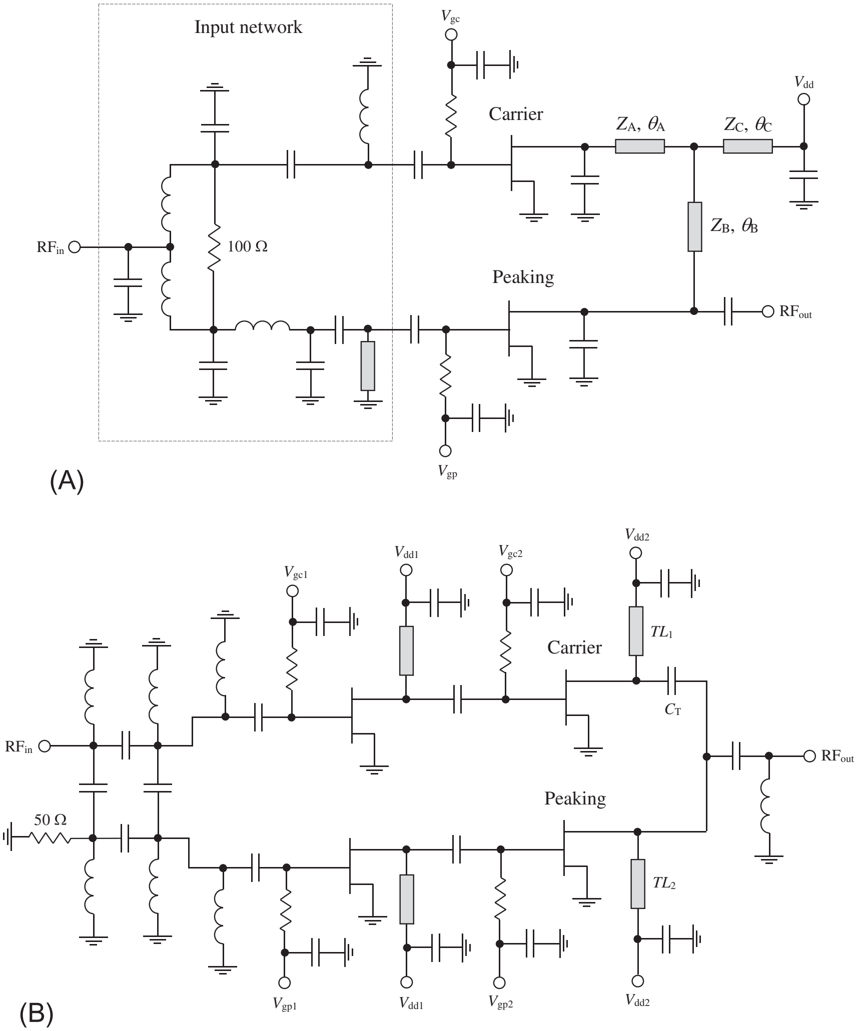

Input network
V_{gc}
Carrier
Z_A, θ_A
Z_C, θ_C
V_{dd}
RF_{in}
100 Ω
Z_B, θ_B
Peaking
RF_{out}
V_{gp}
(A)
V_{dd2}
V_{dd1}
V_{gc2}
V_{gc1}
TL_1
Carrier
C_T
RF_{in}
RF_{out}
Peaking
50 Ω
TL_2
V_{gp1}
V_{dd1}
V_{gp2}
V_{dd2}
(B)

FIG. 11.53

Circuit schematics of monolithic GaN HEMT Doherty amplifiers for sub-6-GHz 5G communication systems.

matching are achieved using a T-type transmission-line network with shunt capacitors.[128] The input network mainly based on lumped elements includes a Wilkinson splitter and a phase shifter where the quarterwave lines are replaced by their low-pass Π-type equivalents, and the IMNs represent their high-pass L-type lumped equivalent circuits. To maximize efficiency at the backoff power, the size ratio of power cells in the carrier (6 × 100 μm) and peaking (12 × 100 μm) amplifiers was optimized to form a 1:2 asymmetric Doherty configuration, with a total chip size of 2.49 × 1.56 mm^2. As a result, the measured maximum output power of 38.7 dBm with a *PAE* of 47.3% and a *PAE* of 49.5% at 6-dB power backoff were achieved at an operating frequency of 5.8 GHz, while keeping *PAE* over 32% across the frequency range of 5.1–5.9 GHz with a power gain of approximately 12 dB.

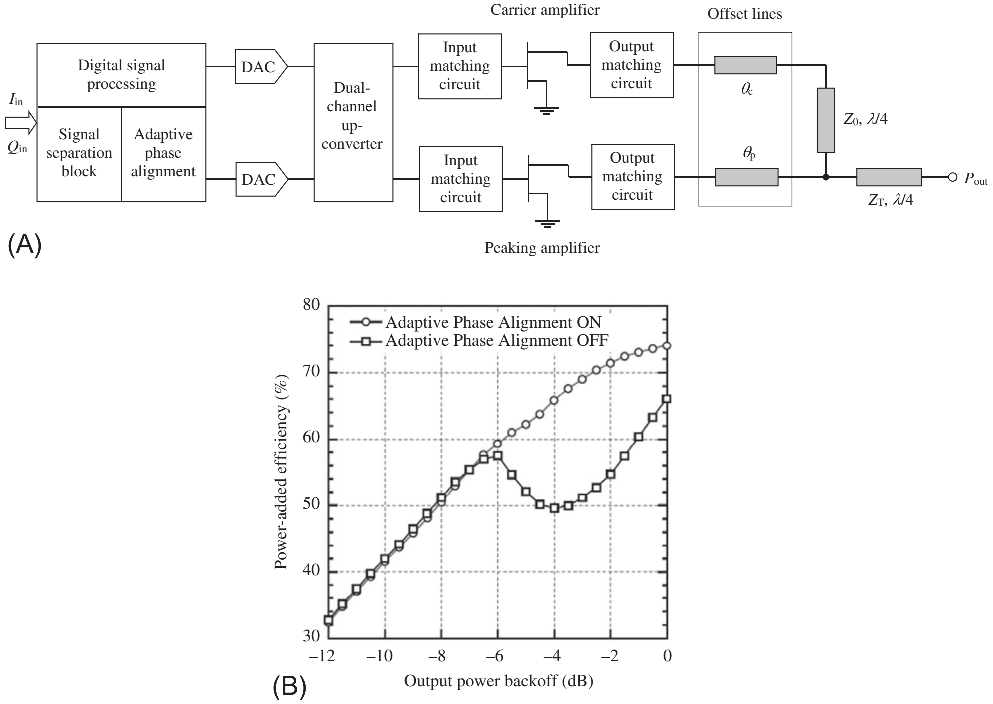
The circuit schematic of a fully integrated *C*-band symmetric GaN HEMT DA is shown in Fig. 11.53B, where the driver stage is used in both carrier and peaking amplifiers and a compact low-loss load network provides high efficiency and minimizes chip size.[129] Here the cell sizes of 10 × 200 μm for carrier and peaking devices and 10 × 125 μm are chosen to maximize gain and efficiency. An input power splitter is represented by a lumped branch-line coupler, whereas a simple L-type high-pass *LC* sections are used for both input and interstage matching. The quarterwave inverter and output impedance transformer are designed in the form of lumped Π-type high-pass equivalent sections, which are then combined to minimize the overall size, and the shunt inductors for inverter are replaced by the corresponding shunt microstrip lines to minimize loss. As a result, a saturated *PAE* of 61% and a *PAE* of 47% at 6-dB power backoff with a power gain of approximately 15 dB were measured across the frequency bandwidth of 4.4–5.1 GHz. For a single-carrier 40-MHz LTE signal with a *PAR* of 7.7 dB, a *PAE* of 42% at an average output power of 33.7 dBm with an *ACLR* of −29 dBc (or −45 dBc after applying DPD) was achieved at 4.7 GHz, with a compact chip size of 3.0 × 2.5 mm^2.

An integrated DA intended to use in 5G handset transmitters can be based on different bias conditions to satisfy efficiency and linearity requirements.[130] In this case, the carrier power cell is biased in Class-AB to have a flat overall power gain response while preserving high efficiency in the backoff region. In efficient mode, the carrier power cell is biased in deep Class-C which enhances the PAE in the low-power region at the expense of linearity. The linear and efficient Doherty modes can be combined by using adaptive bias for the carrier device. The two-stage DA is implemented in a 130-nm silicon-on-insulator (SOI) technology using lumped elements and packaged using a flip-chip technology on a laminate substrate where the driver chip and supply and output matching inductors are located. A two-section output matching network is used to improve both the operating bandwidth and the out-of-band rejection. The carrier and peaking cells represent common-source SOI-LDMOS devices with high breakdown voltage to ensure high reliability. As a result, a maximum *PAE* of 57% was achieved at a peak output power of 32.7 dBm, and a *PAE* of 45% was measured at an output power of 28 dBm with a power gain of 27 dB. For a single-carrier 10-MHz LTE signal, the *PAE* is maintained higher than 40% across the frequency bandwidth of 2.0–2.6 GHz with an *ACLR* lower than −33 dBc, while delivering an average output power of 28 dBm.

11.8 Digitally driven Doherty amplifiers

In a digitally driven dual-input DA architecture, the input signal of each branch is digitally preprocessed and supplied separately to each branch of the DA to optimize its overall performance. In this case, digital signal processing is applied to reduce the performance degradation due to phase impairment in the DA branches achieved by adaptively aligning the phases of the carrier and peaking paths for all power levels after the peaking amplifier is turned on. Generally, a digital signal processor (DSP) includes a DPD system to improve linearity which can be configured to provide a carrier signal component along a carrier amplifier path and a peaking signal component along a peaking amplifier path from a digital input signal. In this case, the carrier and peaking amplifiers can amplify the signal components according to the programmable proportions of the split input signal, and not based on a saturation condition of the carrier amplifier, thus resulting in a higher efficiency. Because the signals are isolated prior to being input to the DA, the DA need not include an asymmetric splitting with input phase-matching delay, and input impedance-matching circuitry is simplified. The DPD system also performs phase and gain adjustments to each of the signal components. To further improve efficiency performance of a two-stage DA, the separated amplitude and phase-modulated signals, produced by the DSP, drive through the corresponding quadrature upconverters both the carrier and peaking amplifiers, each operated in a Class-E mode.[131]

Fig. 11.54A shows the block diagram of a dual-input digitally driven DA with digital signal processing and dual-channel upconverter.[132] In this case, direct access and software control of the individual inputs can bring an improvement in efficiency of a DA between two efficiency peaking points at the maximum and 6-dB backoff output powers, as shown in Fig. 11.54B. The DA design is performed by inserting the offset line with electrical length θ_p to the output of the peaking branch to ensure a



Carrier amplifier
Offset lines
Digital signal processing
I_{in}
Q_{in}
Signal separation block
Adaptive phase alignment
DAC
DAC
Dual-channel up-converter
Input matching circuit
Output matching circuit
Input matching circuit
Output matching circuit
θ_c
θ_p
Z_0, $\lambda/4$
Z_T, $\lambda/4$
P_{out}
(A)
Peaking amplifier
Adaptive Phase Alignment ON
Adaptive Phase Alignment OFF
Power-added efficiency (%)
80
70
60
50
40
30
–12
–10
–8
–6
–4
–2
0
Output power backoff (dB)
(B)

FIG. 11.54

Block diagram and simulated performance of dual-input digital Doherty amplifier.

quasi-open circuit condition and prevent leakage from the carrier amplifier to the output of the peaking amplifier at the low-power region. The offset line with electrical length θ_c was optimized to maximize efficiency around the turn-on point of the DA. Because of the different bias conditions for the carrier amplifier (Class-AB) and the peaking amplifier (Class-C), the degradation in output power due to phase imbalance condition can be as high as 40% after the peaking amplifier is fully turned on, which directly translates into significant deterioration in a drain efficiency of the DA.

However, the dual-input digitally driven Doherty architecture, allowing for the adoption and implementation of a power adaptive phase-alignment mechanism, can minimize the adverse effects of phase imbalance between the carrier and peaking branches. The power-dependent phase offset is adjusted using a power-indexed lookup table (LUT) to correct for the phase disparity at all power levels, where both the carrier and peaking amplifiers contribute to the total output power of the DA. As a result, the phase difference between the carrier and peaking branches is reduced to 0 degree over the input power range spanning from the turn-on of the peaking amplifier until the saturation of the DA. The phase-aligned DA based on two 10-W GaN HEMT transistors demonstrates a *PAE* more than 50% over an 8-dB output power backoff range and a *PAE* of 57% at an average output power of 37 dBm for a single-carrier WiMAX signal with a *PAR* of 7 dB, and thus resulting in an improvement of 7% in *PAE* and 1 dB in average output power with similar linearity performance corresponding to an *ACLR* of −22 dBc compared with the fully analog DA.[132] However, by using a combination of an efficiency-optimized static input splitter and a vector-switched digital predistorter, the linearity of dual-input DAs can be improved while maintaining high efficiency.[133]

Efficiency enhancement in a digital DA over wide power range can also be achieved by using a digitally controlled dynamic input power distribution scheme to minimize the drive power waste into the peaking branch at backoff power levels.[134] In this case, the carrier amplifier should get significantly more input power in comparison with the peaking amplifier at a low-power drive, whereas the carrier amplifier should get slightly less input power in comparison with the peaking amplifier after turn-on point. As a result, the efficiency can be improved by 7% compared with the conventional fully analog symmetrical DA based on two 10-W GaN HEMT devices operating at 2.14 GHz for a single-carrier WiMAX signal with a 9-dB *PAR* and 10-MHz bandwidth.

Another possibility for a dual-input digital DA is related to its bandwidth extension via digital techniques. It was proven theoretically that the bandwidth limitations of conventional DA could be mitigated by means of a frequency-dependent signal decomposition scheme that controls the input power distribution between the carrier and peaking amplifying paths.[135] Moreover, by optimizing efficiency and bandwidth in a complex design space (involving two independent inputs and an output combiner that incorporates transistor parasitics) can lead to high average efficiency over 100% fractional bandwidth. As a result, an output power of 44 ± 0.9 dBm and a *PAE* of 45% at 6-dB output power backoff can be achieved across the frequency bandwidth over 1–3 GHz.[136] As long as the modulated bandwidth of the transmitting signal is not very wide (up to 60 MHz), operation that is near to optimal can be achieved with a decomposition scheme that is static with respect to the frequency components of the input signal. However, when ultra-wideband signals are to be used, the DSP block of a dual-input DA should incorporate a baseband equalizer with finite impulse response (FIR) filters.[137] The role of the equalizer is to execute the optimal signal separation of each frequency component of the transmitting signal. To minimize the power consumption of the DSP, it is important to optimize the design of the FIR filters while minimizing their order. The frequency-periodic load modulation over multiple contiguous frequency bands when both the conventional and inverted Doherty structures with exchanged relationships between the carrier and peaking amplifiers combined with digitally assisted dual-input configuration can provide optimum signal combination, magnitude and phase of dual-input signals, thus resulting in a drain efficiency of 45%–62% over 1.4–4.8 GHz at 6-dB power backoff with an output power of 29.9–32.8 dBm using two identical 0.15-μm GaN HEMT devices.[138]

Fig. 11.55 shows schematically the potential performance enhancement which can be obtained by applying digital techniques to well-designed analog DAs.[139] In this case, there is some room for improving the output power by up to 2 dB, the average efficiency by up to 20% (in proportion), and the fractional bandwidth by a factor of 1.5.

Modern cellular systems with complex modulation schemes to accommodate signals with high data rates within restricted frequency bands require high peak-to-average power ratios, up to 9 dB and higher. However, multistage or multiway DAs can be too complicated for practical implementation, while outphasing systems are characterized by a steep roll-off beyond the high-efficient point at the corresponding power backoff due to the highly reactive loading conditions of the active devices at large outphasing angles. Therefore a combination of the Doherty and outphasing schemes with appropriately sized carrier and peaking devices can provide a good compromise between circuit complexity and overall efficiency performance. Fig. 11.56A shows the simplified schematic of a Doherty-outphasing amplifier configuration, where two symmetrical DAs (DPA1 and DPA2) are connected in parallel to a common load.[140] Here the Chireix power combiner is incorporated in the carrier and peaking amplifying branches by adjusting the electrical length of the matching lines with $\pm\Delta\theta_m$ in the carrier

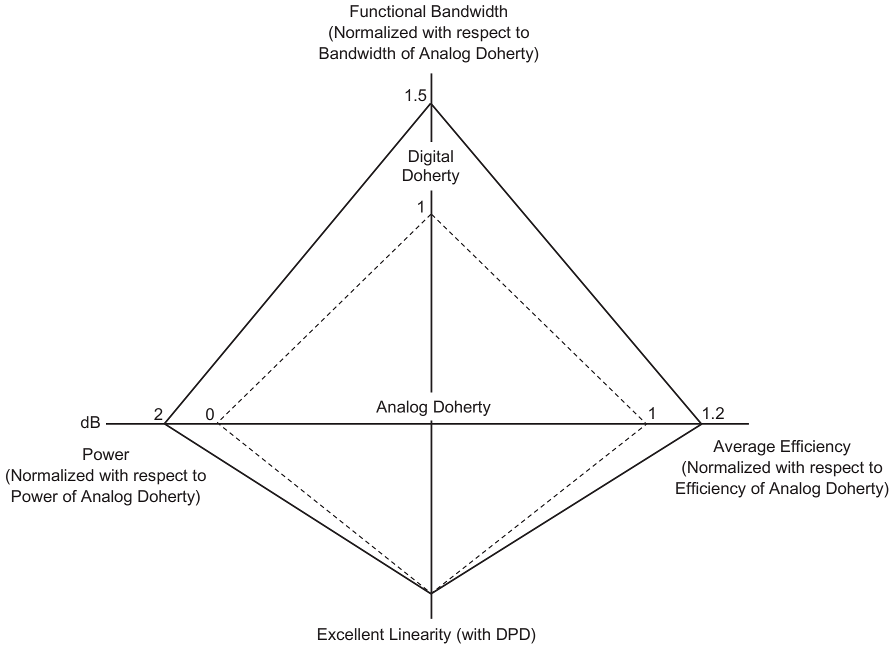

Functional Bandwidth
(Normalized with respect to
Bandwidth of Analog Doherty)
1.5
Digital
Doherty
1
Analog Doherty
dB
2
0
1
1.2
Power
(Normalized with respect to
Power of Analog Doherty)
Average Efficiency
(Normalized with respect to
Efficiency of Analog Doherty)
Excellent Linearity (with DPD)

FIG. 11.55

Analog Doherty amplifier versus digital Doherty amplifier.

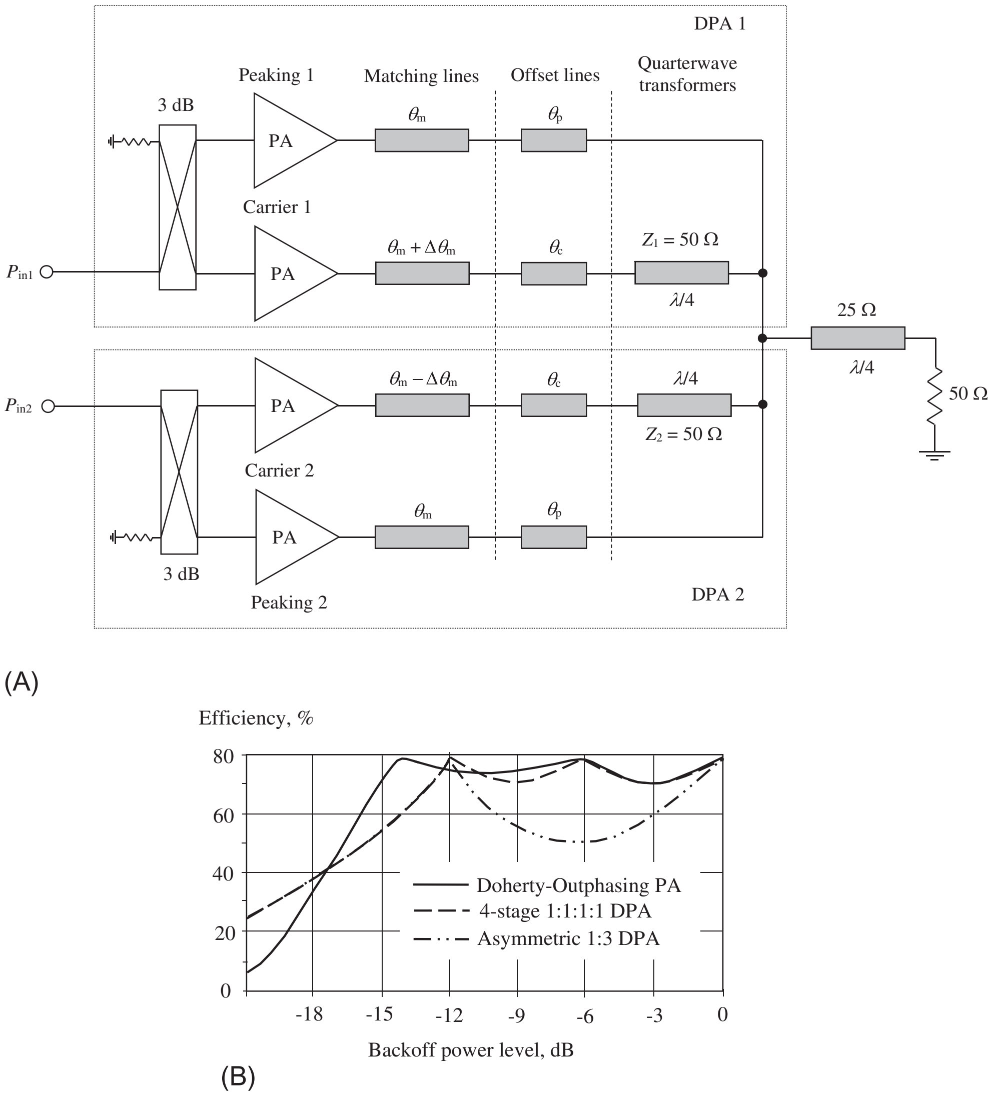

DPA 1
Peaking 1
Matching lines
Offset lines
Quarterwave transformers
3 dB
PA
θ_m
θ_p
Carrier 1
P_{in1}
PA
$\theta_m + \Delta\theta_m$
θ_c
$Z_1 = 50\ \Omega$
$\lambda/4$
25 Ω
$\lambda/4$
50 Ω
P_{in2}
PA
$\theta_m - \Delta\theta_m$
θ_c
$\lambda/4$
$Z_2 = 50\ \Omega$
Carrier 2
PA
θ_m
θ_p
3 dB
Peaking 2
DPA 2
(A)
Efficiency, %
80
60
40
20
0
-18
-15
-12
-9
-6
-3
0
Backoff power level, dB
Doherty-Outphasing PA
4-stage 1:1:1:1 DPA
Asymmetric 1:3 DPA
(B)

FIG. 11.56

Doherty-outphasing power amplifier and instantaneous efficiencies.

amplifying branches, where the value of $\Delta\theta_m$ determines the required outphasing compensation angle. The resulting nonidentical symmetrical DAs with 50-Ω quarterwave lines as the impedance transformers are connected in parallel followed by an output quarterwave impedance-transforming line of 25 Ω to match with 50-Ω load. The related comparative theoretical efficiency versus backoff output power for Doherty-outphasing amplifier along with an asymmetric 1:3 and modified four-stage 1:1:1:1 DAs is shown in Fig. 11.56B. In this case, the combined Doherty-outphasing system utilizes a Doherty operation from peak power to −6 dB backoff power and an outphasing mode between −6 and −14 dB backoff power levels. As seen from Fig. 11.56B, ideally the Doherty-outphasing amplifier can keep efficiency above 70% over 15-dB power backoff range, and still benefit from the soft Class-B-like efficiency roll-off beyond. The measured results of the 2.14-GHz Doherty-outphasing amplifier using two Cree GaN HEMT CGH40045F devices show that a drain efficiency of 66% can be achieved at a peak output power of 50.5 dBm and at an average output power of 44.5 dBm with a DC-supply voltage of 28 V. At the same time, efficiency exceeds 50% at 12-dB power backoff at an average output power of 38.5 dBm.

In an alternative Doherty-outphasing configuration utilizing an outphasing mode from peak power to −6 dB power backoff and a Doherty operation below −6 dB power backoff with different device sizes, ideally a high efficiency over 70% can be kept up to 13.5-dB power backoff range.[141] In this case, the CW measured results of the Doherty-outphasing amplifier using two Cree GaN HEMT CGH40010F and CGH40045F devices for the carrier and peaking amplifiers, respectively, with Chireix combiner based on quarterwave transformers having electrical lengths of $90° \pm \Delta\theta$ and different characteristic impedances Z_1 and Z_2 demonstrate that the drain efficiency of 74% and 61% can be achieved at 10- and 15-dB power backoffs, respectively, with a maximum output power of 51.2 dBm at an operating frequency of 622 MHz with a DC-supply voltage of 28 V. At the same time, a drain efficiency of 70.2% was measured at an average output power of 40.8 dBm for a single-carrier 10-MHz LTE signal.

11.9 Multiband and broadband capability

11.9.1 Multiband Doherty configurations

A multiband capability of the conventional two-stage DA can be achieved when all of its components are designed to provide their corresponding characteristics over the required bands of operation, as shown in Fig. 11.57A.[142] In this case, the carrier and peaking amplifiers should provide broadband performance when, for example, their input and interstage matching circuits are designed as broadband, and the load network generally can represent a low-pass structure with two or three sections tuned to the required frequencies. Some bandwidth extension can be achieved by simply optimizing the characteristic impedances of the quarterwave impedance transformer and quarterwave output combiner in a combining load network.[143, 144] In a broadband Class-E mode, the load network can be composed of the consecutive series and parallel resonant circuits using lumped or transmission-line elements according to reactance compensation technique. For a multiband operation with the center frequency ratio at each of the frequency bands of 2 or greater, the input divider can be configured by a multisection Wilkinson power divider or coupled-line directional coupler. In a dual-band operation mode, a dual-frequency Wilkinson power divider can represent a structure, where each quarterwave branch of a conventional Wilkinson power divider is substituted by two transmission-line sections with different characteristic impedances and electrical lengths.[145, 146] In practical applications, especially if the operating frequencies of one of the frequency bands are sufficiently low, the miniaturized version of a dual-band Wilkinson power divider can be designed based on the concept of a slow wave periodic structure.[147]

A dual-band input power splitter can also represent a Π-shape or T-shape stub-tapped branch-line coupler, as well as an impedance transformer network, which introduces a 90-degree phase shift. Similarly the offset lines and an output quarterwave transformer can be based on a Π-type or T-type

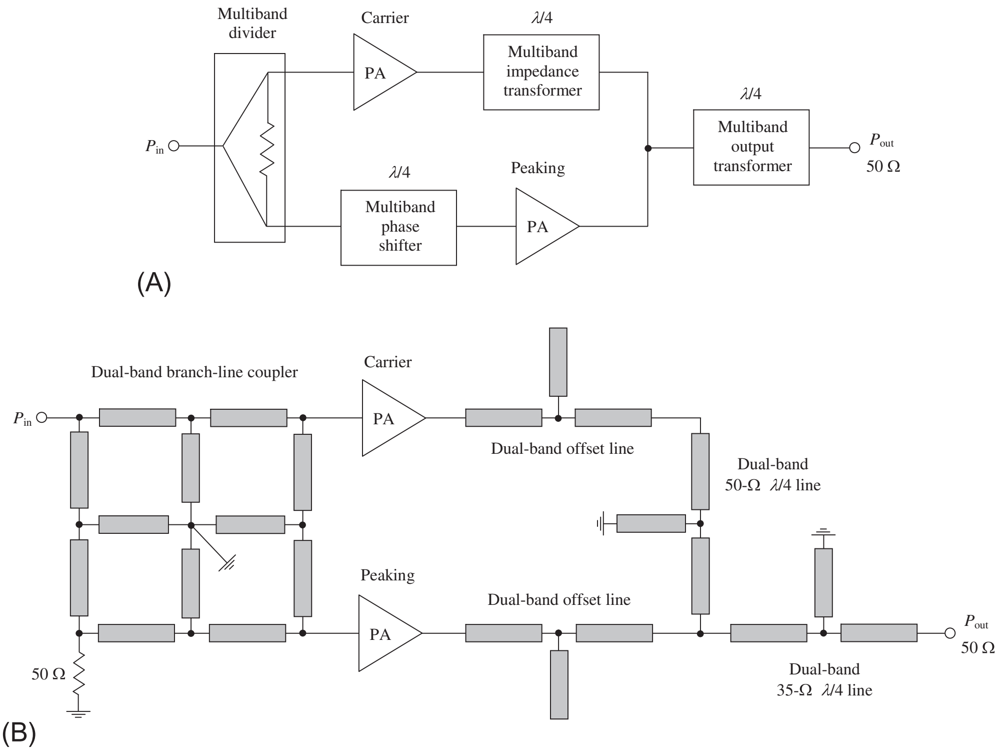

Multiband divider
Carrier
PA
λ/4
Multiband impedance transformer
λ/4
Multiband output transformer
P_{in}
P_{out}
50 Ω
λ/4
Multiband phase shifter
Peaking
PA
(A)
Dual-band branch-line coupler
Carrier
P_{in}
PA
Dual-band offset line
Dual-band 50-Ω λ/4 line
Peaking
Dual-band offset line
PA
P_{out}
50 Ω
50 Ω
Dual-band 35-Ω λ/4 line
(B)

FIG. 11.57

Block diagrams of multiband Doherty amplifiers.

transmission-line impedance-inverting section with proper selected transmission-line characteristic impedances and electrical lengths, where the shunt element is realized by an open- or short-circuit stub, as shown in Fig. 11.57B.[148, 149] However, it should be noted that it is not easy to design a multiband impedance transformer, which should adequately provide two separate matching options simultaneously: first, to operate in a 50-Ω environment without affecting the PA performance in a high-power region, and second, to provide an impedance matching from 25 to 100 Ω in a low-power region. In this case, as an alternative, it is also possible to switch between two quarterwave transmission lines in a dual-band operation when each of the quarterwave transmission line is tuned to the corresponding center bandwidth frequency. However, it may not be so simple in practical implementation because of the load-network complexity and additional power losses.

A concurrent tri-band and quad-band operation of the two-stage DA can be achieved by using a transmission-line multiband impedance inverter, which is realized based on the idea that the transmission-line section having an electrical length equal to a quarter-wavelength at a given LF should be capable of acting as a multiple quarterwave line at higher frequencies.[150, 151] For a quad-band application, the input matching circuit can represent a modified two-way two-stage Wilkinson splitter, while a four-section Chebyshev matching transformer can cover the required broadband frequency range. As a result, the peak drain efficiencies of 60.5%, 58.1%, 52.7%, and 43.3% were achieved at midband frequencies of 960 MHz, 1.5 GHz, 2.14 GHz, and 2.65 GHz, respectively, with the output powers varying between 41.7 and 44.2 dBm. In this design, 10-W and 25-W Cree GaN HEMT devices are used for carrier and peaking amplifiers, respectively.

Generally the multiband impedance transformer can represent a configuration with N ($N \geq 2$) cascade-connected transmission lines with different characteristic impedances. In this case, a simple two-stepped transmission-line impedance transformer can provide a two-pole response with different characteristic impedance ratio and different electrical lengths of the transmission-line sections.[152] It can be used as a dual-band output transformer because it is necessary to provide an impedance transformation from the output impedance of 25 Ω to the standard 50-Ω load in both low-power and high-power regions.[149]

As an example, the dual-band output transformer can be realized using a two-section transmission line, where the characteristic impedance of the first quarterwave transmission-line section is equal to 30 Ω and the characteristic impedance of the second quarterwave transmission-line section is set to 42 Ω, as shown in Fig. 11.58A. In this case, the amplitude variations of ±0.5 Ω shown in Fig. 11.58B by curve 1 and phase variations of ±1 degree shown in Fig. 11.58C by curve 1 can be achieved across the frequency range from 2.0 to 2.8 GHz covering simultaneously 2.1-GHz (2.11–2.17 GHz) and 2.6-GHz (2.62–2.69 GHz) WCDMA/LTE bands. For comparison, the narrowband amplitude and phase responses of a quarterwave single-line impedance transformer are shown in Fig. 11.58B and C by curves 2, respectively. From Fig. 11.58B and C, it follows that the amplitude variations of ±1.0 Ω and phase variations of ±2 degrees can be achieved with a 1-GHz bandwidth from 1.9 to 2.9 GHz, which means that reducing the midband frequency to 2.3 GHz can result in a simultaneous tri-band operation with inclusion of an additional 1.8-GHz (1805–1880 MHz) WCDMA/LTE band.

Fig. 11.59 shows the block schematic of a broadband DA where the impedance transformer is based on a three-section microstrip line with two shunt reactances and the output transformer represents a three-section microstrip line with different characteristic impedances to provide the trade-off for optimum impedances seen by the carrier and peaking amplifiers at backoff and saturation conditions.[153] In this case, the parasitic output capacitances of the identical carrier and peaking devices are respectively absorbed by the impedance transformer. The input broadband network provides a 2:1 asymmetric split and has been optimized to ensure that the currents at the summing node point are amplitude and phase aligned at the maximum drive level. As a result, the DA based on two 50-V LDMOSFET devices in a single package achieved an average output power of 43.5 dBm with a drain efficiency of 33.5% over the frequency bandwidth of 450–750 MHz for an 8-MHz OFDM (64QAM modulation) signal with a *PAR* of 10.5 dB, having the target *ACLR* of −50 dBc at the upper limit of the bandwidth if DPD is applied. Compared with a standard Class-AB push-pull PA developed with the same devices which demonstrates a drain efficiency of 22% under the same biasing conditions, the DA provides more than 50% efficiency improvement.

11.9.2 Bandwidth extension using reactance compensation technique

An *LC* tank at the output of the peaking amplifier, as shown in Fig. 11.60A, can extend the frequency bandwidth of the DA due to reactance compensation effect when it provides an inductive reactance at lower bandwidth frequencies and capacitive reactance at higher bandwidth frequencies which is opposite to the frequency behavior of the series loaded quarterwave transmission line with the

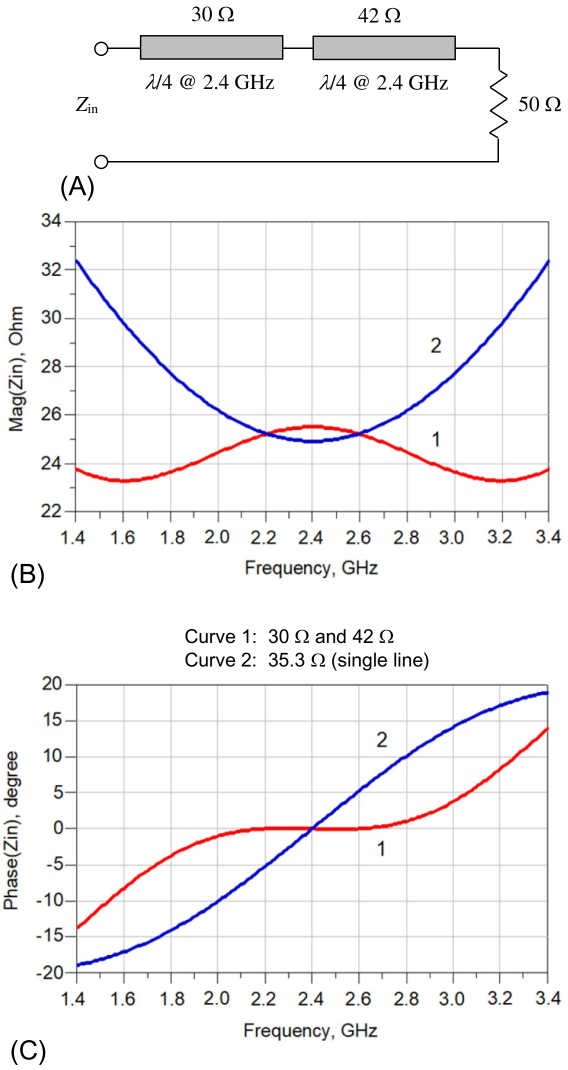


FIG. 11.58

Stepped transmission-line transformer and its input impedances.

characteristic impedance Z_T near the resonant frequency f_0 when $Z_T < 50\,\Omega$.[154] As a result, such an output combiner provides the impedance $\mathrm{Re}Z_m$ of $100\,\Omega$ seen by the carrier device at power backoff mode when the peaking device is turned off over more than 35% fractional bandwidth, compared with less than 10% bandwidth for the conventional output combiner, as shown in Fig. 11.60B. In this case, the output capacitance of the peaking amplifier can be absorbed into the tank capacitance, and the tank inductor can act as the biasing feed for both the carrier and peaking devices which in turn provides

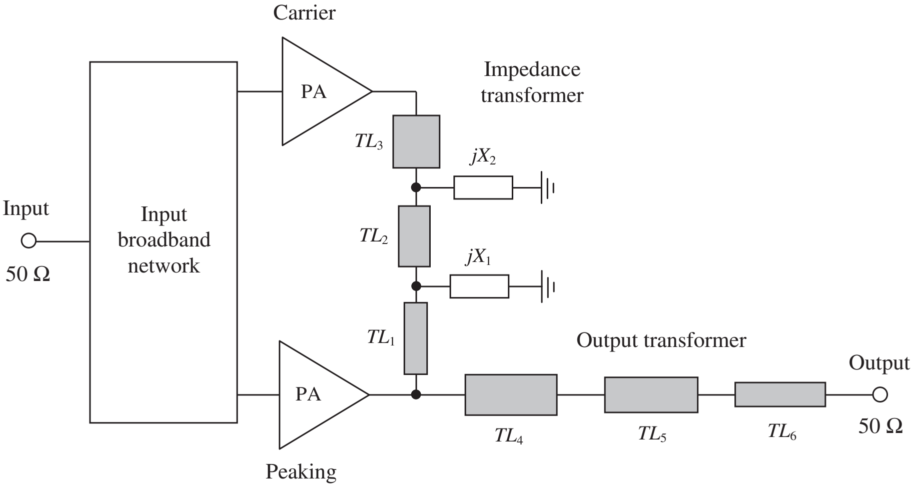

Carrier
PA
Impedance transformer
TL_3
jX_2
Input
50 Ω
Input broadband network
TL_2
jX_1
TL_1
Output transformer
Output
PA
TL_4
TL_5
TL_6
50 Ω
Peaking

FIG. 11.59

Block schematic of broadband Doherty amplifier.

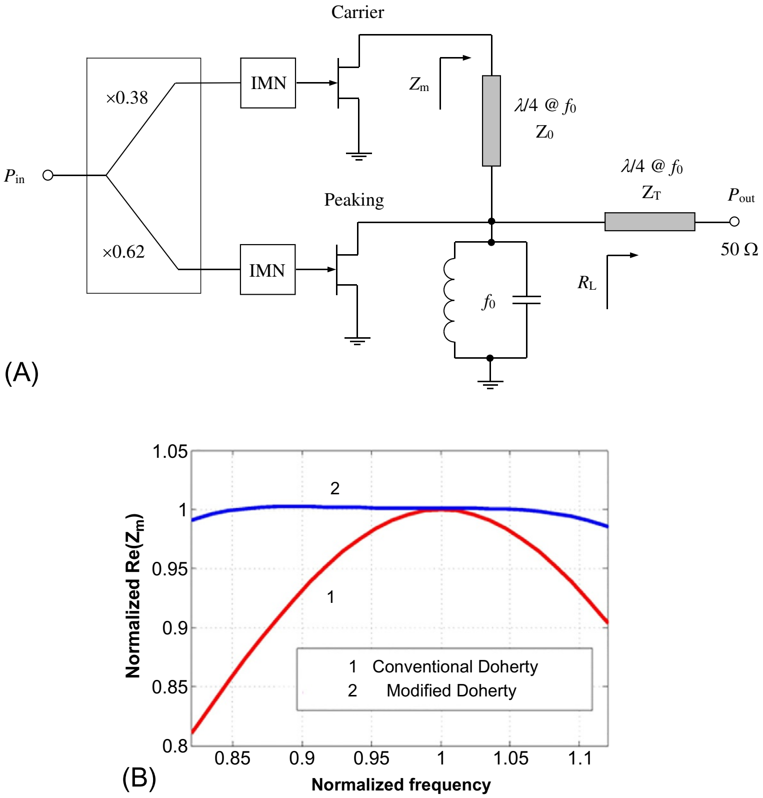


FIG. 11.60

Doherty amplifier with extended bandwidth and its broadband property.

the small baseband impedance at the drain of the carrier and peaking transistors up to a few hundreds of megahertz. Based on 10- and 25-W Cree GaN HEMT devices, a *PAE* of 42% was achieved at an average output power of 33.5 dBm when amplifying a concurrent dual-band 15-MHz WCDMA signal at 750- and 15-MHz LTE signal at 900 MHz with a *PAR* of 9.4 dB.

Similarly, wider bandwidth can be obtained for a three-stage DA in a backoff region when both peaking amplifiers are turned off, and two quarterwave transmission lines connected in series compose a half-wave transmission line, which acts as a shunt resonant circuit. In this case, its input reactance at the fundamental varies in opposite direction to that of the series transmission line connected to the carrier amplifier, and variation of the inductive and capacitive parts of the reactances will depend on the load resistance. To control the second-harmonic impedance, three quarterwave short-circuit stubs were connected to the drain line, and the characteristic impedances of these stubs were individually optimized to achieve high efficiency across the bandwidth.[155] As a result, based on two 25-W and one 10-W Cree GaN HEMT devices, a CW drain efficiency of 49%–64% for output backoff power levels of up to 9 dB was achieved across the bandwidth from 730 to 950 MHz. For a clipped four-carrier 20-MHz WCDMA signal at 900 MHz with a *PAR* of 7.14 dB, an *ACLR* of −51.4 dBc was measured after applying DPD, with an average output power of 35 dBm and a *PAE* of 53%. By using similar approach with shunt short-circuited quarterwave stubs to extend the frequency bandwidth, a drain efficiency more than 53% at saturation and over 40% at 8-dB backoff power were achieved across the frequency range of 2.0–2.6 GHz with a maximum CW output power exceeding 43.6 dBm for a three-way DA based on three identical 10-W Cree GaN HEMT devices.[156]

11.9.3 Broadband Doherty amplifier via real frequency technique

The broadband properties of the DA significantly depend of the broadband capability of the output combining network. In conventional DA, this network includes two quarterwave transmission lines: one as an impedance transformer and the other as an output transformer. Therefore optimizing the characteristic impedances of the quarterwave transmission lines may result in the bandwidth extension of the DA. The obtaining fractional bandwidth when it is necessary to transform the impedance from $Z_L = 25\,\Omega$ to the impedance $Z_m = 100\,\Omega$ seen by the carrier device at power backoff mode can be calculated from

$$\frac{\Delta f}{f_0} = 2 - \frac{4}{\pi}\cos^{-1}\left(\frac{2\Gamma_{\max}}{\sqrt{1-\Gamma_{\max}^2}}\frac{\sqrt{Z_m Z_L}}{|Z_L - Z_m|}\right), \tag{11.39}$$

where f_0 is the center bandwidth frequency, $\Delta f/f_0$ is the fractional bandwidth of the quarterwave line, and $\Gamma_{\max}$ is the maximum reflection coefficient magnitude.[157] From Eq. (11.39), it follows that the fractional bandwidths $\Delta f/f_0 = 17\%$, 35%, and 59% can be achieved for maximum reflection coefficient magnitudes $\Gamma_{\max} = 0.10$, 0.20, and 0.32, respectively. For $\Gamma_{\max} = 0.20$, the corresponding voltage standing wave ratio is equal to 1.5. Besides the bandwidth of the quarterwave transmission line can be enhanced by bringing Z_m and Z_L near to each other, resulting in a reduced transformation ratio of the impedance transformer. In this case, if the common load impedance Z_L is increased from conventional value by 1.4 times, then the transformation ratio of the quarterwave transmission line that interconnects the carrier and peaking amplifiers will reduce to 1:2.85 instead of the conventional 1:4. In this case, the output quarterwave transmission line will also have a reduced transformation ratio, and hence an enhanced frequency bandwidth can be provided.

As a result, the modified DA achieves a better efficiency-enhancement behavior than the conventional DA over frequency at 6-dB backoff efficiency of at least 11% up to 44% fractional bandwidth.[143] For example, if the quarterwave transmission lines have a center bandwidth frequency of 2.4 GHz, then the 6-dB backoff efficiency at 2.14 and 2.655 GHz will be of 68.1%, as shown in Fig. 11.61A. In this case, a first peak efficiency of 71.2% at $f = f_0 \pm 0.11 f_0$ occurs at 6.4-dB output power backoff, as shown in Fig. 11.61B, which is a small degradation from the conventional 6-dB backoff efficiency at f_0.[144]

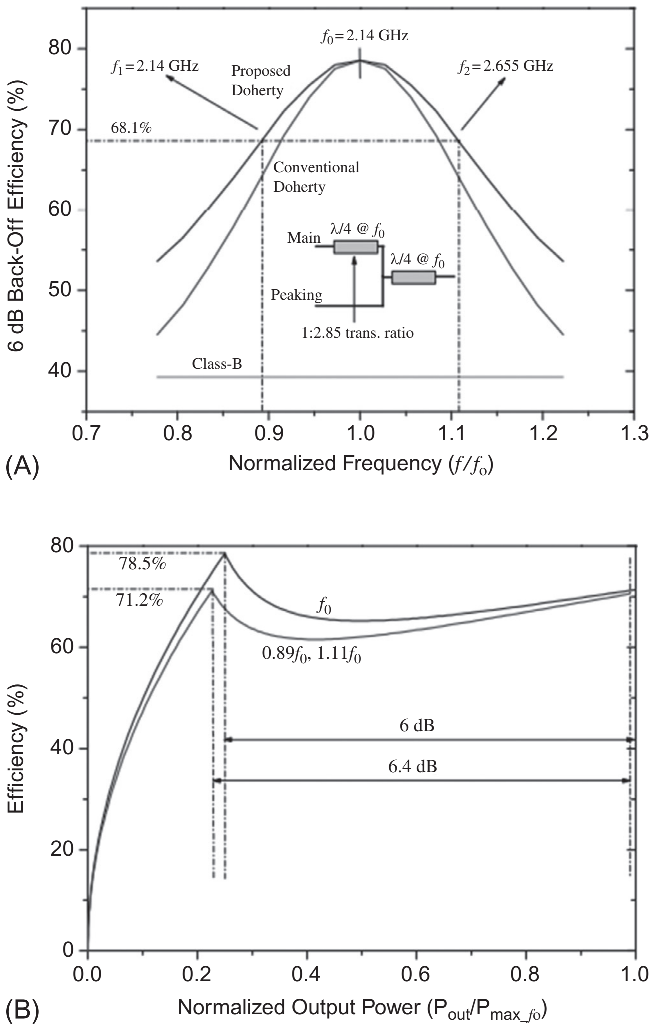


FIG. 11.61

Efficiency of Doherty amplifier with conventional and modified combining network.

An extended frequency bandwidth was achieved for the asymmetric DA with a 10-W Cree GaN HEMT device in the carrier amplifier and a 25-W Cree GaN HEMT device in the peaking amplifier.[143] In this case, the Class-AB and Class-C PAs were designed to provide broadband performance using matching circuits with LF response (comprising series microstrip lines with shunt capacitors). With an optimum load-line impedance of approximately 50 Ω for the carrier device, the modified output combining network was based on two quarterwave transmission lines with the characteristic impedances of 59.16 and 41.83 Ω. The 59.16-Ω line interconnects the carrier and peaking amplifiers and inverts the 100-Ω impedance seen by the carrier device in the low-power region to a common-load impedance of 35 Ω (transformation ratio 1:2.85). The 41.83-Ω line transforms the common-load impedance to the standard load of 50 Ω. As a result, the modified DA shows wider efficiency-enhancement performance than the conventional DA, providing the drain efficiency from 41% to 55% at backoff of 5–6 dB from the maximum output power measured in the range of 42.1–45.3 dBm over the frequency bandwidth of 1.7–2.6 GHz, or 42% fractional bandwidth.

The broadband DA can be optimized at either the backoff or saturation power level. The optimization at the backoff power level implies that the optimum modulated impedance of the carrier PA can be only achieved at the backoff power level, whereas the modulated impedance at the saturation power level assumes only a suboptimum value because of the nonideal load modulation. Fig. 11.62 shows the block diagram demonstrating the design procedure associated with the backoff optimization method.[158] Here the load network of the DA consists of three two-port networks for carrier, peaking,

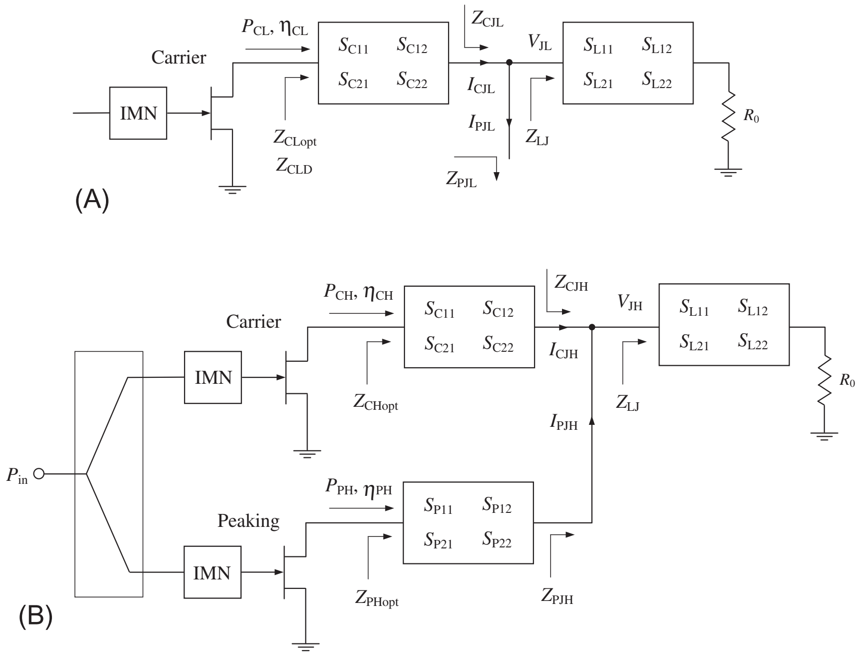

(A)
Carrier
P_{CL}, η_{CL}
IMN
S_{C11} S_{C12}
S_{C21} S_{C22}
Z_{CLopt}
Z_{CLD}
Z_{CJL}
V_{JL}
I_{CJL}
I_{PJL}
Z_{PJL}
Z_{LJ}
S_{L11} S_{L12}
S_{L21} S_{L22}
R_0
(B)
P_{in}
Carrier
Peaking
IMN
IMN
P_{CH}, η_{CH}
S_{C11} S_{C12}
S_{C21} S_{C22}
Z_{CHopt}
Z_{CJH}
V_{JH}
I_{CJH}
I_{PJH}
Z_{LJ}
S_{L11} S_{L12}
S_{L21} S_{L22}
R_0
P_{PH}, η_{PH}
S_{P11} S_{P12}
S_{P21} S_{P22}
Z_{PHopt}
Z_{PJH}

FIG. 11.62

Block diagram for design procedure using real frequency technique.

and output matching paths, whose frequency properties are described by their associated scattering parameters S_{Cij}, S_{Pij}, and S_{Lij}. The impedances Z_{CHopt} and Z_{PHopt} denote the optimized impedances of the carrier and peaking PAs at the saturation power level, the impedance Z_{CLopt} represents the optimized impedance of the carrier PA at the given backoff power level, whereas the impedances Z_{CLD} is defined as the corresponding desired impedance and Z_{PJL} represents the impedance looking into the peaking PA at the junction, when the peaking PA is turned off. During the optimization procedure, both the frequency-dependent drain efficiency and resulting output power of the DA should be as flat and as high as possible.

Generally the transducer power gain of a two-port network doubly terminated with the frequency-dependent source and load impedances Z_{G} and Z_{L} can be defined in terms of the scattering parameters as

$$G_{\mathrm{T}} = \frac{\left(1 - S_{\mathrm{G}}^2\right) |S_{21}|_{\square}^2 \left(1 - S_{\mathrm{L}}^2\right)}{|1 - S_{11} S_{\mathrm{G}}|^2 \left| 1 - \left(S_{22} + \frac{S_{21}^2 S_{\mathrm{G}}}{1 - S_{11} S_{\mathrm{G}}} \right) S_{\mathrm{L}} \right|^2}, \tag{11.40}$$

where S_{G} and S_{L} are the scattering parameters associated with the source and load reflections, respectively.[158] If either S_{G} or S_{L} is frequency independent, the double-matching solution degenerates into the simplified single-matching solution. In this case, the broadband matching is realized by applying the simplified real frequency technique with the desired frequency-dependent optimum impedances.

The design method for broadband DA at the backoff power level based on the real frequency technique is as follows:

- The scattering parameters S_{Lij} are constructed to transfer the load resistance R_0 to low impedance Z_{LJ} over the operating frequency bandwidth. The desired impedance Z_{CLD} associated with the maximum achievable drain efficiency is determined through the harmonic-balance simulation at each frequency point within the specified frequency range. Assuming the "quasi-open-circuit" impedance Z_{PJL}, the impedance Z_{CJL} is obtained based on the knowledge of Z_{LJ}. As shown in Fig. 11.62A, the two-port network $[S_{\mathrm{C}}]$ is optimized so that the transducer power gain, defined by Eq. (11.40), and drain efficiency are as flat and as high as possible.
- The desired frequency-dependent load-modulated impedance Z_{CHopt} is subjectively selected at the saturation power level that enables the calculation of Z_{CJH} and Z_{PJH} shown in Fig. 11.62B.
- The carrier PA is simulated with the frequency-dependent complex load impedance Z_{CJH} at the saturation power level. The drain efficiency η_{CH}, power P_{CH}, and current I_{CJH} at the load termination Z_{CJH} are determined through the harmonic-balance simulation.
- The peaking PA is simulated with the load termination Z_{PJH}, which is transferred to Z_{PHopt} via the two-port network $[S_{\mathrm{P}}]$. The two-port network $[S_{\mathrm{P}}]$ is optimized so that the transistor delivers flat output power around P_{PH} with the minimum drain efficiency η_{PH} over the given frequency range. The "quasi-open-circuit" requirement on Z_{PJL} is also included as an optimization boundary condition.
- The current I_{PJH} is simulated at the load termination Z_{PJH} of the peaking PA. The phase difference between currents I_{CJH} and I_{PJH} is adjusted to equalize the phases in the carrier and peaking paths by tuning the phase-compensating lines in each IMN.
- All the circuit parameters are adjusted to achieve the best performance of the broadband DA.

As an example, the symmetric DA was designed using two Cree CGH40006P GaN HEMT devices with a center bandwidth frequency of 2.6 GHz. An output impedance transformation via optimized three-section ladder *LC* structure provides better broadband matching and results in less influence of the impedance inverter over broader frequency bandwidth. By using a multisection output transmission line with different characteristic impedances, the frequency range from 2.2 to 2.96 GHz can be covered with the drain efficiency over 40% at the output power backoff level of 5–6 dB.[158] However, the measured power gain was sufficiently low, varying between 5.5 and 8.8 dB across the entire frequency range at different output power levels.

11.9.4 Dual-band parallel Doherty architecture

The classical two-stage DA has limited bandwidth capability in a low-power region as it is necessary to provide an impedance transformation from 25 to 100 Ω when the peaking amplifier is turned off, as shown in Figs. 11.63A and 11.64A, thus resulting in a loaded quality factor $Q_L = \sqrt{100/25 - 1} = 1.73$ at 3-dB output power reduction level (approximation by an L-type impedance transformer near resonant frequency[159]), which is sufficiently high for broadband operation. The parallel architecture of a two-stage DA with modified modulated load network, the block schematic of which is shown in Fig. 11.63B, can

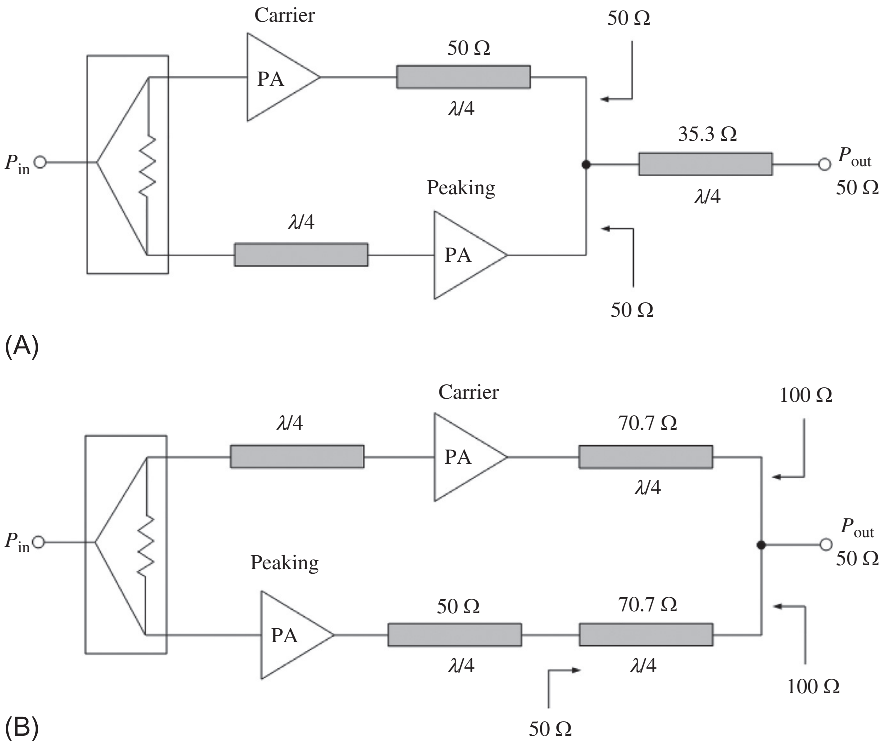


FIG. 11.63

Block diagram of conventional and modified two-stage Doherty amplifiers.

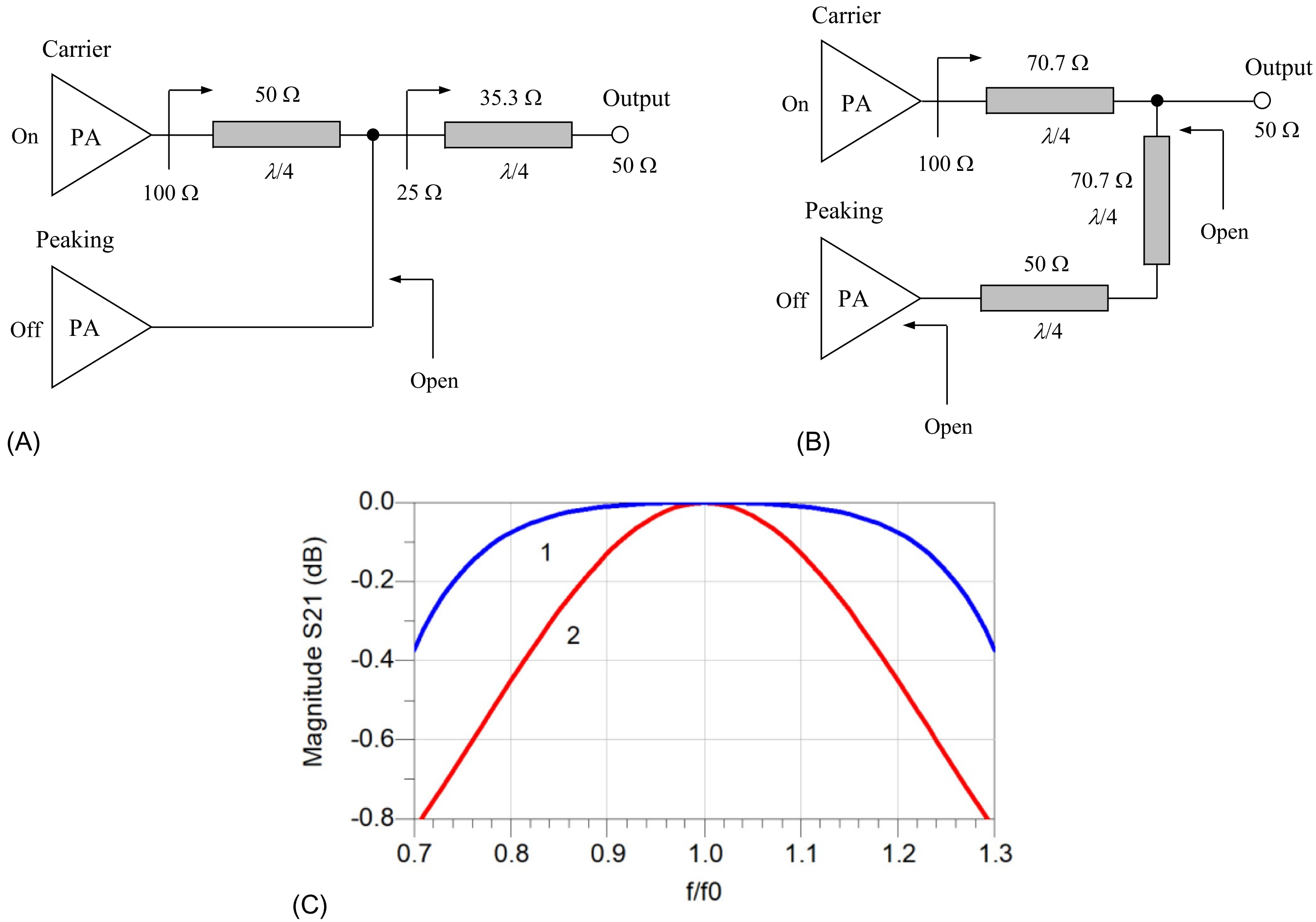

Carrier
On
PA
100 Ω
50 Ω
λ/4
25 Ω
35.3 Ω
λ/4
Output
50 Ω
Peaking
Off
PA
Open
(A)
Carrier
On
PA
100 Ω
70.7 Ω
λ/4
Output
50 Ω
70.7 Ω
λ/4
Open
Peaking
Off
PA
50 Ω
λ/4
Open
(B)
Magnitude S21 (dB)
0.0
-0.2
-0.4
-0.6
-0.8
1
2
0.7
0.8
0.9
1.0
1.1
1.2
1.3
f/f0
(C)

FIG. 11.64

Load-network schematics and broadband properties.

improve bandwidth properties in a low-power region by reducing the impedance transformation ratio by a factor of two.[160] Such an approach is very convenient for a high-power DA when the device optimum output impedances for the carrier and peaking devices are typically equal to a few ohms only. In this case, by providing the transmission-line characteristic impedances greater than the device optimum impedances, the drain efficiency of approximately 48% was achieved at the output powers above 49 dBm in a frequency bandwidth from 800 to 950 MHz for a 20-MHz WCDMA signal with a *PAR* of 7 dB after DPD linearization.[161]

In this case, the load network for the carrier amplifier consists of a single quarterwave transmission line required for impedance transformation, the load network for the peaking amplifier consists of a 50-Ω quarterwave transmission line followed by another quarterwave transmission line required for impedance transformation, and the quarterwave transmission line at the input of the carrier amplifier is necessary for phase compensation. Both impedance-transforming quarterwave transmission lines, having a characteristic impedance of 70.7 Ω each, provide a parallel connection of the carrier and peaking amplifiers in a high-power region by parallel combining of two 100-Ω impedances at their output into a 50-Ω load, with 50-Ω impedances at their inputs seen by each amplifier output. In a low-power region below output-power backoff point of −6 dB when the peaking amplifier is turned off, the required impedance of 100 Ω seen by the carrier amplifier output is achieved by using a single quarterwave transmission line with the characteristic impedance of 70.7 Ω to match with a 50-Ω load, as shown in Fig. 11.64B.

This provides a loaded quality factor $Q_L = \sqrt{100/50 - 1} = 1$, resulting in a 1.73 times wider frequency bandwidth, as shown in Fig. 11.64C by curve 1 compared with a conventional case (curve 2). Because the load network of the peaking amplifier contains two quarterwave transmission lines connected in series, an overall half-wavelength transmission line is obtained, and an open circuit at the peaking amplifier output directly translates to the load providing a significant isolation of the peaking amplifier path from the carrier amplifier path in a wide frequency range. The input in-phase divider and phase-compensating transmission line can be replaced by a broadband coupled-line 90-degree hybrid coupler.

From Fig. 11.64C, it follows that use of a parallel Doherty architecture can provide a broadband operation of 25%–30% around center bandwidth frequency with minimum variation of the load-network transfer characteristic. As a result, a dual-band operation can be easily provided by such an architecture, for example, in 1.8-GHz (1805–1880 MHz) and 2.1-GHz (2.11–2.17 GHz) or in 2.1- and 2.6-GHz (2.62–2.69 GHz) WCDMA/LTE frequency bands, respectively.

Fig. 11.65 shows the simulated circuit schematic of a dual-band parallel GaN HEMT Doherty architecture, where the carrier and peaking PAs are based on broadband transmission-line Class-E PAs. Here the input matching circuits and output load network are based on microstrip lines with their parameters corresponding to a 20-mil RO4360 substrate. The ideal broadband 90-degree hybrid coupler is used at the input to split signals between the carrier and peaking amplifying paths. The electrical lengths of both offset and combining microstrip lines were optimized to maximize efficiency at saturated and backoff output power levels.

Fig. 11.66 shows the simulation results for the corresponding small-signal *S*-parameters versus frequency demonstrating the bandwidth capability of a parallel transmission-line GaN HEMT DA covering a frequency range from 2.0 to 2.8 GHz with a power gain over 10 dB. In this case, an input return loss defined from the magnitude of S_{11} is greater than 5 dB over the frequency bandwidth of 2.1–2.9 GHz.

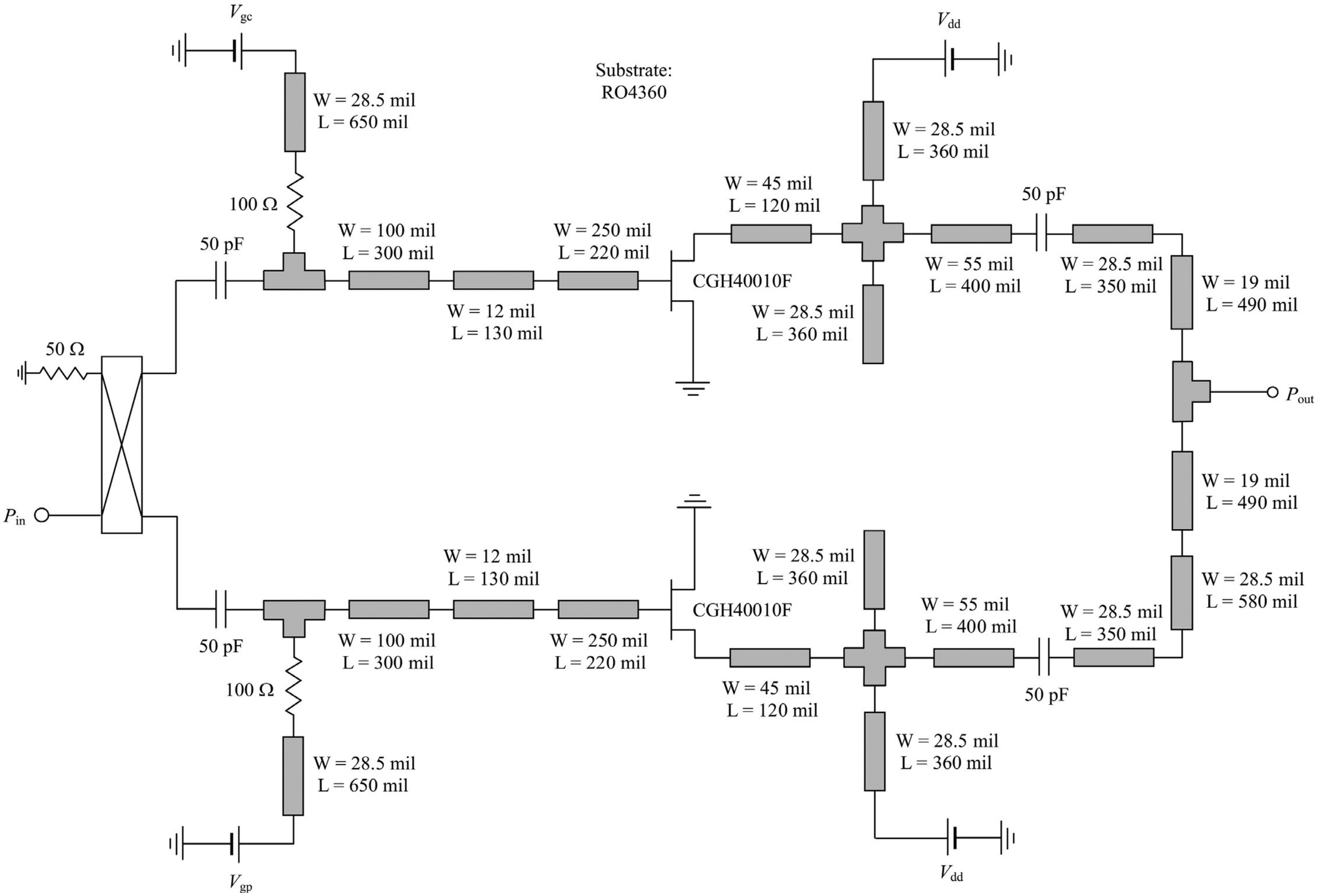

V_{gc}
W = 28.5 mil
L = 650 mil
Substrate:
RO4360
V_{dd}
W = 28.5 mil
L = 360 mil
100 Ω
W = 45 mil
L = 120 mil
50 pF
50 pF
W = 100 mil
L = 300 mil
W = 250 mil
L = 220 mil
W = 55 mil
L = 400 mil
W = 28.5 mil
L = 350 mil
W = 19 mil
L = 490 mil
CGH40010F
W = 12 mil
L = 130 mil
W = 28.5 mil
L = 360 mil
50 Ω
P_{out}
W = 19 mil
L = 490 mil
P_{in}
W = 12 mil
L = 130 mil
W = 28.5 mil
L = 360 mil
W = 28.5 mil
L = 580 mil
W = 55 mil
L = 400 mil
CGH40010F
W = 28.5 mil
L = 350 mil
50 pF
W = 100 mil
L = 300 mil
W = 250 mil
L = 220 mil
100 Ω
W = 45 mil
L = 120 mil
50 pF
W = 28.5 mil
L = 360 mil
W = 28.5 mil
L = 650 mil
V_{gp}
V_{dd}

FIG. 11.65

Circuit schematic of dual-band parallel GaN HEMT Doherty amplifier.

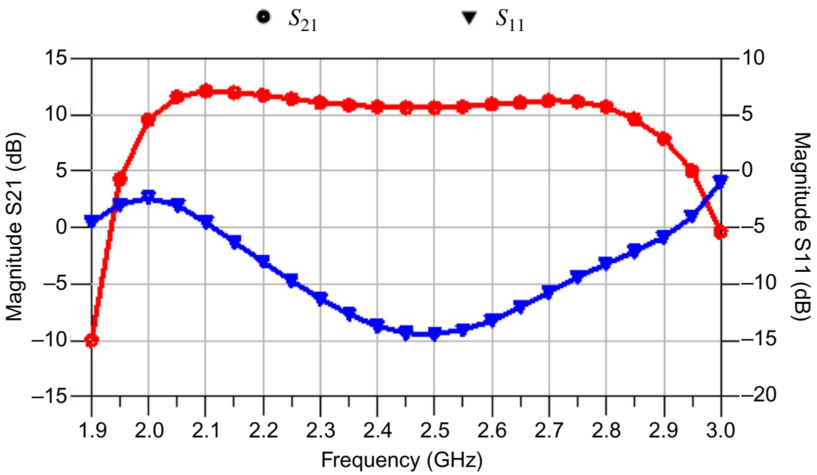


FIG. 11.66

Simulated small-signal S_{11} and S_{21} versus frequency.

The large-signal simulations versus input power were carried out at two center bandwidth frequencies of 2.14 and 2.655 GHz with optimized circuit parameters to achieve maximum performance. Fig. 11.67 shows the simulated large-signal power gain and drain efficiency of a dual-band parallel transmission-line GaN HEMT DA, with a carrier gate bias $V_{gc} = -2.45$ V, a peaking gate bias $V_{gp} = -7$ V, and a DC-supply voltage $V_{dd} = 28$ V. In this case, a linear power gain of approximately 11 dB was achieved at an operating frequency of 2.655 GHz, as shown in Fig. 11.67B, whereas a slightly higher linear power gain of approximately 12 dB was achieved at lower operating frequency of 2.14 GHz, as shown in Fig. 11.67A.[160] At the same time, the drain efficiencies of 64% and 53% were simulated at backoff output powers of 39 dBm (4-dB backoff from saturated power of 43 dBm) and 37 dBm (6-dB backoff) at both center bandwidth frequencies, respectively.

The dual-band transmission-line GaN HEMT DA was fabricated on a 20-mil RO4360 substrate. An input power splitter represents a broadband coupled-line coupler from Anaren, model 11306-3, which provides the maximum phase balance of ±5 degrees and amplitude balance of ±0.55 dB across the frequency range from 2 to 4 GHz. Fig. 11.68 shows the test board of a dual-band parallel DA based on two 10-W Cree GaN HEMT power transistors CGH40010P in metal-ceramic pill packages.[160, 162] The input matching circuit, output load network, and gate and drain bias circuits (having bypass capacitors on their ends) are fully based on microstrip lines of different electrical lengths and characteristic impedances according to the simulation setup shown in Fig. 11.65. Special care should be taken for the device implementation process to minimize the input and output lead inductances of the packaged GaN HEMT device, which can significantly affect the amplifier performance such as power gain, output power, and drain efficiency.

For a single-carrier 5-MHz WCDMA signal with a *PAR* of 6.5 dB, a drain efficiency of 45% with a power gain of approximately 10 dB and an *ACLR* lower than −30 dBc at 2.14 GHz and a drain efficiency of 40% with a power gain of approximately 11 dB and an *ACLR* approximately −30 dBc at 2.655 GHz were achieved at an average output power of 39 dBm.

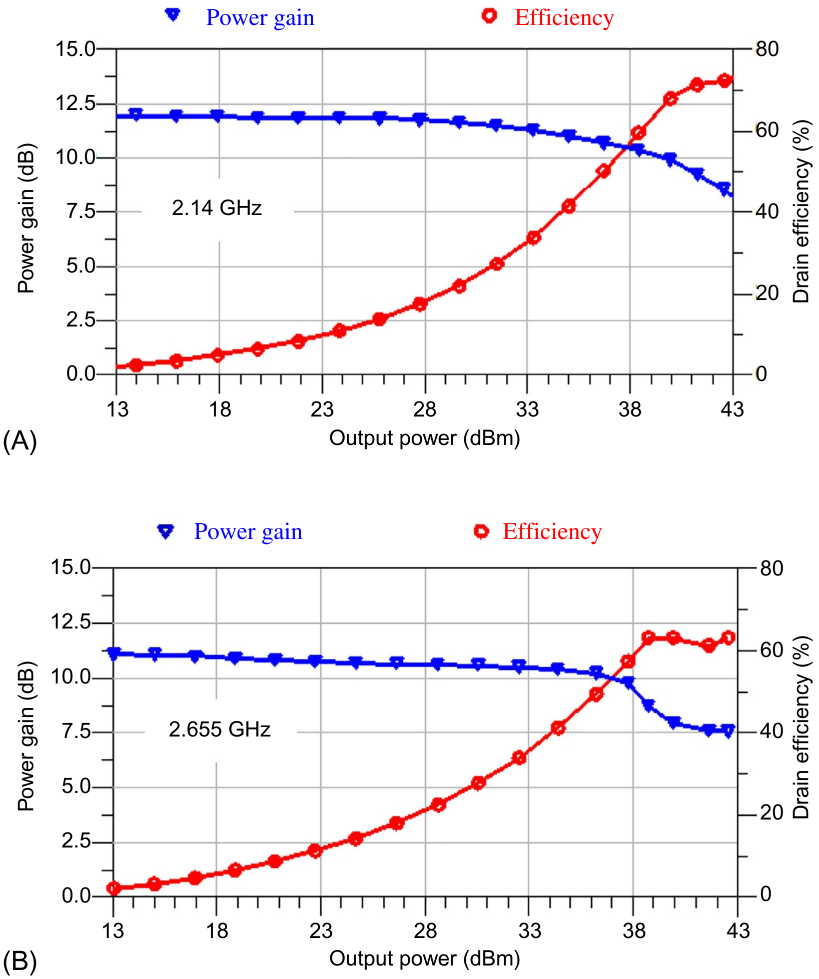


FIG. 11.67

Simulated results of dual-band parallel Doherty amplifier.

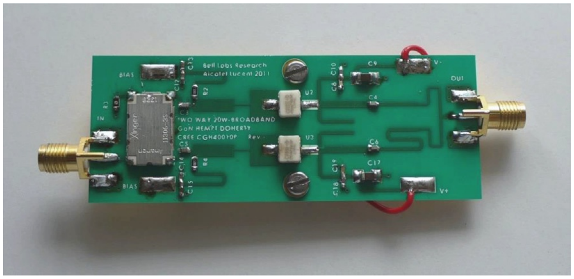


FIG. 11.68

Test board of dual-band GaN HEMT parallel Doherty amplifier.

The load network of a dual-band parallel DA, whose circuit schematic is shown in Fig. 11.65, can be simplified if two extra 35-Ω quarterwave lines ($W = 55$ mil), one in the carrier path and another at the peaking path, required in the load network to match the nominal 25-Ω Class-E load resistance to the standard 50-Ω load, can be omitted.[163] Instead, a single 50-Ω quarterwave line in the carrier path and 35-Ω quarterwave line in the peaking path in addition to offset lines can be used, although providing higher loaded quality factor $Q_L = \sqrt{100/25 - 1} = 1.73$ in a high-power region above 6-dB backoff, which results in a significant variation of the saturated power, drain efficiency, and power gain across the frequency bandwidth of 1.8–2.7 GHz.

11.9.5 Broadband inverted Doherty amplifiers

Fig. 11.69A shows the modified broadband load network of an inverted DA, which consists of a two-section transmission-line output impedance transformer, where each quarterwave transmission line has a different characteristic impedance to match first the initial 25 Ω to intermediate 35.3 Ω and then to 50-Ω load. Such 25- to 50-Ω transformer provides a wide frequency range, as shown in Fig. 11.69B by

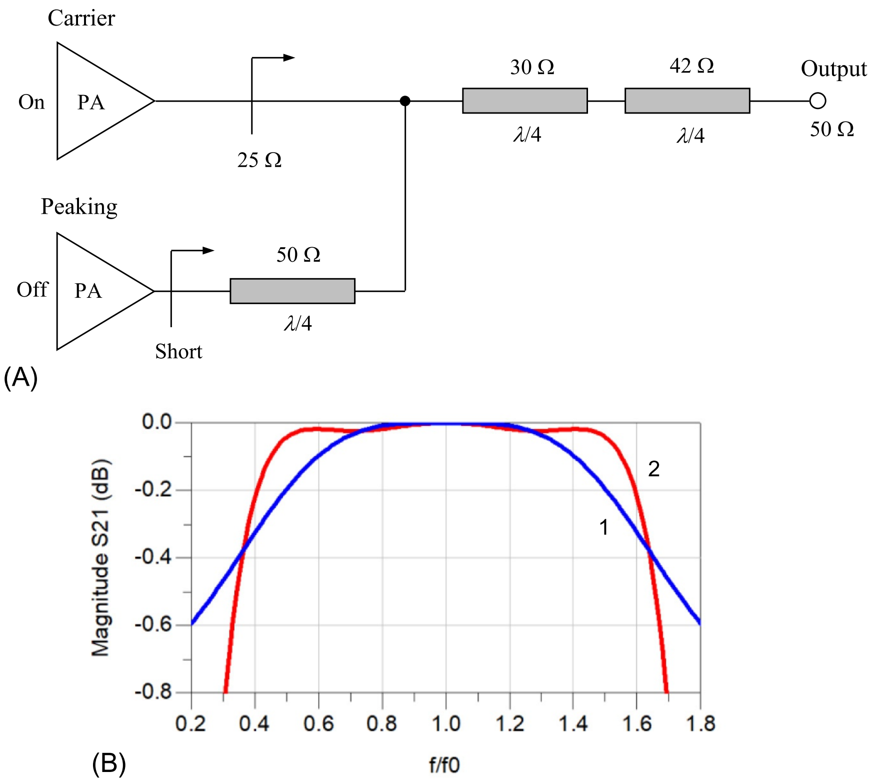


FIG. 11.69

Load-network schematic and broadband properties.

curve 1.[162] However, broader frequency range with flatter frequency response can be achieved with a quarterwave open-circuit stub connected at the input of a two-line transformer when the peaking amplifier is turned off, as shown in Fig. 11.69B by curve 2, resulting in a wider than octave bandwidth in a low-power region at output power levels less than -6 dB backoff point. In this case, it is assumed that the output matching circuit of the carrier amplifier provides ideally a broadband impedance transformation from 25 to 100 Ω or close seen by the device multiharmonic current source. At the same time, broadband performance is also provided in a high-power region when both the carrier and peaking amplifiers are turned on. Such an approach was later used to design a wideband DA operating from 3.0 to 3.6 GHz with a drain efficiency of 45.9%–50.2% and an output power of 34.1–34.6 dBm under a signal-carrier 20-MHz LTE signal with a *PAR* of 7.5 dB.[164]

Fig. 11.70 shows the simulated circuit schematic of a tri-band inverted GaN HEMT DA configuration, where the carrier and peaking amplifiers using Cree CGH40010 devices are based on the same broadband transmission-line Class-E PAs, and the broadband load network corresponds to the impedance-transforming structure shown in Fig. 11.69A.[162] The input matching circuits and output load network are based on microstrip lines with their parameters corresponding to a 20-mil RO4360 substrate. In this case, it was found that a short-circuit condition for Z_{match} is achieved when the broadband Class-E PA operating as a peaking amplifier is turned off. As result, the overall combining load network is significantly simplified, and only a small optimization of the electrical lengths of the short- and open-circuit stubs in the load networks of each carrier and peaking amplifier is required to achieve broader frequency response. The broadband 90-degree hybrid coupler is used at the input to split signals between the carrier and peaking amplifying paths and to provide a 90-degree phase shift at the input of the carrier amplifier across the entire frequency bandwidth. The impedance conditions of the peaking amplifier when it is turned off indicate nearly zero reactance at high bandwidth frequency of 2.7 GHz and increasing capacitive reactance when the operating frequency reduces to 1.8 GHz for Z_{match}, and an open-circuit condition at higher bandwidth frequencies with sufficiently high inductive reactances at lower bandwidth frequencies for Z_{peaking}. Hence, such an inverted Doherty structure is a very attractive in terms of broadband performance and can represent a very compact structure which is easily implemented in a practical board.

Fig. 11.71 shows the simulation results for the small-signal S_{21}-parameters versus frequency, demonstrating the bandwidth capability of a modified inverted transmission-line GaN HEMT DA, which potentially can cover a wide frequency range of 1.6–3.0 GHz with a power gain over 11 dB.

Fig. 11.72 shows the simulated large-signal power gain and drain efficiency of a transmission-line tri-band inverted GaN HEMT DA, with a carrier gate bias $V_{\text{gc}} = -2.45$ V, a peaking gate bias $V_{\text{gp}} = -7.45$ V, and a DC-supply voltage $V_{\text{dd}} = 28$ V. In this case, a linear power gain of approximately 11.5 dB was achieved at higher bandwidth frequencies of 2.655 and 2.14 GHz, while a slightly higher linear power gain of approximately 13 dB was achieved at lower bandwidth frequency of 1842.5 MHz. At the same time, the drain efficiencies of 71.5%, 69.0%, and 64.0% at backoff output powers of 40 dBm (4-dB backoff from saturated power of 44 dBm) and 59.0%, 57.0%, and 53.5% at backoff output powers of 38 dBm (6-dB backoff) were simulated at center bandwidth frequencies of 1842.5, 2140, and 2655 MHz, respectively. Here the drain efficiency with a maximum value at near 4-dB backoff output power at low bandwidth frequency of 1842.5 MHz and at medium bandwidth frequency of 2.14 GHz are clearly seen, while high efficiency maintains almost constant at high output powers at high bandwidth frequency of 2.655 GHz.

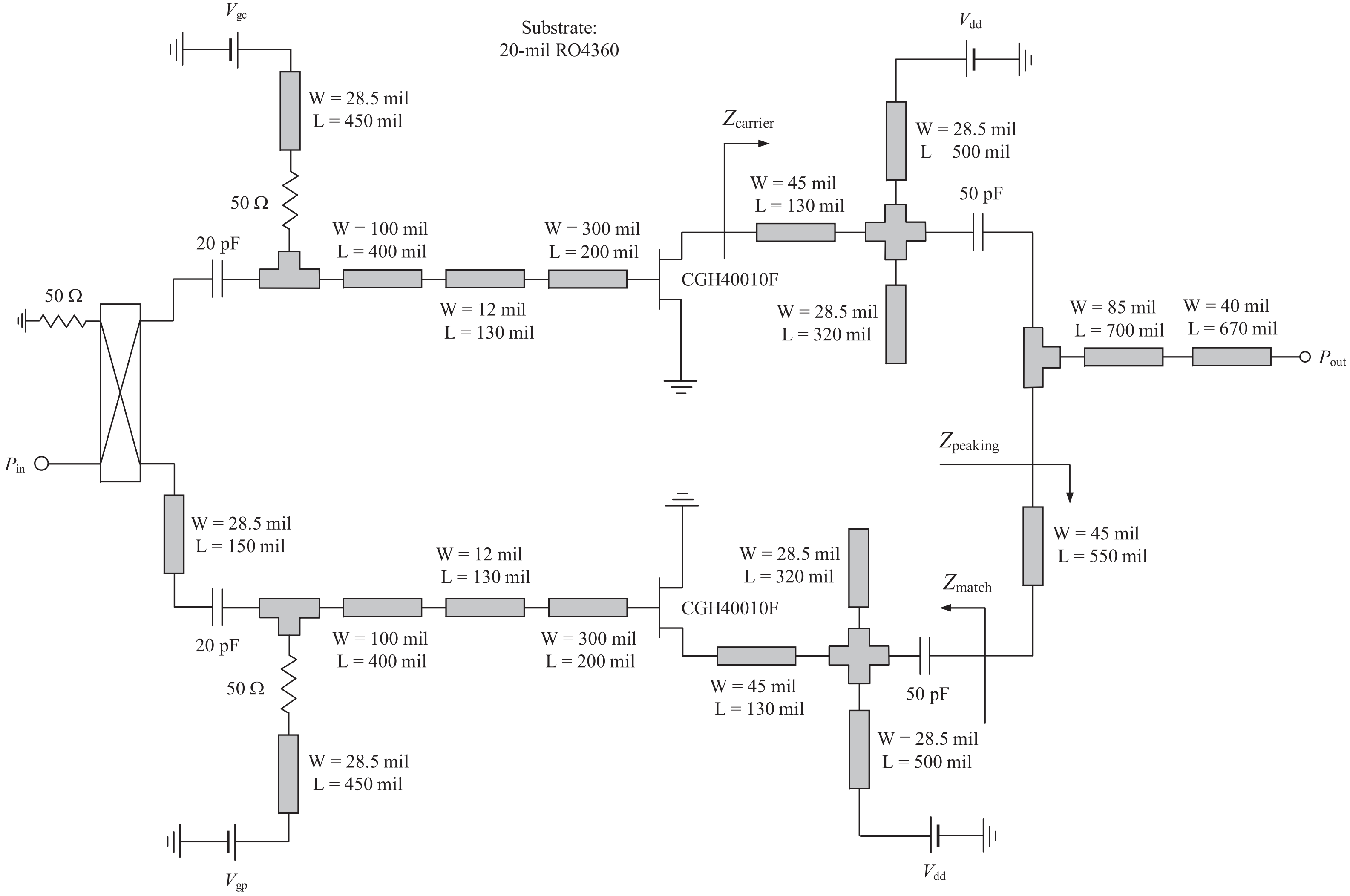

V_{gc}
Substrate:
20-mil RO4360
V_{dd}
W = 28.5 mil
L = 450 mil
$Z_{carrier}$
W = 28.5 mil
L = 500 mil
W = 45 mil
L = 130 mil
50 Ω
50 pF
W = 100 mil
L = 400 mil
W = 300 mil
L = 200 mil
20 pF
CGH40010F
50 Ω
W = 12 mil
L = 130 mil
W = 28.5 mil
L = 320 mil
W = 85 mil
L = 700 mil
W = 40 mil
L = 670 mil
P_{out}
$Z_{peaking}$
P_{in}
W = 28.5 mil
L = 150 mil
W = 45 mil
L = 550 mil
W = 12 mil
L = 130 mil
W = 28.5 mil
L = 320 mil
Z_{match}
CGH40010F
20 pF
W = 100 mil
L = 400 mil
W = 300 mil
L = 200 mil
50 Ω
W = 45 mil
L = 130 mil
50 pF
W = 28.5 mil
L = 500 mil
W = 28.5 mil
L = 450 mil
V_{dd}
V_{gp}

FIG. 11.70

Circuit schematic of tri-band inverted GaN HEMT Doherty amplifier.

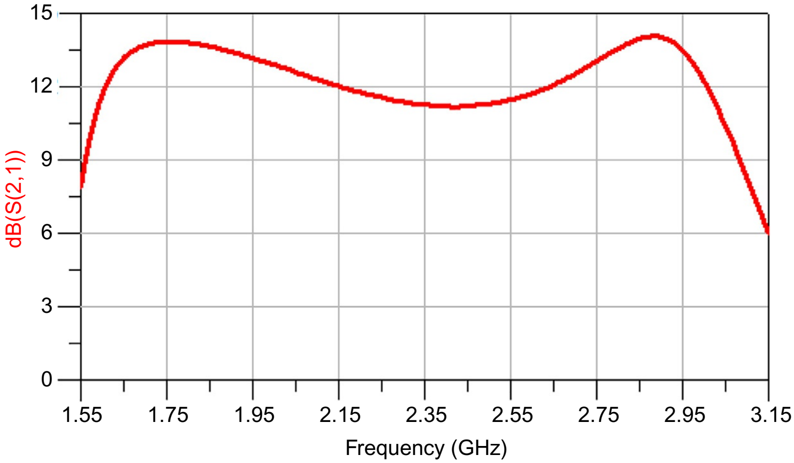


FIG. 11.71

Simulated small-signal S_{21} versus frequency.

The tri-band transmission-line GaN HEMT DA was fabricated on a 20-mil RO4360 substrate. An input splitter represents a broadband 3-dB hybrid coupler from Anaren, model X3C17A1-03WS, which provides the maximum phase balance of ±5 degrees and amplitude balance of ±0.5 dB across the frequency range of 690–2700 MHz. Fig. 11.73 shows the test board of a tri-band inverted DA based on two 10-W Cree GaN HEMT CGH40010P devices in metal-ceramic pill packages.[162] The input matching circuit, output load network, and gate and drain bias circuits (having bypass capacitors on their ends) are fully based on microstrip lines of different electrical lengths and characteristic impedances according to the simulation setup shown in Fig. 11.70. Special care should be taken for device implementation process to minimize the input and output lead inductances of the packaged GaN HEMT device. Additional tuning in the input matching circuits was necessary to maximize a power gain over the entire frequency range.

For a single-carrier 5-MHz WCDMA signal with a *PAR* of 6.5 dB, the drain efficiencies of 58%, 50%, and 42% at an average output power of 38 dBm with a power gain of more than 11 dB were achieved at the operating frequencies of 1.85, 2.15, and 2.65 GHz, respectively, with the *ACLR* (at 5-MHz offset) measured from −32 dBc at 1.85 GHz to −37 dBc at 2.65 GHz. The gate bias voltages for carrier (Class-AB mode with a quiescent current of 100 mA) and peaking (Class-C mode) amplifiers were the same for all three frequencies. Similar results with an output power of approximately 40 dBm and drain efficiency of 45%–55% for a single-carrier 5-MHz 6.5-dB WCDMA signal with an *ACLR* of approximately −30 dBc across the frequency bandwidth of 1.7–2.6 GHz were obtained for an inverted DA based on two Cree GaN HEMT CGH40010F devices with an input two-section Wilkinson divider and open-circuit stubs for broadband matching in the load network.[165]

A high-power operation of the GaN HEMT device can be achieved with wider gate periphery resulting in a greater output power capability in a given package. The corresponding increase in a gate-source capacitance when multiplicity of the basic device cells is connected in parallel reduces the input impedance to very low values, close to one or a few tenths of ohm. Therefore it is very important for

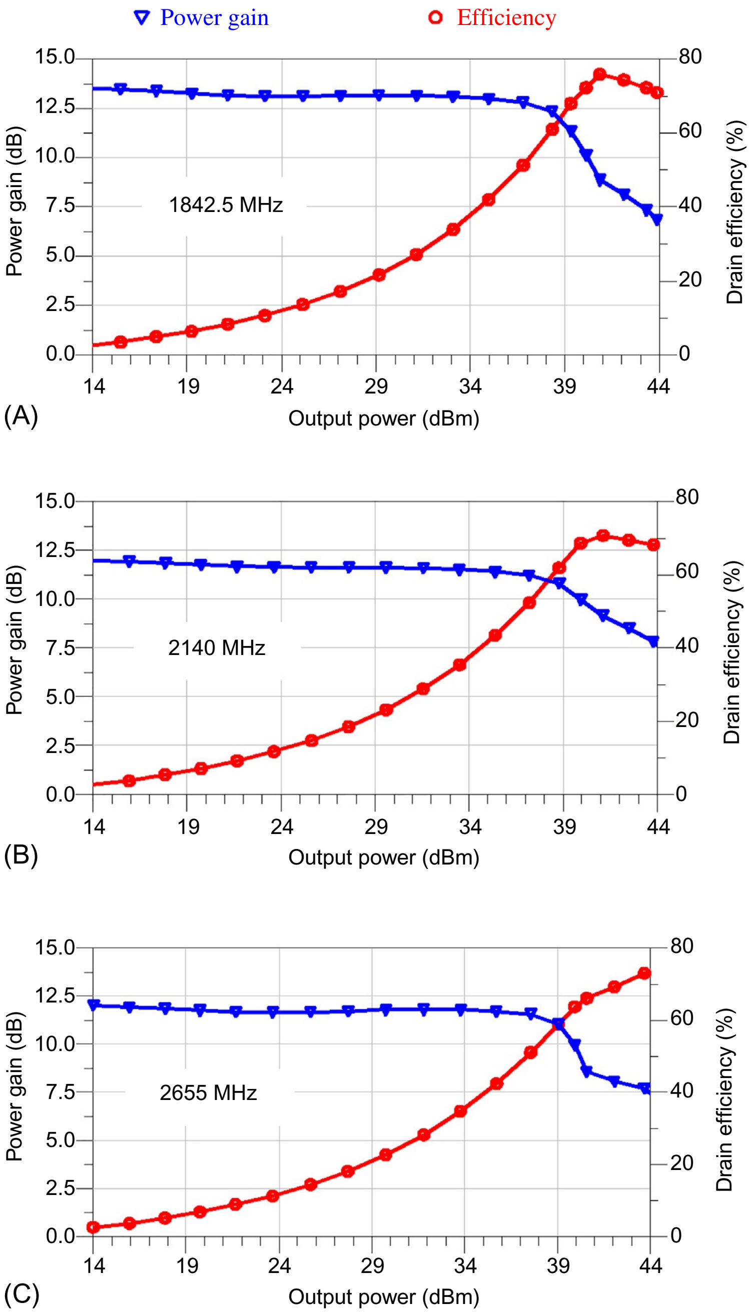


FIG. 11.72

Simulated power gain and drain efficiencies of tri-band inverted Doherty amplifier.

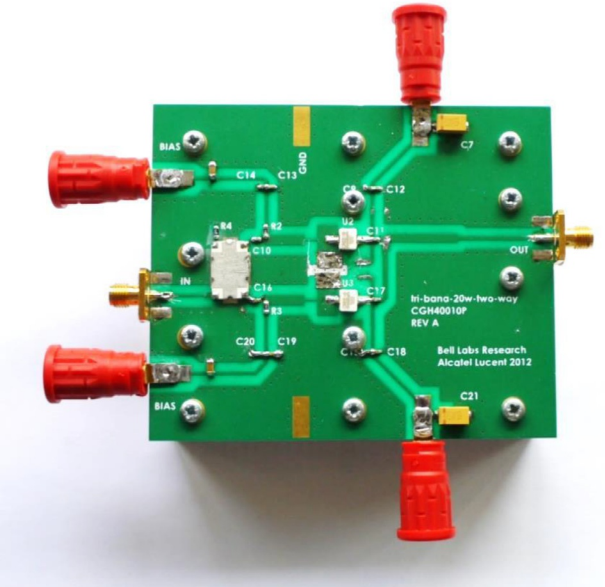


FIG. 11.73

Test board of tri-band inverted GaN HEMT Doherty amplifier.

matching circuits to be partly implemented inside the device package to achieve an average output power of 20 W (43 dBm) and higher. Fig. 11.74A shows the complete structure of the device inside the package with input matching elements and the small-signal S_{11}-parameters at the input of the internal input matching circuit including package leadframe.[166] Here the Sumitomo 50-V device is composed of six basic 15-W GaN HEMT cells connected in parallel and capable to provide the output power greater than 80 W at saturation across the entire frequency bandwidth of 1.8–2.7 GHz. A three-section microstrip transformer was implemented using an alumina substrate with high permittivity of 250 and thickness of 0.16 mm for compact structure to transform the device input impedance to the input impedance of 10 Ω with the S_{11} magnitude less than −25 dB. Fig. 11.74B shows the schematic diagram of an inverted broadband DA configuration with an impedance transformer based on a quarterwave line connected to the output of the peaking amplifier.

To better understand the operation principle of an inverted DA, consider separately the load network shown in Fig. 11.75A, where the peaking amplifier is turned off. In a low-power region the phase adjustment of the offset line with electrical length θ causes the peaking amplifier to be short-circuited (ideally equal to 0 Ω), and the matching circuit in conjunction with offset line provides the required impedance transformation from 25 Ω to the high output impedance Z_{out} seen by the carrier device output at the 6-dB power backoff (ideally equal to 100 Ω with a quarterwave transformer), as shown in Fig. 11.75B. In this case, the short circuit at the end of the quarterwave line transforms to the open circuit at its input so that it prevents power leakage to the peaking amplifying path when the peaking transistor is turned off. In a high-power region, both carrier and peaking amplifiers are operated in a

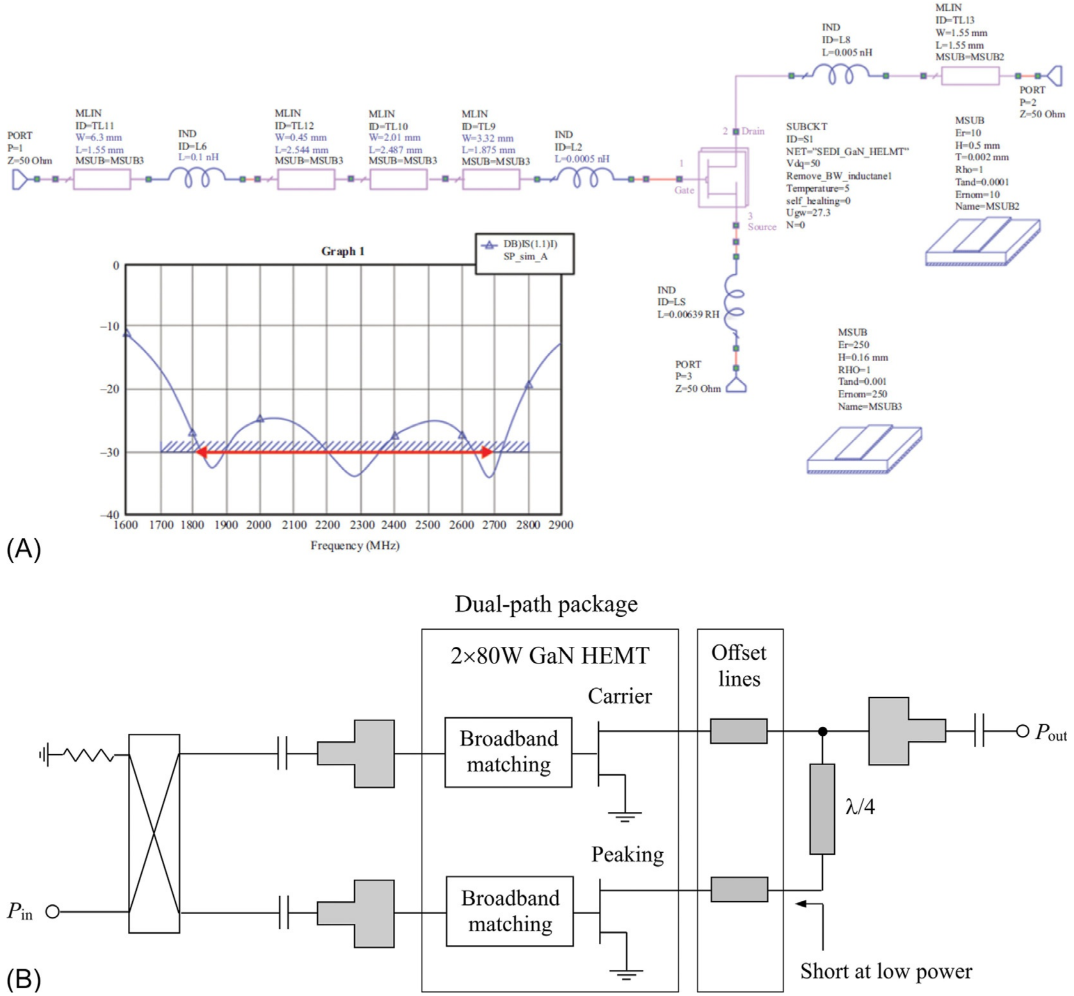

PORT
P=1
Z=50 Ohm
MLIN
ID=TL11
W=6.3 mm
L=1.55 mm
MSUB=MSUB3
IND
ID=L6
L=0.1 nH
MLIN
ID=TL12
W=0.45 mm
L=2.544 mm
MSUB=MSUB3
MLIN
ID=TL10
W=2.01 mm
L=2.487 mm
MSUB=MSUB3
MLIN
ID=TL9
W=3.32 mm
L=1.875 mm
MSUB=MSUB3
IND
ID=L2
L=0.0005 nH
IND
ID=L8
L=0.005 nH
MLIN
ID=TL13
W=1.55 mm
L=1.55 mm
MSUB=MSUB2
PORT
P=2
Z=50 Ohm
2 Drain
1 Gate
3 Source
SUBCKT
ID=S1
NET="SEDI_GaN_HELMT"
Vdq=50
Remove_BW_inductane1
Temperature=5
self_healting=0
Ugw=27.3
N=0
MSUB
Er=10
H=0.5 mm
T=0.002 mm
Rho=1
Tand=0.0001
Ernom=10
Name=MSUB2
IND
ID=LS
L=0.00639 RH
PORT
P=3
Z=50 Ohm
MSUB
Er=250
H=0.16 mm
RHO=1
Tand=0.001
Ernom=250
Name=MSUB3
Graph 1
DB)IS(1.1)I)
SP_sim_A
0
−10
−20
−30
−40
1600 1700 1800 1900 2000 2100 2200 2300 2400 2500 2600 2700 2800 2900
Frequency (MHz)
(A)
Dual-path package
2×80W GaN HEMT
Offset lines
Carrier
Broadband matching
Peaking
Broadband matching
P_{out}
$\lambda/4$
P_{in}
Short at low power
(B)

FIG. 11.74

Block schematic of high-power broadband inverted Doherty amplifier.

50-Ω environment in parallel, and the output quarterwave line with the characteristic impedance of 35.3 Ω transforms the obtained 25 Ω to the required 50-Ω load.

The impedance conditions at different points of the load network of the peaking amplifier when it is turned off are shown in Fig. 11.76, where Z_{match} shown in Fig. 11.76A indicates low reactance (short) at the output of the load network over the required frequency range from 1.8 to 2.7 GHz, having near zero reactance at midband frequency with some inductive and capacitive reactances when operating frequency approaches to the bandwidth edges. However, by using a series transmission line of a quarter-wavelength long at high bandwidth frequency, an open-circuit condition is provided at higher bandwidth frequencies with sufficiently high inductive and capacitive reactances across the frequency

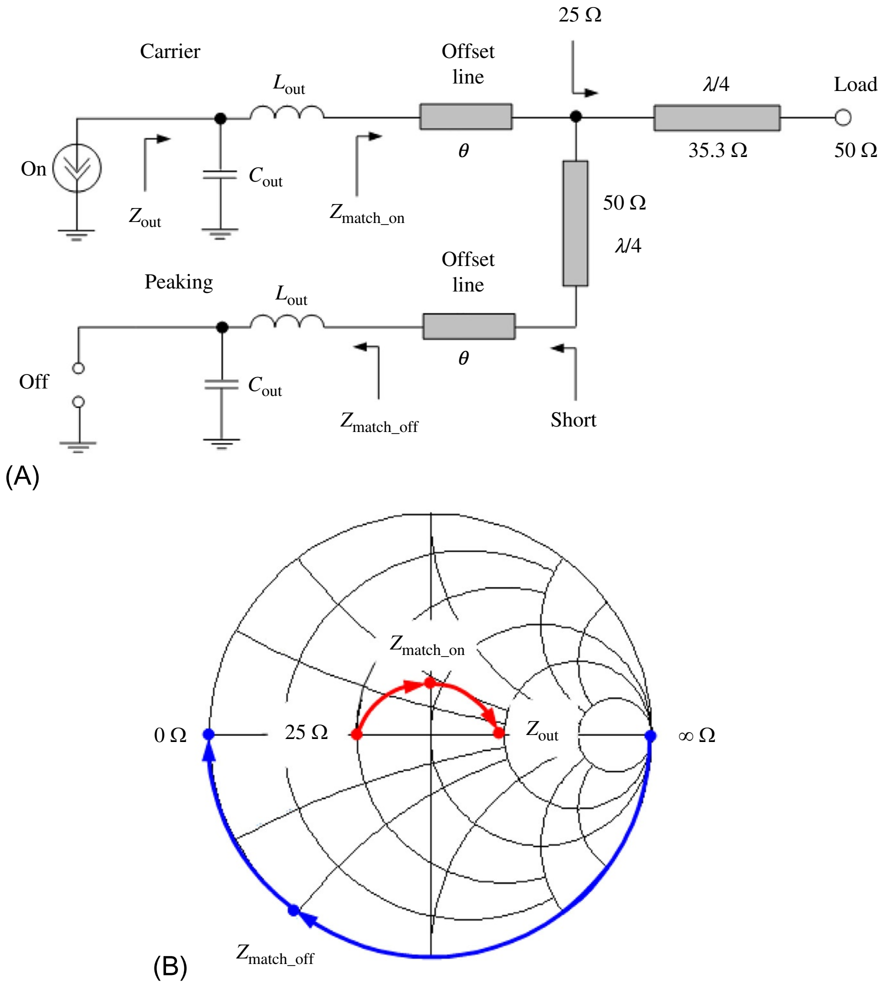

25 Ω
Carrier
L_{out}
Offset line
λ/4
Load
On
Z_{out}
C_{out}
θ
35.3 Ω
50 Ω
Z_{match_on}
50 Ω
λ/4
Peaking
L_{out}
Offset line
Off
C_{out}
θ
Z_{match_off}
Short
(A)
Z_{match_on}
0 Ω
25 Ω
Z_{out}
∞ Ω
Z_{match_off}
(B)

FIG. 11.75

Load-network schematic and impedances.

bandwidth, indicating by $Z_{peaking}$ shown in Fig. 11.76B. Hence the broadband performance of such an inverted Doherty structure can potentially be achieved in a practical realization.

Fig. 11.77A shows the load-network equivalent circuit for the carrier PA with a frequency behavior of the impedance $Z_{carrier}$ seen by the carrier device, the real component of which slightly varies approximately 10 Ω, as shown in Fig. 11.77B. This means that, taking into account the device output shunt capacitance C_{out} of approximately 5 pF and series output inductance L_{out} provided by the overall bondwire and package leadframe inductances, the impedance seen by the device multiharmonic current source at the fundamental frequency across the entire frequency bandwidth of 1.8–2.7 GHz has been increased by two times from initial 5 Ω at the input of the broadband output impedance transformer,

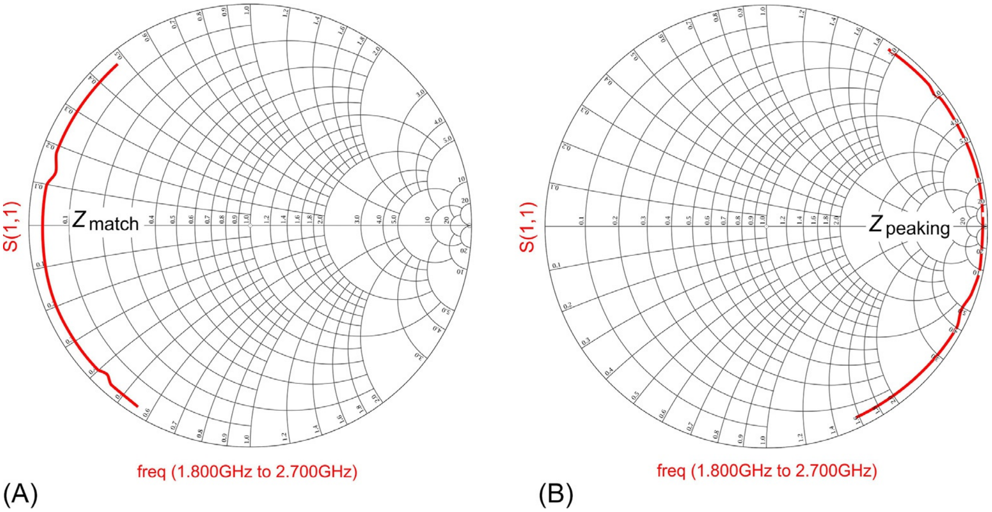


FIG. 11.76

Impedances for peaking amplifier.

which is high enough to achieve high efficiency at backoff output power levels. In this case, the device output capacitance and bondwire inductor constitute a low-pass L-type matching section to increase the load impedance seen internally by the device multiharmonic current source at the fundamental frequency.

The test board of a tri-band inverted DA based on two 80-W Sumitomo GaN HEMT power transistors with internal input matching in metal-ceramic flange packages was fabricated on a 20-mil RO4350 substrate, as shown in Fig. 11.78A. An input splitter represents a broadband 90-degree hybrid coupler from Anaren, model X3C17A1-03WS, which provides the maximum phase balance of ±5 degrees and amplitude balance of ±0.5 dB across the frequency range of 690–2700 MHz. The input matching circuit, output load network, and gate and drain bias circuits (having bypass capacitors on their ends) were fully based on microstrip lines of different electrical lengths and characteristic impedances. The three-section microstrip line provides the broadband output matching with a 50-Ω load. Special care was taken for device implementation process to minimize the output lead inductances of the packaged GaN HEMT device, with some tuning of the parameters of the impedance transformer using copper foil.

Fig. 11.78B shows the measured power gain and drain efficiency of a transmission-line GaN HEMT inverted DA across the entire frequency bandwidth for five frequencies. In this case, a power gain of more than 9 dB was achieved in a frequency range of 1.8–2.7 GHz.[166] At the same time, the drain efficiencies over 55% at an output power P_{3dB} corresponding to 3-dB gain compression point and approximately 50% at 7-dB backoff output powers were measured across the entire frequency bandwidth, with a maximum drain efficiency exceeding 70% at lower bandwidth frequencies below 1.95 GHz and peak efficiency points at maximum backoff output powers of approximately 6 dB over the entire frequency range. For concurrent transmission of a 4-carrier GSM signal and 10-MHz LTE signal with a *PAR* of 8 dB, the drain efficiency of 51% with an average total output power of 45.5 dBm (18.2 W for

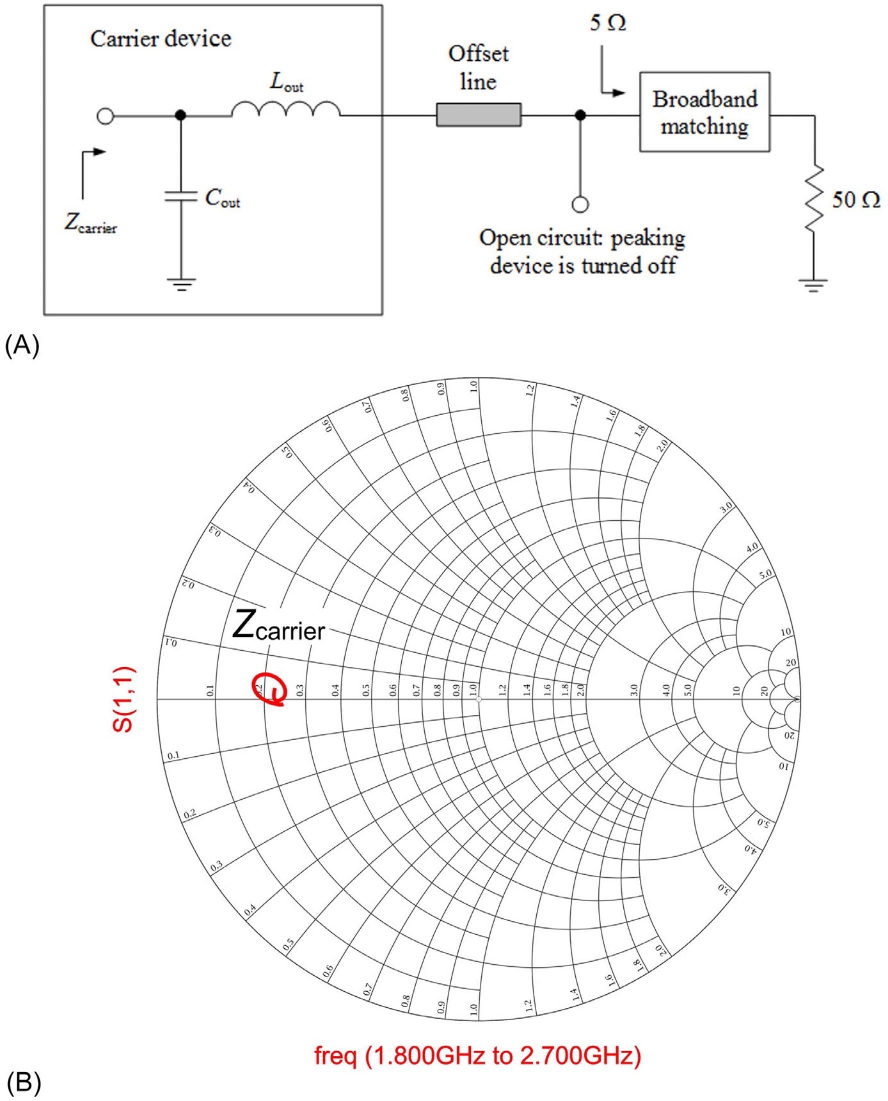

Carrier device
L_{out}
C_{out}
$Z_{carrier}$
Offset line
5 Ω
Broadband matching
50 Ω
Open circuit: peaking device is turned off
(A)
Zcarrier
S(1,1)
freq (1.800GHz to 2.700GHz)
(B)

FIG. 11.77

Matching network and load impedance for carrier amplifier.

GSM signal and 17 W for LTE signal) was achieved, with the out-of-band intermodulation level lower than −70 dBc for a 4-carrier GSM signal and *ACLR* lower than −57 dBc for a single-carrier 10-MHz LTE signal after dual-band DPD linearization. By using similar approach for designing a broadband inverted DA based on two Cree GaN HEMT CGHV40100 devices with additional harmonic tuning, a drain efficiency of 40%–50.2% at 6-dB backoff with a saturation output power of 52.7–54.3 dBm was

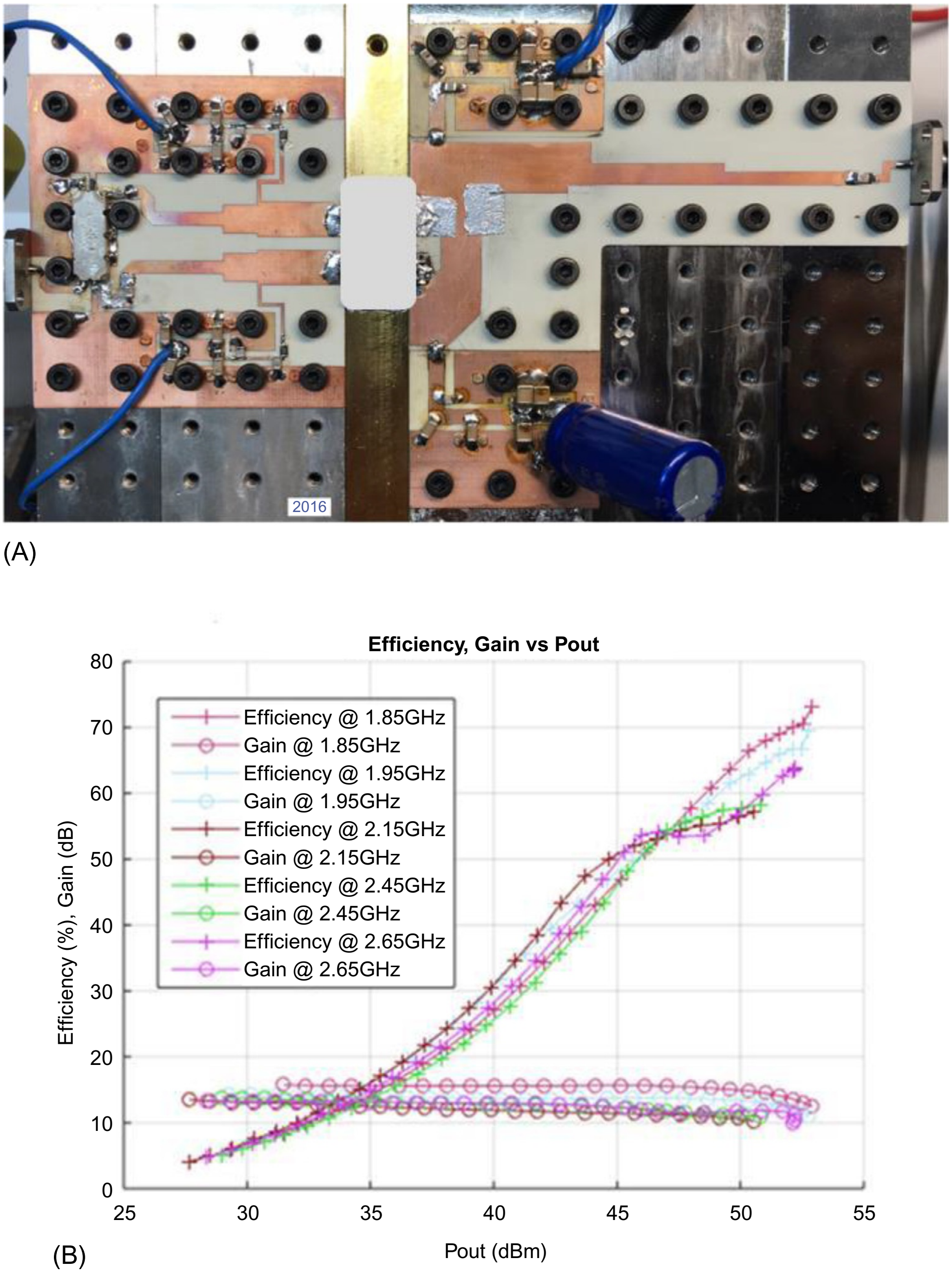


FIG. 11.78

Test board and performance of broadband inverted Doherty amplifier based on two 80-W Sumitomo GaN HEMT devices.

obtained across the frequency bandwidth of 1.7–2.7 GHz, with a drain efficiency approximately 45% at an average output power of 46 dBm for a single-carrier 10-MHz LTE signal with a *PAR* of 7.5 dB.[167]

An additional difficulty to design the broadband transistor PA apart from the broadband impedance transformation with large impedance ratio and prescribed reactive constraints is that the matching networks must be designed with prescribed tapered magnitude characteristics to compensate for the transistor gain roll-off at higher frequencies that is inherent with any type of transistors. The gain tapering is a direct consequence of the fact that the transistor maximum available gain decreases with increasing frequency. Thus for a flat overall gain response, matching networks with tapered magnitude characteristics must be used, where the exact frequency dependence of the taper or gain slope varies with specific types of transistors. Besides, for better spectral purity, the broadband load network should be designed using both low-pass and high-pass filter sections to additionally suppress the LF mixing products and HF intermodulation and harmonic components.

The bandpass filtering can be applied to the stepped transmission line based on three quarterwave lines with different characteristic impedances shown in Fig. 11.79A and achieved by replacing the second quarterwave line by the low-pass L-type section with short series transmission line and shunt capacitor (indicated with parasitic inductance) and the third quarterwave transmission line by the high-pass L-type section with series capacitor and shunt transmission line, as shown in Fig. 11.79B. In this case, the smaller overall size of the load network will be achieved. To compare the spectral performance of the broadband inverted DA without and with additional harmonic suppression, the two 20-MHz two-tone signals separated by 650 MHz were used at the input of an inverted 1.8–2.7 GHz high-power GaN HEMT DA to provide a total average output power of more than 46 dBm. The simulation results show that significant suppression of the envelope and intermodulation components below 1 GHz by more than 12 dB and harmonic and intermodulation components above 5 GHz by more than 20 dB can be achieved. In the latter case, the self-resonant condition of the shunt capacitor is of great importance to minimize the higher-order harmonic and intermodulation components.

Fig. 11.80A shows the schematic diagram of an inverted broadband DA configuration based on two 120-W GaN HEMT devices in a single package with internal input matching and a quarterwave line connected to the output of the peaking amplifier. Similarly the external input broadband matching technique using two quarterwave lines with different characteristic impedances in each carrier and peaking amplifying path and the output broadband impedance-transforming network consisting of three quarterwave lines with different values of their characteristic impedances line were used to cover the frequency range of 1.8–2.7 GHz. Fig. 11.80B shows the measured power gain and drain efficiency of such a tri-band transmission-line GaN HEMT inverted DA fabricated on a 20-mil RO4350 substrate across the frequency bandwidth of 1.8–2.7 GHz. In this case, a linear power gain of more than 13 dB was achieved in an entire frequency range. At the same time, the drain efficiencies over 65% at saturation power $P_{3\text{dB}} \geq 54$ dBm and more than 50% at 7-dB backoff output powers were measured across the entire frequency bandwidth at a DC-supply voltage of 55 V, with a maximum drain efficiency of approximately 70% at higher bandwidth frequencies.[168] Much more compact structure can be achieved by replacing a quarterwave inverter in a peaking amplifying path by a compensation network with a series capacitor and a shunt stub to provide an open circuit seen from the carrier path when the carrier amplifier is turned off.[169] However, in this case, a peak output power of 53–54 dBm was achieved with a drain efficiency of 48%–54% at 6-dB power backoff across the frequency bandwidth of 1.8–2.7 GHz, and a drain efficiency of 42.7%–47.6% was measured at an average output power of 46 dBm with an *ACLR* better than −50 dBc for a single-carrier 10-MHz LTE signal with a *PAR* of 7.5 dB.

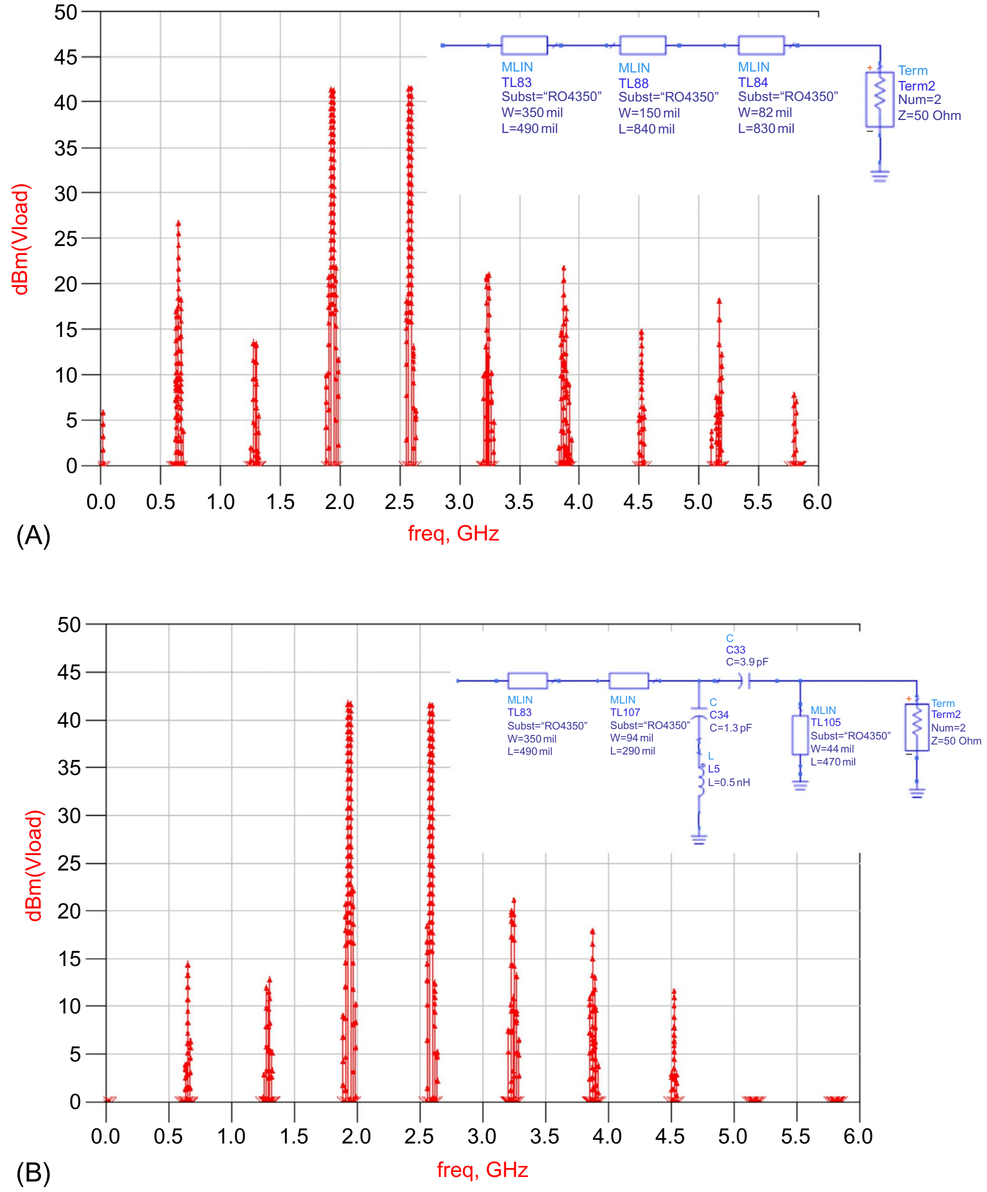


FIG. 11.79

Spectral performance of broadband inverted Doherty amplifier (A) without and (B) with additional harmonic suppression.

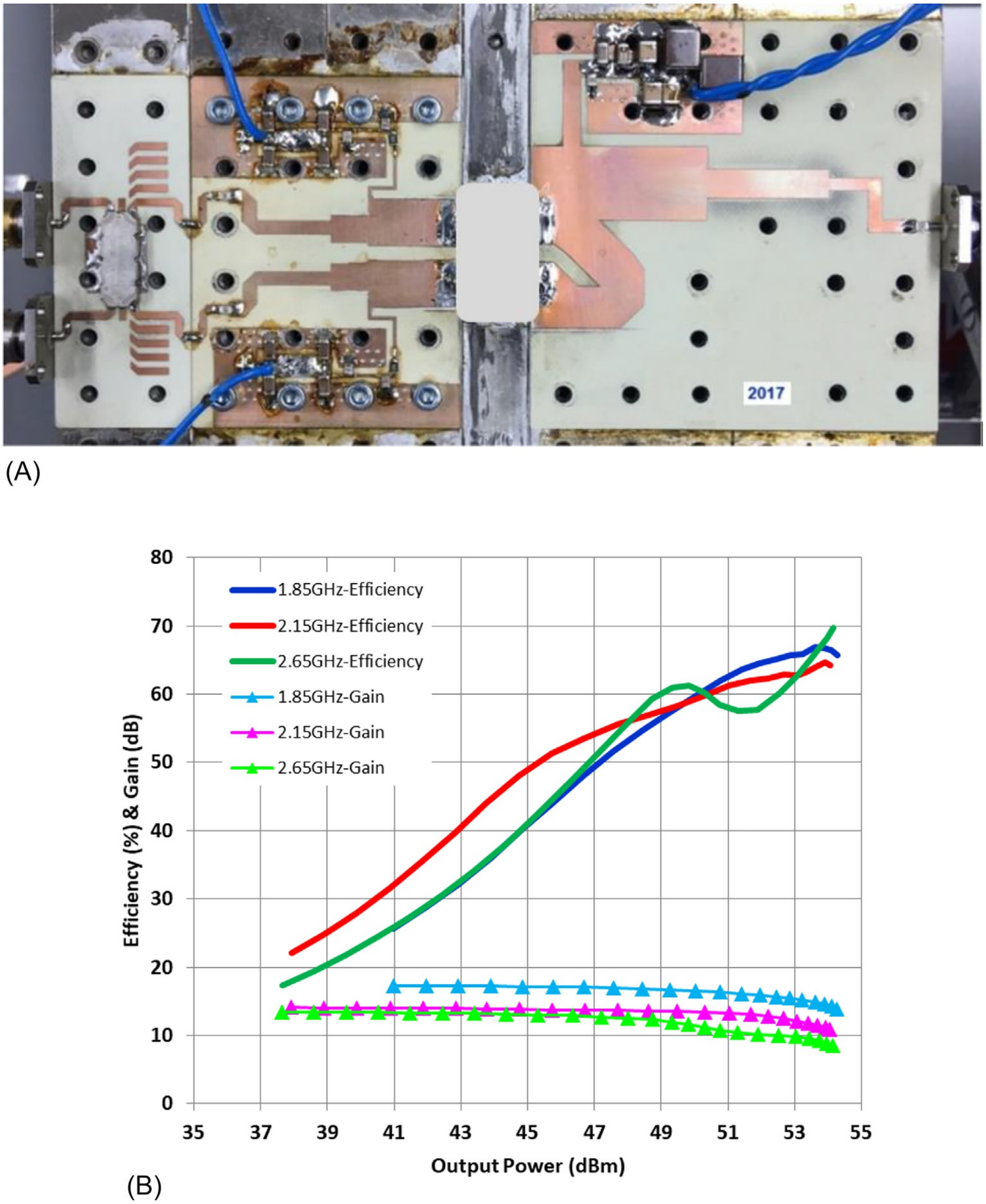


FIG. 11.80

Test board and performance of broadband inverted Doherty amplifier based on two 120-W Sumitomo GaN HEMT devices.

As a result of technical changes in telecommunications, especially related to a switchover to digital television, large part of frequency spectrum including analog TV channels below 700 MHz have become free because digital transmissions can be packed in into adjacent channels and the whole band can be compressed into fewer channels, while the rest ones can be used for mobile communications. Fig. 11.81A shows the test board of an inverted DA based on two 10-W Cree GaN HEMT CGH40010P devices using a 20-mil RO4360 substrate intended to operate across the frequency bandwidth of 470–700 MHz. An input splitter represents a broadband 3-dB hybrid coupler from Anaren, model 1F1304-3S, which provides the maximum phase balance of ±3° and amplitude balance of ±0.5 dB across the frequency range of 470–860 MHz. Because the lengths of the microstrip lines in a load network including DC-supply lines, matching circuits and impedance inverter are sufficiently long at these frequencies, each of them represents a meander-type line to minimize overall dimension. The output impedance transformer was implemented based on a four-stepped microstrip line to satisfy bandwidth requirements. An additional tuning was provided in the load network to optimize power gain and efficiency over the required frequency range. Preliminary, a drain efficiency over 55% was simulated at 37.5 dBm with a saturated power of 43.5–44 dBm and a linear power gain of 12 dB and higher, as shown in Fig. 11.81B. For a single-carrier 5-MHz WCDMA signal with a *PAR* of 6.5 dB, the drain efficiencies over 50% at an average output power of 37 dBm was measured across the frequency bandwidth of 470–700 MHz, with an *ACLR* better than −35 dBc.

Fig. 11.82 shows the demonstration board of a high-power DA based on a balanced NXP BLF888D transistor intended to cover a full UHF TV bandwidth of 470–803 MHz.[170–172] Here, each of two output DC-supply inductors connected in parallel to the corresponding device drain-source capacitance C_{ds} determines the LF resonance, which can cause the parasitic oscillations. Therefore it should be a compromise between influence of this inductance on the RF amplifying path when the inductance is too small and a sufficiently low resonance condition when the inductance is too high that can affect modulation bandwidth with increased memory effects. To improve bandwidth properties, an impedance inverter providing wider frequency bandwidth was used by adding a half-wave transmission line at the output of the peaking amplifier which can also flatten the efficiency bandwidth based on a reactance compensation due to open-circuit half-wave line operating as a parallel resonant circuit when the peaking amplifier is turned off.

In a practical implementation, such a configuration represents structurally an inverted DA with a quarterwave line at the output of a peaking amplifying path, where the required impedance transformation in the carrier amplifying path with the resulting open-circuit impedance condition seen from the main (carrier) path when the peaking device is turned off is provided in conjunction with the device shunt drain-source capacitances and series packaged inductances with additional external lines. In this case, the input quarterwave line should be included at the input of the main (carrier) amplifier for proper phase compensation between carrier and peaking amplifying paths. A two-section Wilkinson divider with meandered quarterwave microstrip lines isolates the carrier and peaking amplifying paths from each other over the desired bandwidth to minimize the impact of input reflections. To match the combining point impedance of 12.5 Ω to a standard 50-Ω load, a wideband multisection microstrip line was used. As a result, a drain efficiency of 38%–47% at an average outpower of 115 W was achieved satisfying the linearity requirements with an *ACLR* of −38 dBc over the entire bandwidth of 470–803 MHz for an input digital video broadcasting-terrestrial (DVB-T) signal with a *PAR* of 9.5 dB, with a peak output power of more than 750 W. Higher output power with narrower frequency bandwidths can be achieved by using a more powerful BLF888E device when a drain efficiency over 50% with a power

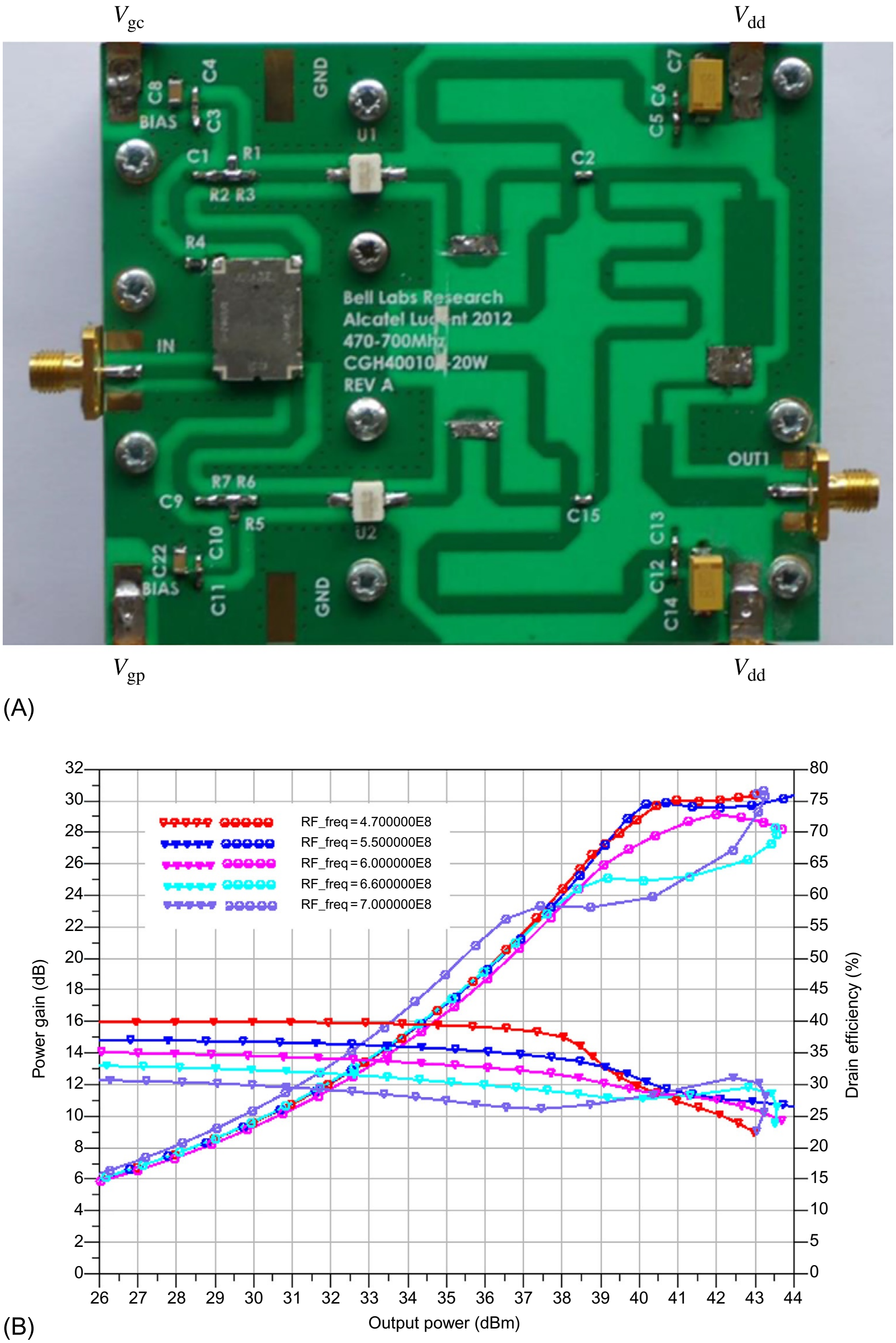


FIG. 11.81

Test board and performance of broadband UHF inverted Doherty GaN HEMT amplifier.

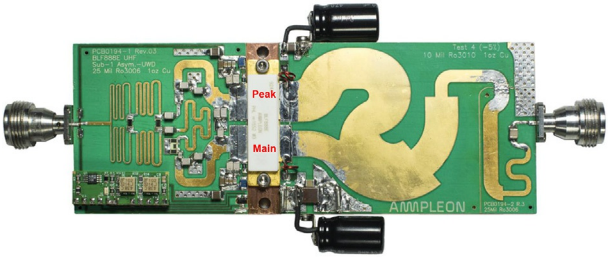


FIG. 11.82

Test board of high-power broadband UHF inverted Doherty GaN HEMT amplifier.

gain greater than 17 dB in a frequency bandwidth of 470–610 MHz, a drain efficiency over 50% with a power gain greater than 16 dB in a frequency bandwidth of 600–700 MHz, and a drain efficiency over 48% with a power gain greater than 15 dB in a frequency bandwidth of 650–800 MHz at an average output power of 150 W with an ACLR lower than −38 dBc were achieved.[172]

Similar technique with compensated impedance inverter based on shortening and lengthening of the transmission line depending on the impedance at its end was used to design a wideband high-power DA operating in a frequency range of 650–950 MHz.[173] To transform the low impedance of approximately 4 Ω at the conjunction node to the 50-Ω load, a multistage broadband matching network including tapered sections was implemented. In addition a small inductor in parallel to the output of the carrier device was inserted to terminate the second harmonic and to optimize the efficiency across the bandwidth. As a result, in a pulsed CW mode with 10% duty cycle, a peak output power of 54.2 dBm with a maximum drain efficiency of 72.5% at 700 MHz, while a drain efficiency of 50.8% at 960 MHz with the second efficiency peaks at 4-dB power backoff were achieved for a wideband inverted DA based on a 300-W PTVA042502FC LDMOSFET device biased at 50 V. For a single-carrier 20-MHz LTE signal with a *PAR* of 7.5 dB, a drain efficiency of 37%–47% at an average output power of 47.0–49.5 dBm with a power gain ranging from 14.4 to 16.6 dB (keeping a *PAR* of ~5 dB due to signal compression) was measured within the frequency bandwidth of 650–950 MHz.

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CHAPTER

Predistortion linearization techniques

12

Wireless devices have become a ubiquitous part of the daily life for billions of people. The projections of sales for these devices, particularly those tailored for mobile applications, do not seem to show any signs of slowing down. Because the radio spectrum is a finite natural resource, one method to accommodate an ever-increasing number of users is to utilize highly efficient modulation schemes that can convey as much information as possible within the narrowest bandwidth. Like with most things in nature, there is a trade-off with this approach. Highly spectrum-efficient modulation schemes utilize multilevel combinations of amplitude and phase modulation (PM), which results in a nonconstant envelope. A low level of distortion will be required for a receiver to be able to recover the information conveyed during the modulation process at the transmitter. Most modern communication systems make use of error-correcting codes to maximize the throughput of information despite channel distortions. However, the radio frequency (RF) power amplifier remains the major contributor of distortion in the communication channel.

Several techniques can be used to minimize the distortion of an RF power amplifier. Among the simplest is to operate the amplifier within its linear region, also known as "back-off" operation.[1] Unfortunately, the efficiency of the amplifier is degraded by this approach. A lower efficiency translates into more energy consumption and higher heat dissipation. Systematic methods to reduce power amplifier distortion, or linearization, which allow for an increase in power efficiency, have been extensively developed. Among the most common linearization techniques, predistortion is the most popular because of its ease of use and possibility to be implemented utilizing analog or digital techniques.

This chapter treats the power amplifier from a system perspective, introducing a simple black-box model. It continues describing the fundamentals of predistortion linearization, including the sensitivity of the method to various parameters. It later presents practical predistorters implemented using analog and digital techniques. Finally, memory effects are described and how they can diminish the effectiveness of a memoryless predistorter.

12.1 Modeling of RF power amplifiers with memory

Distortion in RF power amplifiers is a major problem in modern communication systems. Complex modulation schemes with nonconstant envelope require highly linear processing. Power amplifiers play an important role because they are a main contributor to the overall distortion of a communication system. If the dynamic range of an amplifier is fully utilized, high-amplitude signals will be subject to significant nonlinear distortion.

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Fig. 12.1 shows a plot of the measured gain of a typical solid-state power amplifier as a function of its input power when driven by a constant-frequency single tone. Gain compression and phase shift are observed at large signal levels. These effects are also known as AM/AM and AM/PM, respectively, because they denote a variation in amplitude (AM) or phase (PM) at the output with respect to a variation in amplitude at the input.

When gain compression occurs, the input and output transfer characteristics of a power amplifier are as shown in Fig. 12.2. The output signal y increases linearly with respect to the input signal x for small drive levels. Consequently, this is the linear region of the amplifier transfer characteristic, and its gain is constant. However, when the input signal is further increased, the transfer characteristic becomes nonlinear and a decrease in the rate at which the output power increases with respect to the input power is observed. This phenomenon is equivalent to a decrease in gain. All practical power amplifiers will reach a saturation point where there will be no further increase in output power despite an increase in input power.

The memoryless transfer characteristic $y(t)=T[x(t)]$ shown in Fig. 12.2 can be approximated by a polynomial of degree n. Complex coefficients are required because the power amplifier can exhibit a phase shift as a function of input level,

$$y(t) \approx \sum_{i=0}^{n} (a_i + jb_i)x^i(t). \tag{12.1}$$

Because the saturation of a real power amplifier is unavoidable because of physical limitations, the best possible transfer characteristic for a power amplifier in terms of linearity is shown in Fig. 12.3. This type of characteristic is often called *ideal limiter*. The gain of the amplifier is constant until saturation is reached; above this point the gain decreases at the same rate the input power increases. The phase shift must be zero for all input power levels below saturation.

The transfer characteristics shown so far occupy two quadrants and represent input and output voltage relations. This allows for the representation of even-order distortion, which can only occur when there is asymmetry in the transfer characteristic, i.e., the first and third quadrants of the transfer characteristic are different from each other. However, quite often, the transfer characteristic of a power amplifier is shown for the first quadrant only. This allows for the use of the input and output power relation instead of the voltage, but it does not permit the representation of any even-order distortion. The transfer characteristic of a power amplifier can be approximated by Eq. (12.1) over a very narrow frequency range. To extend the model over a wider spectrum, memory could be incorporated by using, for example, a Volterra series-based model.[2] However, alternative simpler models can be successfully used over moderate bandwidths, depending on the characteristics of the amplifier.

Frequency dependence can be added to a memoryless nonlinearity by inserting a linear filter in front of it.[3] This technique is based on the work by Wiener. The insertion loss of the filter at each frequency will determine the signal level that reaches the input of the memoryless nonlinearity, which will result in a different nonlinear behavior as a function of frequency. An alternative approach, developed by Hammerstein,[4, 5] involved the insertion of a linear filter after the nonlinearity. In both cases, the use of only one filter adds memory effects to the model. It is possible to utilize two filters for enhanced accuracy, one before and one after the nonlinearity. This is known as the Wiener–Hammerstein model.[6, 7] Fig. 12.4 shows such a system, in which the memoryless nonlinearity $T[x(t)]$ of Fig. 12.2 is preceded by the linear system H_1 and followed by the linear system H_2.

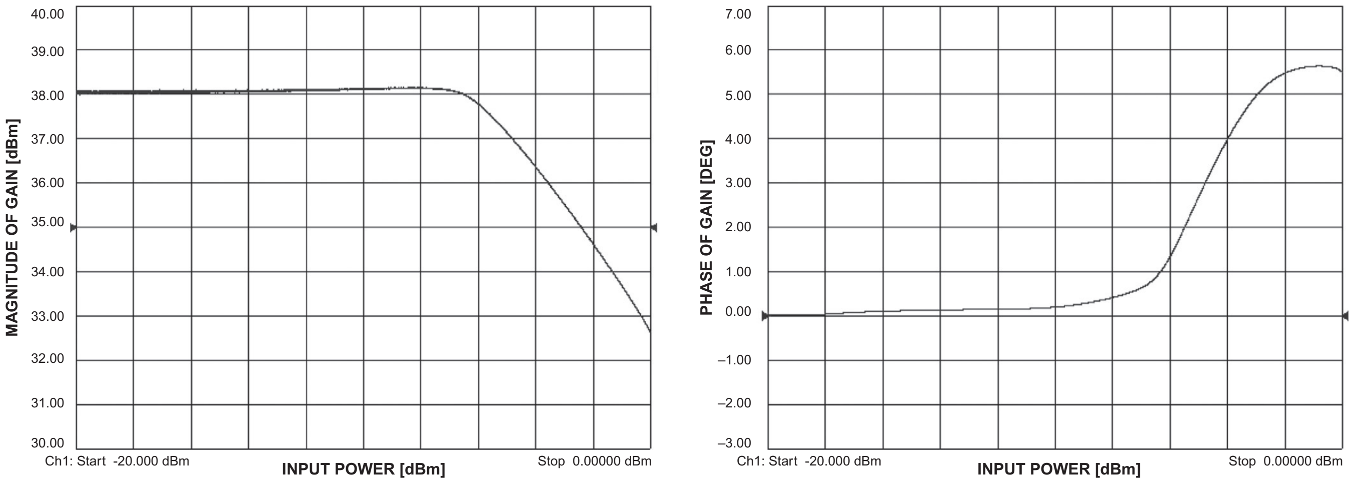

FIG. 12.1

Measured magnitude and phase of the gain of a typical solid-state RF power amplifier as a function of its input power.

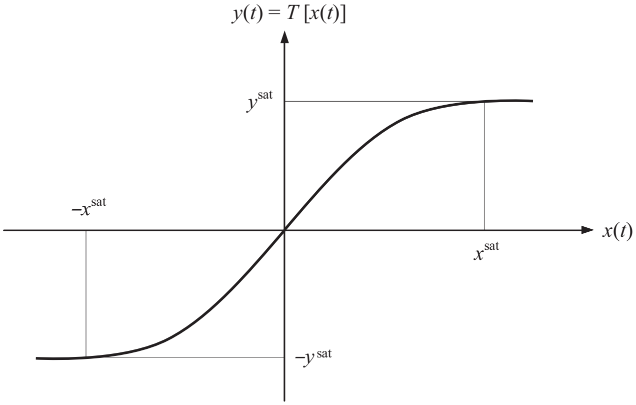

FIG. 12.2

Transfer characteristic of a memoryless RF power amplifier.

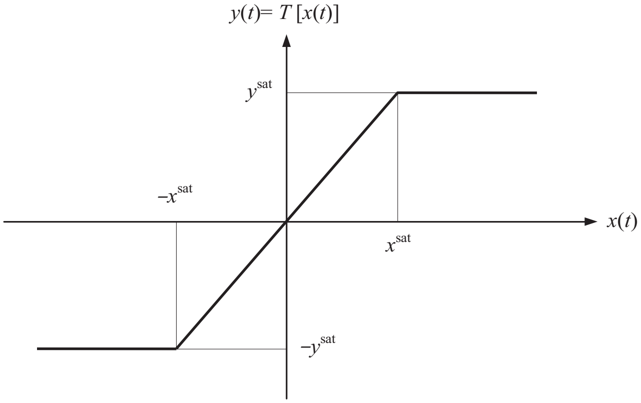

FIG. 12.3

Transfer characteristic of a memoryless RF power amplifier for optimum linearity up to the saturation point.

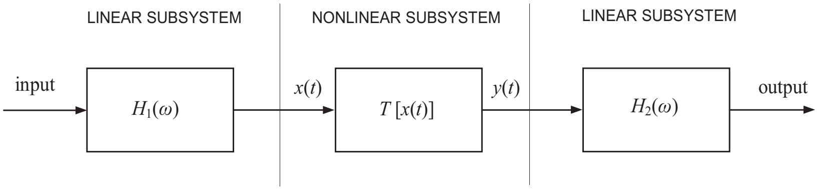
LINEAR SUBSYSTEM
NONLINEAR SUBSYSTEM
LINEAR SUBSYSTEM
input
$H_1(\omega)$
$x(t)$
$T[x(t)]$
$y(t)$
$H_2(\omega)$
output

FIG. 12.4

Power amplifier model.

The small signal transfer function $H_{ss}(\omega)$ of the system of Fig. 12.4 can be written as

$$H_{ss}(\omega) = H_1(\omega)\,T_{ss}H_2(\omega), \tag{12.2}$$

where T_{ss} is the small signal gain of the nonlinear subsystem defined as.

$$T_{ss} = \left.\frac{|y(t)|}{|x(t)|}\right|_{|y(t)| \ll y^{sat}}. \tag{12.3}$$

From Eq. (12.2), the transfer function $H_1(\omega)$ of the first filter can then be written as.

$$H_1(\omega) = \frac{H_{ss}(\omega)}{T_{ss}H_2(\omega)}. \tag{12.4}$$

The transfer function of the second filter $H_2(\omega)$ is given by.

$$H_2(\omega) = H_{sat}(\omega)T_{sat}, \tag{12.5}$$

where $H_{sat}(\omega)$ is the transfer function of the amplifier at the saturation point and T_{sat} is the gain of the nonlinear subsystem at saturation, defined as.

$$T_{sat} = \left.\frac{|y(t)|}{|x(t)|}\right|_{|y(t)| \geq y^{sat}}. \tag{12.6}$$

Both $H_{sat}(\omega)$ and $H_{ss}(\omega)$ are measurable parameters in a power amplifier.

Fig. 12.5 shows the measured magnitude of the gain of a power amplifier at 1.0, 1.1, and 1.2 GHz for an input power level ranging from −10 to 0 dBm, whereas Fig. 12.6 shows the measured output power versus the input power under the same conditions. The measured phase of the gain at the same three frequencies for an input power of −20 to 0 dBm is shown in Fig. 12.7. The phase measurements were normalized to the same phase value at the minimum input power for an easier comparison. The measurements show that the response of the amplifier is very similar across the evaluated frequency range, except for some small displacements in the vertical and horizontal axis.

Fig. 12.8 depicts the measured complex gain of the amplifier from 1.0 to 1.2 GHz. These data were used in conjunction with Eqs. (12.4), (12.5) to calculate the frequency response of the linear subsystems H_1 and H_2, as shown in Fig. 12.9. The results are only presented in magnitude for simplicity.

12.2 Predistortion linearization

12.2.1 Introduction

Linearization is any systematic method of nonlinear distortion reduction. Predistortion linearization is performed by a predistorter, which is a device that always precedes the RF power amplifier. The magnitude of the predistorter gain increases when the magnitude of the power amplifier gain decreases, and the phase of the predistorter gain is the negative of the phase of the power amplifier gain. The net result is that the magnitude and phase of the gain of the two devices in cascade becomes approximately a constant until the power amplifier reaches saturation. A block diagram of a predistorter—power amplifier cascaded system is shown in Fig. 12.10.

When the frequency of operation of the amplifier covers less than an octave, only the odd-order intermodulation products need to be canceled by the predistorter because even-order intermodulation

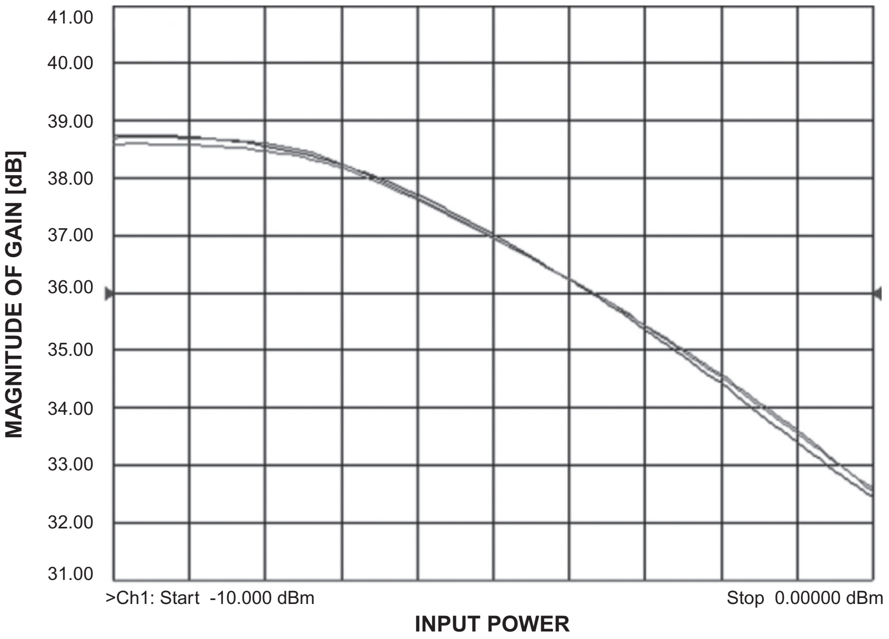

FIG. 12.5

Measured magnitude of the gain as a function of input power for a solid-state power amplifier at 1.0, 1.1, and 1.2 GHz.

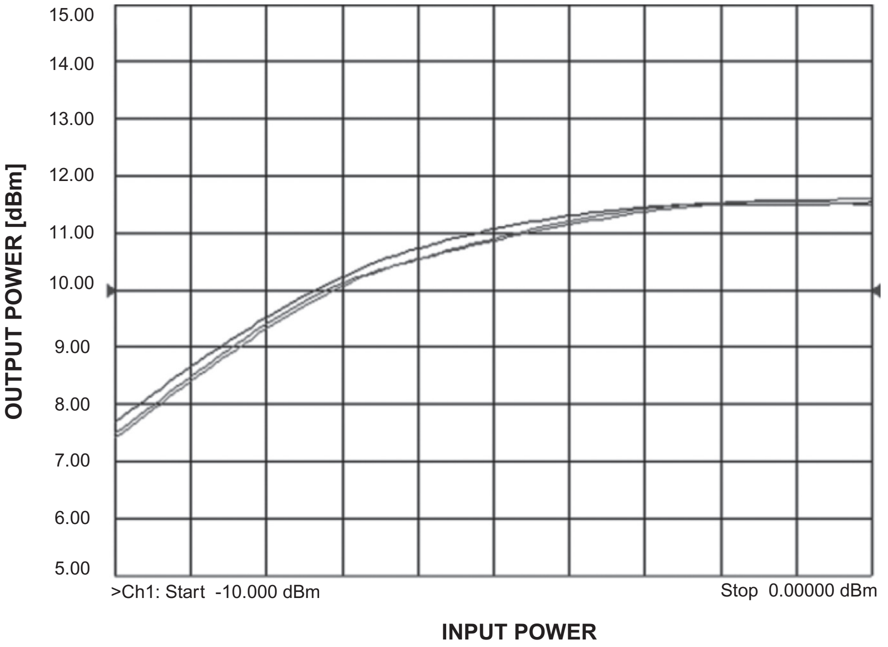

FIG. 12.6

Measured output power as a function of input power for a solid-state power amplifier at 1.0, 1.1, and 1.2 GHz.

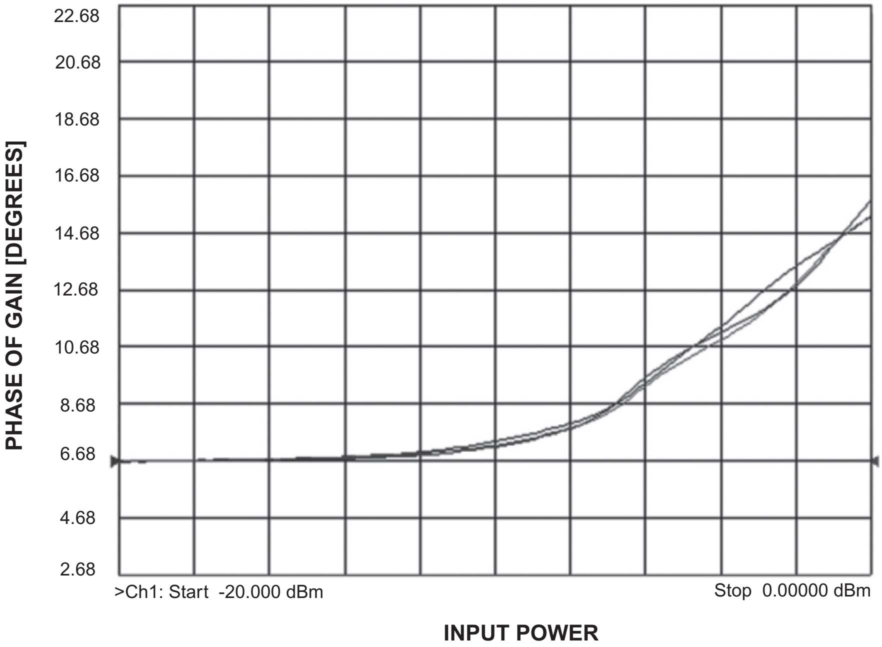

FIG. 12.7

Measured phase of the gain as a function of input power for a solid-state power amplifier at 1.0, 1.1, and 1.2 GHz.

distortion (IMD) and all harmonics fall outside the amplifier's passband and can be attenuated by a filter. Consequently, the following analysis of the predistorter will be restricted to the first zone.

If the input signal to the predistorter V_i is given by

$$V_\mathrm{i} = r(t)e^{j\theta(t)}, \tag{12.7}$$

where $r(t)$ is the magnitude and $\theta(t)$ is the phase of V_i, the output of the predistorter will be

$$V_\mathrm{p} = P_\mathrm{m}[r(t)]e^{j\left(\theta(t)+P_\mathrm{p}[r(t)]\right)}, \tag{12.8}$$

where $P_\mathrm{m}[.]$ and $P_\mathrm{p}[.]$ are the magnitude and the phase, respectively, of the gain P of the predistorter. Both $P_\mathrm{m}[.]$ and $P_\mathrm{p}[.]$ are a function of the magnitude of V_i, i.e., $r(t)$.

The output of the power amplifier that follows the predistorter is

$$V_\mathrm{o} = T_\mathrm{m}\{P_\mathrm{m}[r(t)]\}\, e^{j\left\{\theta(t)+P_\mathrm{p}[r(t)]+T_\mathrm{p}\left(P_\mathrm{p}[r(t)]\right)\right\}}, \tag{12.9}$$

where $T_\mathrm{m}[.]$ and $T_\mathrm{p}[.]$ are the magnitude and the phase of the gain of the power amplifier, also known as AM/AM and AM/PM, respectively.

The goal of the predistorter is to achieve a constant magnitude of the predistorter–power amplifier system gain k_m

$$T_\mathrm{m}\{P_\mathrm{m}[r(t)]\} = k_\mathrm{m}r(t), \tag{12.10}$$

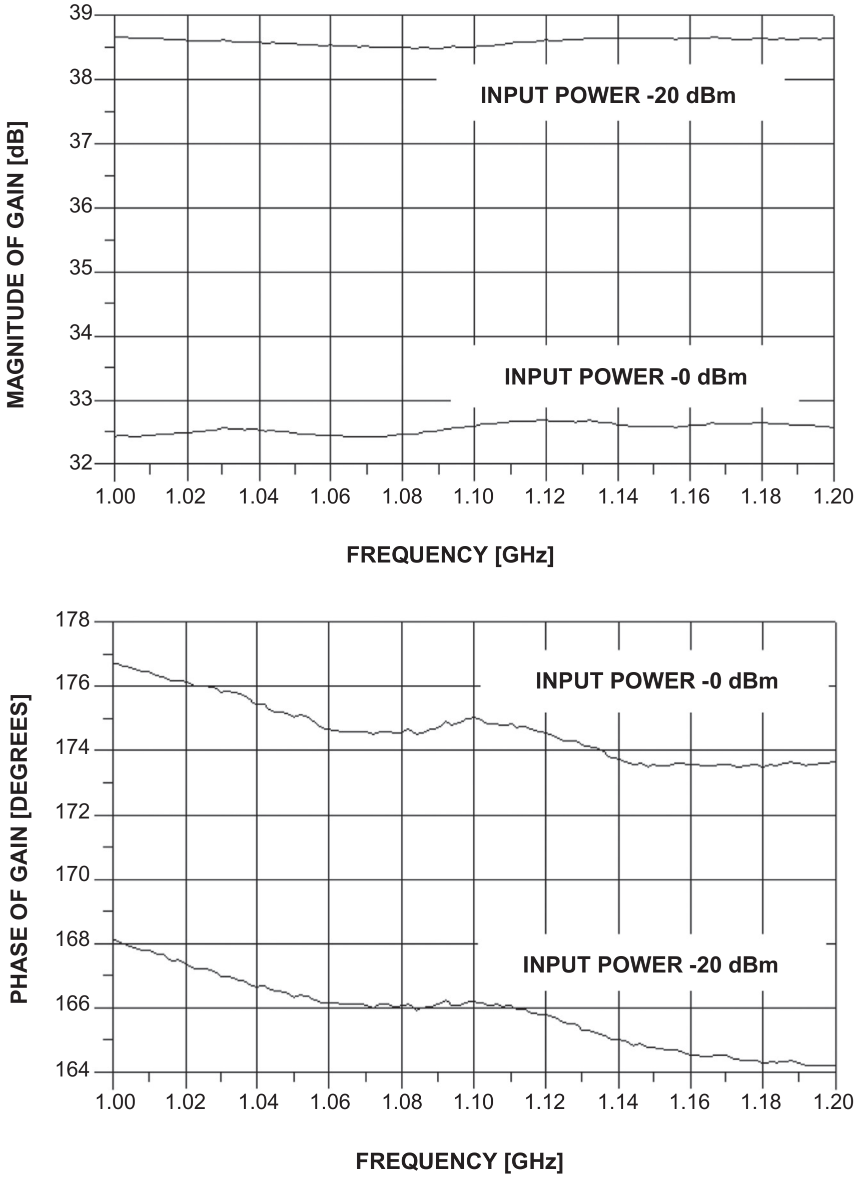

FIG. 12.8

Measured magnitude and phase of the gain of a solid-state amplifier as a function of frequency.

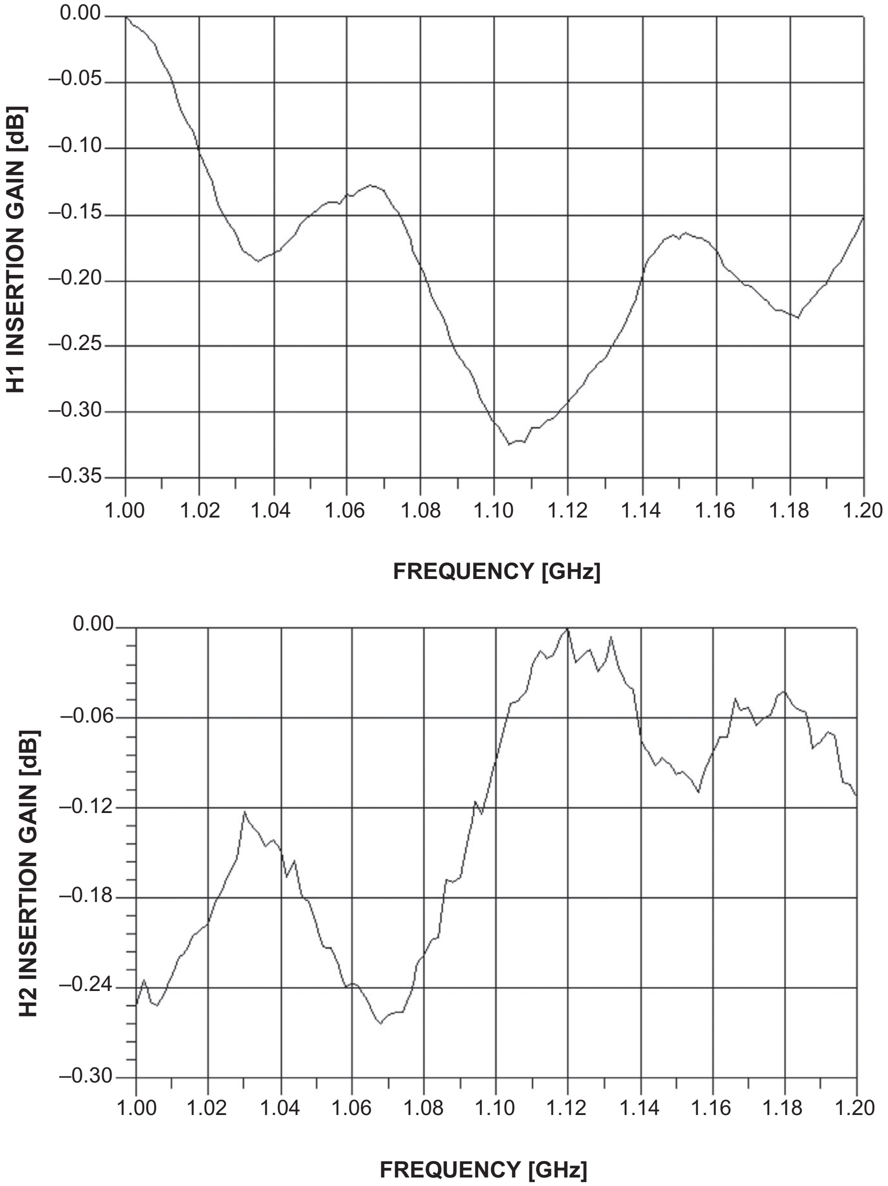

FIG. 12.9

Calculated frequency response (magnitude) of the linear subsystems H_1 and H_2.

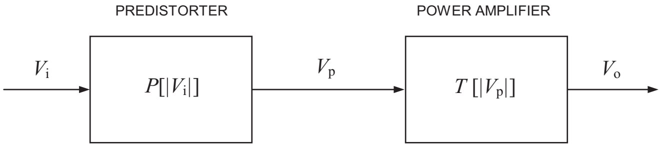

FIG. 12.10

Block diagram of a predistorter—power amplifier system.

and a constant phase k_{ph}

$$P_p[r(t)] + T_p\{P[r(t)]\} = k_{ph}. \tag{12.11}$$

Fig. 12.11 shows the magnitude of the gain and the transfer characteristic of an ideal predistorter for the correction of odd-order IMD of a power amplifier. The gain of the power amplifier and the predistorter was normalized to unity at saturation.

12.2.2 Memoryless predistorter for octave-bandwidth amplifiers

At first glance, it could be presumed that the predistorter gain could be calculated as the reciprocal of the power amplifier gain. Unfortunately, every time the predistorter increases its gain to compensate for the power amplifier gain compression, the predistorter output signal level also increases. This forces the gain of the power amplifier (at this new larger input signal) to compress even more. This effect can be overcome if the predistorter transfer characteristic is calculated as a function of *the output of the*

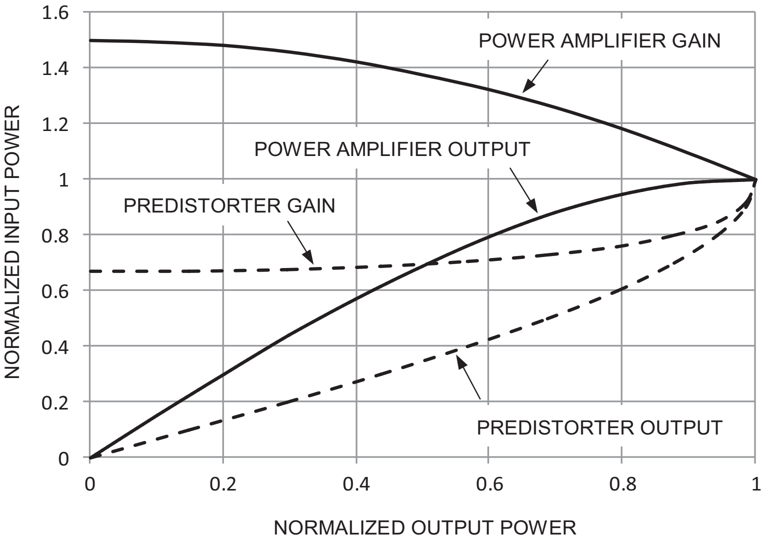

FIG. 12.11

Normalized magnitude of the gain and transfer characteristic of an ideal predistorter for the correction of the odd-order intermodulation distortion of a power amplifier.

power amplifier instead of the input to the predistorter, after the gain and output signal of the power amplifier are both normalized to unity at saturation. From Fig. 12.10, it follows that

$$P[|V_\mathrm{o}|] = \frac{1}{T[|V_\mathrm{i}|]}, \tag{12.12}$$

where P is the transfer characteristic of the predistorter and T is the transfer characteristic of the power amplifier, both normalized to unity at saturation. It must be noted that an iterative solution to Eq. (12.12) is required.

For a better comprehension of the meaning of Eq. (12.12), the memoryless transfer characteristics of the power amplifier and the predistorter are shown in Fig. 12.12. Because the power amplifier transfer characteristic had been normalized to unity at saturation, the process to obtain the predistorter transfer characteristic simply involves the swapping of the axes.

The following conclusions can be drawn at this point:

- The slope of the predistorter transfer characteristic at the saturation point is infinite, which could only be achieved by infinite predistorter gain. Therefore, it is not possible to effectively predistort once the amplifier reaches saturation.
- The gain of the power amplifier cannot be zero in any part of its domain because it would require infinite gain from the predistorter. This could be the case of a Class-C power amplifier in which the conduction angle is less than 180°.
- The transfer characteristic must be a monotonically increasing function to avoid ambiguity in the calculation of the predistorter transfer characteristic.

The last two cases are illustrated in Fig. 12.13.

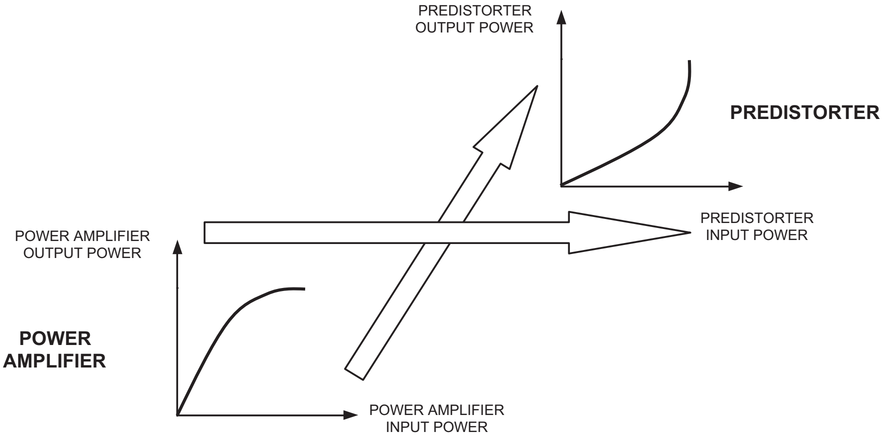

FIG. 12.12

The transfer characteristic of the predistorter can be obtained by swapping the axes of the amplifier transfer characteristic after its normalization to unity at saturation.

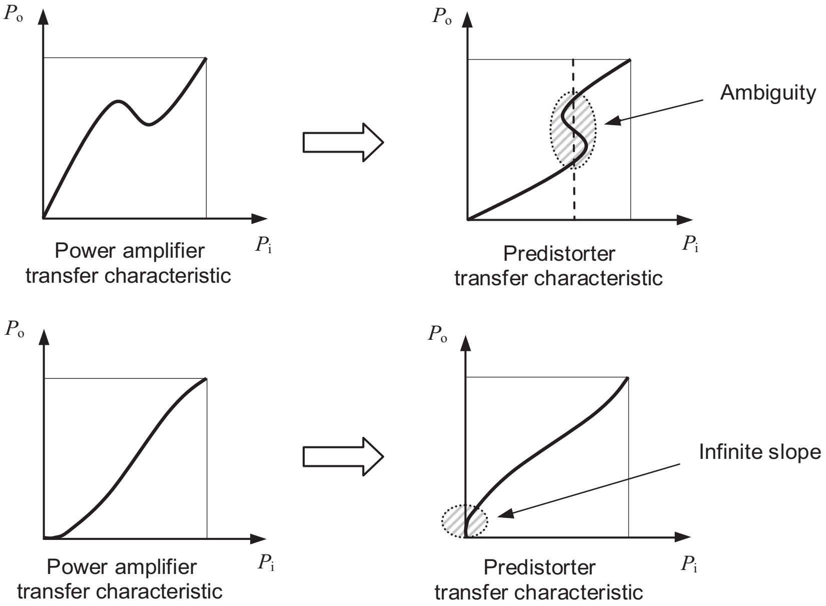
P_o
P_i
Power amplifier
transfer characteristic
P_o
P_i
Ambiguity
Predistorter
transfer characteristic
P_o
P_i
Power amplifier
transfer characteristic
P_o
P_i
Infinite slope
Predistorter
transfer characteristic

FIG. 12.13

Power amplifier transfer characteristic—special cases for which a predistorter cannot be implemented. *Po* and *Pi* are the output and input powers, respectively.

The predistorter transfer characteristic can also be calculated by inverting the power series that represents the power amplifier transfer characteristic. If only the odd IMD is considered, the transfer characteristic of the power amplifier can be written as

$$y(t) = \sum_{n=0}^{\infty} k_{(2n+1)} x^{(2n+1)}(t), \tag{12.13}$$

where n is any positive integer, $y(t)$ and $x(t)$ are the output and input signals of the power amplifier, respectively, and $k_{(2n+1)}$ are complex coefficients.

For the analysis, it will be supposed that the power amplifier only has third-order IMD (IMD3) by truncating Eq. (12.13) to its third power, which results in

$$y(t) = k_1 x(t) + k_3 x^3(t). \tag{12.14}$$

If $y(t)$ and $x(t)$ are normalized to unity at saturation by manipulating the coefficients k_1 and k_3, then the transfer characteristic of the predistorter can be obtained by inverting Eq. (12.14),

$$x'(t) = \sum_{n=0}^{\infty} K_{(2n+1)} y'^{(2n+1)}(t), \tag{12.15}$$

where x' is now the output of the predistorter (same as the input to the power amplifier), y' is the input to the predistorter (same as the output of the power amplifier because its output at saturation is unity), and n is any positive integer. As an example, the coefficients K up to order 7 can be calculated as follows[8]:

$$K_1 = {k_1}^{-1}, \tag{12.16}$$

$$K_3 = -{k_1}^{-4}k_3, \tag{12.17}$$

$$K_5 = 3{k_1}^{-7}{k_3}^2, \tag{12.18}$$

$$K_7 = -12{k_1}^{-10}{k_3}^3. \tag{12.19}$$

It is important to observe in Eq. (12.15) that the predistorter transfer characteristic contains an infinite number of terms even when the power amplifier transfer characteristic was truncated to the third degree. A predistorter transfer characteristic of this type cannot be realized in practice because it would require an infinite bandwidth. As a result, only a partial cancellation of the IMD products produced by the power amplifier can be achieved.

Bandwidth restrictions in the predistorter can also be understood by analyzing Fig. 12.14, in which a third-order predistorter is placed in front of a power amplifier with also a third-order transfer characteristic. A two-tone signal $r(t)$ of the form.

$$r(t) = \cos\omega_1 t + \cos\omega_2 t \tag{12.20}$$

is applied to the input of the predistorter. The tones of angular frequency ω_1 and ω_2 are of unity amplitude and zero phase to simplify the analysis. The output of the predistorter will be.

$$x(t) = p_1(\cos\omega_1 t + \cos\omega_2 t) + p_3(\cos\omega_1 t + \cos\omega_2 t)^3. \tag{12.21}$$

By operating and expanding the cubic term, we have.

$$\begin{gathered} x(t) = p_1\cos\omega_1 t + p_1\cos\omega_2 t, \\ +p_3\left(\cos^3\omega_1 t + 3\cos^2\omega_1 t\cos\omega_2 t + 3\cos\omega_1 t\cos^2\omega_2 t + \cos^3\omega_2 t\right). \end{gathered} \tag{12.22}$$

After grouping the terms of equal frequency and eliminating the harmonics,

$$\begin{gathered} x(t) = \left[p_1 + \frac{9}{4}p_3\right]\cos\omega_1 t, \\ +\left[p_1 + \frac{9}{4}p_3\right]\cos\omega_2 t + \frac{3}{4}p_3[\cos(2\omega_1 - \omega_2)t + \cos(2\omega_2 - \omega_1)t]. \end{gathered} \tag{12.23}$$

From Eq. (12.23), it follows that the output of the predistorter only contains third-order inter distortion (IMD), which will effectively cancel out the power amplifier's IMD3 products. However, the

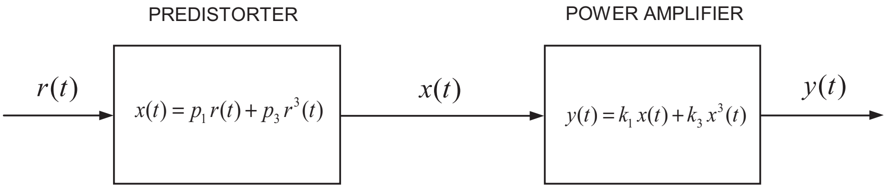
PREDISTORTER
POWER AMPLIFIER
$r(t)$
$x(t) = p_1 r(t) + p_3 r^3(t)$
$x(t)$
$y(t) = k_1 x(t) + k_3 x^3(t)$
$y(t)$

FIG. 12.14

Third-order predistorter with coefficients p_1 and p_3 followed by a third-order power amplifier with coefficients k_1 and k_3.

predistorter's output contains *four tones* (ω_1, ω_2, $2\omega_1$-ω_2, and $2\omega_2$-ω_1), two more than the original signal $r(t)$. When these four tones are applied to the third-order power amplifier, the large number of IMD products will occur. Because the mathematical resolution of this problem is rather complex, Fig. 12.15 shows this process graphically, where only the upper IMD products are shown for clarity. The IMD3 products are mixed with the fundamental tones to produce fifth- and seventh-order IMD products, whereas the third-order tones provide ninth-order IMD products by themselves. The only way the predistorter could be able to cancel the fifth-, seventh-, and ninth-order IMD products is by also generating IMD products of that same order, which requires an increase in bandwidth. Unfortunately, the process would repeat infinitely, which means that the predistorter bandwidth must be unlimited for the perfect cancellation of the IMD of a power amplifier with just a third-order transfer characteristic.

The effects of bandwidth restrictions can also be analyzed by evaluating the nonlinear gain characteristics of the predistorter. Fig. 12.16 shows the power gain and output power of a third-, fifth-, seventh-, and infinite-bandwidth predistorter followed by a third-order power amplifier. The output power is shown for the predistorter and the power amplifier individually, as well as for the cascaded connection of both. The band-limited predistorters are not capable of effectively linearizing the power amplifier to saturation.

12.2.3 Predistorter with memory for octave-bandwidth amplifiers

Fig. 12.4 shows the power amplifier model that contains memory introduced by two linear subsystems located before and after the memoryless nonlinearity. This memory must be removed before calculating the predistorter transfer characteristic using Eq. (12.12), which can be accomplished by placing two more linear subsystems, one before and one after the predistorter, as shown in Fig. 12.17. The transfer functions of the linear subsystems H_4 and H_3 are calculated so they cancel out the memory introduced by H_1 and H_2. The net result is that the gain of the cascaded systems H_1–H_4 and H_2–H_3 becomes unity with zero phase shift across the passband of the amplifier.

The linear subsystems H_3 and H_4 affect the predistorter-amplifier system frequency response, forcing it to be flat across the passband of the power amplifier. To recover the original frequency

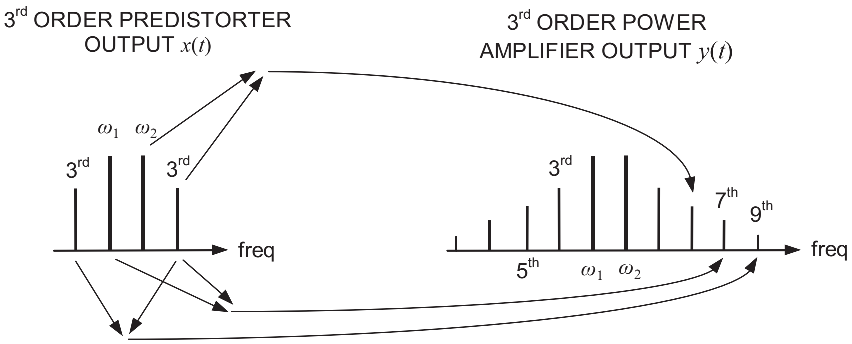
3rd ORDER PREDISTORTER OUTPUT $x(t)$
3rd ORDER POWER AMPLIFIER OUTPUT $y(t)$
ω_1
ω_2
3rd
3rd
freq
3rd
7th
9th
freq
5th
ω_1
ω_2

FIG. 12.15

Graphical representation of the output spectrum of the predistorter and power amplifier of Fig. 12.14.

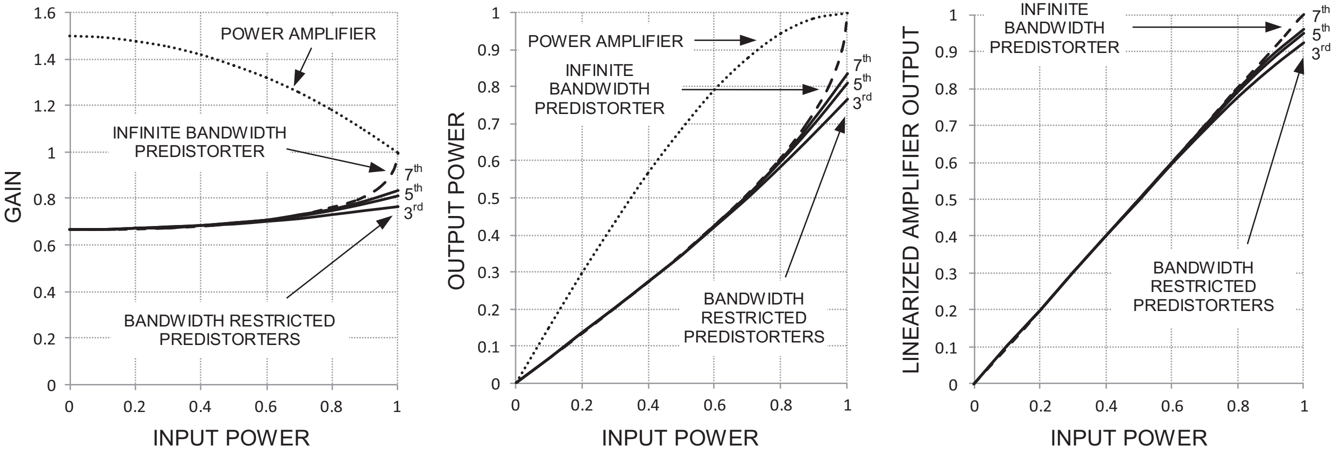

FIG. 12.16

Effects of bandwidth restrictions in predistortion.

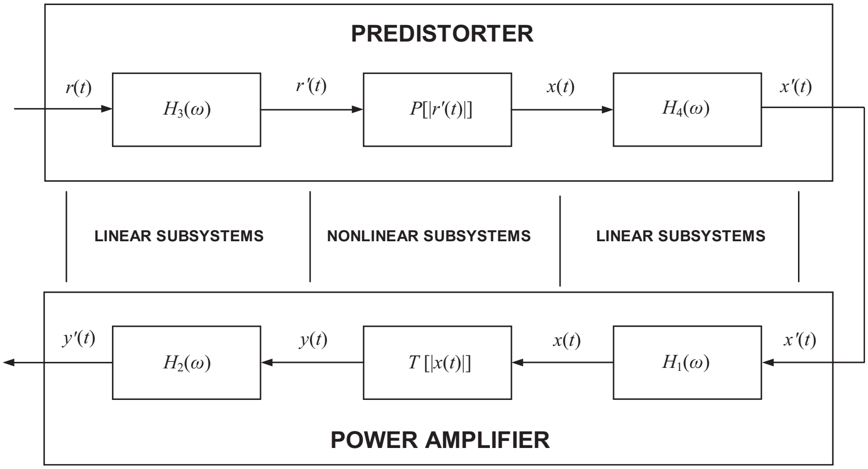
PREDISTORTER
r(t)
H3(ω)
r′(t)
P[|r′(t)|]
x(t)
H4(ω)
x′(t)
LINEAR SUBSYSTEMS
NONLINEAR SUBSYSTEMS
LINEAR SUBSYSTEMS
y′(t)
H2(ω)
y(t)
T [|x(t)|]
x(t)
H1(ω)
x′(t)
POWER AMPLIFIER

FIG. 12.17

System block diagram used for the calculation of the predistorter function $P[|r'(t)|]$ when the power amplifier has memory.

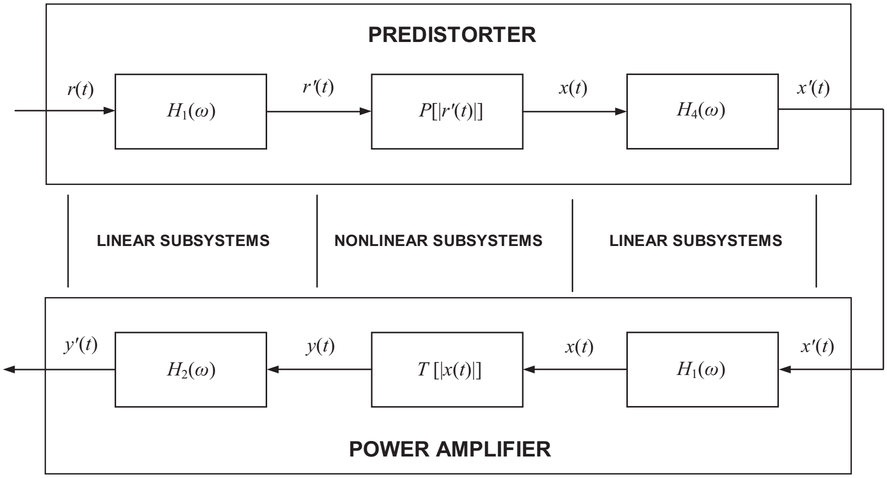
PREDISTORTER
r(t)
H1(ω)
r′(t)
P[|r′(t)|]
x(t)
H4(ω)
x′(t)
LINEAR SUBSYSTEMS
NONLINEAR SUBSYSTEMS
LINEAR SUBSYSTEMS
y′(t)
H2(ω)
y(t)
T [|x(t)|]
x(t)
H1(ω)
x′(t)
POWER AMPLIFIER

FIG. 12.18

System block diagram of the predistorter-power amplifier with memory. H_3 is replaced by H_1 from Fig. 11.17 to preserve the power amplifier frequency response.

response of the power amplifier, the predistorter-amplifier system must be as shown in Fig. 12.18, where the memory between the predistorter and the power amplifier is eliminated, allowing for memoryless predistortion, but the original frequency response of the power amplifier is preserved by replacing H_3 with H_1.

12.2.4 Postdistortion

The use of a predistortion linearizer can reduce the IMD of a nonlinear system, but it can also affect its performance. For example, the noise figure of an amplifier can be degraded by the insertion of a predistorter in front of it,[9] or the use of a predistorter may be simply not feasible, like in the case of an optical receiver.[10]

In cases like those described above, the linearizer can be inserted after the nonlinear device, in which case it is called a *postdistorter*. Its transfer characteristic is identical to that of the predistorter given in Eq. (12.12) because the predistorter transfer characteristic was actually calculated as a postdistorter when the output of the power amplifier was used as the input to the predistorter after the normalization to unity at saturation, as described in Section 12.2.2 while analyzing a memoryless predistorter for octave-bandwidth amplifiers.

12.3 Analog predistortion implementation

12.3.1 Introduction

It is certainly possible to implement the transfer characteristic of a predistorter using analog components. The predistorter can directly be implemented at the operating frequency of the RF power amplifier. However, in cases where there is an up-conversion in the early stages of the signal generation, the predistorter can be inserted at an intermediate frequency (IF). In all cases, bandwidth restrictions must be considered to determine the effectiveness of the predistorter. This is particularly important with IF implementations because the signal is usually tightly filtered to remove spurious caused by the up-mixing process.

Increasing the gain of a device and changing its insertion phase as a function of its input signal level is not a trivial task if such performance will effectively predistort a power amplifier. Moreover, achieving this goal over a wide bandwidth is even more complex. The following sections show the principles of the most common analog predistortion techniques available.

12.3.2 Reflective predistorters

The most common reflective predistorter consists of a branch-line coupler (quadrature hybrid), an open-circuited transmission line, and a nonlinearity implemented with two diodes in antiparallel configuration, also known as limiter.[11] Fig. 12.19 shows a simplified schematic of such a predistorter. An alternative implementation can include nonlinearities connected to ports 2 and 3 of the branch line coupler.

The branch line coupler can be represented by the following S-parameter matrix,

$$S_{90} = -\frac{1}{\sqrt{2}}\begin{vmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{vmatrix}. \tag{12.24}$$

The coupler equally splits the input signal applied to port 1 into two components shifted 90 degrees from each other, available at ports 2 and 3. Because these two ports are terminated into a mismatch,

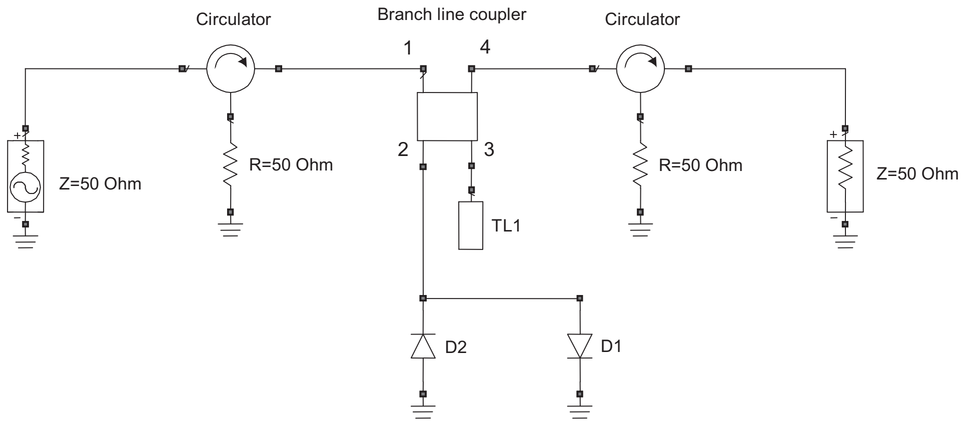

FIG. 12.19

Simplified schematic of a reflective predistortion linearizer utilizing a branch-line coupler and a diode limiter.

the majority of the energy is reflected back into the coupler. The energy reflected into port 2 is now equally split between ports 1 and 4, whereas the energy reflected into port 3 is equally split between ports 4 and 1.

The voltage V_3 at port 3 is given by

$$V_3 = S_{31}V_1\Gamma_3 = -\frac{V_1}{\sqrt{2}}\frac{Z_{\text{in}} - Z_0}{Z_{\text{in}} + Z_0}, \tag{12.25}$$

where V_1 is the voltage at port 1, Γ_3 is the reflection coefficient at port 3, and Z_{in} is the input impedance of the open-circuited transmission line $TL1$ of electrical length θ, which can be written as

$$Z_{\text{in}} = -jZ_0\cot\theta. \tag{12.26}$$

The voltage V_2 at port 2 is given by.

$$V_2 = S_{21}V_1\Gamma_2 = -\frac{jV_1}{\sqrt{2}}\frac{Z_d - Z_0}{Z_d + Z_0}, \tag{12.27}$$

where Γ_2 is the reflection coefficient at port 2, and Z_d is the impedance of the diode antiparallel, which is an inverse function of the voltage applied across the diodes.

The output voltage of the predistorter V_4 can be calculated from Eqs. (12.24), (12.25), (12.27) as

$$V_4 = S_{42}V_2 + S_{43}V_3 = -\frac{V_2}{\sqrt{2}} - \frac{jV_3}{\sqrt{2}}, \tag{12.28}$$

$$V_4 = \frac{jV_1}{2}\frac{Z_d - Z_0}{Z_d + Z_0} + \frac{jV_1}{2}\frac{Z_{\text{in}} - Z_0}{Z_{\text{in}} + Z_0}. \tag{12.29a}$$

The gain of the reflective predistorter G_{RP} can be derived from Eqs. (12.26), (12.29a), (12.29b) as

$$G_{\text{RP}} = \frac{V_4}{V_1} = \frac{j}{2}\left(\frac{Z_d - Z_0}{Z_d + Z_0} - \frac{Z_0 + jZ_0\cot\theta}{Z_0 - jZ_0\cot\theta}\right). \tag{12.29b}$$

By carefully choosing θ, it is possible to obtain gain expansion (lower insertion loss) when Z_d decreases after the application of a large input signal level at port 1. Because the input impedance of the reflective predistorter varies as a function of the input signal level, an isolator is necessary at the input of the device to ensure proper performance. An additional isolator at the output of the predistorter must be added if a good output impedance match is desired.

Fig. 12.20 provides simulation results of the reflective predistorter of Fig. 12.19.

12.3.3 Transmissive predistorters

The basic transmissive predistorter is depicted in Fig. 12.21. It consists of a linear signal path in parallel with a nonlinear signal path. The nonlinear signal path gain is reduced by the nonlinearity at large input signal levels. By subtracting the nonlinear path from the linear path, gain expansion and phase shift can be achieved.

Like in the reflective predistorter, the nonlinearity can be implemented with a diode limiter. A phase shifter and an attenuator can be used to adjust the nonlinear characteristics of the predistorter. The predistorter input impedance varies as a function of the input signal level, for which an isolator is needed at the input for proper performance. An optional isolator at the output can improve the output impedance match as well.

Fig. 12.22 shows the simulated magnitude and phase of the gain of the transmissive predistorter of Fig. 12.21.

It is possible to achieve gain expansion and phase shift as a function of signal level without resorting to the subtraction of parallel paths. A typical example is the series diode predistorter shown in Fig. 12.23.[12]

The current through a forward-biased diode I_D can be represented by Shockley's equation,

$$I_\mathrm{D} = I_\mathrm{S}\left(e^{\frac{V_\mathrm{D}}{V_\mathrm{T}}} - 1\right), \tag{12.30}$$

where I_S is the reverse saturation current, V_D is the voltage across the diode, and V_T is the thermal voltage (26 mV at room temperature). The diode is assumed to be ideal.

The dynamic conductance of the diode can be obtained by differentiating Eq. (12.30) with respect to V_D as.

$$g_\mathrm{d} = \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{D}} = \frac{I_\mathrm{S}}{V_\mathrm{T}} \exp\left(\frac{V_\mathrm{D}}{V_\mathrm{T}}\right). \tag{12.31}$$

Expressing Eq. (12.31) in terms of the dynamic resistance of the diode $r_\mathrm{d} = 1/g_\mathrm{d}$ results in.

$$r_\mathrm{d} = \frac{V_\mathrm{T}}{I_\mathrm{S} \exp\left(\frac{V_\mathrm{D}}{V_\mathrm{T}}\right)}. \tag{12.32}$$

Eq. (12.32) is significantly nonlinear for small values of V_D. If the predistorter input signal is superimposed to a low dc voltage, the resulting nonlinearity will produce a larger decrease of the dynamic resistance of the diode during the positive half-cycle of the input signal compared to the increase that occurs during the negative half-cycle of the input signal. The net result of this process is an average decrease in the diode dynamic resistance r_d for large input signals to the predistorter. Because the diode

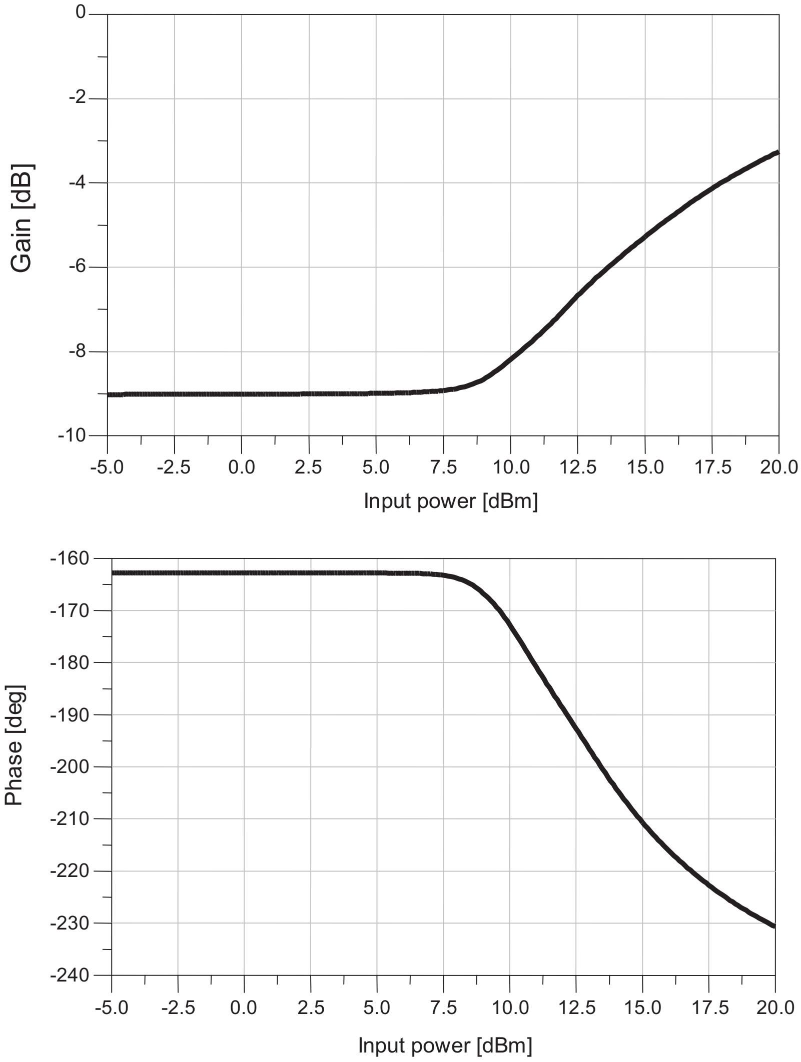

FIG. 12.20

Simulated magnitude and phase of the gain of the reflective predistortion linearizer shown in Fig. 12.19.

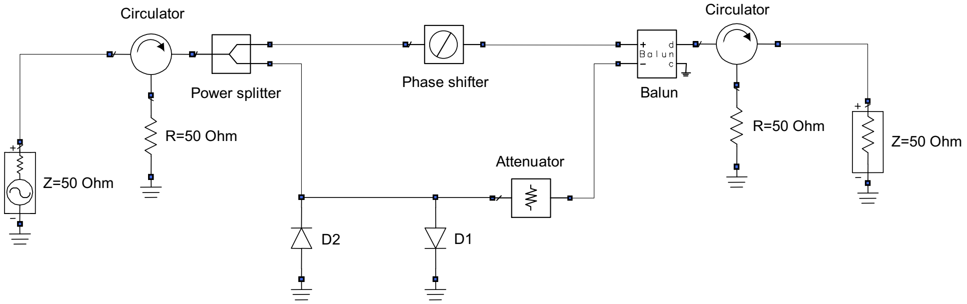
Circulator
Power splitter
R=50 Ohm
Z=50 Ohm
Phase shifter
Attenuator
D2
D1
Balun
Circulator
R=50 Ohm
Z=50 Ohm

FIG. 12.21

Simplified schematic of a transmissive predistortion linearizer utilizing parallel paths and a diode limiter.

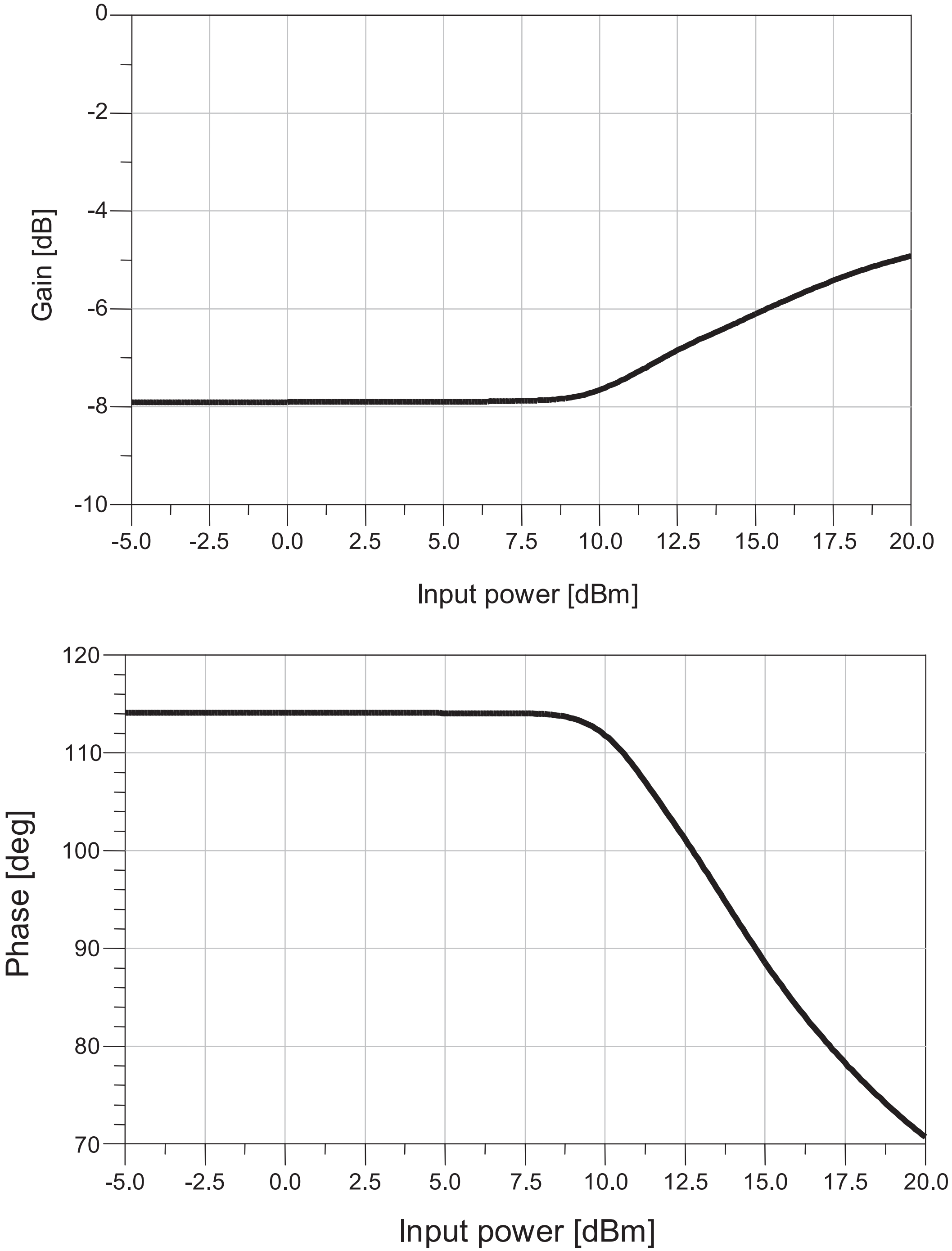

FIG. 12.22

Simulated magnitude and phase of the gain of the transmissive predistortion linearizer shown in Fig. 12.21.

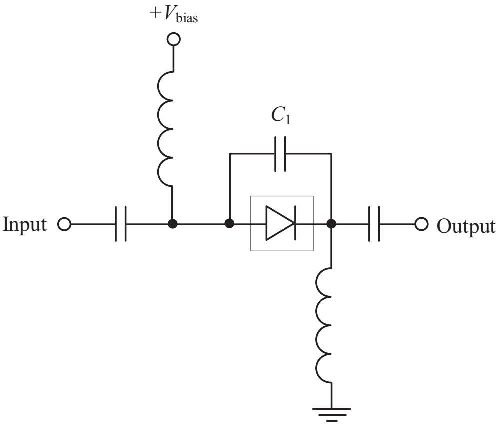

FIG. 12.23

Simplified schematic of a transmissive predistortion linearizer utilizing a series diode.[12]

in the predistorter is in series with the signal path, any r_d decrease at high input signal levels will result in a reduction in the predistorter insertion loss, which can also be interpreted as a gain expansion.

The predistorter gain expansion can be used to compensate for the effects of gain compression in the power amplifier (AM/AM). To also obtain a nonlinear phase shift in the predistorter to compensate for the amplifier's AM/PM, a reactance can be added in parallel with the diode. This reactance, represented by C_1 in Fig. 12.23 in conjunction with the dynamic resistance of the diode, will introduce a phase shift that is a function of the input signal level to the predistorter.

The predistorter gain can be controlled by adjusting the diode bias voltage and the value of the capacitor C_1. Fig. 12.24 shows the magnitude and phase of the gain of the predistorter for three different bias voltages with a capacitor placed in parallel with the diode. The capacitor introduces a negative AM/PM behavior.

Similar to the other predistorters described earlier, the series diode predistorter requires isolators at the input and the output for good performance because the input and output impedances are a function of the input signal level.

Other transmissive predistorter implementations include the parallel diode approach[13] and field-effect transistors.[14, 15]

12.4 Digital predistortion implementation

12.4.1 Introduction

Most modern communication systems utilize digital techniques for the signal generation, which simplifies the implementation of predistortion linearization at baseband or at an IF while the signal is still in the digital domain, i.e., in the form of discrete time samples instead of a continuous function of time. The analog predistortion concepts described earlier in the chapter also apply to digital predistortion.

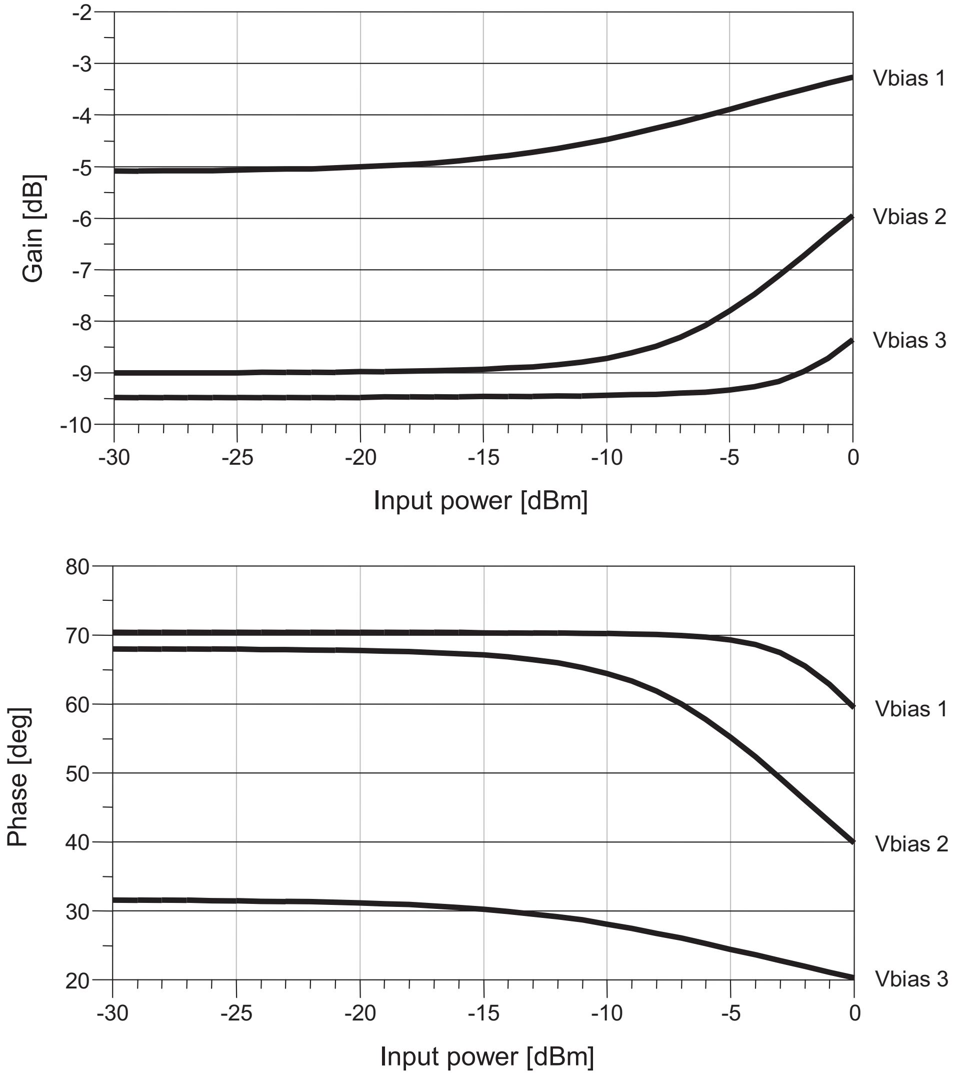

FIG. 12.24

Simulated magnitude and phase of the gain of the diode predistorter of Fig. 12.23 as a function of input power. Values for three different bias voltages.

Digital predistortion has the advantage of being able to generate predistortion transfer characteristics that would be difficult to implement with discrete components and analog signals. The fabrication cost of a predistorter can be relatively low because the digital processing power is already present for the signal generation, and the predistortion function may consist of additional lines of code. However, the signal instantaneous bandwidth, which includes its IMD products, is limited by the sampling rate of the digital system. As a result, wideband digital predistortion is much more challenging than its analog counterpart.

12.4.2 Principles of memoryless digital predistortion

In today's designs, it is quite common to generate the baseband signal in digital form. Usually, the Cartesian, in-phase I, and quadrature Q components are used for most types of modulation schemes. A possible predistorter implementation consists of a device with its outputs I' and Q' mapped to its inputs I and Q. The mapping is defined by $P[I,Q]$ where P is the gain of the predistorter. Note that P is a two-dimensional function, and it consists of $P_1[I,Q]$ and $P_2[I,Q]$. The output of the mapping device can be written as.

$$I' = P_1[I, Q], \tag{12.33}$$

$$Q' = P_2[I, Q]. \tag{12.34}$$

The block diagram of this type of linearizer, called *mapping predistorter*, is shown in Fig. 12.25. The mapping can be implemented by means of a look up table stored in memory.[16, 17] Because every possible input complex signal amplitude must have its correspondent complex output, the amount of memory needed can be quite large. The total number of memory entries M as a function of the quantization level n is.

$$M = 2\left(2^{2n}\right). \tag{12.35}$$

The memory size requirements can be reduced with a *gain-based predistorter*, as shown in Fig. 12.26.[18] The idea behind this predistorter consists of using interpolation to find intermediate values not included in the predistorter gain table, and to use the magnitude squared of the complex input signal as the table index, which restricts the nonlinear distortion cancellation to odd-order IMD products. Individual tables for the I and Q signals are required. It is possible to make the input to the tables a nonuniform distribution to maximize performance. The power amplifier nonlinearity is stronger at high input signal levels, so a greater number of table entries can be stored for large input signals, leaving a smaller number for weak signals, for which the power amplifier is almost linear. Only 64 entries per each table were found to be satisfactory for good performance, which compares very favorably to the mapping predistorter according to Eq. (12.35).[18]

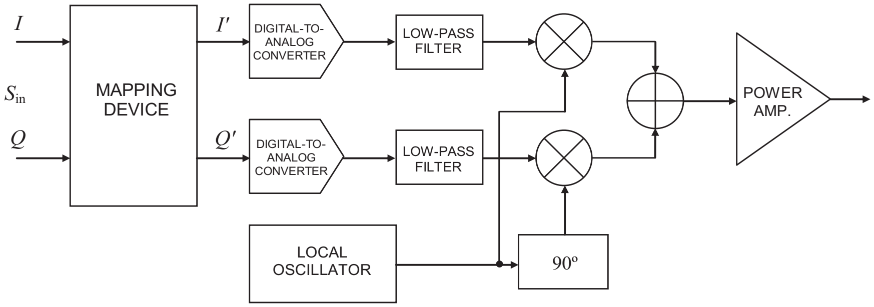

FIG. 12.25

Digital mapping predistorter block diagram.

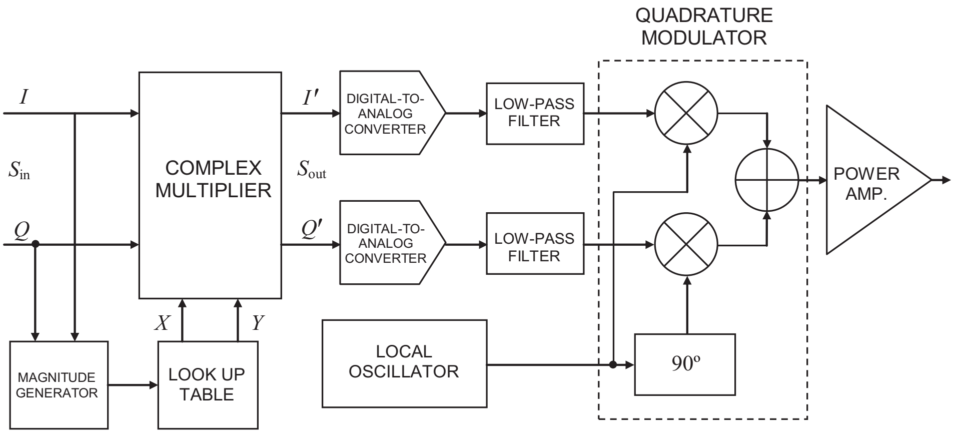
QUADRATURE MODULATOR
I
S_in
Q
COMPLEX MULTIPLIER
I′
S_out
Q′
DIGITAL-TO-ANALOG CONVERTER
DIGITAL-TO-ANALOG CONVERTER
LOW-PASS FILTER
LOW-PASS FILTER
POWER AMP.
X
Y
MAGNITUDE GENERATOR
LOOK UP TABLE
LOCAL OSCILLATOR
90°

FIG. 12.26

Gain-based predistorter simplified block diagram.

The input signal to the predistorter S_{in}, with real and imaginary components I and Q, can be written as.

$$S_{\text{in}} = I + jQ. \tag{12.36}$$

The complex predistortion coefficient P, with real and imaginary parts X and Y, is given by.

$$P\left[|S_{\text{in}}|^2\right] = X + jY. \tag{12.37}$$

The output of the predistorter S_{out} will be.

$$S_{\text{out}} = P\left[|S_{\text{in}}|^2\right] S_{\text{in}} = (X + jY)(I + jQ), \tag{12.38}$$

$$S_{\text{out}} = \begin{cases} I' = IX - QY \\ Q' = IY + QX \end{cases}, \tag{12.39}$$

$$S_{\text{out}} = I' + jQ'. \tag{12.40}$$

Section 12.2.2 showed that the predistorter increases the bandwidth of the input signal to include its own distortion products intended to cancel the IMD of the power amplifier. Therefore, the predistorter of Fig. 12.26 must operate at a sampling rate that is high enough to include all the distortion produced by the predistortion function. The simplest way to accomplish this task is to upsample the input signal to the predistorter to accommodate the wider bandwidth.[19] The upsampler inserts $U-1$ zero-amplitude samples between existing time samples, increasing the sample rate by U times, where U is the upsampling rate. The output X_{out} of the upsampler as a function of the sample index or discrete time variable n can be written as.

$$X_{\text{out}}[n] = \begin{cases} X_{\text{in}}[n/U] & n = kU \\ 0 & \text{otherwise} \end{cases}, \tag{12.41}$$

where X_{in} is the input to the upsampler, and k is any integer.

The insertion of zero samples introduces changes in the spectrum of the signal. Therefore, a low-pass filter is required to remove undesired frequency components. From a time domain perspective, the filter performs a linear interpolation between the samples for the reconstruction of the original signal. The cutoff frequency f_c of this low-pass filter is given by.

$$f_c = \frac{f_s}{2U}, \tag{12.42}$$

where f_s is the original sampling frequency.

Fig. 12.27 shows a block diagram of the digital signal processing section of the memoryless gain-based predistorter.

12.4.3 Digital predistortion adaptation

The analog predistorters presented in Sections 12.3.2 and 12.3.3 are open-loop devices, i.e., they are designed to perform a specific predistortion function without the possibility of adapting to changes in the transfer characteristic of the power amplifier over time. The dynamic adaptation of a predistorter is a difficult task that must be carefully implemented to guarantee system stability and actual distortion reduction under a wide range of operating parameters.

The situation is quite different for a digital predistorter. The predistortion function is not produced by analog components but by coefficients stored in a look-up table. It is, therefore, much simpler to implement an adaptation algorithm through the straightforward manipulation of the look-up table coefficients compared to trying to alter the nonlinear characteristics of an analog predistorter by varying, for instance, a bias voltage.

A typical adaptation algorithm performs the comparison between the output signal of the power amplifier and the input signal to the predistorter. The difference between these two signals becomes the error function to minimize by operating on the values stored in the look-up table, with the goal of obtaining a constant magnitude and phase of the gain of the predistorter-power amplifier system as a function of the input power, as described by Eqs. (12.10), (12.11).

Several convergence algorithms can be used for the minimization of the error function.[20, 21] The look-up table values can be dynamically modified after the initial convergence is achieved to maintain optimum performance under variations of the operating parameters. The mapping predistorter described earlier will be slower to converge than the gain-based predistorter because every possible entry of its large look-up table must be updated to complete the adaptation process.

Fig. 12.28 shows the simplified block diagram of an adaptive digital predistorter. The output of the power amplifier is sampled and downconverted to baseband using a quadrature demodulator that shares the same local oscillator used by the quadrature modulator. A time delay must be introduced to align the feedback and forward signals in time. The adaptation algorithm performs the calculation of the look-up table coefficients. A signal that exercises the full dynamic range of the power amplifier is necessary to allow for the calculation of the look-up table coefficients. A two-tone signal or a single-tone ramp can be used, provided that the peak output power of the amplifier reaches the saturation point to ensure that the look up table values include the entire dynamic range of the power amplifier. Other modulated signals that follow the above criteria can be used, but their probability density function can affect the look-up table accuracy because the signal may only spend brief periods of time at certain power levels.

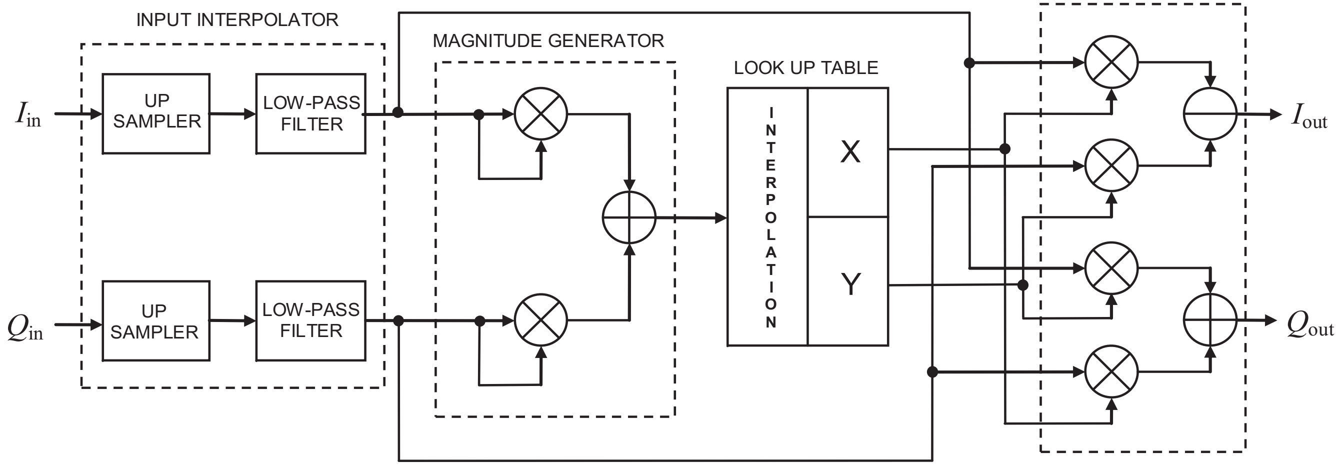
INPUT INTERPOLATOR
I_{in}
UP SAMPLER
LOW-PASS FILTER
Q_{in}
UP SAMPLER
LOW-PASS FILTER
MAGNITUDE GENERATOR
LOOK UP TABLE
INTERPOLATION
X
Y
I_{out}
Q_{out}

FIG. 12.27

Digital signal processing section of the memoryless gain-based predistorter.

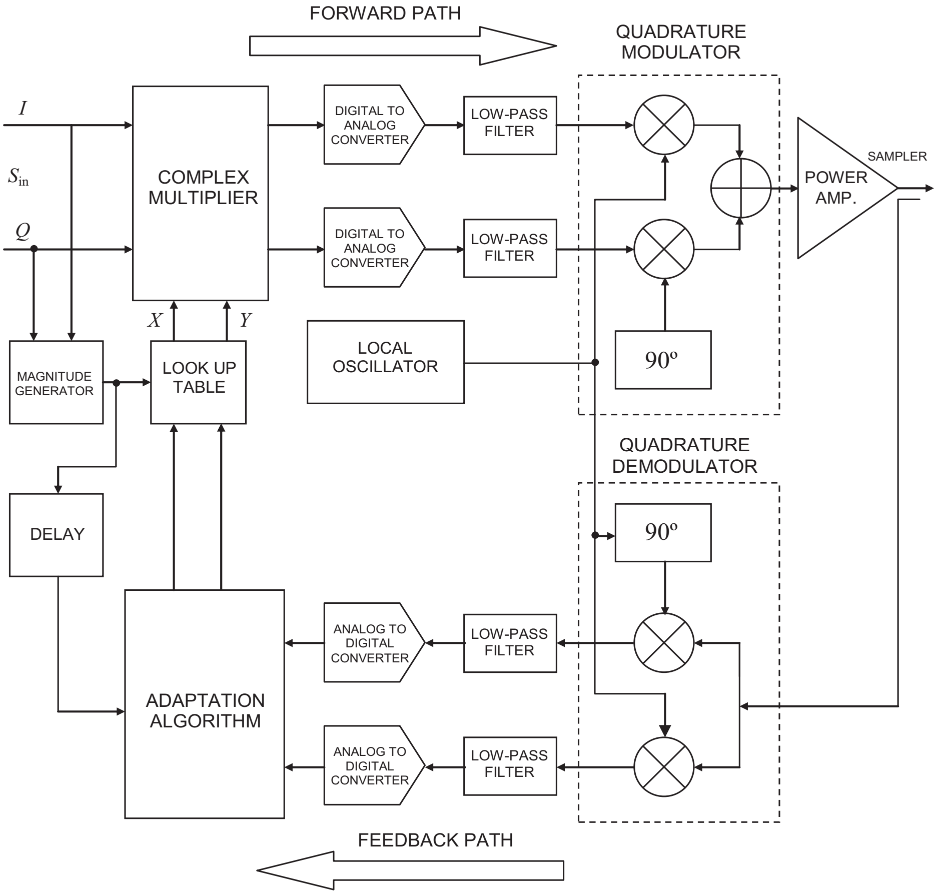
FORWARD PATH
QUADRATURE MODULATOR
I
S_{in}
Q
COMPLEX MULTIPLIER
DIGITAL TO ANALOG CONVERTER
DIGITAL TO ANALOG CONVERTER
LOW-PASS FILTER
LOW-PASS FILTER
SAMPLER
POWER AMP.
X
Y
MAGNITUDE GENERATOR
LOOK UP TABLE
LOCAL OSCILLATOR
90º
QUADRATURE DEMODULATOR
DELAY
90º
ADAPTATION ALGORITHM
ANALOG TO DIGITAL CONVERTER
ANALOG TO DIGITAL CONVERTER
LOW-PASS FILTER
LOW-PASS FILTER
FEEDBACK PATH

FIG. 12.28

Simplified block diagram of an adaptive digital predistorter.

12.4.4 Digital predistorter performance

Fig. 12.29 shows the spectrum of a solid-state power amplifier after the application of digital predistortion. The test signal consists of two identical tones with a separation of 2 MHz. The power amplifier was operated at 3-dB output back-off, which coincides with the peak-to-average ratio of the two-tone signal. The digital predistorter can reduce the IMD3 by more than 10 dB.

Fig. 12.30 shows the spectrum of a digitally predistorted traveling-wave tube amplifier. In this case, 11 equal-amplitude carriers are used as the test signal. The carriers are all in phase, for which the peak-to-average ratio is 10.4 dB. The spectrum on the left was obtained by operating the amplifier at 10-dB output back-off, whereas the spectrum on the right was measured at 11-dB output back-off. A significant improvement in distortion cancellation can be achieved when the output power level is such that the peak amplitude of the signal does not reach the saturation level of the amplifier.

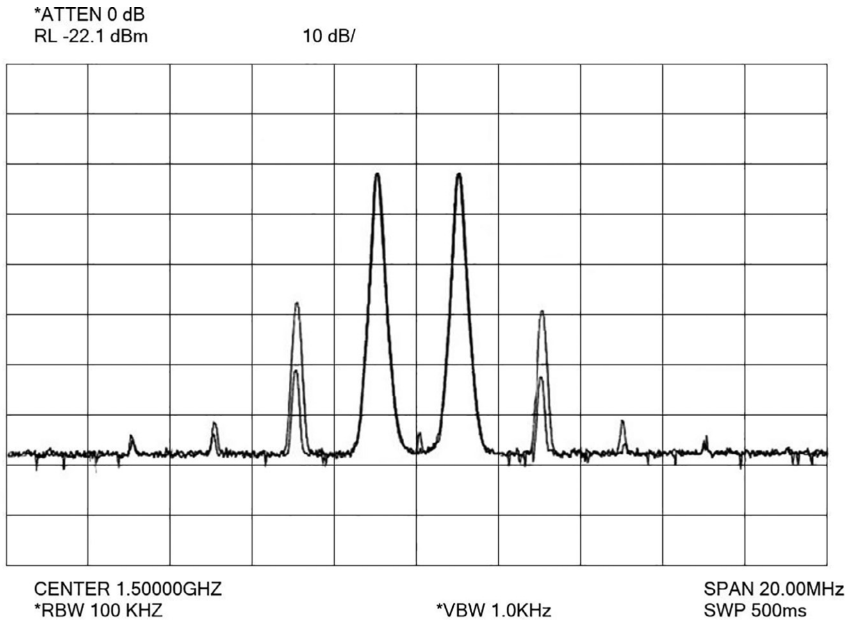

FIG. 12.29

Digital predistortion of a solid-state power amplifier using a two-tone signal.

12.5 Memory effects in predistortion linearization

12.5.1 Introduction

A system is said to have memory when its transfer characteristic depends on the past values of its input signal. For example, the transfer characteristic of an RF power amplifier may be different if the amplifier is excited by a steady carrier or by a pulsed carrier, both having the same amplitude. In the steady carrier case, the temperature may rise slowly over time, but when the amplifier is pulsed, the temperature may rise and fall between the pulses, affecting the gain of the amplifier, among other of its characteristics. Reactive elements, such as capacitors and inductors, mainly in the bias network, will charge and discharge during the carrier pulses, creating additional spectrum at the output of the amplifier due to the modulation of the bias voltages.[22]

12.5.2 Spectral regrowth due to memory effects

Memory in RF and microwave power amplifiers can generate additional spectrum that may look almost identical, at first glance, to that generated by nonlinear distortion. For example, Fig. 12.31 shows the effect of a two-tone signal mixing with its envelope; the resulting frequencies are identical to the IMD3 products. A similar situation could be caused by the second harmonic mixing with the fundamental.[23] If a predistorter is designed to cancel out distortion generated by nonlinearity in the active device of a power amplifier, its cancellation effectiveness can be degraded by the spectrum generated by memory

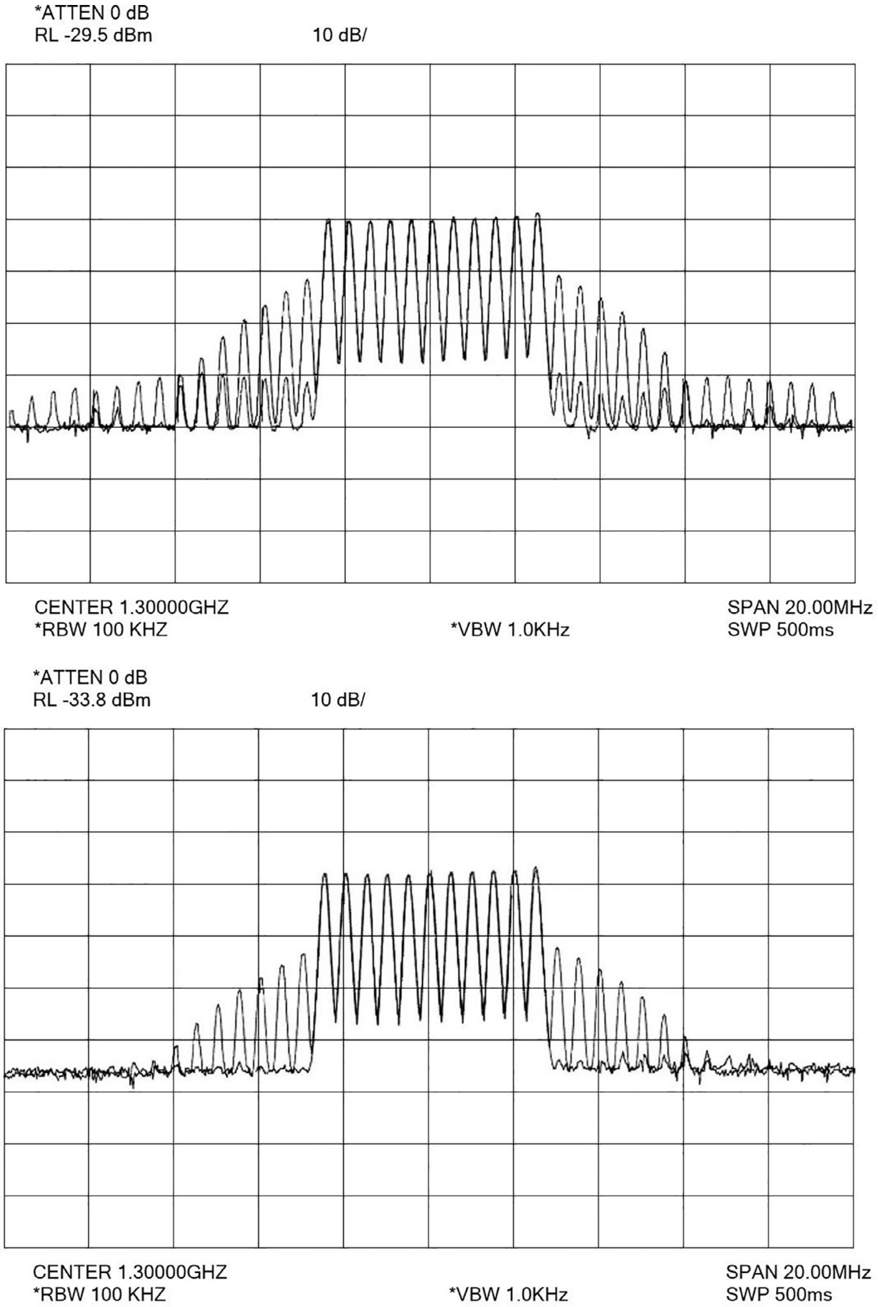

FIG. 12.30

Digital predistortion of a traveling wave tube amplifier using 11 equal-amplitude, coherent carriers. Top: 10-dB output back-off; bottom: 11-dB output back-off.

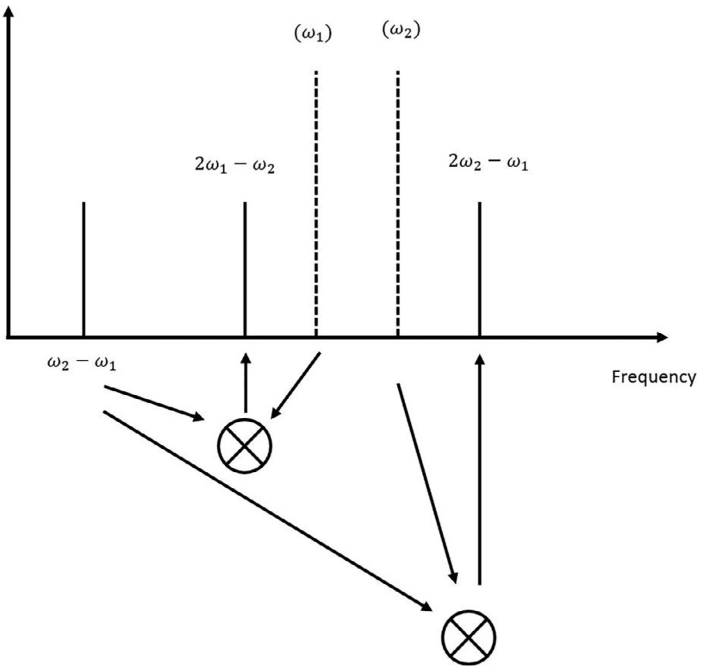

FIG. 12.31

The envelope frequency can generate mixing products at the same frequency of the IMD3, as shown with this two-tone signal.

effects. Two possible solutions to this problem are the use of a predistorter with memory, or preferably, the minimization of memory effects by design.

The main source of memory effects in a power amplifier is usually caused by its bias networks, which require reactive elements such as capacitors and inductors to achieve the desired impedances across the spectrum, while supplying the necessary dc voltage to the active device of the amplifier. These reactive elements will charge and discharge following the envelope of the signal, introducing memory, sometimes called *bias-induced* memory effects.[22] Variations of the supply voltage to an amplifier as a function of the envelope of the signal will cause the amplitude and PM of the output of the amplifier, generating modulation sidebands that will interfere with the cancellation of IMD of a memoryless predistorter.

12.5.3 Bias-induced memory effects and modulation sideband asymmetry

Fig. 12.32 shows the simplified schematic of an RF power amplifier. The active device is represented by a current source that is controlled by an input voltage (or current, depending on the type of active device) and a voltage-dependent capacitor C_{ds}. When the active device draws dc current from the bias network to generate RF power, there will be a voltage drop across the inductor and its associated resistor that represents the inductor's resistive loss. This voltage drop will cause amplitude modulation

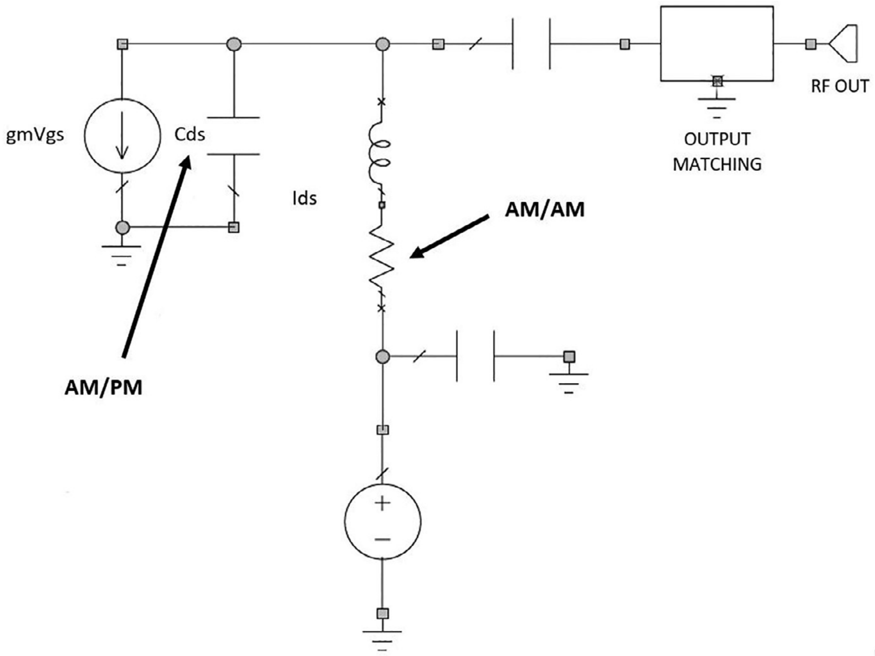

FIG. 12.32

Simplified schematic of an RF power amplifier showing the key elements that generate memory effects.

(AM) of the output as a function of AM of the input (AM/AM) as well as PM of the output because of AM of the input (AM/PM) because of the dependence of the capacitor C_{ds} on the voltage applied to it.

Although the modulation waveforms may not be perfectly sinusoidal, even for a two-tone envelope, a sinusoidal analysis can still be useful in demonstrating the bias modulation mechanism in analytical form. Eq. (12.43) shows the output voltage V_0 of a power amplifier in which simultaneous amplitude and PM of its output is taking place,

$$V_0(t) = \left[\frac{1}{2} + \frac{A}{2}\cos\omega_m t\right]\cos\left[\omega_c t + \varphi\cos(\omega_m t + \theta)\right], \tag{12.43}$$

where A is the amplitude modulation index, ω_c is the carrier angular frequency, t is the time, φ is the maximum value of phase modulation ($<\pi/2$), and θ is the relative phase between the AM and the PM.

Because the PM is a constant-envelope process, the AM can be analyzed independently as

$$V_{AM}(t) = \left[\frac{1}{2} + \frac{A}{2}\cos\omega_m t\right]\cos(\omega_c t), \tag{12.44}$$

$$V_{AM}(t) = \frac{1}{2}\cos(\omega_c t) + \frac{A}{2}\left[\cos(\omega_c t)\cos(\omega_m t)\right], \tag{12.45}$$

$$V_{AM}(t) = \frac{1}{2}\cos(\omega_c t) + \frac{A}{4}\left[\cos(\omega_c - \omega_m)t + \cos(\omega_c + \omega_m)t\right]. \tag{12.46}$$

The last two terms of Eq. (12.46) are the upper and lower sideband of the AM.

The PM process can be analyzed as

$$V_{PM}(t) = \cos\left[\omega_c t + \varphi\cos(\omega_m t + \theta)\right]. \tag{12.47}$$

$$V_{PM}(t) = \cos(\omega_c t)\cos\left[\varphi\cos(\omega_m t + \theta)\right] - \sin(\omega_c t)\sin\left[\varphi\cos(\omega_m t + \theta)\right]. \tag{12.48}$$

Using Bessel functions of the first kind and order 0 and 1 and ignoring the higher-order terms, Eq. (12.48) can be analyzed for the carrier and the modulation sidebands.

$$\begin{cases} \cos(a\cos b) \approx J_0(a) \\ \sin(a\cos b) \approx 2J_1(a)\cos b\text{'} \end{cases} \tag{12.49}$$

$$V_{PM}(t) = \cos(\omega_c t)J_0(\varphi) - \sin(\omega_c t)2J_1(\varphi)\cos(\omega_m t + \theta), \tag{12.50}$$

$$\begin{aligned} V_{PM}(t) = J_0(\varphi)\cos(\omega_c t) - J_1(\varphi)\sin\left[(\omega_c - \omega_m)t - \theta\right] \\ -J_1(\varphi)\sin\left[(\omega_c + \omega_m)t + \theta\right]. \end{aligned} \tag{12.51}$$

If the relative phase θ between the AM and the PM is $\pm\frac{\pi}{2}$,

$$V_{PM\left[\theta=\pm\frac{\pi}{2}\right]}(t) = J_0(\varphi)\cos(\omega_c t) \mp J_1(\varphi)\sin(\omega_c - \omega_m)t \pm J_1(\varphi)\sin(\omega_c + \omega_m)t. \tag{12.52}$$

If $\theta = 0$; π, then.

$$V_{PM[\theta=0;\,\pi]}(t) = J_0(\varphi)\cos(\omega_c t) \mp J_1(\varphi)\sin(\omega_c - \omega_m)t \mp J_1(\varphi)\sin(\omega_c + \omega_m)t. \tag{12.53}$$

In Eqs. (12.52), (12.53), the last two terms represent the modulation sidebands because of PM. For phase angles $\theta = 0$ or π, the PM sidebands add to the AM sidebands according to Eq. (12.46), producing a symmetrical sideband spectrum at both sides of the carrier. However, for phase angles $\theta = \pm\pi/2$, the upper and lower sidebands add and subtract, producing an asymmetrical spectrum; the sidebands will attenuate or reinforce, depending on the sign of θ and the AM and PM modulation indices. Other values of θ not mentioned above will produce asymmetrical modulation sideband spectra, too. Even if a highly effective predistorter can completely cancel IMD3, the output of the amplifier will still show significant energy at the frequencies because of the amplitude and PM introduced by the bias network.

The gate or base bias network of a power amplifier can cause the same effects described above. The currents involved are usually much lower than for drain or collector biasing, but the sensitivity to voltage variations is much higher.

To illustrate the effect of the memory effects introduced by the bias network, an 800-MHz RF power amplifier was simulated and excited by two carriers separated by 5 MHz. Its drain supply voltage is 6 V. Fig. 12.33 shows the drain voltage as a function of time using a low-pass filter to reject the 800-MHz carriers and the output spectrum. There is good symmetry of the IMD products. No envelope-frequency ripple can be observed on the drain collector dc supply. A small resistor was then added in series with the bias network to introduce ripple at the envelope frequency, as shown in Fig. 12.34. The spectrum is still symmetrical because there is no reactance added to the bias network, making $\theta = 0$ in Eq. (12.53). However, the IMD products are now higher because they also include the contributions from the AM and PM caused by the voltage drop across the resistor. Finally, Fig. 12.35 shows the drain waveform when a large inductor is added to the bias network. The reactance introduced by the inductor is significant at the envelope frequency of 5 MHz, generating ripple and, consequently, AM and PM. The inductive reactance also introduced a delay between voltage and current, making $\theta \neq 0$; π, as in Eq. (12.52), causing the IMD spectrum to become asymmetrical because of the

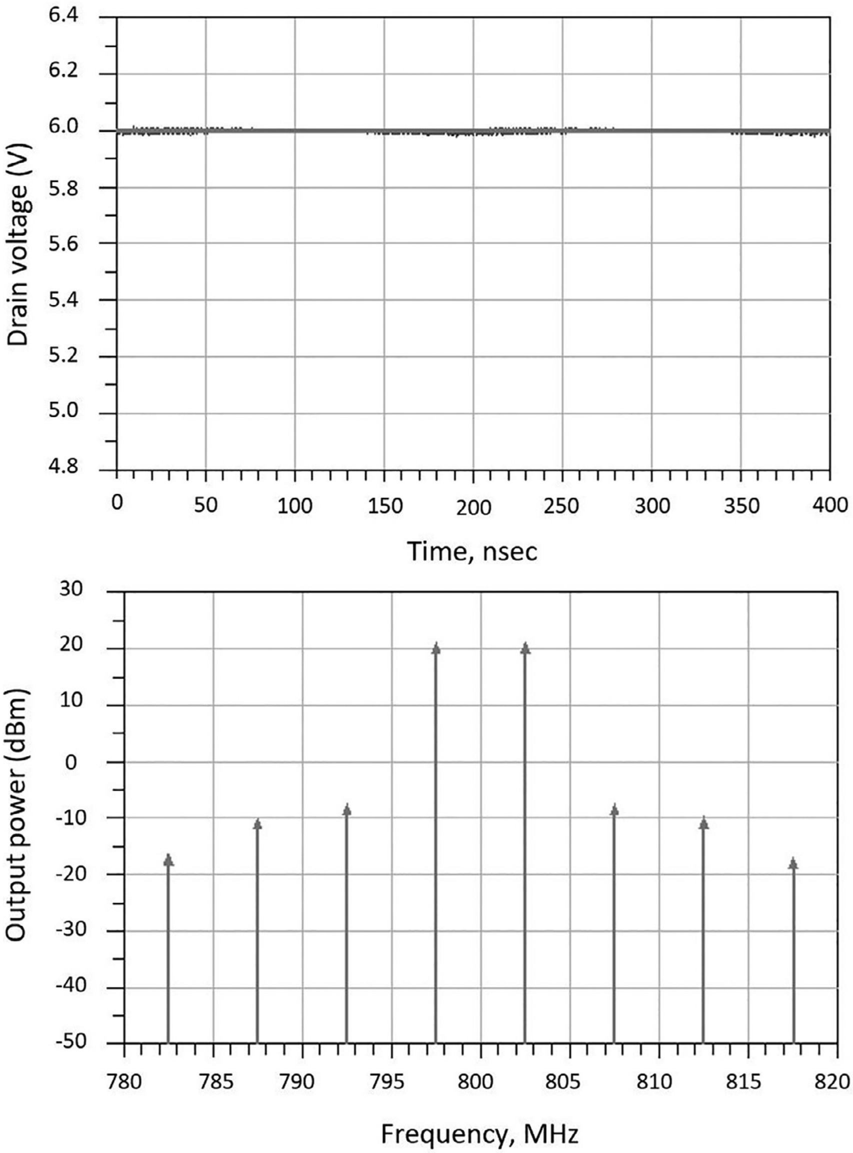

FIG. 12.33

Drain voltage waveform and output spectrum of an RF power amplifier with a small inductor in its drain bias network. The output spectrum is symmetrical.

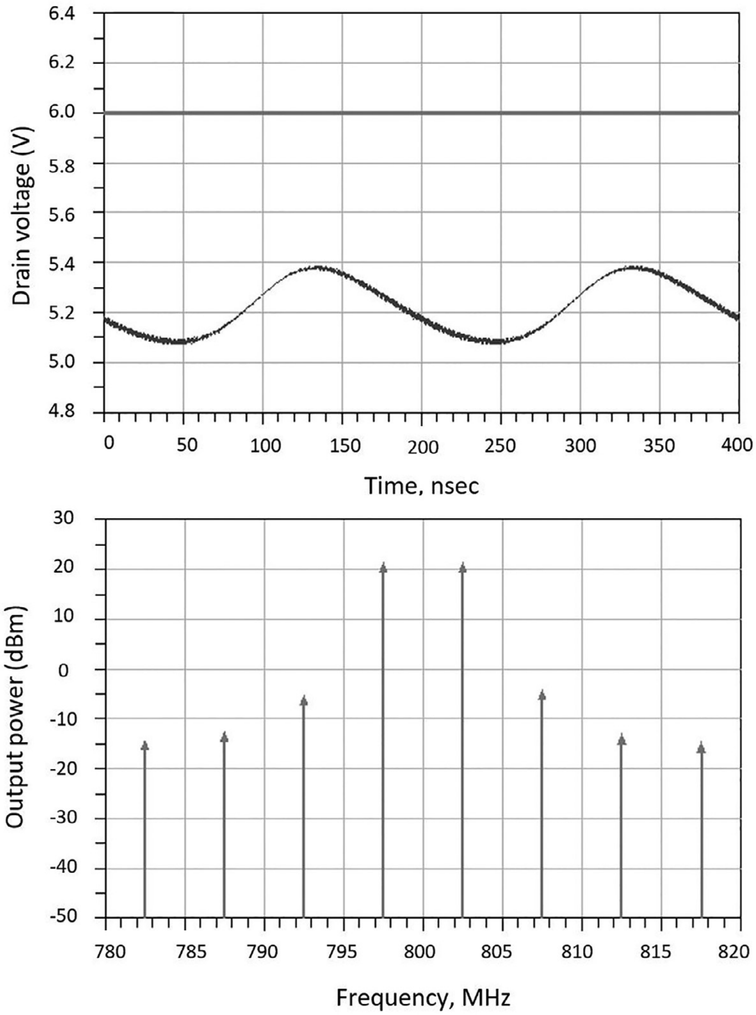

FIG. 12.34

Drain voltage waveform and output spectrum of an RF power amplifier with a resistor in its drain bias network. The output spectrum is symmetrical.

reinforcement and attenuation of the IMD products due to the modulation sidebands. The highest IMD product, in this case, the lower IMD3, is higher than in Fig. 12.33, whereas the upper IMD3 is lower. Applying a memoryless predistorter in this scenario will cancel the IMD component of the combined IMD/modulation sidebands, but it will not cancel the modulation sidebands, limiting the effectiveness of the predistorter. The asymmetry will vary as a function of the output power; at high power, the IMD will dominate the spectrum, whereas the modulation sidebands will dominate at lower power.

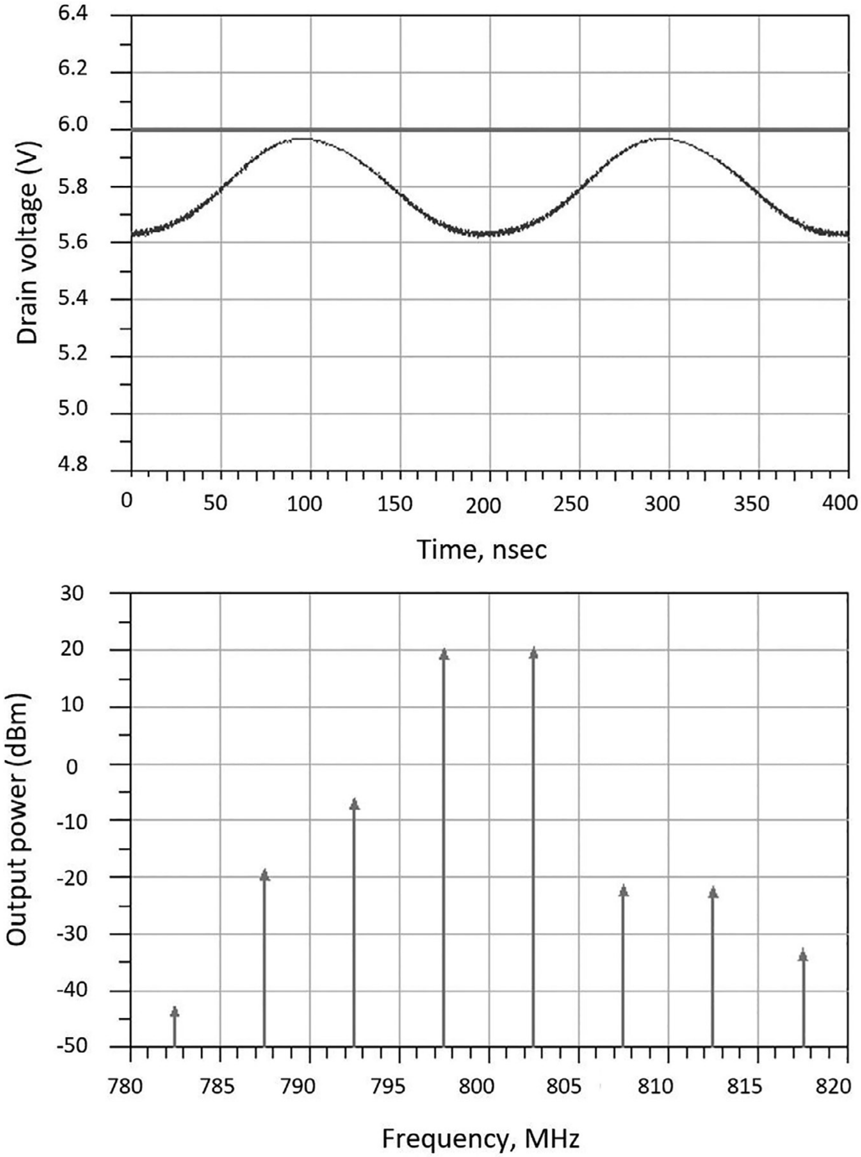

FIG. 12.35

Drain voltage waveform and output spectrum of an RF power amplifier with a large inductor in its drain bias network. Asymmetry is observed in the output spectrum.

The impedance presented by the bias networks of an RF power amplifier can significantly influence its linearity by introducing memory. Presenting a low impedance at the envelope frequency is important to keep the envelope from modulating the power amplifier and causing additional spectrum regrowth. The signal bandwidth increases with the use of a predistorter, for which the power amplifier must be capable of supporting the increased bandwidth without introducing memory.

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CHAPTER

Computer-aided design of switchmode power amplifiers

13

Nonlinear circuit simulation in the frequency and time domains is a very important tool for analysis, design, and optimization of high-efficiency switchmode power amplifiers of Classes-D,DE, and E. The advantages are as follows: significantly reduced development time and final product cost, better understanding of the circuit behavior, and faster obtaining of the optimum design. It is especially important at very high frequencies, including microwaves and millimeter waves, and for microwave monolithic integrated circuit (MMIC) development, where the transistor and circuit parasitics can significantly affect the overall power-amplifier performance. Therefore it is very important to incorporate into the simulator as accurate a transistor model as possible, to approximate correctly the device behavior, not only at the fundamental frequency but also at the second- and higher-order harmonics of the operating frequency. In this chapter, the different computer-aided design (CAD) programs are described to analyze the time- and frequency-domain behavior of the switchmode high-efficiency power amplifiers in different frequency ranges from high frequencies to microwaves, including HB-PLUS and SPICE CAD tools for Class-D and Class-DE circuits and HEPA-PLUS, SPICE, and ADS CAD tools for Class-E circuits. The detailed simulation example of a high-efficiency two-stage 1.75-GHz HBT MMIC power amplifier that uses microstrip transmission lines in the supply and load networks is presented and discussed.

13.1 HB-PLUS program for half-bridge and full-bridge direct-coupled voltage-switching Class-D and Class-DE circuits

Program capabilities. The HB-PLUS CAD program can simulate and automatically optimize resonant and nonresonant half-bridge or full-bridge circuits with a load that receives the output power, driven through a load network.[1] Several versions of the circuit are described in Chapter 2; the simplest tuned version is shown in Fig. 2.6. The switching power transistors can be operated in the hard-switching mode (Class-D; both switches operating at 50% duty ratio, and the transistor switch is turned on with the full DC supply voltage across the transistor), or the soft-switching mode (Class-DE; each transistor is turned on with nearly zero voltage across the transistor, achieved by using smaller than 50% duty ratio of each transistor). The circuit can be used as an RF or microwave power amplifier, as a DC-DC converter, as a DC-AC inverter, or as an AC (including RF and microwave) power generator. The HB-PLUS program performs the following functions:

- Simulates very rapidly the steady-state periodic response of the circuit, 100–1000 times as fast as with SPICE and about 10 times as fast as with Agilent ADS. The outputs are time-domain graphical

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plots and frequency domain spectra of all important circuit voltage and current waveforms, and a tabulation of input power from the DC supply, RF output power, efficiency, inefficiency, and power dissipation in each circuit element (including the parasitic power losses in each inductor and capacitor). The spectrum is computed for frequencies from DC through the 31st harmonic of the operating frequency.
- Simulates the cycle-by-cycle transient response, from any computed or user-specified starting condition, to any combination of time-varying circuit parameters, such as switching frequency, switch duty ratio, DC supply voltage, and load impedance. The available outputs are the same as for the steady-state periodic response.
- Sweeps up to 28 circuit parameters and plots one or two output variables versus the swept parameter.
- Optimizes the design automatically, according to tradeoffs that can be specified among input DC power, output RF power, efficiency, inefficiency, and each component of power loss.
- Computes transfer functions: any output variable versus any circuit parameter.

The steady-state periodic response of the circuit to the periodic input drive is the circuit operation after the start-up transient has died away, which is the operation, usually observed in experimental results. HB-PLUS simulates the voltage-switching Class-D or Class-DE circuit very quickly and the simulation requires approximately 8 ms on a Pentium III/667-MHz computer.

Using the cycle-by-cycle transient response, it is possible to evaluate transient stresses

- occurring during equipment turn-on and turn-off
- resulting from transient changes of load (including load faults of shorted or open load, or any arbitrary impedance magnitude and angle)
- resulting from application or removal of input drive with the DC supply voltage present
- resulting from transient changes of DC supply voltage
- resulting from failure of any circuit element

or simulate the transient response to modulation of any combination of time-varying circuit parameters. This text refers to the half-bridge circuit; the *HB-PLUS User Manual* also explains how to simulate and optimize the full-bridge circuit.

Circuit topologies. Fig. 13.1A shows the general model of a half-bridge voltage-switching Class-D or Class-DE circuit used in HB-PLUS including a DC power supply V_{cc}, a load network and load, and two switches. The switch-enhanced macro-model, which can accurately represent any type of input-controlled solid-state switches based on different types of bipolar junction transistors (BJTs), metal-oxide-semiconductor field-effect transistors (MOSFETs) or metal-semiconductor field-effect transistors (MESFETs) is shown in Fig. 13.1B where V_o is the saturation offset voltage, V_t is the turn-on threshold voltage of internal or external anti-parallel diode (the parasitic substrate diode of a silicon MOSFET or an external diode intentionally connected from emitter to collector of a BJT), R_d is the ohmic resistance of the anti-parallel diode, R_{on} is the on-resistance ($R_{ds(on)}$ for a MOSFET or $R_{ce(sat)}$ for a BJT), and C_{out} is the equivalent transistor output capacitance characterized by its parasitic resistance $R_{C_{out}}$.[2]

The load-network configuration shown in Fig. 13.2 includes a general-purpose multiple-inductor/multiple-capacitor network. It can be used to represent a nonresonant network or a resonant network that is series-loaded, parallel-loaded, or split-reactor-loaded, where either loss resistances or quality factors for all inductors and capacitors can be specified. The extended configuration of the load

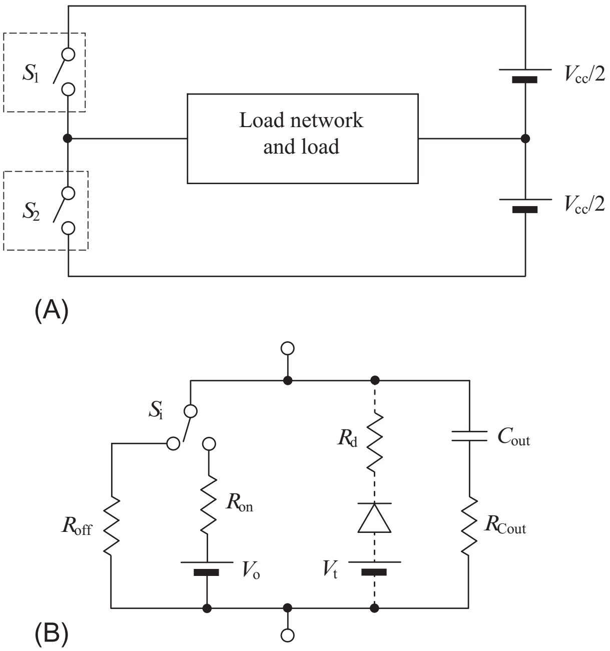

S_1
S_2
Load network and load
$V_{cc}/2$
$V_{cc}/2$
(A)
S_i
R_{off}
R_{on}
V_o
R_d
V_t
C_{out}
R_{Cout}
(B)

FIG. 13.1

General model of half-bridge voltage-switching Class-D power amplifier: (A) basic circuit and (B) equivalent switch model.

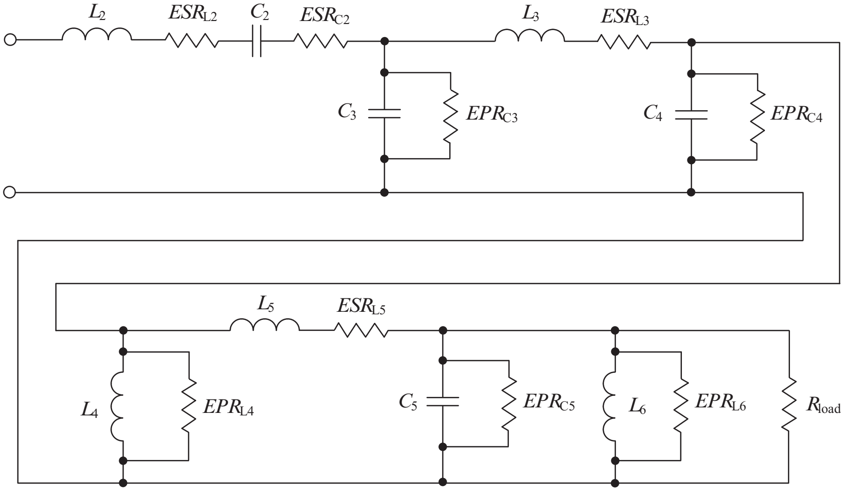

L_2
ESR_{L2}
C_2
ESR_{C2}
L_3
ESR_{L3}
C_3
EPR_{C3}
C_4
EPR_{C4}
L_5
ESR_{L5}
L_4
EPR_{L4}
C_5
EPR_{C5}
L_6
EPR_{L6}
R_{load}

FIG. 13.2

Load network and load in HB-PLUS.

network provides considerable flexibility for representing a particular circuit arrangement, where R_{load} is a resistor to which the RF output power is delivered. The inductor and capacitor that are adjacent to R_{load} allow representing the load as generic *RLC* impedance. Alternatively, R_{load} and its adjacent L and C can represent the input-port impedance of an external two-port network that performs the functions of coupling, tuning, and impedance-transformation of a load located at the output port. Which L and C components will be adjacent to R_{load} depends on which reactive components the user includes in the load network; the user can remove unwanted components. The two-port network's input/output transmission function can include attenuation, by using the *ESR* and *EPR* components that are associated with the L and C that are adjacent to R_{load}. For example, the two-port network's input/output transmission function has an attenuation $(1/EPR_{\mathrm{C5}}+1/EPR_{\mathrm{L6}})/(1/EPR_{\mathrm{C5}}+1/EPR_{\mathrm{L6}}+1/R_{\mathrm{load}})$. The full high-frequency T-model of a transformer includes mutual inductance and core loss (L_4 and EPR_{L4}), primary and secondary leakage inductances (L_3 and L_5), winding resistances (ESR_{L3} and ESR_{L5}), and winding capacitances (C_3 and C_5). The capacitor C_4 represents a distributed model of winding capacitance. The inductor L_2 can be the inductor of a resonant load network or the commuting inductor of a nonresonant soft-switching (zero-voltage turn-on) load network. The capacitor C_2 can be the resonance capacitor of a resonant load network or the DC-blocking capacitor of a nonresonant network. If the user is not using the two-port macro-modeling technique discussed previously, R_{load}, L_6, C_5, EPR_{L6}, and EPR_{C5} can represent a general-purpose *RLC* network that models any chosen four parameters of any arbitrary load impedance, for example, magnitude and phase at the operating frequency, magnitude or phase at the third-harmonic frequency (the even-harmonic voltages and currents are usually negligibly small in bridge-type power converters), and fractional power loss (attenuation) at all frequencies, as discussed earlier. Alternatively, C_4L_4 can represent a parallel resonator, C_2C_3 can represent a split resonance capacitor, L_3L_4 (or L_5L_6) can represent a split resonance inductor, and others. Using a two-port macro-model for the external two-port network yields accurate results with faster computation than would be obtained by computing separately the voltages and currents of all individual components that collectively provide the functions modeled by the two-port macro-model.

Class-D versus *Class-DE*. P.J. Baxandall published the first description of a Class-D circuit, in a paper discussing voltage-switching and current-switching self-excited oscillators.[3] Later publications by other authors discussed the use of the circuit in tuned and untuned amplifiers. In those early publications, the transistor switches were operated with "on" duty ratio of 50%, resulting in "hard turn-on switching" of the transistors: a turning-on upper transistor (S_1 in Fig. 13.1A) would charge the switching-node capacitance from ground up to the positive-supply rail, and a turning-on lower transistor (S_2 in Fig. 13.1A) would discharge that capacitance from the positive-rail voltage down to ground. The switching-node capacitance is the output capacitances of the two transistors, plus circuit wiring capacitance. The charging and discharging power dissipations resulting from hard-switching were $(CV^2f)/2$ at each turn-on transition (twice per cycle of the switching frequency), where C is the node capacitance, f is the switching frequency, and V is the DC supply voltage (labeled "$2V_{\mathrm{cc}}$" in Figs. 2.6 and 2.7, and "V_{cc}" in Fig. 13.1A). When the circuit was being used at audio frequencies that power dissipation was not a problem but as users applied the technique at frequencies higher than a few-hundred kHz, the capacitor-discharge power dissipation became objectionable.

S.A. Zhukov and V.B. Kozyrev published a technique for eliminating the power dissipation associated with charging and discharging the node capacitance.[4] The duty ratio of each transistor switch is reduced from 50% to a lower value, leaving a "conduction gap" during which both switches are "off,"

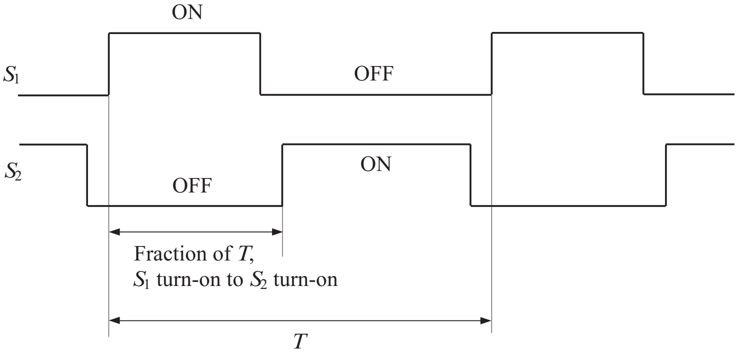


FIG. 13.3

Switch timing for Class-DE.

as shown in Fig. 13.3. During that conduction gap, the current in the inductor of the load network can charge the node capacitance up to the positive rail, and discharge that capacitance down to ground. They suggested choosing the circuit parameters to yield a switch-voltage waveform that has zero voltage and zero-voltage slope, at the time the switch will be turned “on.” Those conditions are the same as in the nominal waveform of a Class-E amplifier described in Chapter 5. Because the circuit operates like Class-D, modified to have turn-on transitions like Class-E, later authors referred to that variant of Class-D as “Class-DE.” D.C. Hamill updated this publication and made it easily available to the English-speaking part of the world.[5]

If the load-network inductance value is intentionally made larger than the value needed for resonance with the network capacitance at the switching frequency, zero-voltage turn-on switching can be achieved with a larger switch duty ratio (narrower conduction gap) than would be needed if the inductance resonated with the capacitance at the switching frequency. That increases the output power available at a given level of peak current in the transistor, or it decreases the peak current needed for a specified output power. A unique feature of HB-PLUS program is the ability to adjust automatically the values of the circuit elements (capacitors, inductors, and resistors) and circuit parameters (switching frequency and switch conduction duty ratio) to achieve optimum performance. The meaning of “optimum” is defined by an *objective function* which comprises a series of terms, each of which pertains to one aspect of circuit performance. For each performance parameter of interest, a *target* value and a *handicap* (tradeoff) value are entered. The target value is the value which is required to achieve representing, for example, the number of watts of output power. The handicap value represents the relative number of units of that performance parameter that corresponds in importance to the specified handicap values of each of the other performance parameters. For example, if the handicap for efficiency is 2.0 and the handicap for output power is 5.0, the program will understand that an increase of efficiency of 2.0% points has the same importance as an increase of output power of 5.0 W. A handicap value of zero instructs the program to ignore that parameter in computing the objective function.

13.2 HEPA-PLUS CAD program for Class-E

Program capabilities. The HEPA-PLUS CAD program can be used to simulate a variety of topologies of tuned and untuned single-ended and push-pull power amplifiers operating in Classes-AB,B, and C in output-power saturation and in Class-E and some types of Class-F.[6] The program performs the following design functions:

- Evaluates a priori the performance achievable with a candidate transistor in a nominal-waveform Class-E circuit using inductors and capacitors with specified quality factors. The output is plots of efficiency versus frequency at four values of output power, for specified ranges of frequency and output power.
- Automatically makes a preliminary circuit design to meet the specified design goals using inductors and capacitors with specified quality factors. The output is a complete set of circuit-element values, which can be a starting point for a circuit optimization.
- Simulates very rapidly the steady-state periodic response of the circuit 100–1000 times as fast as with SPICE and about 10 times as fast as with Keysight ADS. The outputs are time-domain graphical plots and frequency-domain spectra of all circuit voltage and current waveforms and a tabulation of input power from the DC supply, output power, efficiency, inefficiency, power dissipation in each element (including the parasitic power losses in each inductor and capacitor), and transistor peak voltage and current in the normal and inverse directions.
- Simulates the cycle-by-cycle transient response, from any starting condition, to a transient change of any combination of input drive, DC supply voltage, and circuit-parameter values. The available outputs are the same as for the steady-state periodic response.
- Sweeps any of the 25 circuit parameters and plots any one or two output variables versus the swept parameter.
- Optimizes the design automatically according to the specified trade-offs, among seven evaluation factors that include output power, efficiency, and transistor stresses.
- Computes required control functions: value of any circuit parameter versus any other circuit parameter to maintain a specified output voltage, current, or power, e.g., transistor conduction angle (duty ratio) versus required output-voltage amplitude, in a linear-amplifier or high-level modulator application.

Steady-state periodic response. The steady-state periodic response of the circuit to the periodic input drive is the circuit operation after the start-up transient has died away, which is the operation usually observe in experimental measurements. HEPA-PLUS simulates the switchmode Class-E circuit very quickly. For example, the simulation required approximately 8 ms on a 667-MHz computer making a 256-points frequency sweep from 13.5 to 14 MHz of the built-in default circuit.

Transient response. Using the cycle-by-cycle transient response, it is possible to evaluate transient stresses

- occurring during equipment turn-on and turn-off
- resulting from transient changes of load (including load faults of shorted or open load, or any arbitrary impedance magnitude and angle)
- resulting from application or removal of input drive with the DC supply voltage present
- resulting from transient changes of DC supply voltage
- resulting from failure of any circuit component

or simulate the transient response to modulation of any combination of time-varying circuit parameters such as DC supply voltage, input-drive frequency, transistor duty ratio (conduction angle), or any circuit-element value.

Circuit topology. Fig. 13.4 shows the generic single-ended topology used in HEPA-PLUS including both a switch and a load network. The switch model comprises a saturation offset voltage V_o, a turn-on threshold voltage V_t of internal or external anti-parallel diode (the parasitic substrate diode of a silicon MOSFET or an external diode intentionally connected from emitter to collector of a BJT), an ohmic resistance of the anti-parallel diode R_d, an on-resistance R_{on} ($R_{ds(on)}$ for a MOSFET or $R_{ce(sat)}$ for a BJT), an equivalent nonlinear transistor output capacitance C_{out} characterized by its parasitic resistance $R_{C_{out}}$, and a series parasitic inductance L_q modeling the inductance of the emitter or source bondwires. The load network includes five resonators (main series resonator L_2C_2 with parasitic loss resistances ESR_{L2} and ESR_{C2}, main parallel resonator L_3C_3 with parasitic loss resistances EPR_{L3} and EPR_{C3}, two auxiliary series resonators L_QC_{out} and $L_{C1}C_1$ and auxiliary parallel resonator $C_{out}L_{C1}$, an arbitrary *RLC* load impedance that can be placed at the R_2 location in series with the resonator L_2C_2 or at the R_3 location in parallel with resonator C_3L_3, and parasitic loss resistances for all circuit components). The resonators can each be made resonant at any chosen frequency, not necessarily at the operating frequency and not necessarily all at the same frequency. Components not used in a particular circuit can be deleted from the generic circuit topology by giving them negligibly small or negligibly large values or removing them.

Optimization. The HEPA-PLUS CAD program optimizes all components of the load network shown in Fig. 13.4, including simultaneous optimization of the load-network resistance and the impedance transformation (matching) network that transforms the external load impedance (connected at the matching-network's output port) to the optimum value of load-network resistance (presented at the matching-network's input port). That is, the external load R_3 is shunted by C_3, and the equivalent series C and lower-resistance R are tuned to purely resistive by adding an inductance in series with the

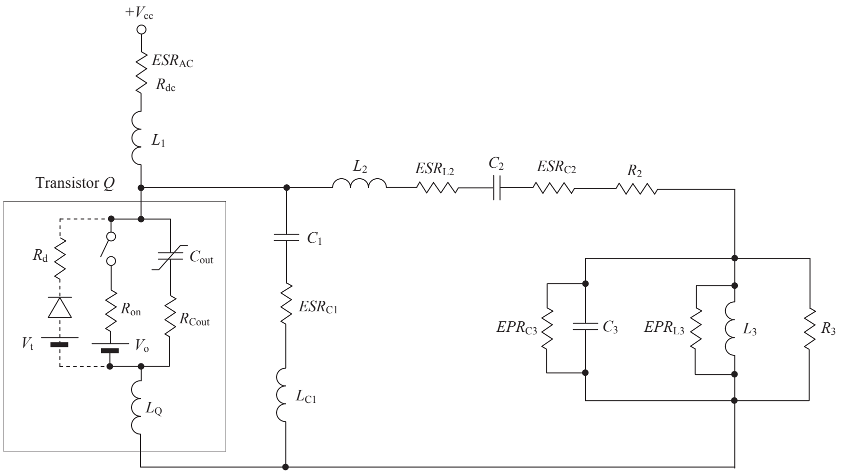


FIG. 13.4

Generic single-ended circuit topology (two such circuits are used for push-pull amplifiers; three types of combiners are available for combining the "push" and "pull" halves of the push-pull circuit).

equivalent C and R. The optimum values of C_3 and the added inductance are found automatically by the optimizer. That needed inductance is automatically added to the value of L_2 that would have been used as a resonator with C_2 and a purely resistive load. The external load impedance can be any arbitrary parallel RLC circuit (e.g., R_3, L_3, and C_3), not necessarily the commonly used purely resistive 50 Ω. The *HEPA-PLUS User Manual* gives full information on this useful feature.

13.3 Effect of Class-E load-network parameter variations

Mistuning of the Class-E load network parameters can have a significant effect on the output power and efficiency. In this case, it is convenient to define this effect visually based on the collector current and voltage waveforms to faster tune the load-network parameters to their optimum values. The effect of a change in the load angle $\psi = \tan^{-1}(\omega L/R)$ or normalized series inductance L on collector voltage and current waveforms of a Class-E power amplifier with shunt capacitance is shown in Fig. 13.5.[7] For values of ψ slightly less inductive than optimum of 49.05 degrees, the collector voltage at the turn-on instant attains a certain positive value, as shown in Fig. 13.5A. However, for values of ψ slightly more inductive than optimum, a small negative voltage swing appears, as shown in Fig. 13.5B. For capacitive loading and larger inductive loading, the collector voltage becomes large at the turn-on time, causing low efficiency. For extremely reactive loads, the collector voltage tends toward the ramp shape, which it would have with no load at all. The negative current capability is needed whenever the load is more inductive than the ideal 49.05 degrees. It should be mentioned that the efficiency remains close to 100% for load angles between ~40 and 70 degrees.

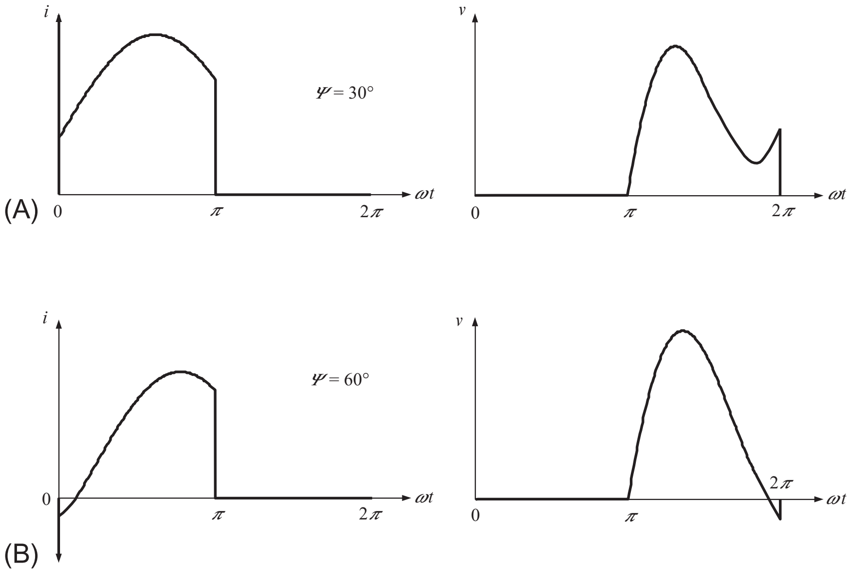


FIG. 13.5

Collector waveforms as functions of load angle.

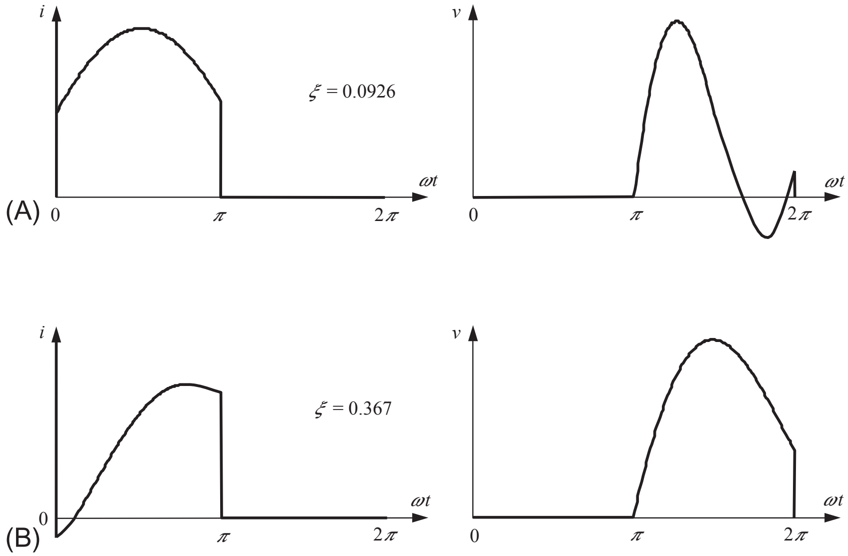


FIG. 13.6

Collector waveforms as functions of normalized shunt capacitance.

Fig. 13.6 illustrates the effect in the collector current and voltage waveforms of a change in the normalized shunt susceptance $\xi = \omega CR$ in a Class-E power amplifier with shunt capacitance of otherwise-nominal design.[7] In this case, low values of shunt susceptance produce a collector voltage that swings to both large positive and large negative values, as shown in Fig. 13.6A. While the voltage at turn-on time is never negative, the negative current is required for some values of ξ, as shown in Fig. 13.6B. As the shunt susceptance becomes large for the same load resistance, it tends to dominate, producing a ramp voltage waveform and drawing such current as is necessary to charge the capacitor. Under these conditions, the output power becomes constant but is small. It should be noted that the power amplifier is quite tolerant of variations of shunt susceptance and maintains high efficiency for values ξ between 0.06 and 0.3. The effect caused by deviation of the load resistance R from its optimum value shows that efficiency varies gradually, remaining at 95% or more for variations in the load resistance of +55% to −37%.

Fig. 13.7A shows the low-order Class-E load network with shunt capacitance and the typical mistuned collector voltage waveform demonstrating the transistor turn-on, turn-off, and waveform "trough." The inductor L_1 is considered an RF choke with high reactance to isolate DC and RF paths between each other. The reactance of the series circuit composing of L_2 and C_2 is inductive. At the turn-on time of the transistor, the collector voltage waveform has zero slope and zero voltage. An actual load network can approximate the idealized optimum (or nominal) conditions by adjusting its parameters C_1, C_2, and/or L_2. If R is not already the desired value for the desired output power, it may need adjustment as well. The circuit will operate with the nominal Class-E waveform, while delivering the specified output power at the specified frequency, if the chosen parameter values are installed in the actual hardware. The possible need for tuning results from tolerances on the component values

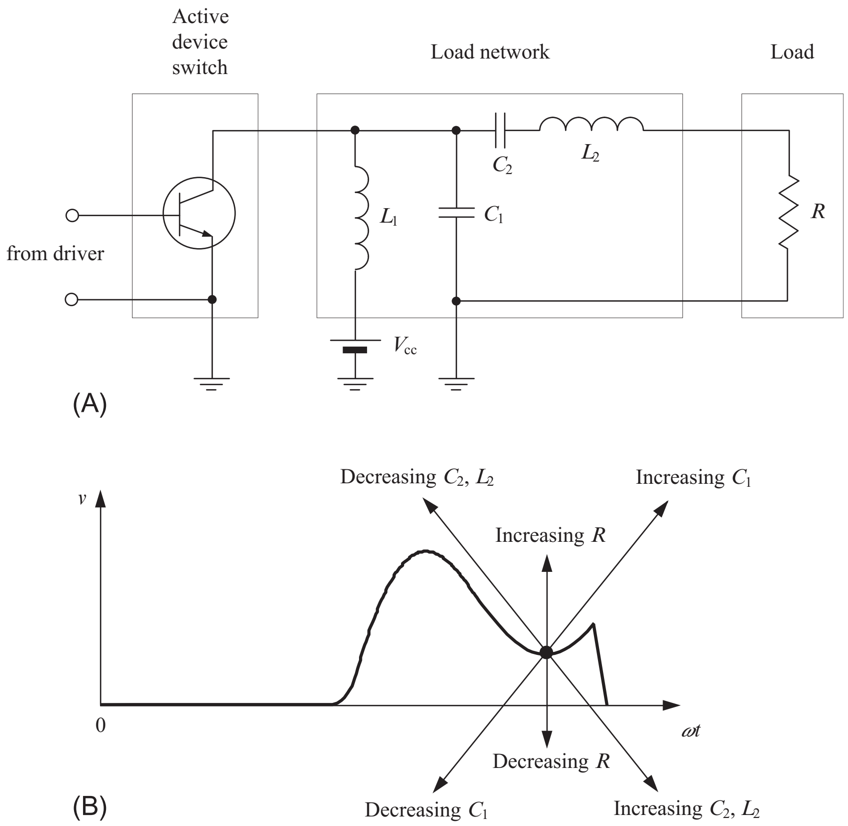

Active device switch
Load network
Load
from driver
L_1
C_1
C_2
L_2
R
V_{cc}
(A)
v
0
ωt
Decreasing C_2, L_2
Increasing C_1
Increasing R
Decreasing R
Decreasing C_1
Increasing C_2, L_2
(B)

FIG. 13.7

Load network and effect of adjusting its components.

(normally not a problem because Class-E has low sensitivity to component tolerances) and the possibility of unknown-value reactances in series with R (therefore in series with L_2 and C_2) after the load resistance has been transformed to the chosen value of R. Those series reactances require that the reactances of L_2 and C_2 be reduced by the amounts of the unknown inserted inductive and capacitive series reactances, but how can we do that when those inserted reactances are unknown?

If we know how changes of L_2 and C_2 will affect the collector voltage waveform, we can adjust L_2 and C_2 to meet two criteria at the operating frequency: achieve close to the nominal collector voltage waveform and deliver the specified value of output power.[8] Fig. 13.7B shows how L_2 and C_2 affect the collector voltage waveform. We know also that increasing L_2 reduces the output power and vice versa. In practice, with an oscilloscope displaying the voltage waveform and a directional power meter indicating the power delivered to the load, we can adjust L_2 and C_2 to simultaneously fulfill the two desired conditions (nominal waveform and desired output power) even if the reactances in series with R are unknown.

If C_1 (comprised of the transistor output capacitance and the external capacitor connected in parallel with it) is within approximately 10% of the intended value, C_1 will normally not need adjustment. When there is a large deviation from the design value, C_1 can be adjusted to achieve the nominal collector voltage waveform, using the information in Fig. 13.7B about the effects of C_1 on this waveform. In that case, the three components C_1, C_2, and L_2 can be adjusted to achieve three conditions simultaneously at the operating frequency: desired output power, transistor saturation voltage just before transistor turn-on, and zero slope of the voltage waveform just before turn-on.

Changes in the values of the load network components affect the collector voltage waveform as follows:

- Increasing C_1 moves the trough of the waveform upward and to the right.
- Increasing C_2 moves the trough of the waveform downward and to the right.
- Increasing L_2 moves the trough of the waveform downward and to the right.
- Increasing R moves the trough of the waveform upward (R is not normally an adjustable circuit element).

Knowing these effects, it is easy to adjust the load network for nominal Class-E operation by observing the collector voltage waveform. The adjustment procedure is as follows:

- Set R to the desired value or accept what exists.
- Set L_2 for the desired $Q_L = \omega L_2/R$ or accept what exists.
- Set the frequency as desired.
- Adjust C_1 and/or C_2 as shown in Fig. 13.7B.

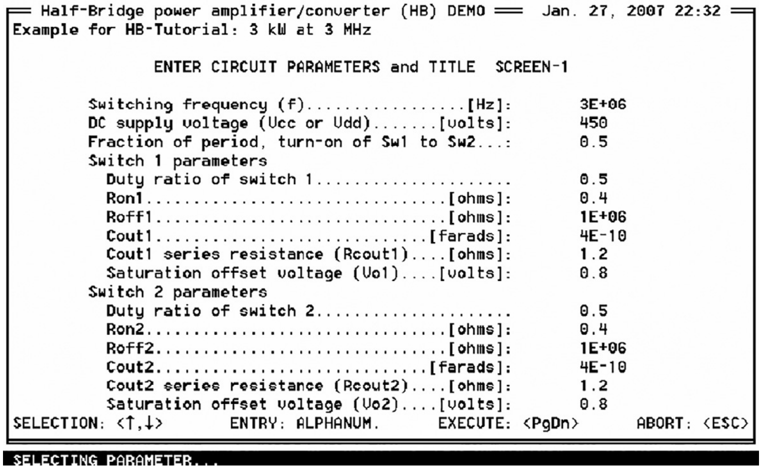
13.4 HB-PLUS CAD examples for Class-D and Class-DE

Section 13.1 introduces the basic features of the HB-PLUS program. Now, we shall demonstrate the use of HB-PLUS to simulate and analyze a 3-kW 3-MHz half-bridge (voltage-switching Class-D) tuned DC-AC power inverter, AC power amplifier, or RF power generator (different specialists use those different terms for what is basically the same thing). The circuit uses a pair of International Rectifier IRFP460 TO-247 MOSFETs, operating from a 450-V DC supply.

After that, we reduce the duty ratio of both switches to generate a Class-DE version of the circuit in the simplest possible way, using the same transistors, inductors, and capacitors as in the Class-D circuit. For this simplest possible demonstration of the advantages of Class-DE operation, we omit the full optimization that could be achieved by having the optimizer adjust the values of all important parameters, avoiding the need for a more-arcane explanation of subtle details. In this example, we demonstrate the benefit of using soft switching (i.e. having the switch turn on at nearly zero switch voltage, and therefore not discharging, through the turning-on switch, a node capacitance that is charged to the full supply voltage). To obtain soft switching, a conduction gap (dead time) is provided between the turn-off of one switch and the turn-on of the other switch shown in Fig. 13.3, and the load network can also be made slightly inductive at the switching frequency. The inductive characteristic can shift the phase of the sinusoidal current, so that the current at switch turn-off can be larger (higher up on the falling part of the sine wave). That higher current will discharge the node capacitance more quickly. During the switch conduction gap, the inductive load current charges the node capacitance from the former voltage level to the new voltage level, or to nearly that level. Consequently the turning-on transistor turns on at near-zero voltage, rather than with the node capacitance charged to the full power supply voltage, thus avoiding the power dissipation that would occur if the turning-on transistor would charge or discharge the node capacitance. This example shows the general case, illustrating both waveform features: (1) the node capacitance is charged by the inductive load current to nearly the new voltage level, and (2) the turning-on switch charges the capacitance the rest of the way. In a full optimization, that combination might result in the smallest total power dissipation at the specified output power and frequency, depending on the set of numerical values of all circuit parameters.

Class-D with hard switching. As noted previously, the example Class-D circuit is a 3-kW, 3-MHz power amplifier with a duty ratio of 50% for each of the two switches. Hence, this circuit does not yet have the conduction gap (dead time, as shown in Fig. 13.3) that provides soft switching; we shall add that later, after we compute the efficiency of the amplifier output stage and the power losses at different places in the circuit, without yet providing the soft-switching operation. The "Enter Circuit Parameters" screens of Figs. 13.8 and 13.9 show the numerical values of all of the circuit parameters. The "Efficiency and Powers" screen of Fig. 13.10 shows the drain efficiency and inefficiency, and each of the components of power dissipation. Summarizing the results for Class-D operation: 3213.4 W output at 82.733% drain efficiency, with 612.94 W power dissipation in the two transistors (19.1% of the output power). That amount of power dissipation is higher than desired and can be reduced significantly by reducing the duty ratio of the two switches to provide soft switching in the Class-DE mode of operation. A major portion of the power loss in each transistor occurs during turn-on switching; that portion will be essentially eliminated by providing soft-switching operation.

Fig. 13.11 shows graph plots of the waveforms V_{sw1} (the voltage across switch S_1) and $I_{\text{sw1(actv)}}$ (the current in the active portion of switch S_1, i.e., not including the current in the output capacitance of the switch). Note the large spike of switch current at transistor turn-on, while the node capacitance is being discharged from +450 V down to ground; that current spike is the source of much of the transistors' power dissipation, in the on-resistance (R_{on}) of the turning-on transistor and in the series resistances ($R_{C_{\text{out}}}$) of the output capacitances of both transistors.



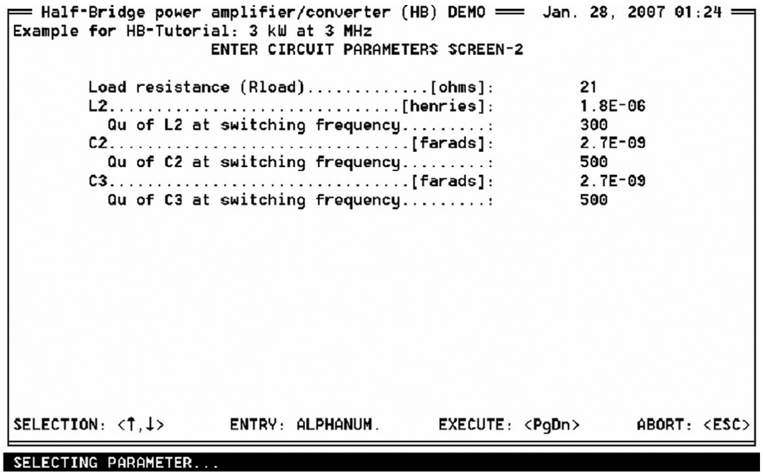
```
== Half-Bridge power amplifier/converter (HB) DEMO ==  Jan. 27, 2007 22:32 ==
Example for HB-Tutorial: 3 kW at 3 MHz

               ENTER CIRCUIT PARAMETERS and TITLE  SCREEN-1

        Switching frequency (f)................[Hz]:       3E+06
        DC supply voltage (Ucc or Udd).......[volts]:       450
        Fraction of period, turn-on of Sw1 to Sw2...:       0.5
        Switch 1 parameters
          Duty ratio of switch 1....................        0.5
          Ron1...............................[ohms]:       0.4
          Roff1..............................[ohms]:       1E+06
          Cout1............................[farads]:       4E-10
          Cout1 series resistance (Rcout1)....[ohms]:       1.2
          Saturation offset voltage (Vo1)....[volts]:       0.8
        Switch 2 parameters
          Duty ratio of switch 2....................        0.5
          Ron2...............................[ohms]:       0.4
          Roff2..............................[ohms]:       1E+06
          Cout2............................[farads]:       4E-10
          Cout2 series resistance (Rcout2)....[ohms]:       1.2
          Saturation offset voltage (Vo2)....[volts]:       0.8
SELECTION: <↑,↓>      ENTRY: ALPHANUM.     EXECUTE: <PgDn>     ABORT: <ESC>
SELECTING PARAMETER...
```

FIG. 13.8

"Enter circuit parameters—Screen 1" for Class-D.



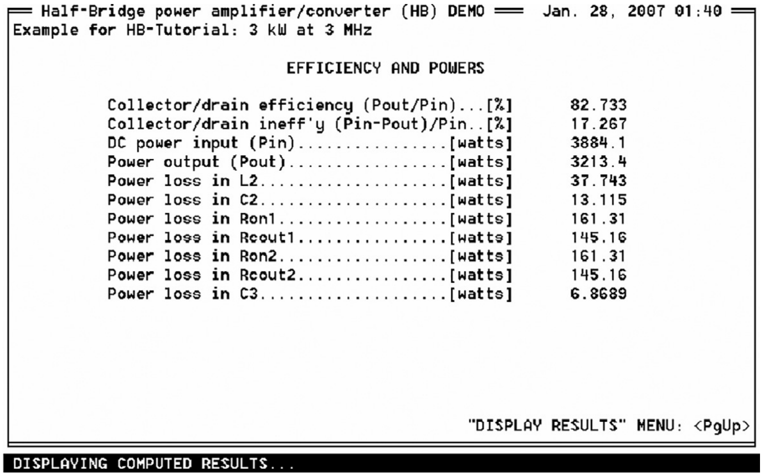
```
══ Half-Bridge power amplifier/converter (HB) DEMO ══  Jan. 28, 2007 01:24 ══
Example for HB-Tutorial: 3 kW at 3 MHz
                    ENTER CIRCUIT PARAMETERS SCREEN-2

        Load resistance (Rload)............[ohms]:        21
        L2...............................[henries]:        1.8E-06
          Qu of L2 at switching frequency.........:        300
        C2................................[farads]:        2.7E-09
          Qu of C2 at switching frequency.........:        500
        C3................................[farads]:        2.7E-09
          Qu of C3 at switching frequency.........:        500

SELECTION: <↑,↓>       ENTRY: ALPHANUM.       EXECUTE: <PgDn>      ABORT: <ESC>
SELECTING PARAMETER...
```

FIG. 13.9

"Enter circuit parameters—Screen 2" for Class-D.



```
══ Half-Bridge power amplifier/converter (HB) DEMO ══  Jan. 28, 2007 01:40 ══
Example for HB-Tutorial: 3 kW at 3 MHz

                          EFFICIENCY AND POWERS

          Collector/drain efficiency (Pout/Pin)...[%]      82.733
          Collector/drain ineff'y (Pin-Pout)/Pin..[%]      17.267
          DC power input (Pin)................[watts]      3884.1
          Power output (Pout).................[watts]      3213.4
          Power loss in L2....................[watts]      37.743
          Power loss in C2....................[watts]      13.115
          Power loss in Ron1..................[watts]      161.31
          Power loss in Rcout1................[watts]      145.16
          Power loss in Ron2..................[watts]      161.31
          Power loss in Rcout2................[watts]      145.16
          Power loss in C3....................[watts]      6.8689

                                           "DISPLAY RESULTS" MENU: <PgUp>
DISPLAYING COMPUTED RESULTS...
```

FIG. 13.10

"Efficiency and powers" screen for Class-D.

Class-DE with soft switching. To obtain soft-switching operation in a simple way, as explained in Section 13.1, we change only the duty ratio of the two transistors, from the original 50% in Class-D operation down to 40%. Repeating the simulation with only that one change, we obtain the following results: Fig. 13.12 shows the voltage and current waveforms for S_1. Note that the current spike previously existing during the Class-D turn-on switching shown in Fig. 13.11 has almost completely disappeared because the conduction gap allows the inductive load current to pull almost all of the stored

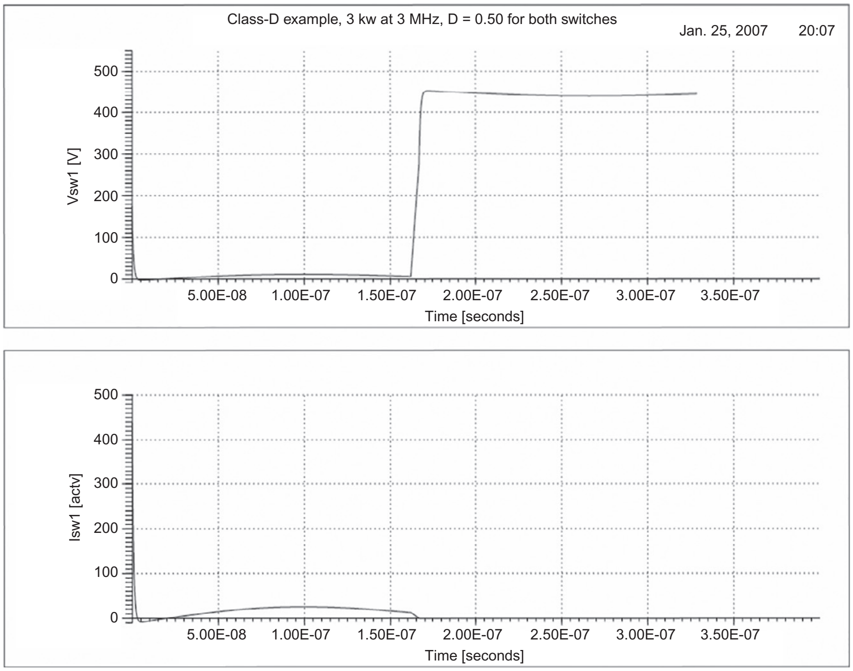


FIG. 13.11

Voltage and current waveforms for Class-D.

energy from the node capacitance before the turning-on switch is commanded to turn on (i.e., the node voltage swings most of the way toward the new voltage level before the switch turns on). When the switch turns on, it pulls the node voltage the rest of the way to the new voltage level, in approximately a step change of voltage. Fig. 13.13 shows the "Efficiency and Powers" screen for Class-DE operation that can be compared with Fig. 13.10 for the Class-D circuit. Now the drain efficiency is 93.56%, 10.8 percentage points higher than the 82.733% obtained with switch duty ratios of 0.5. The output power is 3073.9 W, 95.7% of the 3213.4 W output of the Class-D circuit. But the transistors' power dissipation has been reduced from 612.9 W in the two transistors in Class-D operation to only 156.5 W in Class-DE operation, a reduction by a factor of 3.92. This reduction of power dissipation and increase of drain efficiency are the result of the soft-switching circuit operation. (In this simple example, ~95% of the voltage swing is achieved by lossless charging of the node capacitance by the inductive load-network current; the remaining ~5% of the voltage swing is accomplished by the turning-on transistor charging the capacitance. The combination of load-network parameter values determines what fraction of the voltage swing is accomplished by lossless charging of the capacitance; under some conditions, it can be the full voltage swing.)

We can sweep the duty ratio D of both switches from 0.38 to 0.50 to see continuous functions of the efficiency and output power versus duty ratio, to verify that the chosen duty ratio is a good choice. The drop of efficiency between the almost-zero-voltage-switching operation at $D=0.4$ and the hard-switching operation at $D=0.5$ should be approximately a quadratic function of the increase of duty

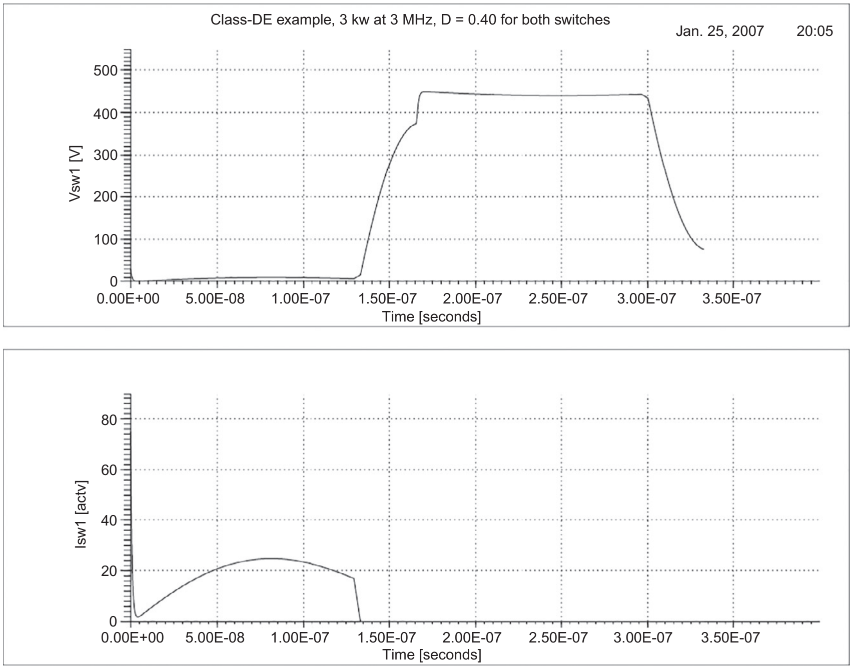
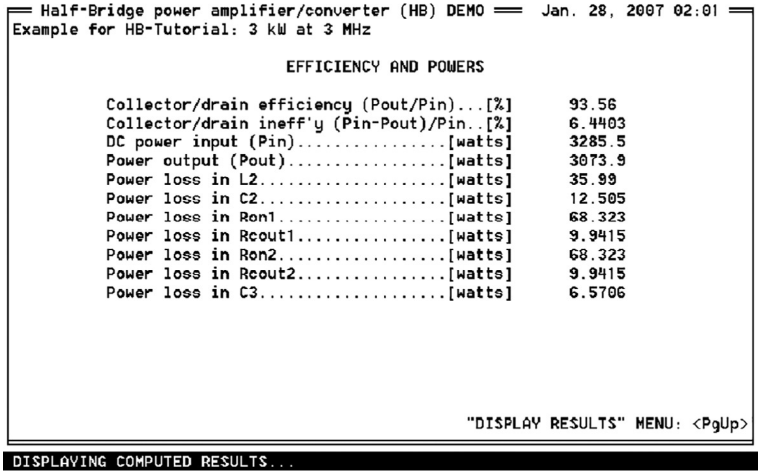


FIG. 13.12

Voltage and current waveforms for Class-DE.



```
══ Half-Bridge power amplifier/converter (HB) DEMO ══  Jan. 28, 2007 02:01 ══
Example for HB-Tutorial: 3 kW at 3 MHz

                           EFFICIENCY AND POWERS

          Collector/drain efficiency (Pout/Pin)...[%]      93.56
          Collector/drain ineff'y (Pin-Pout)/Pin..[%]      6.4403
          DC power input (Pin)................[watts]      3285.5
          Power output (Pout).................[watts]      3073.9
          Power loss in L2....................[watts]      35.99
          Power loss in C2....................[watts]      12.505
          Power loss in Ron1..................[watts]      68.323
          Power loss in Rcout1................[watts]      9.9415
          Power loss in Ron2..................[watts]      68.323
          Power loss in Rcout2................[watts]      9.9415
          Power loss in C3....................[watts]      6.5706



                                       "DISPLAY RESULTS" MENU: <PgUp>
DISPLAYING COMPUTED RESULTS...
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FIG. 13.13

“Efficiency and powers” screen for Class-DE.

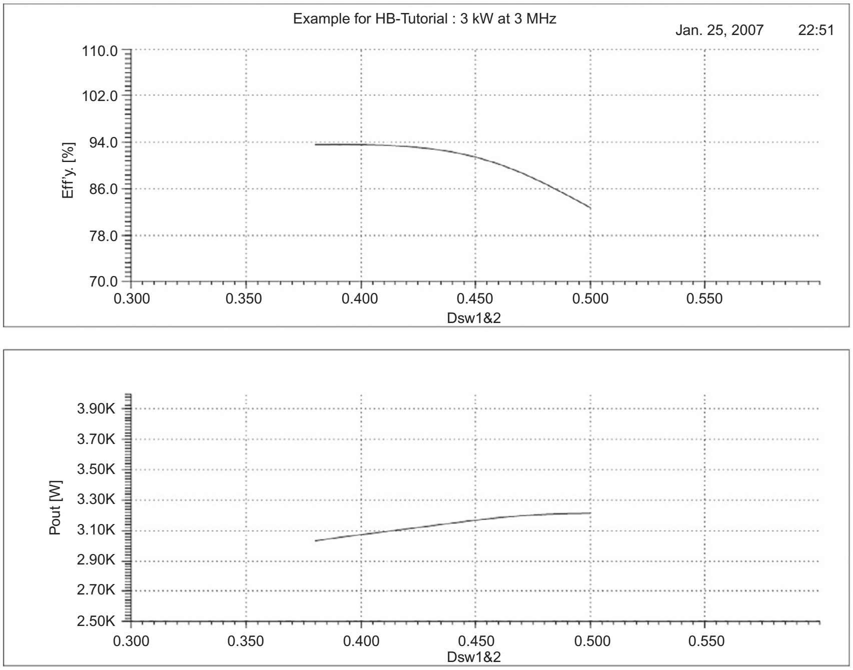


FIG. 13.14

Efficiency and output power versus duty ratio for Class-DE.

ratio beyond the value at the borderline of soft switching. This is because (1) the power dissipation when the transistors charge the node capacitance is proportional to the square of the voltage change through which the transistors charge the capacitance, and (2) the voltage change is approximately proportional to the shortage of conduction gap below the value that just provides soft switching. We can confirm this prediction by sweeping the duty ratio of both switches from 0.40 to 0.50; the result is shown in Fig. 13.14. Sweeping the duty ratio and observing the change of efficiency with duty ratio also demonstrate that the sensitivity of efficiency to changes of duty ratio is quite small in the vicinity of the chosen operating point of $D = 0.4$.

The program displays the numerical results for each point in the sweep as that point is computed. In about a second, the program completes the sweep and plots the two requested variables (efficiency and output power) versus the swept variable (duty ratio of switches S_1 and S_2). Note that the shape of the curve of efficiency versus duty ratio confirms the predictions in the preceding paragraph.

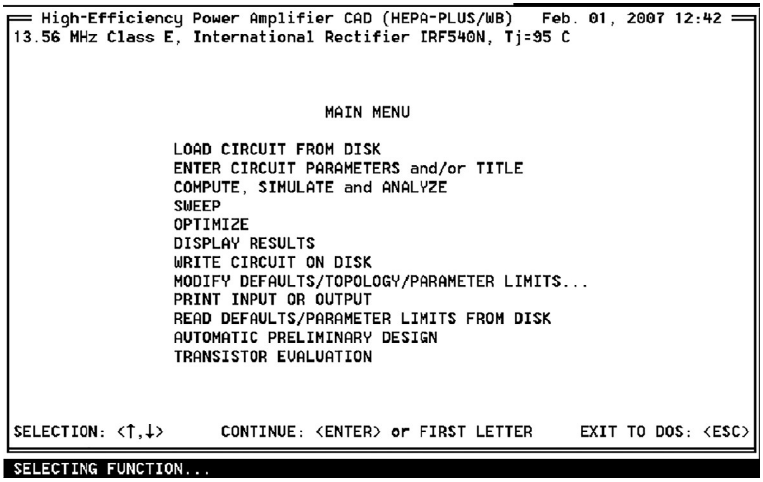
13.5 HEPA-PLUS CAD example for Class-E

Section 13.2 introduces the basic features of HEPA-PLUS program. Now, we shall demonstrate a typical design procedure using HEPA-PLUS to design a 13.56-MHz, 100-W Class-E RF power amplifier with a bandwidth of approximately 5 MHz.

Evaluate a candidate transistor. As a first step, it is necessary to evaluate a candidate transistor. In this case, the user examines the amplifier efficiency that can be achieved with one or more candidate transistors, at the desired output power of 100 W at 13.56 MHz. For this example, we use the transistor parameters for the International Rectifier IRF540N silicon MOSFET, and quality factors of 150 for inductors and 1000 for capacitors. We assume that the transistor internal temperature is 95°C, obtained as a 60°C rise above an ambient air temperature of 35°C. We use the vendor-specified maximum $R_{\mathrm{ds(on)}}$ of 0.044 Ω at 25°C, and increase that value by a factor of 1.72 to obtain the increased value at 95°C. $R_{C_{\mathrm{out}}}$ is never specified by the vendors of silicon-gate transistors; it is typically five times as large as $R_{\mathrm{ds(on)}}$[2]; we used that factor.

To begin, the user goes from the "Main Menu" shown in Fig. 13.15 to "Transistor Evaluation" shown in Fig. 13.16. The user enters the transistor parameters, the desired frequency range, the amplifier relative bandwidth (the ratio of the frequencies at the upper and lower edges of the desired operating frequency band), and the desired range of output power to be accessed. The desired output power is 100 W; the user brackets that value by specifying the power range to be evaluated as 50 to 200 W, to be able to see quantitatively the trade-off between efficiency and output power (lower output power yields higher efficiency). The user presses <Page Down> to execute the transistor evaluation. After a few seconds, a family of curves is displayed with frequency on the *X*-axis, efficiency on the *Y*-axis, and output power as a parameter, as shown in Fig. 13.17. Observe that for a 13.56-MHz Class-E circuit with an output power of 100 W, the expected efficiency of a nominal-waveforms Class-E circuit is approximately 87.5%. For the present design example, we shall assume that this efficiency is satisfactory. In an actual design, if there were other candidate transistors, the user would check the expected efficiency of each, in turn, by modifying the transistor characteristics entered on the "Transistor Evaluation" screen.

Use the Automatic Preliminary Design module to obtain a nominal-waveform Class-E design. The user goes to the "Automatic Preliminary Design" screen by pressing A at the "Main Menu."



```
High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 12:42
13.56 MHz Class E, International Rectifier IRF540N, Tj=95 C

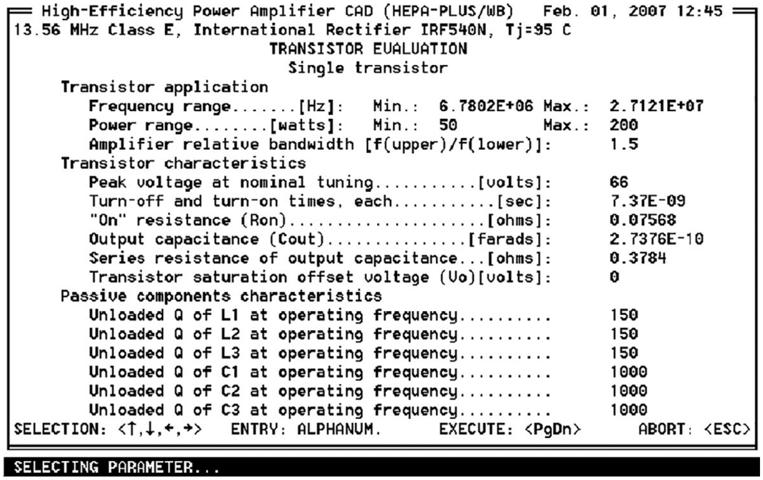

                              MAIN MENU

                 LOAD CIRCUIT FROM DISK
                 ENTER CIRCUIT PARAMETERS and/or TITLE
                 COMPUTE, SIMULATE and ANALYZE
                 SWEEP
                 OPTIMIZE
                 DISPLAY RESULTS
                 WRITE CIRCUIT ON DISK
                 MODIFY DEFAULTS/TOPOLOGY/PARAMETER LIMITS...
                 PRINT INPUT OR OUTPUT
                 READ DEFAULTS/PARAMETER LIMITS FROM DISK
                 AUTOMATIC PRELIMINARY DESIGN
                 TRANSISTOR EVALUATION


SELECTION: <↑,↓>      CONTINUE: <ENTER> or FIRST LETTER      EXIT TO DOS: <ESC>
SELECTING FUNCTION...
```

FIG. 13.15

Main menu.



```
== High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 12:45 ==
13.56 MHz Class E, International Rectifier IRF540N, Tj=95 C
                          TRANSISTOR EVALUATION
                            Single transistor
     Transistor application
        Frequency range.......[Hz]:   Min.:  6.7802E+06 Max.:  2.7121E+07
        Power range........[watts]:   Min.:  50         Max.:  200
        Amplifier relative bandwidth [f(upper)/f(lower)]:      1.5
     Transistor characteristics
        Peak voltage at nominal tuning...........[volts]:      66
        Turn-off and turn-on times, each..........[sec]:      7.37E-09
        "On" resistance (Ron)....................[ohms]:      0.07568
        Output capacitance (Cout)..............[farads]:      2.7376E-10
        Series resistance of output capacitance...[ohms]:      0.3784
        Transistor saturation offset voltage (Vo)[volts]:      0
     Passive components characteristics
        Unloaded Q of L1 at operating frequency..........      150
        Unloaded Q of L2 at operating frequency..........      150
        Unloaded Q of L3 at operating frequency..........      150
        Unloaded Q of C1 at operating frequency..........      1000
        Unloaded Q of C2 at operating frequency..........      1000
        Unloaded Q of C3 at operating frequency..........      1000
SELECTION: <↑,↓,←,→>   ENTRY: ALPHANUM.      EXECUTE: <PgDn>      ABORT: <ESC>
SELECTING PARAMETER...
```

FIG. 13.16

Transistor evaluation.

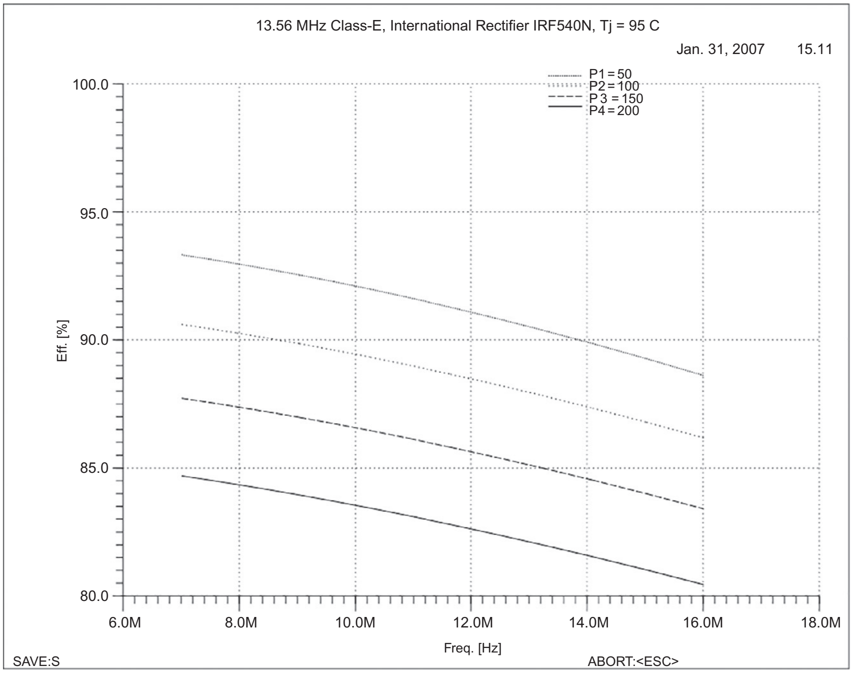


FIG. 13.17

Transistor evaluation: efficiency versus frequency and output power.

The Automatic Preliminary Design module designs a nominal-waveforms Class-E circuit (transistor voltage and voltage slope both zero at transistor turn-on time[8]), and calculates the expected amplifier efficiency, using parameters:

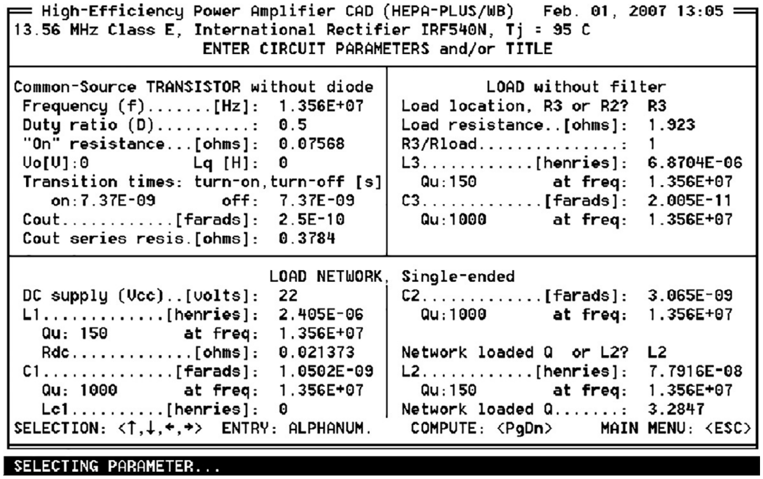
- Desired frequency band
- Two of the following: output power, DC supply voltage, and AC load resistance
- Transistor parameters (saved from "Transistor Evaluation")
- Quality factors of inductors and capacitors (saved from "Transistor Evaluation").

To begin, the user specifies a 1.5:1 frequency band with a geometric mean of approximately 13.56 MHz: 11.296–16.296 MHz (a bandwidth of 5 MHz centered at 13.56 MHz). The user specifies a desired output power of 100 W and a DC drain-supply voltage V_{dd} of 22 V to have the nominal $V_{ds(pk)}$ (estimated as $\sim 3.4V_{dd}$ after optimization) be approximately 75% of the maximum rated V_{dd} of 100 V, to provide a 30% safety factor to allow for off-nominal loads and component tolerances. The user enters "Transistor turn-off and turn-on times" as (in this example) 10% of the RF period, hence 7.37 ns (5%–10% of the RF period is usually quite satisfactory). The user presses <Page Down> to execute the Automatic Preliminary Design. Almost immediately, the program displays (without making a simulation) a predicted drain efficiency, for this nominal-waveforms design of 87.8%, and displays the load resistance to be provided at the R_3 location as 1.923 Ω. The impedance-transformation (matching) network (not yet designed) will transform the external load resistance (e.g., 50 Ω) to this computed value. The results so far are deemed to be acceptable, so there is no need to evaluate other candidate transistors. The user transfers the computed circuit design to the "Enter Circuit Parameters" screen by pressing <Page Up>, after which the user will simulate the circuit to verify its correctness. If it is deemed correct, it will be the starting point for an optimization. The result is shown in the screen "Enter Circuit Parameters and/or Title," as shown in Fig. 13.18.

Simulate the nominal-waveforms circuit. Pressing <Page Down> at the "Enter Circuit Parameters" screen simulates the circuit in approximately 8 ms on a Pentium III/667 MHz, and faster on faster computers. The result is shown in the screen "Efficiency, Powers, and Stresses," as shown in Fig. 13.19. The drain efficiency ($P_{out}/P_{in,DC}$) is 87.686% and the output power is 96.848 W. The peak transistor voltage and current are 75.346 V and 13.827 A, well within the transistor's maximum ratings of 100 V and 110 A. The Automatic Preliminary Design module, using explicit design equations and no simulation, was designed for 100 W output and achieved within 3.2% of that target value, and had predicted 87.8% efficiency, within 0.11 percentage points of the results of the accurate simulation.

Fig. 13.20 shows the transistor voltage and current waveforms of this nominal-waveforms Class-E power amplifier. They are seen to be the same as the theoretical waveforms in Figs. 5.5 and 6.8 except that the simulation includes the nonzero switching times, not included in those theoretical waveforms. Note that high voltage and high current do not exist simultaneously, even if the transistor turn-on and turn-off transition times are appreciable fractions of the RF cycle. That is the fundamental characteristic of a high-efficiency power amplifier. In this 13.56-MHz design, the transistor turns on at the left edge of the plot at $t = 0$ and begins to turn off near the middle of the plot at $t = 33.2$ ns.

RF output spectrum. A spectrum of the RF output power delivered to R_3 is available at the screen "Display Spectrum of Plot Variable $VR_3/L_3/C_3$," shown for the optimized circuit in Fig. 13.21. [Other voltages and currents can be chosen also, as the variable to be displayed. For example, the harmonic content of I_{L_1}, the DC current drawn from the DC power supply, gives an indication of how much bypass-capacitance filtering is needed on the V_{dd} line to maintain the conducted electromagnetic



```
== High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 13:05 ==
13.56 MHz Class E, International Rectifier IRF540N, Tj = 95 C
                      ENTER CIRCUIT PARAMETERS and/or TITLE

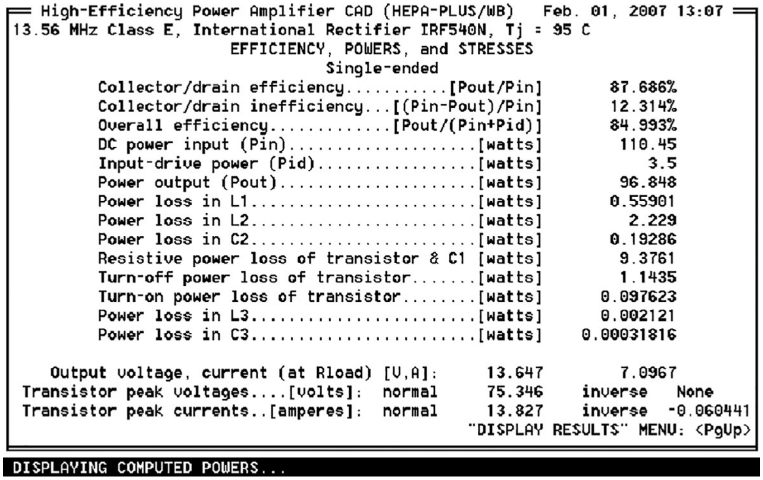
Common-Source TRANSISTOR without diode |        LOAD without filter
 Frequency (f).......[Hz]:  1.356E+07  | Load location, R3 or R2?  R3
 Duty ratio (D)..........:  0.5        | Load resistance..[ohms]:  1.923
 "On" resistance...[ohms]:  0.07568    | R3/Rload...............:  1
 Vo[V]:0           Lq [H]:  0          | L3...........[henries]:  6.8704E-06
 Transition times: turn-on,turn-off [s]|   Qu:150         at freq:  1.356E+07
    on:7.37E-09       off:  7.37E-09   | C3............[farads]:  2.005E-11
 Cout...........[farads]:  2.5E-10     |   Qu:1000        at freq:  1.356E+07
 Cout series resis.[ohms]:  0.3784     |

                         LOAD NETWORK, Single-ended
 DC supply (Vcc)..[volts]:  22         | C2............[farads]:  3.065E-09
 L1............[henries]:  2.405E-06   |   Qu:1000        at freq:  1.356E+07
   Qu: 150        at freq:  1.356E+07  |
   Rdc............[ohms]:  0.021373    | Network loaded Q  or L2?  L2
 C1.............[farads]:  1.0502E-09  | L2...........[henries]:  7.7916E-08
   Qu: 1000       at freq:  1.356E+07  |   Qu:150         at freq:  1.356E+07
   Lc1.........[henries]:  0           | Network loaded Q.......:  3.2847
SELECTION: <↑,↓,←,→>  ENTRY: ALPHANUM.   COMPUTE: <PgDn>     MAIN MENU: <ESC>

SELECTING PARAMETER...
```

FIG. 13.18

Enter circuit parameters and/or title.



```
== High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 13:07 ==
13.56 MHz Class E, International Rectifier IRF540N, Tj = 95 C
                      EFFICIENCY, POWERS, and STRESSES
                                Single-ended
        Collector/drain efficiency..........[Pout/Pin]       87.686%
        Collector/drain inefficiency...[(Pin-Pout)/Pin]       12.314%
        Overall efficiency............[Pout/(Pin+Pid)]       84.993%
        DC power input (Pin)...................[watts]        110.45
        Input-drive power (Pid)................[watts]           3.5
        Power output (Pout)....................[watts]        96.848
        Power loss in L1.......................[watts]       0.55901
        Power loss in L2.......................[watts]         2.229
        Power loss in C2.......................[watts]       0.19286
        Resistive power loss of transistor & C1 [watts]       9.3761
        Turn-off power loss of transistor......[watts]        1.1435
        Turn-on power loss of transistor.......[watts]      0.097623
        Power loss in L3.......................[watts]      0.002121
        Power loss in C3.......................[watts]    0.00031816

    Output voltage, current (at Rload) [V,A]:     13.647         7.0967
 Transistor peak voltages....[volts]:  normal     75.346    inverse   None
 Transistor peak currents..[amperes]:  normal     13.827    inverse  -0.060441
                                                 "DISPLAY RESULTS" MENU: <PgUp>

DISPLAYING COMPUTED POWERS...
```

FIG. 13.19

Efficiency, powers, and stresses.

interference (EMI) current below a desired maximum allowed value.] The first spectrum screen shown in Fig. 13.21 lists the dBc values from DC (actually zero output, listed as −74.06 dBc, an approximation to –∞ dBc) through the 17th harmonic. A similar second screen (not shown here) lists the values for the 18th through 31st harmonics. At each harmonic, the difference between the listed value and the maximum allowed harmonic output is the number of dB of suppression needed in the post-amplifier harmonic-suppression filter. For example, if all harmonics must be below −65 dBc, the 7th and higher

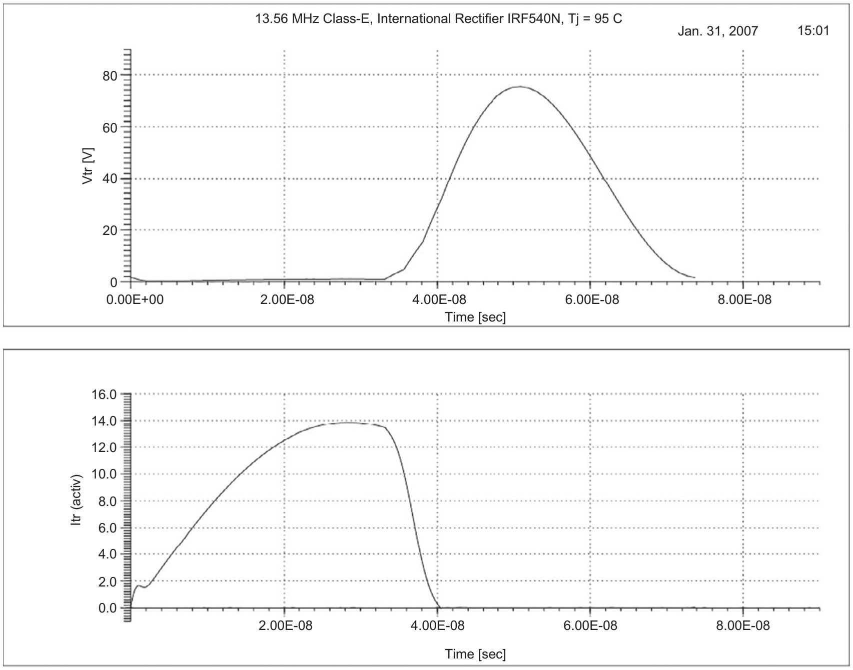
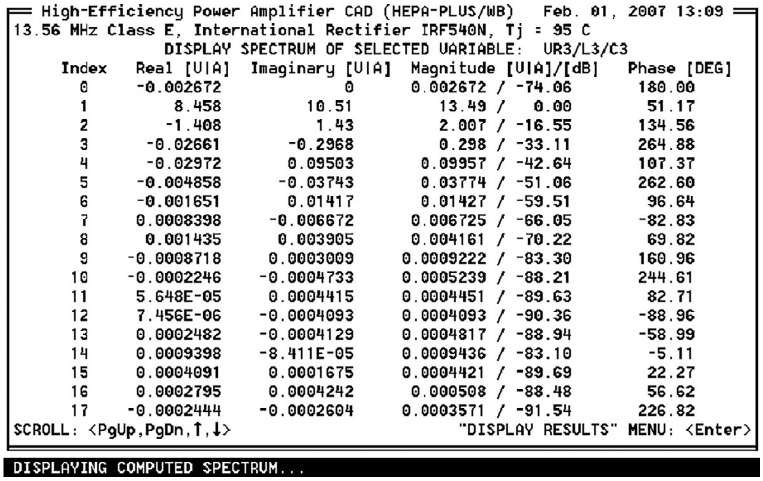


FIG. 13.20

Transistor voltage and current waveforms of nominal-waveforms Class-E power amplifier.



```
══ High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 13:09 ══
13.56 MHz Class E, International Rectifier IRF540N, Tj = 95 C
                    DISPLAY SPECTRUM OF SELECTED VARIABLE:  UR3/L3/C3
      Index    Real [U|A]  Imaginary [U|A]  Magnitude [U|A]/[dB]    Phase [DEG]
        0      -0.002672              0      0.002672 / -74.06       180.00
        1          8.458          10.51         13.49 /   0.00        51.17
        2         -1.408           1.43         2.007 / -16.55       134.56
        3       -0.02661        -0.2968         0.298 / -33.11       264.88
        4       -0.02972        0.09503       0.09957 / -42.64       107.37
        5      -0.004858       -0.03743       0.03774 / -51.06       262.60
        6      -0.001651        0.01417       0.01427 / -59.51        96.64
        7      0.0008398      -0.006672      0.006725 / -66.05       -82.83
        8       0.001435       0.003905      0.004161 / -70.22        69.82
        9     -0.0008718      0.0003009     0.0009222 / -83.30       160.96
       10     -0.0002246     -0.0004733     0.0005239 / -88.21       244.61
       11      5.648E-05      0.0004415     0.0004451 / -89.63        82.71
       12      7.456E-06     -0.0004093     0.0004093 / -90.36       -88.96
       13      0.0002482     -0.0004129     0.0004817 / -88.94       -58.99
       14      0.0009398     -8.411E-05     0.0009436 / -83.10        -5.11
       15      0.0004091      0.0001675     0.0004421 / -89.69        22.27
       16      0.0002795      0.0004242      0.000508 / -88.48        56.62
       17     -0.0002444     -0.0002604     0.0003571 / -91.54       226.82
SCROLL: <PgUp,PgDn,↑,↓>                         "DISPLAY RESULTS" MENU: <Enter>
 DISPLAYING COMPUTED SPECTRUM...
```

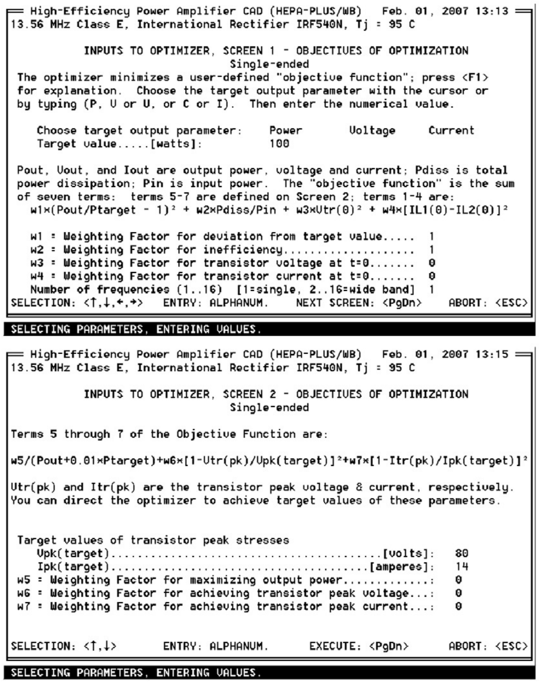
FIG. 13.21

Display spectrum of plot variable $VR_3/L_3/C_3$.

harmonics need no suppression, $2f$ (-16.55 dBc) needs $65-16.55=48.45$ dB of suppression, $3f$ (-33.11 dBc) needs $65-33.11=31.89$ dB of suppression.

Optimize the design, using the nominal-waveforms design as a starting-point. The Optimizer module is entered by pressing O at the Main Menu or by highlighting that line and pressing the <Enter> key. That takes the user to the screen "Inputs to Optimizer, Screen 1—Objectives of Optimization," shown as the upper screen in Fig. 13.22. That upper screen shows the first four of the seven performance characteristics that can be used to define the meaning of "optimum" for this application; the next three characteristics are on the continuation Screen 2, shown below Screen 1 in Fig. 13.22. For this example, we shall give the weighting factors w_1 (deviation from the target value of output power) and w_2 (inefficiency) equal weights of 1 and leave the remaining five weighting factors at their default values of zero. Note that all mathematicians except the Russians optimize by *minimizing* the "badness" of the design (here, w_1 is for the *deviation* from the target value of output power and w_2 is for the *in*efficiency); the Russians optimize by *maximizing* the "goodness" of the design. Both methods work well and are basically equivalent.

The optimization can be done at one frequency or at up to 16 frequencies simultaneously, useful for wideband designs. For simplicity, we shall illustrate the optimization at one frequency of 13.56 MHz. The user proceeds to the screen "Inputs to Optimizer, Screen 3—Circuit Parameters to be Varied by the Optimizer," shown in Fig. 13.23. Here the user can choose which parameters the Optimizer can vary,



```
High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 13:13
13.56 MHz Class E, International Rectifier IRF540N, Tj = 95 C

          INPUTS TO OPTIMIZER, SCREEN 1 - OBJECTIVES OF OPTIMIZATION
                              Single-ended
 The optimizer minimizes a user-defined "objective function"; press <F1>
 for explanation.  Choose the target output parameter with the cursor or
 by typing (P, V or U, or C or I).  Then enter the numerical value.

    Choose target output parameter:    Power      Voltage     Current
    Target value.....[watts]:          100

 Pout, Vout, and Iout are output power, voltage and current; Pdiss is total
 power dissipation; Pin is input power.  The "objective function" is the sum
 of seven terms:  terms 5-7 are defined on Screen 2; terms 1-4 are:
   w1×(Pout/Ptarget - 1)² + w2×Pdiss/Pin + w3×Vtr(0)² + w4×[IL1(0)-IL2(0)]²

   w1 = Weighting Factor for deviation from target value.....  1
   w2 = Weighting Factor for inefficiency....................  1
   w3 = Weighting Factor for transistor voltage at t=0.......  0
   w4 = Weighting Factor for transistor current at t=0.......  0
   Number of frequencies (1..16)  [1=single, 2..16=wide band]  1
SELECTION: <↑,↓,←,→>   ENTRY: ALPHANUM.    NEXT SCREEN: <PgDn>    ABORT: <ESC>
SELECTING PARAMETERS, ENTERING VALUES.
```

```
High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 13:15
13.56 MHz Class E, International Rectifier IRF540N, Tj = 95 C

          INPUTS TO OPTIMIZER, SCREEN 2 - OBJECTIVES OF OPTIMIZATION
                              Single-ended

Terms 5 through 7 of the Objective Function are:

w5/(Pout+0.01×Ptarget)+w6×[1-Vtr(pk)/Vpk(target)]²+w7×[1-Itr(pk)/Ipk(target)]²

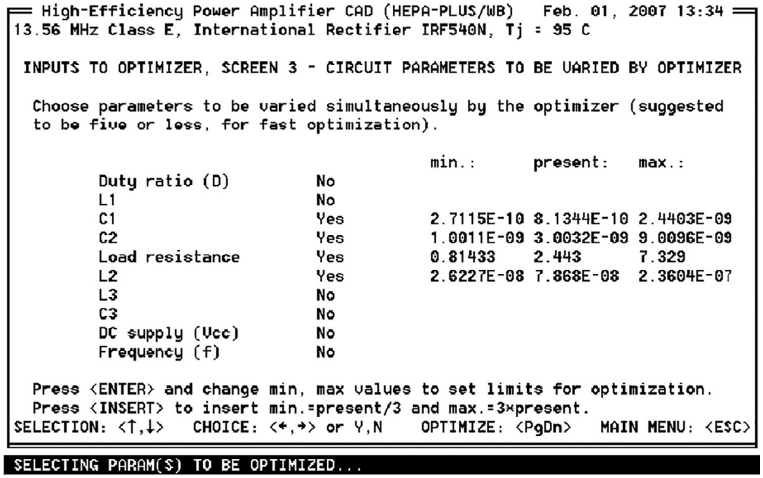
Vtr(pk) and Itr(pk) are the transistor peak voltage & current, respectively.
You can direct the optimizer to achieve target values of these parameters.


 Target values of transistor peak stresses
    Vpk(target).......................................[volts]:   80
    Ipk(target).....................................[amperes]:   14
 w5 = Weighting Factor for maximizing output power............:   0
 w6 = Weighting Factor for achieving transistor peak voltage...:   0
 w7 = Weighting Factor for achieving transistor peak current...:   0


SELECTION: <↑,↓>       ENTRY: ALPHANUM.      EXECUTE: <PgDn>      ABORT: <ESC>
SELECTING PARAMETERS, ENTERING VALUES.
```

FIG. 13.22

Inputs to optimizer—objectives of optimization.



```
High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 13:34
13.56 MHz Class E, International Rectifier IRF540N, Tj = 95 C

 INPUTS TO OPTIMIZER, SCREEN 3 - CIRCUIT PARAMETERS TO BE VARIED BY OPTIMIZER

  Choose parameters to be varied simultaneously by the optimizer (suggested
  to be five or less, for fast optimization).

                                           min.:      present:   max.:
         Duty ratio (D)         No
         L1                     No
         C1                     Yes        2.7115E-10 8.1344E-10 2.4403E-09
         C2                     Yes        1.0011E-09 3.0032E-09 9.0096E-09
         Load resistance        Yes        0.81433    2.443      7.329
         L2                     Yes        2.6227E-08 7.868E-08  2.3604E-07
         L3                     No
         C3                     No
         DC supply (Vcc)        No
         Frequency (f)          No

  Press <ENTER> and change min, max values to set limits for optimization.
  Press <INSERT> to insert min.=present/3 and max.=3×present.
SELECTION: <↑,↓>   CHOICE: <←,→> or Y,N    OPTIMIZE: <PgDn>   MAIN MENU: <ESC>

SELECTING PARAM(S) TO BE OPTIMIZED...
```

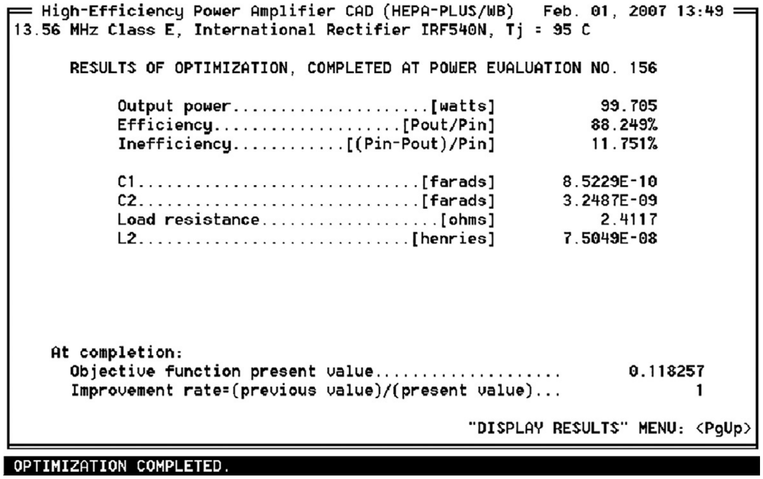
FIG. 13.23

Inputs to optimizer, Screen 3—circuit parameters to be varied by the optimizer.

and the minimum and maximum allowed values of those parameters, as constraints on the Optimizer. We shall choose C_1, C_2, L_2, and Load Resistance as the parameters to be varied in the search for the optimum combination. Parameters not chosen to be varied:

1. The Duty ratio is set to 50%, already known to be a reasonable compromise among conflicting trade-off factors.
2. L_1 is effectively “infinite”; higher inductance will have essentially no effect, and lower inductance is not needed.
3. L_3 and C_3 are tuned to the operating frequency but are given high enough reactance values that they are essentially removed from the circuit. They are available if a tuned load is desired but that is not needed in this case. For harmonic suppression a better way to use an inductor and a capacitor (such as L_3 and C_3) would be to place them in a low-pass LC filter (−6 dB per octave above the operating frequency), rather than as a parallel resonator at the load (−3 dB per octave above the operating frequency).
4. The DC supply voltage was already chosen as 22 V to provide enough margin against excessive peak transistor voltage.
5. The operating frequency was already chosen as 13.56 MHz, according to the requirements placed on the design.

The user presses the < Page Down > key to begin the optimization. In a few seconds, the result is shown at the screen “Results of Optimization, Completed at Power Evaluation No. nnn,” where *nnn* is the number of evaluations made on the way to finding the optimum (156 in this example). Fig. 13.24 shows that screen for the case computed here. The initial value of efficiency of the starting circuit (87.686% for the nominal-waveforms design shown in Fig. 13.19, already quite high) was improved by 0.563 percentage points to the listed value of 88.249% shown in Fig. 13.24. The optimizer usually reduces the power dissipation by approximately 30% of its value for the starting circuit, usually increasing the



```
High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 13:49
13.56 MHz Class E, International Rectifier IRF540N, Tj = 95 C

     RESULTS OF OPTIMIZATION, COMPLETED AT POWER EVALUATION NO. 156

         Output power....................[watts]          99.705
         Efficiency..................[Pout/Pin]          88.249%
         Inefficiency...........[(Pin-Pout)/Pin]          11.751%

         C1............................[farads]       8.5229E-10
         C2............................[farads]       3.2487E-09
         Load resistance.................[ohms]           2.4117
         L2...........................[henries]       7.5049E-08




   At completion:
     Objective function present value....................       0.118257
     Improvement rate=(previous value)/(present value)...              1

                                          "DISPLAY RESULTS" MENU: <PgUp>
OPTIMIZATION COMPLETED.
```

FIG. 13.24

Results of optimization, completed at power evaluation no. 156.

drain efficiency by approximately 5 percentage points. But if the starting circuit already has high efficiency, the increase of efficiency from optimizing can be small. To illustrate the larger improvement that can be obtained when the nominal-waveforms circuit does not *already* have high efficiency, the authors increased the required output power from 100 W to 300 W, and reduced the Q values of L and C from 150 and 1000 to 50 and 200, respectively; both changes increase the resistive power losses. As a result, for nominal-waveforms circuit: 300 W at 75.207% efficiency, with waveforms similar to Fig. 13.20; for optimized circuit: 302 W at 80.585% efficiency, efficiency increased by 5.378 percentage points, with waveforms similar to Fig. 13.25.

The transistor voltage and current waveforms in the first optimized circuit are shown in Fig. 13.25; they are off-nominal as compared with the nonideal nominal waveforms shown in Fig. 13.20 or the idealized nominal waveforms shown in Figs. 5.6 and 6.8. The user can read out X and Y numerical values from the plot by pressing the left/right cursor keys to move a vertical read-out cursor to the point of interest. The numerical values are displayed at the upper-left and lower-left corners of the plots. The read-out cursor is positioned at the peak of the transistor-voltage waveform; the peak voltage is seen to be 74.79 V, the same as the value that would be listed at the bottom of the screen “Efficiency, Powers, and Stresses” for the optimized circuit.

Use the SWEEP function. The program can sweep any of 25 circuit parameters and display graph-plots of one or two of 18 available output variables. At the Main Menu, the user presses S for Sweep. The program presents the screen “Sweep Menu” shown in Fig. 13.26. For this demonstration, we shall sweep Frequency, chosen from a menu of 20 available parameters. The user enters values to compute the results at 13 points from 11 to 17 MHz in an algebraic sweep (equal steps of the swept variable between adjacent points). Also available is Geometric sweep, that has a given multiplication factor on the swept variable between adjacent points. The program determines the step value, given the user-specified range, number of points, and type of sweep.

The user chooses to plot the default output variables: Output Power and Efficiency. The user presses <Page Down> to execute the sweep. During the sweep calculations, the latest values of the swept

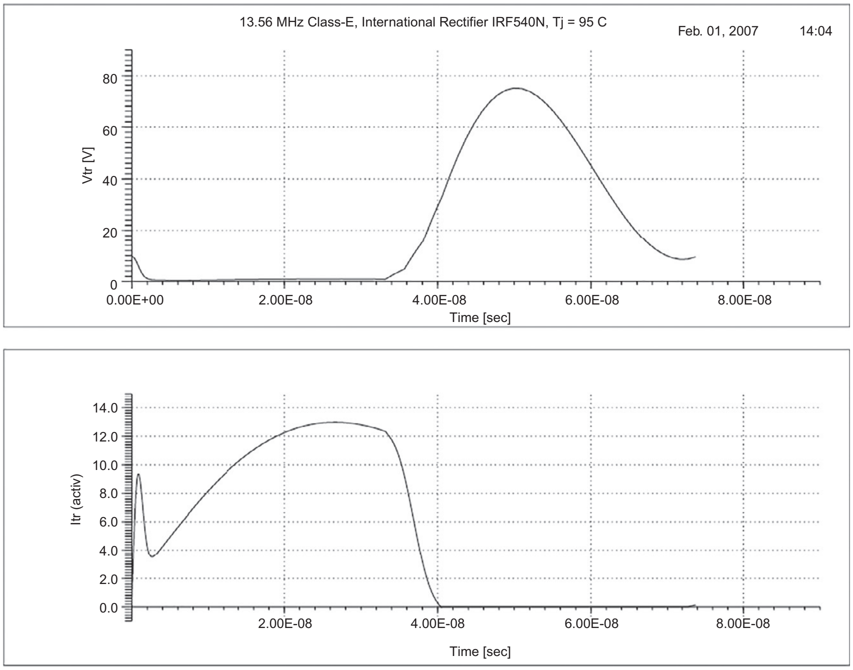
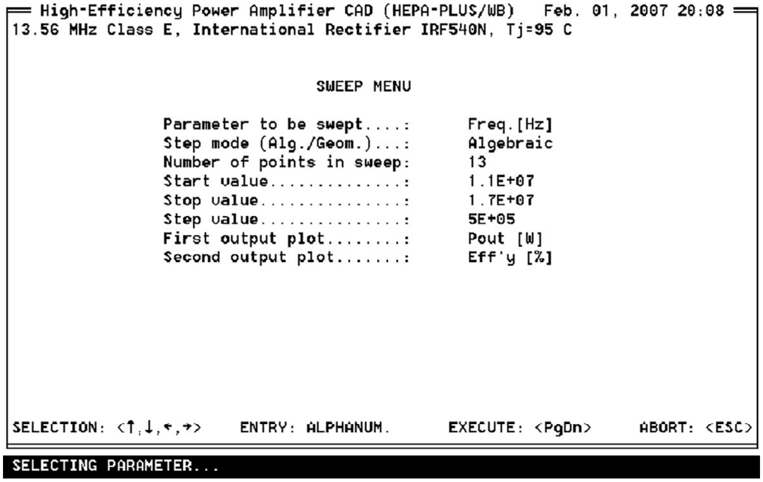


FIG. 13.25

Transistor optimized off-nominal voltage and current waveforms in optimized circuit.



```
═ High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 20:08 ═
13.56 MHz Class E, International Rectifier IRF540N, Tj=95 C


                              SWEEP MENU

                Parameter to be swept....:      Freq.[Hz]
                Step mode (Alg./Geom.)...:      Algebraic
                Number of points in sweep:      13
                Start value..............:      1.1E+07
                Stop value...............:      1.7E+07
                Step value...............:      5E+05
                First output plot........:      Pout [W]
                Second output plot.......:      Eff'y [%]


SELECTION: <↑,↓,←,→>    ENTRY: ALPHANUM.     EXECUTE: <PgDn>     ABORT: <ESC>
SELECTING PARAMETER...
```

FIG. 13.26

Sweep menu.

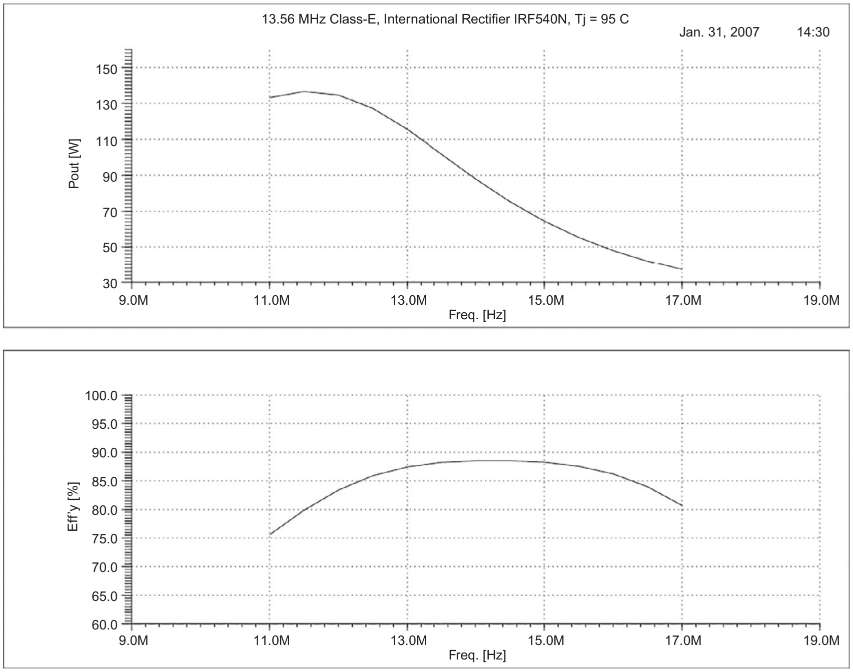


FIG. 13.27

Output power and efficiency versus swept frequency.

parameter and the variables to be plotted are displayed in a table at the right side of the screen; the user can watch that table change during the sweep. At the completion of the computation, the program displays graphs of Output Power and Efficiency versus frequency, as shown in Fig. 13.27.

Two more interesting waveforms to display are the currents in the power transistor. We can examine both $I_{tr(activ)}$ (the current in *the active part* of the transistor) and $I_{tr(total)}$ (*the terminal current*, which is the sum of the currents in the active part and in the transistor's output capacitance), and we can compare the two current waveforms. If we wish, we can also display separately the current in the transistor's output capacitance. To begin, return to the screen "Variable(s) to be plotted" by pressing <Enter>, <Page Up>, and P. Then press <6> to open a window showing a list of variables that can be plotted. Move the cursor to $I_{tr(activ)}$ and press <Enter>. Then press <6> to place the cursor on $I_{tr(total)}$ and press <Enter>. Press <Page Down> to display the two waveforms, as shown in Fig. 13.28.

In the laboratory, using an oscilloscope, you can observe only $I_{tr(total)}$, and that only up to approximately 50 MHz. Unfortunately, this does not give you a clear picture of the details of circuit operation. With the program, however, you can observe clearly the circuit operation with $I_{tr(activ)}$, and you can also see $I_{tr(total)}$ at the same time. By means of the latter, you can compare experimental observations with the computer simulation, or you can *predict* what you can *expect* to see in a laboratory test.

Similarly, you can observe two versions of the transistor voltage waveform when the transistor internal wiring inductance (L_Q in Fig. 13.4) is nonzero: the transistor *internal* voltage at the transistor die, termed $V_{tr(inter)}$, and the transistor *terminal* voltage $V_{tr(term)}$, which includes also the voltage across

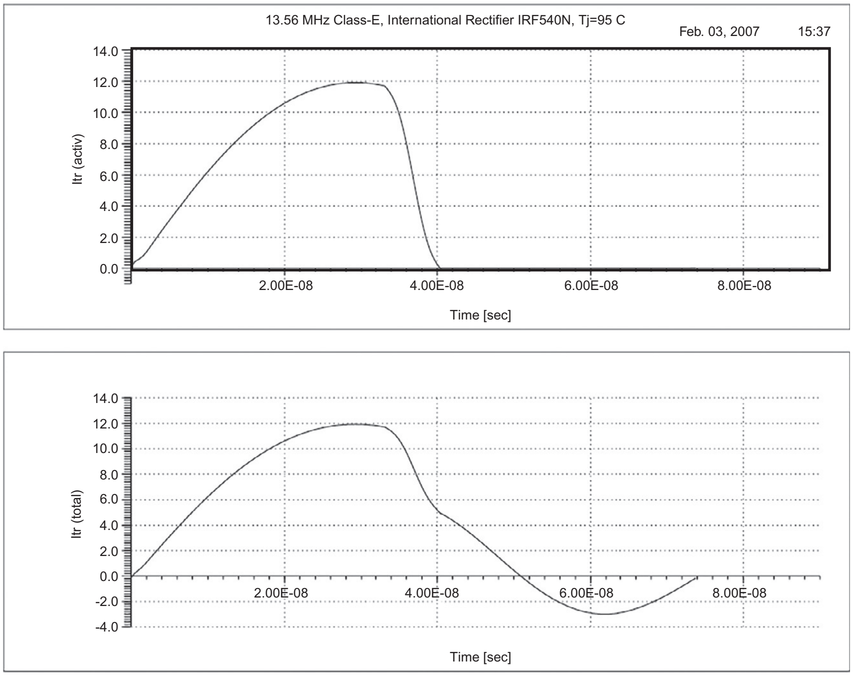


FIG. 13.28

Waveforms of current in active part of transistor and total transistor current.

L_Q. Experimentally, you can observe only $V_{tr(term)}$, but $V_{tr(inter)}$ which you cannot observe experimentally gives you much more information about the circuit operation. You can easily observe both voltages with the program; if you have set L_Q to a nonzero value at the screen "Enter Circuit Parameters." If L_Q is zero, the internal and external voltages are identical, so the transistor voltage is called simply V_{tr}.

13.6 Class-E power amplifier with flat-top voltage waveform

In the classical Class-E power amplifier with shunt capacitance and series filter, the theoretical switch peak voltage ratio V_{sw_pk}/V_{dd} is equal to 3.562 which is a limitation in many applications, especially when the device breakdown voltage is not high enough. In this case, the output resonant circuit can be modified, as shown in Fig. 13.29, by adding a resonant parallel L_3C_3 circuit in series with the load.[9] The second harmonic can provide a flat-top shape of the switch voltage waveform. The L_3C_3 parallel resonator is tuned to the second harmonic of the switching frequency ($2f_0$) and placed in series with L_2C_2, thus resulting in some reduction of the $2f_0$ power delivered to the load ($2f_0$ is the harmonic with the largest amplitude in the ordinary Class-E circuit). That reduction of $2f_0$ output power is useful for communications applications that need low-harmonic content in the output power.

The design of the amplifier was done with HEPA-PLUS software, and the normalized values of radian frequency $\omega_0 = 1$ rad/second ($f_0 = \omega_0/2\pi = 0.159154943$), a load $R_{load} = 0.9\,\Omega$, and a supply

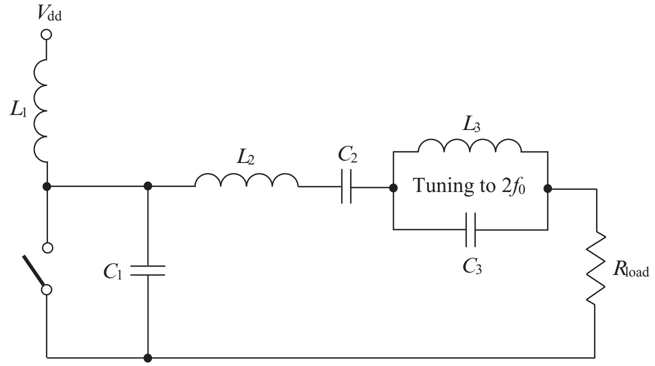
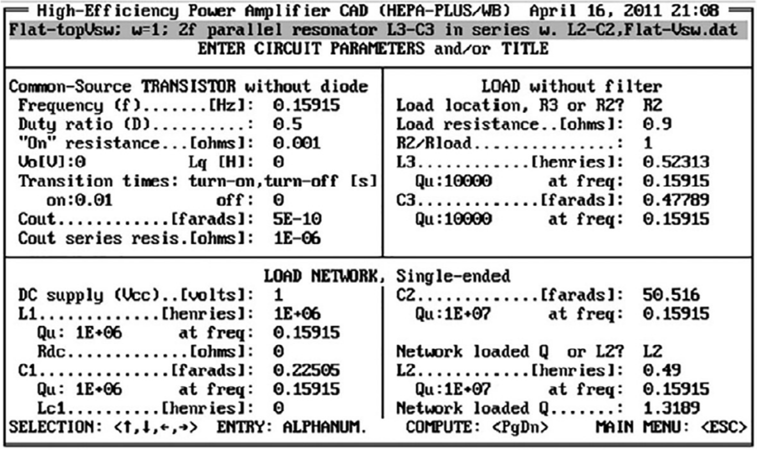


FIG. 13.29

Flat-top Class-E topology.



```
== High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)  April 16, 2011 21:08 ==
Flat-topVsw; w=1; 2f parallel resonator L3-C3 in series w. L2-C2,Flat-Vsw.dat
                      ENTER CIRCUIT PARAMETERS and/or TITLE

Common-Source TRANSISTOR without diode         LOAD without filter
 Frequency (f).......[Hz]:  0.15915    Load location, R3 or R2?  R2
 Duty ratio (D)..........:  0.5        Load resistance..[ohms]:  0.9
 "On" resistance...[ohms]:  0.001      R2/Rload...............:  1
 Vo[V]:0           Lq [H]:  0          L3...........[henries]:  0.52313
 Transition times: turn-on,turn-off [s]  Qu:10000       at freq:  0.15915
    on:0.01           off:  0          C3............[farads]:  0.47789
 Cout...........[farads]:  5E-10         Qu:10000       at freq:  0.15915
 Cout series resis.[ohms]:  1E-06

                         LOAD NETWORK, Single-ended
 DC supply (Vcc)..[volts]:  1        | C2............[farads]:  50.516
 L1............[henries]:  1E+06     |   Qu:1E+07       at freq:  0.15915
   Qu: 1E+06      at freq:  0.15915  |
   Rdc............[ohms]:  0         | Network loaded Q  or L2?  L2
 C1.............[farads]:  0.22505   | L2...........[henries]:  0.49
   Qu: 1E+06      at freq:  0.15915  |   Qu:1E+07       at freq:  0.15915
   Lc1.........[henries]:  0         | Network loaded Q.......:  1.3189
SELECTION: <↑,↓,←,→>  ENTRY: ALPHANUM.   COMPUTE: <PgDn>     MAIN MENU: <ESC>
```

FIG. 13.30

Normalized Class-E flat-top HEPA screen.

voltage $V_{dd} = 1$ V together with the normalized values of the output resonant circuit elements were used, as shown in HEPA-PLUS screen of Fig. 13.30.

The corresponding normalized values of the output resonant circuit elements (included in HEPA-PLUS screen) required for the design a flat-top version of the Class-E power amplifier are as follows:

$L_1 = 1 \times 10^6$ H	$C_1 = 0.225$ F
$L_2 = 0.49$ H	$C_2 = 50.516$ F
$L_3 = 0.523$ H	$C_3 = 0.478$ F.

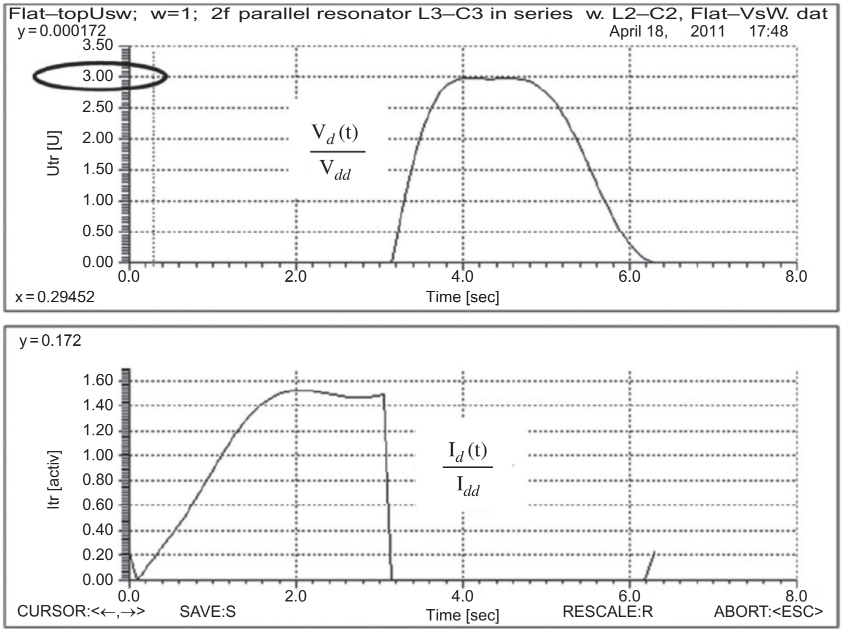


FIG. 13.31

Normalized Class-E flat-top HEPA waveforms.

where the inductances are given in Henries (H) and the capacitances are given in Farads (F).

Fig. 13.31 shows the simulated normalized switch current and voltage for the proposed topology, clearly showing the obtained flat-top voltage waveform.[9] In this case, the peak value of a flat-top voltage is 81% of the peak value of classical Class-E power amplifier when $V_{\text{sw\_pk}}/V_{\text{dd}}$ is equal to

2.976	for flat-top Class-E load network
3.562	for classical Class-E load network

To verify the simulation results, a flat-top Class-E power amplifier was designed and built at an operating frequency of 1 MHz (50% duty ratio) to minimize parasitic effects and high output power was not considered to avoid the need for a low nominal load resistance. As a result, two 50-Ω load resistors in parallel were used to represent the load with $R_{\text{load}} = 25\,\Omega$. The amplifier was designed based on an IRF520N transistor with on-resistance $R_{\text{ds(on)}} = 0.2\,\Omega$ and output capacitance $C_{\text{oss}} = 92\,\text{pF}$ at 25 V. For a DC-supply voltage of 12.2 V, the measurement results show a peak drain voltage of 36.9 V (or $V_{\text{sw\_pk}}/V_{\text{dd}} = 3.024$) and an output power of 2.22 W with a drain efficiency of 80.4%. Note that, because of the limited value of the resonant circuit loaded quality factor, the second- and higher-order harmonics are dissipated on the load contributing to some efficiency reduction. A more sinusoidal wave shape across the load can be obtained by adding a low-pass filter at the amplifier output.

To provide a flat-top switch voltage waveform with higher efficiency, an additional shunt capacitance C_1 can be added to a conventional Class-E load network between the series inductance L and series L_0C_0 filter, as shown in Fig. 13.32A.[10] In this case, due to the series filter tuned to the fundamental, the theoretical efficiency of 100% can be achieved in view of the infinite loaded quality factor of the series filter and zero switching loss in the transistor for a lossless Class-E load network. By providing the required zero-voltage and zero voltage-derivative switching conditions, the load-network parameters can be calculated through the normalized parameter q derived as

$$q = \sqrt{1+k}\,q_1 \tag{13.1}$$

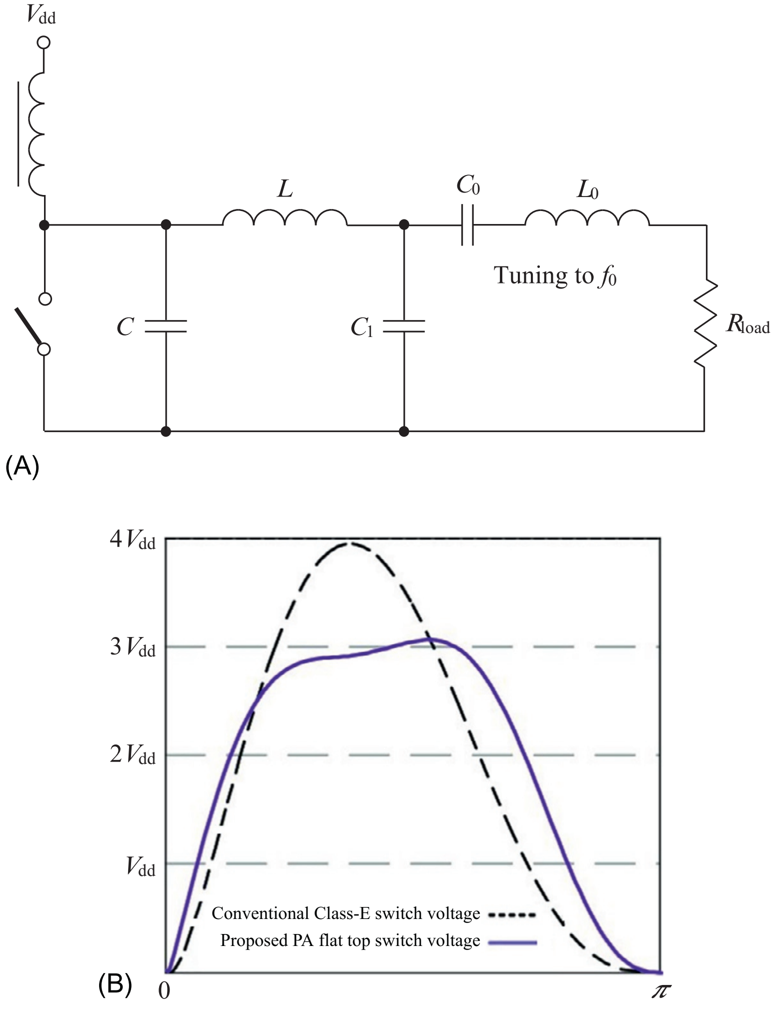

V_{dd}
L
C_0
L_0
Tuning to f_0
C
C_1
R_{load}
(A)
$4V_{dd}$
$3V_{dd}$
$2V_{dd}$
V_{dd}
Conventional Class-E switch voltage
Proposed PA flat top switch voltage
(B)
0
π

FIG. 13.32

Equivalent circuit of flat-top Class-E power amplifier with simulated switch voltage waveform.

where

$$k = \frac{C_1}{C} \tag{13.2}$$

$$q_1 = \frac{1}{\omega\sqrt{LC_1}}. \tag{13.3}$$

Fig. 13.32B shows the flat-top switch voltage waveform of the proposed flat-top Class-E power amplifier compared with the switch voltage waveform of a conventional Class-E power amplifier with shunt capacitance when the elements L and C_1 resonate at the third harmonic with $q_1 = 3$, where the simulated peak switch voltage is obtained approximately as high as $3V_{\mathrm{dd}}$, which is similar to a Class-E/F$_3$ mode described in Section 10.3.2. By using an IRF530 power MOSFET as a switching device when $k = 0.64$ including the external shunt and internal drain-source capacitances, an output power of 13.12 W with a drain efficiency of 90.3% was achieved at an operating frequency of 1 MHz at $V_{\mathrm{dd}} = 20$ V.[10]

13.7 Class-E power amplifier design using SPICE

The high-voltage MOSFET devices are preferable to provide a very high output power at high frequencies operating in the switchmode Class-E. Fig. 13.33 shows the simulated circuit schematic of a 13.56-MHz 400-W MOSFET Class-E power amplifier implemented in SPICE.[11] The MOSFET device IRFP450LC is modeled as a switch with a linear capacitor C_t and a nonlinear voltage source E_{ct} to model the square-root behavior of the drain-source capacitance. To simulate an accurate frequency-domain behavior, it is important to include the parasitic inductance L_{cd} of the drain-source capacitor C_{d} and the parasitic capacitor C_{r} due to the heatsink, insulating pad, and MOSFET

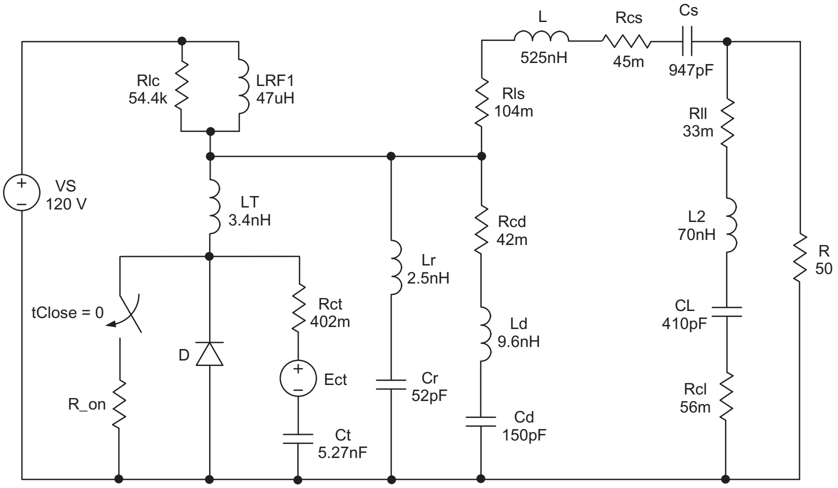


FIG. 13.33

13.56-MHz Class-E power amplifier SPICE model.

assembly. The sum of the inductances L_T and L_r along with a capacitance C_r predicts the resonant frequency at the 22nd harmonic component or 298 MHz. The final SPICE simulation involved the calculation of component losses using the measured values of the resistances for the inductors and capacitors. The accuracy of the drain efficiency and output power simulations was of approximately 1% compared with the experiment. The practical circuit schematic of this high-power Class-E MOSFET power amplifier is shown in Fig. 5.33A in Chapter 5.

High-voltage MOSFETs are available in mirror image pairs and the heat spreader of the plastic package is connected to the source. They can operate up to supply voltage of 300 V and at frequencies up to 100 MHz. The device used for this amplifier is ARF448A (or its more rugged version ARF460A) having a breakdown voltage of 450 V and drain junction thermal resistance of 0.55 °C/W. The power gain in Class-C is more than 25 dB at 27 MHz. The drain-source capacitance C_{oss} is 125 pF at a supply voltage V_{dd} of 125 V, and the saturation resistance $R_{ds(on)}$ is 0.4 Ω. These data-sheet parameters were entered in the HEPA-PLUS Class-E design program and it generated starting design values for the Class-E load network. The circuit schematic of a 27.12-MHz 500-W MOSFET power amplifier common to most Class-E amplifiers is shown in Fig. 13.34.[12]

In Class-E amplifiers, there is a capacitor shunted across the drain to source. There is none used here because the output capacitance of the device is slightly larger than the optimum value for that component required for Class-E. This defines the upper-frequency limit for efficient Class-E operation of a particular device. The parasitic series resistance of 3 Ω of the lossy drain-source capacitance C_{oss} is one of the primary loss mechanisms in the circuit. However, C_{oss} exhibits little of the parasitic inductance. The output circuit values were adjusted slightly for maximum efficiency at an output power of 490 W.

While the designing of the output circuit is straightforward enough, it was not reduced to practice very easily. The main problem was providing enough RF voltage to the gate to drive the drain into voltage saturation. The input impedance of the gate at 27 MHz is $(0.1 - j2.7)$ Ω and the gate-source capacitance C_{iss} is 1400 pF. If 10 V of peak gate drive is needed, a reasonable match between the drive source and gate is required. There is approximately 9 nH of parasitic series gate inductance. This is enough inductance to make it impossible to observe with an oscilloscope the actual voltage applied

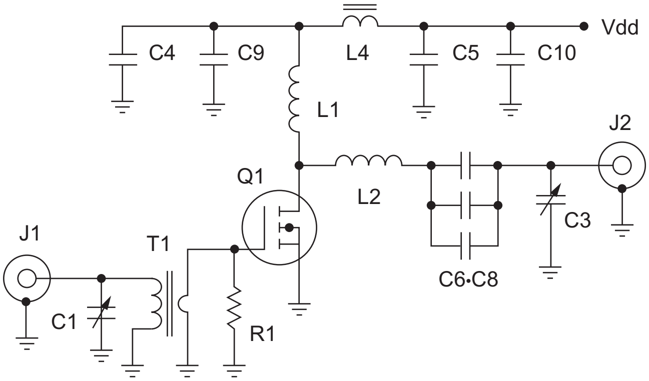
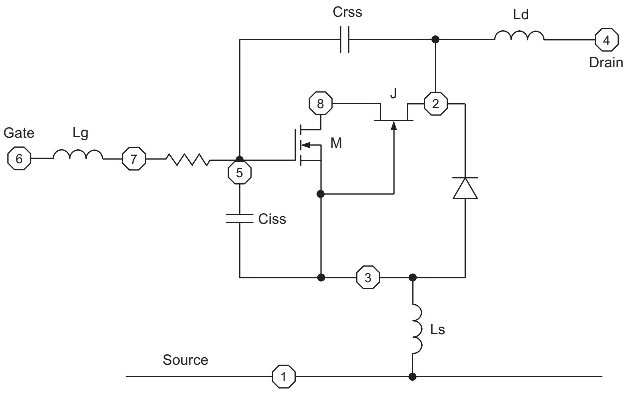


FIG. 13.34

Circuit schematic of 27.12 MHz MOSFET Class-E power amplifier.



```
*       PSPICE MODEL RF N-CHANNEL POWER
        MOSFET
*       ARF448A/B             27 July 1998
**                            G D S
*       .SUBCKT ARF448        6  4  1
CISS    3  5  1450P
CRSS    5  2  65P
LG  7  6  4  6N
M 8 5 3 3 125-050M L=2U W=1.4; DGSB LEVEL1
J1  8  3  2  125-050J
D  3  2  125-050D
LS  1  3  2  3N
RGATE  7  5  .29
LD  4  2  4  5N
.MODEL 125-050M NMOS (VTO=3.4 KP=14u
        Lambda=1m Gamma=.2 RD=130m RS=13m)
.MODEL 125-050J NJF (VTO=-25.5 BETA=.01
        Lambda=.5)
.MODEL 125-050D D (BV=550 RS=230M
CJO=422P
        VJ=670M M=330M)
.ENDS
```

FIG. 13.35

SPICE model for ARF448 MOSFET.

to the gate. A SPICE macro model for the device is shown in Fig. 13.35.[12] The goal was to design a network using SPICE to match the gate impedance sufficiently to permit sine-wave drive.

The input circuit using a 4:1 transformer and a low-pass *L*-network was designed using Smith chart software program. To stabilize the power amplifier operation, a 25-Ω 5-W padding resistance was placed across the gate representing the parallel equivalent of the capacitance 2200 pF in parallel with the resistance 210 Ω. This raises the effective input impedance to $(0.38 - j2.6)$ Ω, lowers the network quality factor, and makes it much easier to match and drive properly. The input transformer is made from a two-hole ferrite "binocular" bead balun. The secondary winding consists of two 7/8-in. pieces of 3/16-in. diameter brass tubing connected with copper shim stock. The four-turn primary is wound inside the tubes for maximum coupling and minimum leakage which measured 19 nH referenced to the secondary side. High-quality passive components are required in the output network. Most important of these is the series inductor L_2 with a quality factor of 375 and a calculated dissipation of 4.2 W, which was wound from bare copper wire, as described in Table 13.1. This coil is not capable of continuous duty operation unless it is attached with high-temperature solder and/or separate mechanical termination support is used. It was necessary to parallel three 10-nF ceramic coupling capacitors (type BX or Y5V) to carry the RF current. Table 13.1 shows the components values of a 27.12-MHz 500-W Class-E power amplifier.[12]

A simple SPICE model of the power amplifier was compared with HEPA simulation and measured results. Overall, the agreement was good, especially between HEPA and the ideal circuit SPICE model. Attempts to insert the SPICE macro model of the transistor into the amplifier were not successful. A much more sophisticated model is needed to adequately simulate the effects of the nonlinear capacitances of the MOSFET. However, the SPICE model was very useful for the understanding the gate-drive problem mentioned earlier. HEPA assumes that the device is being driven into voltage saturation; the only input parameter it considers is input drive power used for the overall efficiency calculation. The gate drive was the biggest problem in the design because a large RF-capable power MOSFET has very small input impedance. One of the best tests for reliability of an amplifier is mismatch load testing.

Table 13.1 27.12 MHz Class-E power amplifier component values.

C1, C3	75–380 pF mica trimmer, ARCO 465
C4–C8	0.01 μF 1 kV disc ceramic
C9, C10	0.01 μF 500 V disc ceramic
L1	0.6 μH. 25 t #24 ga.enam. 0.5″ dia.
L2	210 nH. 4 t #8 ga. 0.75″ id, 1″ long
L4	2t #20 PTFE on 0.5″ ferrite bead $\mu = 850$
Q1	APT ARF448A
R1	25 Ω 5 W noninductive
T1	Pri: 4t #20 PTFE, Sec: 1t brass tube on 2 hole balun bead Fair-Rite #2843010302 $\mu = 850$

The ARF448 has approximately 175 W of available dissipation in the test amplifier with its air-cooled heat sink. The performance at eight points around a 2:1 *VSWR* mismatch circle was calculated using HEPA. It was found that there is a region with the high inductive impedance that should be avoided. Without protection, the output power soared to 750 W and the drain current was almost twice normal. The efficiency stayed quite constant, never losing more than 11% at any load angle. The measured gate and drain voltage waveforms are shown in Fig. 13.36.[12] The peak drain voltage measures 430 V. The highest efficiency of 83% was measured at 490 W, which is 5.5% below the simulated due to the lossy nonlinear drain-source capacitance and longer switching time.

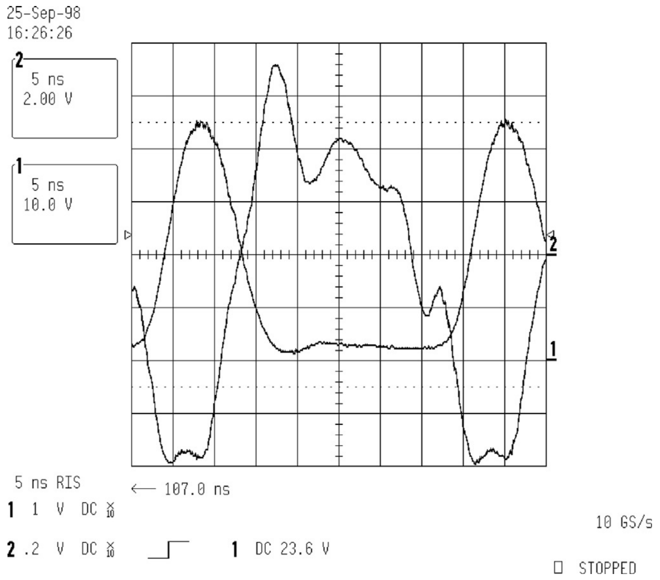
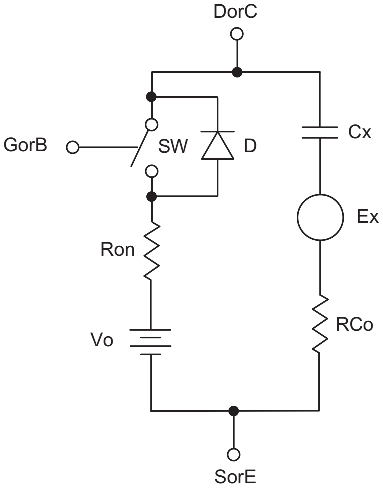


FIG. 13.36

Measured gate and drain voltage waveforms.



```
.SUBCKT  T_MODEL  DorC  GorB  SorE
         + PARAMS: Co=1pF  phi=0.6V  n=0.5  Ron=0.5
         + RCo=3  Vo=0
.MODEL   ONOFF  VSWITCH  (RON=0.01
         + ROFF=1e8  VON=4  VOFF=0)
.MODEL         Dmode  D( )
Sw       DorC  E  GorB  SorE  ONOFF
Dsw      E              DorC           Dmodel
Ron      E              K              {Ron}
Vo       K              SorE           {Vo}
Cx       DorC           H              {phi*Co/(1-n)}
Ex       H       J      VALUE={V(DorC,SorE)-
         +PWRS((1+V(DorC,SorE)/phi),(1-n))}
RCo      J       SorE                  {RCo}
.ENDS
```

FIG. 13.37

PSPICE model of transistor switching mode.

Fig. 13.37 shows the PSPICE model describing the transistor switchmode operation with the output voltage-dependent capacitance.[13] The five basic elements are included in this model: ideal switch SW, transistor on-resistance R_{on} which normally can be found from data sheet, saturation offset voltage V_{o} which is equal to zero for FET devices, nonlinear equivalent for the output capacitance (C_{X} in series to E_{X}), and equivalent series resistance R_{Co} due to lossy output capacitance.

To implement the nonlinear voltage dependence of the output capacitance (the SPICE standard capacitor supports only linear capacitance), its nonlinear behavior can be represented by the junction voltage dependence in the form of

$$C(v) = \frac{C_0}{\left(1 + \frac{v}{\phi}\right)^n} \tag{13.4}$$

where C_0 is the capacitance for $v = 0$ and n is the junction profile coefficient. During optimization procedure, the parameters C_0, n, and ϕ are considered the fitting parameters that can be extracted from the data-sheet curve for the output MOSFET capacitance C_{oss}.

The nonlinear voltage dependence can be modeled with a fixed capacitor C_{X} and a series voltage-controlled voltage source E_{X}, which can be found from the expression for the total voltage v given by

$$v = v_{\mathrm{C}} + E_{\mathrm{X}}(v) \tag{13.5}$$

where v_{C} is the voltage across the capacitor C_{X} and E_{X} is defined as

$$E_{\mathrm{X}}(v) = v - \left(1 + \frac{v}{\phi}\right)^{1-n}. \tag{13.6}$$

By differentiating both parts of Eq. (13.5) and taking into account that $i/C = dv/dt$ and $i/C_X = dv_C/dt$, the fixed capacitor can be determined using Eq. (13.4) as

$$C_X = C_0 \frac{\phi}{1-n}. \tag{13.7}$$

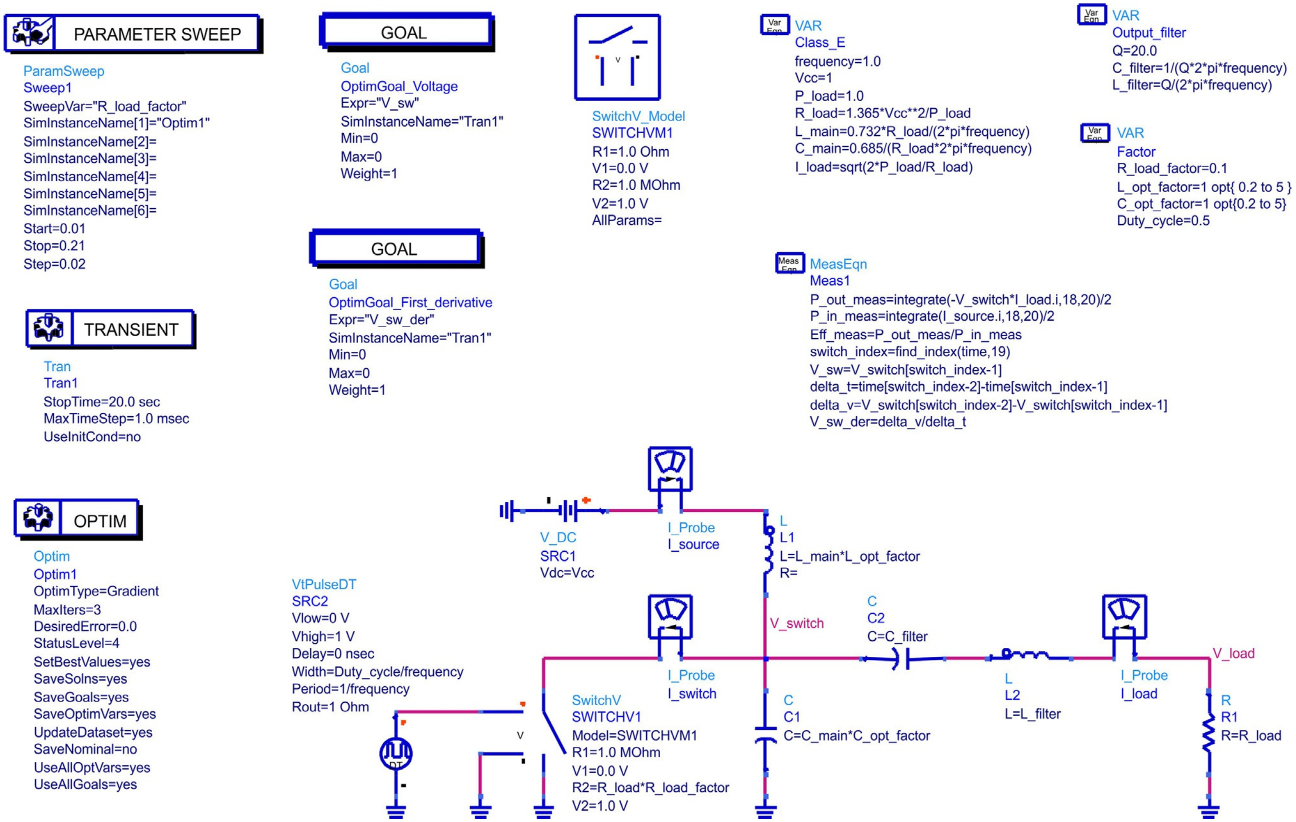
The model parameters R_{on} and R_{Co} can be measured or estimated from the device data sheet. The subcircuit shown in Fig. 13.37 must be connected to nodes D or C (drain or collector), SorE (source or emitter), and GorB (gate or base). A VSWITCH element should be used for the ideal switch SW, with two resistance values (low and high) following the control voltage applied to the gate terminal. If this voltage is equal or greater than VON (default value 4 V), the switch turns on to low resistance RON (default value 0.01 Ω). Otherwise, the switch turns off to high resistance ROFF (default value 1E8 Ω). The diode D parameters can be adjusted through its.MODEL description. The parameters C_0, n, ϕ, R_{Co}, and R_{on} can be more accurately modeled using the optimization procedure based on a discrete-time technique for the steady-state analysis of the nonlinear switched circuits with inconsistent initial conditions.[14] Using NGSPICE which is a latest version of Berkeley SPICE, the optimization procedure for the entire Class-E power amplifier (including input circuit) based on the time-domain shooting method for finding the steady-state responses can be fully implemented.[15]

13.8 Advanced Design System circuit simulator and its applicability to switchmode Class-E

The Keysight Advanced Design System (ADS) circuit simulator representing a comprehensive simulator of linear and nonlinear circuits in the frequency and time domains. It can be used directly to model and simulate the performance of the switchmode Class-E power amplifiers. This can be done using the transient, envelope, and harmonic balance simulation engines.

Fig. 13.38 shows the simulation setup for ideal parallel-circuit Class-E operation in the time domain. The active device is represented by a voltage-controlled switch with off-resistance of 1 MΩ and small finite on-resistance, the value of which can generally be varied. The input source represents a voltage source with pulse train defined at discrete time steps used in envelope and transient simulators. The use of discrete time pulse source, as opposed to a standard pulse source, can guarantee that there is no timing jitter in the pulse edge due to the waveform being sampled asynchronously by a fixed-time interval simulation. The simulation time is significantly faster than the period of a square wave.

To provide the circuit simulation in time domain, the transient simulator is added to the simulation template. The stop time of 20 s is chosen for a normalized frequency of 1 Hz which is sufficient to reach a steady-state mode for a simulated operating frequency normalized to unity, as shown on the example of the waveforms of the (a) switch voltage and (b) load current shown in Fig. 13.39. The inductors and capacitors are lossless and the loaded quality factor Q_L of the series resonant circuit is chosen to be as high as 20. The measure equations MeasEqn include the conditions when the switch voltage V_sw and its voltage derivative V_sw_der must take zero values at the instant just before the switch is turned on. The efficiency is calculated in the 19th + 20th period since the products of instantaneous current and voltage are integrated over these two periods and divided by two. The function “integrate” automatically deals with the nonconstant time steps in the transient simulation results. The term “switch_index” is the number (index) of the simulation points for 19 s, the instant when the switch is turned on, while the term “switch_index-1” is therefore the simulation point just before the switch is turned on.



ParamSweep
Sweep1
SweepVar="R_load_factor"
SimInstanceName[1]="Optim1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=
Start=0.01
Stop=0.21
Step=0.02

Tran
Tran1
StopTime=20.0 sec
MaxTimeStep=1.0 msec
UseInitCond=no

Optim
Optim1
OptimType=Gradient
MaxIters=3
DesiredError=0.0
StatusLevel=4
SetBestValues=yes
SaveSolns=yes
SaveGoals=yes
SaveOptimVars=yes
UpdateDataset=yes
SaveNominal=no
UseAllOptVars=yes
UseAllGoals=yes

Goal
OptimGoal_Voltage
Expr="V_sw"
SimInstanceName="Tran1"
Min=0
Max=0
Weight=1

Goal
OptimGoal_First_derivative
Expr="V_sw_der"
SimInstanceName="Tran1"
Min=0
Max=0
Weight=1

SwitchV_Model
SWITCHVM1
R1=1.0 Ohm
V1=0.0 V
R2=1.0 MOhm
V2=1.0 V
AllParams=

VAR
Class_E
frequency=1.0
Vcc=1
P_load=1.0
R_load=1.365*Vcc**2/P_load
L_main=0.732*R_load/(2*pi*frequency)
C_main=0.685/(R_load*2*pi*frequency)
I_load=sqrt(2*P_load/R_load)

VAR
Output_filter
Q=20.0
C_filter=1/(Q*2*pi*frequency)
L_filter=Q/(2*pi*frequency)

VAR
Factor
R_load_factor=0.1
L_opt_factor=1 opt{ 0.2 to 5 }
C_opt_factor=1 opt{0.2 to 5}
Duty_cycle=0.5

MeasEqn
Meas1
P_out_meas=integrate(-V_switch*I_load.i,18,20)/2
P_in_meas=integrate(I_source.i,18,20)/2
Eff_meas=P_out_meas/P_in_meas
switch_index=find_index(time,19)
V_sw=V_switch[switch_index-1]
delta_t=time[switch_index-2]-time[switch_index-1]
delta_v=V_switch[switch_index-2]-V_switch[switch_index-1]
V_sw_der=delta_v/delta_t

V_DC
SRC1
Vdc=Vcc

I_Probe
I_source

L
L1
L=L_main*L_opt_factor
R=

VtPulseDT
SRC2
Vlow=0 V
Vhigh=1 V
Delay=0 nsec
Width=Duty_cycle/frequency
Period=1/frequency
Rout=1 Ohm

I_Probe
I_switch

SwitchV
SWITCHV1
Model=SWITCHVM1
R1=1.0 MOhm
V1=0.0 V
R2=R_load*R_load_factor
V2=1.0 V

C
C1
C=C_main*C_opt_factor

C
C2
C=C_filter

L
L2
L=L_filter

I_Probe
I_load

R
R1
R=R_load

FIG. 13.38

Simulation setup to maintain Class-E mode in time domain.

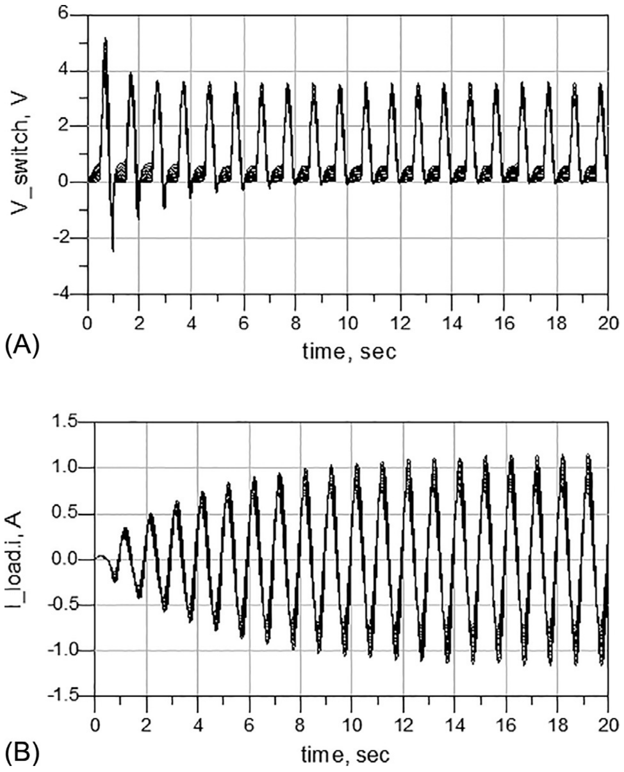


FIG. 13.39

Transient response of switch voltage and load current.

After the transient simulation has settled to a steady-state mode, the simulation results for the optimum parallel-circuit Class-E load-network parameters calculated from Eqs. (6.79) to (6.81) in Chapter 6 demonstrate the ideal Class-E voltage and current waveforms. The optimization simulator added to the simulation template shown in Fig. 13.38 is necessary to optimize the load-network parameters by varying their factors for a nonideal switch with finite on-resistance. The optimization is performed to minimize the switch voltage and voltage-derivative values to zero.

Fig. 13.40 shows a set of the switch (a) voltage and (b) current waveforms with a duty cycle (or ratio) of 0.5 obtained for zero voltage and voltage-derivative conditions by sweeping the switch resistance load factor from 0.01 to 0.21 with a step of 0.02. The total simulation time for a 1.6-GHz processor is 1.2 h. In this case, the peak voltage and current values are the smallest for maximum values of the switch on-resistance, and the saturation voltage becomes significant resulting in a lower output power and efficiency. The output power and efficiency drop by approximately 45% and 39%, respectively, when a ratio r_{sat}/R reaches the value of 0.15, as shown in Fig. 13.41A. This is achieved for an increased capacitance by 29% and a reduced inductance by 29%, as shown in Fig. 13.41B. When $r_{\mathrm{sat}}/R = 0.1$, the efficiency is equal to 73.4%.

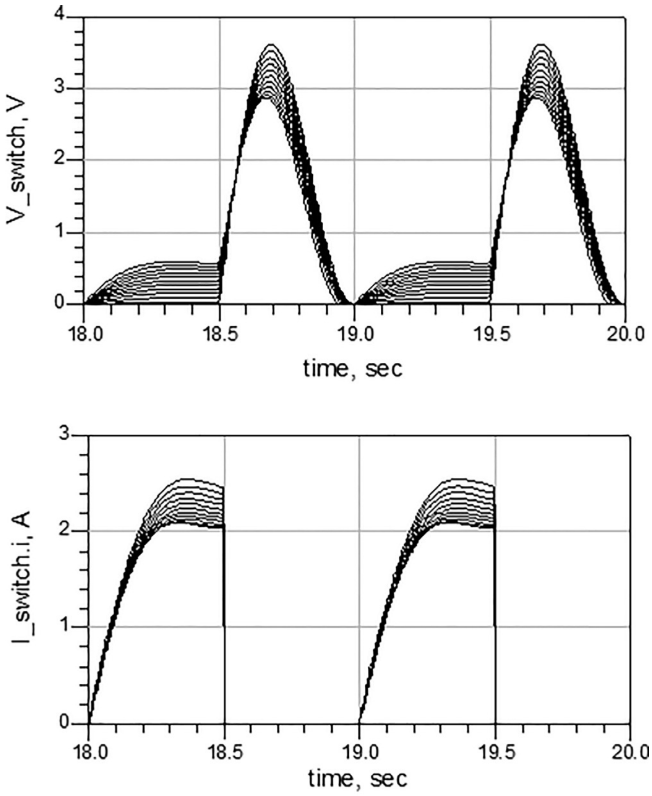


FIG. 13.40

Parallel-circuit Class-E optimum waveforms with finite on-resistance.

However, the Class-E zero voltage and zero voltage-derivative conditions become nonoptimum for finite values of the on-resistance. This means that higher efficiency can be achieved when these Class-E conditions are nonzero. Consequently, some voltage is present at the capacitor before the switch is turned on. By maintaining the switch transient time to almost zero and the optimum parameters of the load network, one can observe the discharge of this voltage in the shape of a current spike. Fig. 13.42 shows the switch (*a*) voltage and (*b*) current waveforms as a function of the normalized switch saturation resistance r_{sat}/R_L varying from 0.05 to 0.3 with a step of 0.05. Here, higher spikes correspond to lower values of r_{sat}/R_L, and then decreases with larger values of r_{sat}/R_L. As a result, for $r_{sat}/R = 0.1$, the efficiency is equal to 75.7%, which is by 2.3% greater than in a nominal case; for $r_{sat}/R = 0.15$, the efficiency is equal to 67.2%, which is by 6.2% greater than in a nominal case. This means that, for the normalized saturation resistance r_{sat}/R equal or smaller than 0.1, it makes sense to use the nominal values of a parallel-circuit Class-E load network, since it will simplify significantly the entire design procedure (no need optimization) and the efficiency will be close to theoretically achievable maximum.

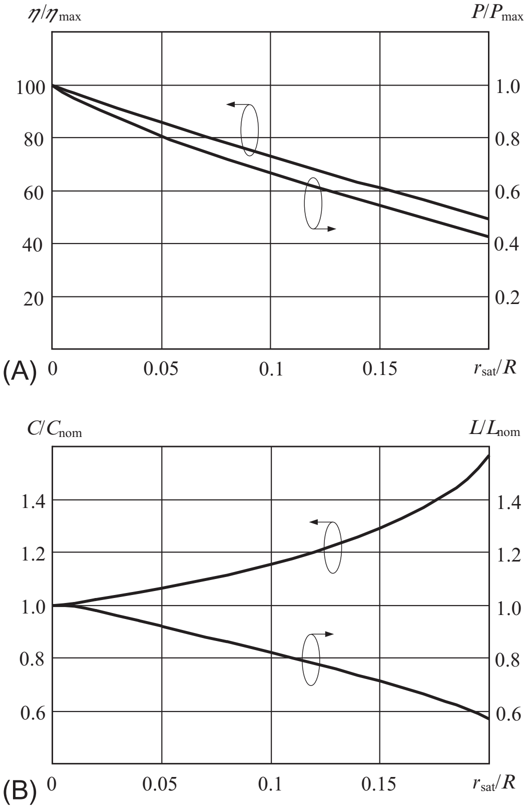


FIG. 13.41

Optimum parameters versus on-resistance.

Fig. 13.43 shows the simulation setup for ideal parallel-circuit Class-E operation in the frequency domain. Using the frequency domain enables the overall simulation procedure to be much faster than that in the time domain and can take a few seconds. However, because the number of harmonic components is not infinite, the simulation waveforms and numerical results for the optimum load-network parameters are not so accurate. In this case, the input source is changed and represents a voltage source with Fourier-series expansion of period square wave used in a harmonic-balance simulator. The harmonic order is chosen to 100. The optimization procedure can be applied with respect to the efficiency as an optimization parameter. Since the simulation time is very short, the number of iterations can significantly be increased for more accuracy. Fig. 13.44 shows the switch (a) voltage and (b) current waveforms obtained for the optimum parameters of the parallel-circuit Class-E load network. Unlike the time-domain simulations, there are smoother transitions between the positions when the switch is turned on and the switch is turned off and vice versa. Nevertheless, for $r_{sat}/R=0.01$, the efficiency is equal to 96.9%, which is only by approximately 0.1% smaller than that using the time-domain simulation.

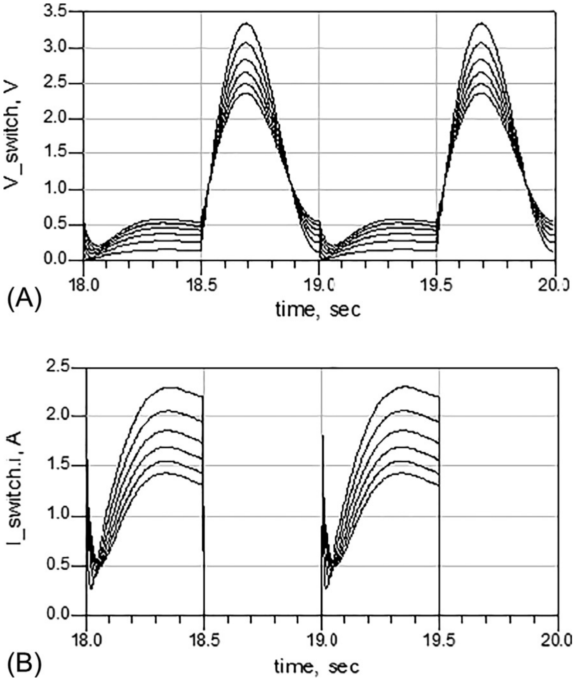


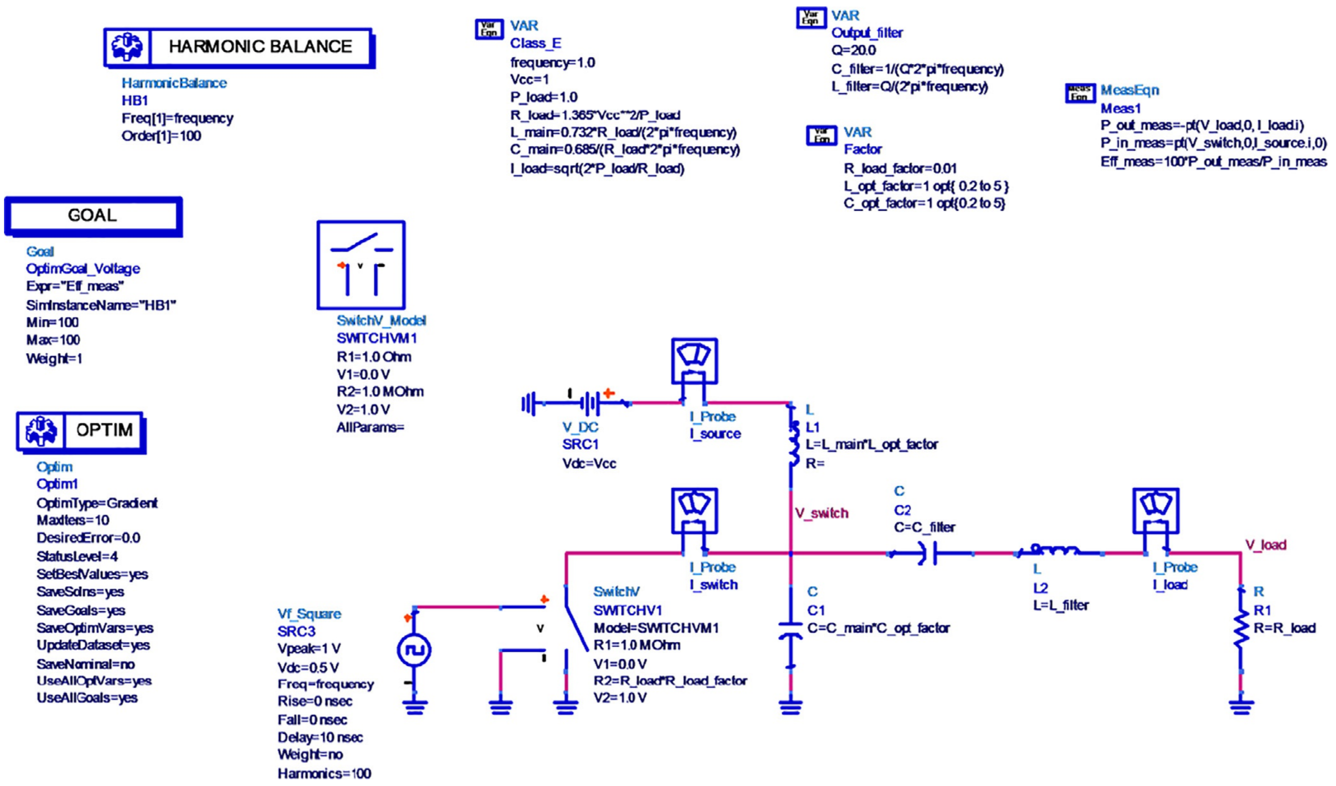
FIG. 13.42

Parallel-circuit Class-E waveforms with finite on-resistance.

13.9 ADS CAD design example: High-efficiency two-stage 1.75-GHz microwave monolithic integrated circuit HBT power amplifier

Since the ADS harmonic-balance circuit simulator gives a real possibility to enough accurately describe the nonlinear circuit behavior in the frequency domain, including active device and passive circuits, it can be very useful to simulate the entire high-efficiency power amplifier in a switchmode Class-E approximation as well. Generally the high-efficiency power amplifier design procedure can include the following several basic steps:

- The proper selection of the active device, accurate measurements of its small-signal *S*-parameters under different bias conditions in a wide frequency range, transformation of the *S*-parameters to the impedance *Z*- and admittance *Y*-parameters to describe the device electrical behavior through the nonlinear model in the form of its equivalent circuit with generally nonlinear parameters.
- The analytical calculation of the optimum parameters of the proper load network in a high-efficiency mode for given output power, supply voltage, and device output capacitance to provide the maximum collector efficiency and required harmonic suppression.
- The choice of a proper bias circuit to optimize the quiescent current and minimize the reference current and variations over temperature for maximum power gain and power-added efficiency.



HarmonicBalance
HB1
Freq[1]=frequency
Order[1]=100

VAR
Class_E
frequency=1.0
Vcc=1
P_load=1.0
R_load=1.365*Vcc**2/P_load
L_main=0.732*R_load/(2*pi*frequency)
C_main=0.685/(R_load*2*pi*frequency)
I_load=sqrt(2*P_load/R_load)

VAR
Output_filter
Q=20.0
C_filter=1/(Q*2*pi*frequency)
L_filter=Q/(2*pi*frequency)

VAR
Factor
R_load_factor=0.01
L_opt_factor=1 opt{ 0.2 to 5 }
C_opt_factor=1 opt{0.2 to 5}

MeasEqn
Meas1
P_out_meas=-pt(V_load,0, I_load.i)
P_in_meas=pt(V_switch,0,I_source.i,0)
Eff_meas=100*P_out_meas/P_in_meas

Goal
OptimGoal_Voltage
Expr="Eff_meas"
SimInstanceName="HB1"
Min=100
Max=100
Weight=1

SwitchV_Model
SWTCHVM1
R1=1.0 Ohm
V1=0.0 V
R2=1.0 MOhm
V2=1.0 V
AllParams=

Optim
Optim1
OptimType=Gradient
MaxIters=10
DesiredError=0.0
StatusLevel=4
SetBestValues=yes
SaveSolns=yes
SaveGoals=yes
SaveOptimVars=yes
UpdateDataset=yes
SaveNominal=no
UseAllOptVars=yes
UseAllGoals=yes

V_DC
SRC1
Vdc=Vcc

I_Probe
I_source

L
L1
L=L_main*L_opt_factor
R=

C
C2
C=C_filter

I_Probe
I_switch

C
C1
C=C_main*C_opt_factor

L
L2
L=L_filter

I_Probe
I_load

R
R1
R=R_load

SwitchV
SWTCHV1
Model=SWTCHVM1
R1=1.0 MOhm
V1=0.0 V
R2=R_load*R_load_factor
V2=1.0 V

Vf_Square
SRC3
Vpeak=1 V
Vdc=0.5 V
Freq=frequency
Rise=0 nsec
Fall=0 nsec
Delay=10 nsec
Weight=no
Harmonics=100

FIG. 13.43

Simulation setup to maintain Class-E mode in frequency domain.

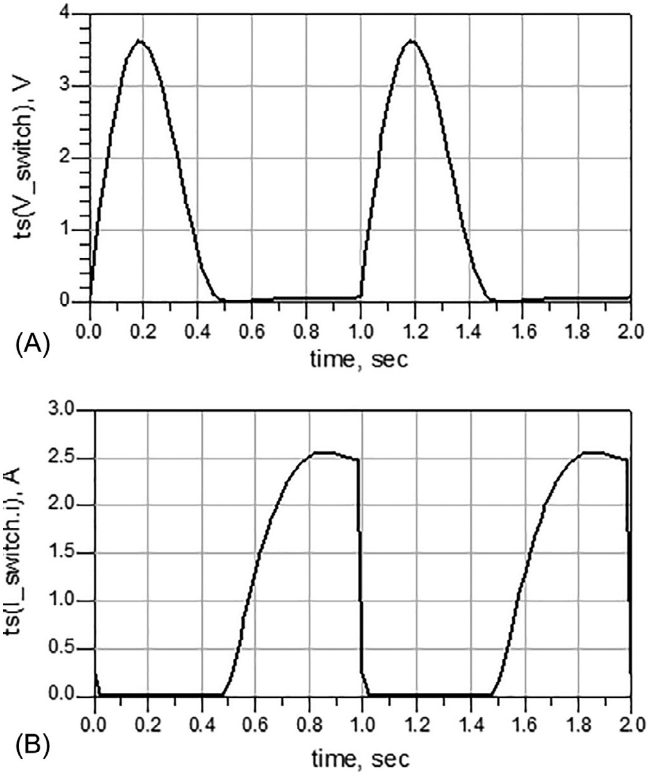


FIG. 13.44

Parallel-circuit Class-E nominal switch waveforms.

- The design of the input and interstage matching circuits to provide the minimum input return loss, maximum power gain and power-added efficiency, and stable operating conditions.
- The final circuit parameter optimization to maximize power-added efficiency.

As an example, our objective is to design a high-efficiency monolithic Class-E bipolar power amplifier operating at 1.75 GHz with an output fundamental-frequency power $P_{\text{out}} = 33\,\text{dBm}$, a transducer power gain $G_T = 27\,\text{dB}$, and a supply voltage $V_{\text{cc}} = 5\,\text{V}$. To satisfy these requirements, our decision is to choose a two-stage topology and HBT devices with a minimum saturation voltage at low supply voltage and a transition frequency $f_T > 25\,\text{GHz}$. Fig. 13.45 shows the nonlinear equivalent circuit of an InGaP/GaAs HBT transistor with the circuit parameters corresponding to the device emitter area of $3 \times 30\,\mu\text{m}^2$ (when $A = 1$). The most nonlinear parameters such as R_{bd} and C_{bd} representing the input diode forward-biased junction can be found by S-parameter simulation as a result of the S-parameter transformation to the input impedance Z_{in} or input admittance Y_{in}. Since, in a high-efficiency mode, the voltage swing is very high, the junction base-collector (or collector) capacitance C_{bc} can be chosen at some middle bias point, between the base and collector DC voltages. In our case, $C_{\text{bc}} = 4.25\text{e-}14{*}A$ in Farads.

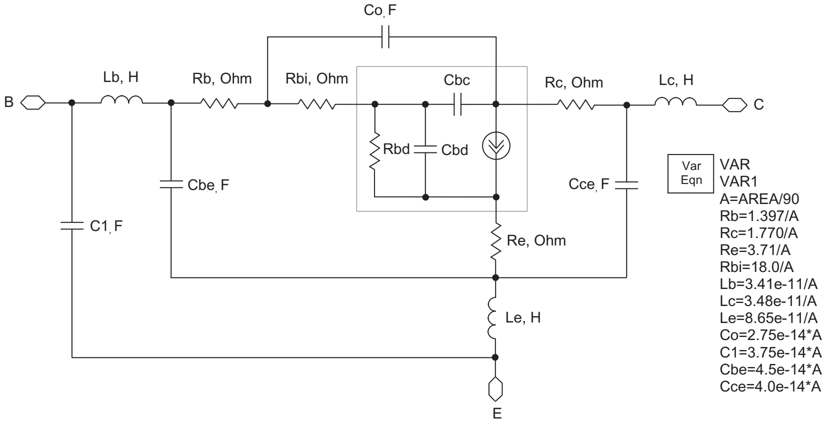


FIG. 13.45

Nonlinear high-frequency InGaP/GaAs HBT equivalent circuit.

Ideally, in a switchmode operation, the active device should act as an ideal switch, driven to be turned on or off by the input RF signal. Assuming the collector efficiency of the second-stage transistor of 80%, the DC power is equal to $P_0 = 2\,\text{W}/0.8 = 2.5\,\text{W}$ with the DC supply current $I_0 = P_0/V_{cc} = 2.5\,\text{W}/5\,\text{V} = 500\,\text{mA}$. Since, for a selected HBT device, the recommended DC current density for a reliable operation over wide temperature range should not exceed 15 mA per 90 μm^2, the overall emitter area was chosen with some margin to be equal to 5400 μm^2. The DC output characteristics $I_{ce}(V_{ce})$ of such an InGaP/GaAs HBT transistor for different base bias voltage V_{be} varying from 1.2 to 1.6 V with a voltage step of 30 mV are shown in Fig. 13.46. In this case, the peak collector current for a parallel-circuit Class-E mode according to Eq. (6.84) given in Chapter 6 is equal to $I_{max} = 2.647 I_0 = 2.15$ A. The idealized Class-E load line (with instant transition between pinch-off and saturation regions) is shown as a heavy line in two sections: horizontal at zero current (transistor is pinched off) and slanted upward to the right (transistor conducts current). As it is seen, the operating point moves along the horizontal V_{ce} axis (pinch-off region) and then along the collector current saturated line (voltage saturation region) until $I_{ce} = 2.15$ A. At this final point, the saturation voltage can be found as equal to $V_{sat} = 0.3$ V. This means that the power loss due to the finite device saturation resistance can be calculated as $P_{sat} = I_0 V_{sat} = 150\,\text{mW}$ with degradation in the collector efficiency of $P_{sat}/P_0 = 0.06$ or 6%.

First, we shall design the second stage for a maximum collector efficiency with some intermediate value of the source resistance much less than 50 Ω. The optimum parameters of a parallel-circuit Class-E load network can be calculated using Eqs. (6.79)–(6.81) given in Chapter 6 (including the saturation voltage V_{sat}) as.

$$R = 1.365\,\frac{(V_{cc} - V_{sat})^2}{P_{out}} = 15\Omega$$

$$L = 0.732\;\frac{R}{\omega} = 1.0\text{nH}$$

$$C = \frac{0.685}{\omega R} = 3.9\text{pF}.$$

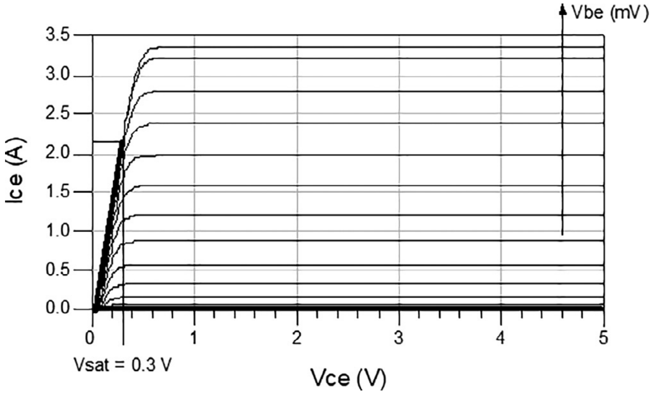


FIG. 13.46

Device output current–voltage characteristics and load line.

It should be noted that, in view of a saturation voltage, the calculated parameters of the Class-E load network generally cannot be considered optimum unlike the ideal case of zero saturation voltage. However, they can be considered as a sufficiently accurate initial guess for final design and optimization when efficiency is sufficiently high. In addition, the collector capacitance can be larger than required, especially at higher frequencies and for the transistor with large emitter area required for high output power. In our case, the total output capacitance can be estimated as $C_{out} = C_{ce} + C_0 + C_{bc} = 6.6\,\text{pF}$ for emitter area of $5400\,\mu\text{m}^2$, which is 1.5 times greater than required for nominal parallel-circuit Class-E mode. The excessive output capacitance of $6.6 - 3.9\,\text{pF} = 2.7\,\text{pF}$ is responsible for additional switching losses which occur during the transitions from the saturation mode to the pinch-off mode of the device operation. To compensate for this capacitance at the fundamental frequency, it is necessary to connect the inductance in parallel, which value is equal to 3 nH. Hence, the parallel connection of the two inductors with values of 1 and 3 nH results in a final value of $(1 \times 3)/(1 + 3) = 0.75$ nH.

Assuming the quality factor of the series filter of $Q_L = 10$, the series capacitance C_0 and inductance L_0 are calculated as

$$C_0 = \frac{1}{\omega R Q_L} = 0.6\,\text{pF}$$

$$L_0 = \frac{1}{\omega^2 C_0} = 13.8\,\text{nH}.$$

Since the input device impedance is sufficiently low, the intermediate source resistance is chosen to be equal to 5 Ω. In this case, it will be enough to use only one input matching section. The input matching circuit is composed in the form of a high-pass L-type section with a shunt inductor and a series capacitor. The parameters of this matching circuit can be simulated in a large-signal mode to minimize input return loss as a criterion by using Smith chart tuning procedure.

Fig. 13.47 shows the simulation setup of the second amplifying stage designed to operate in a parallel-circuit Class-E mode. To simulate the electrical characteristics and waveforms, the corresponding current probes and voltage wire labels are incorporated into the circuit. As a

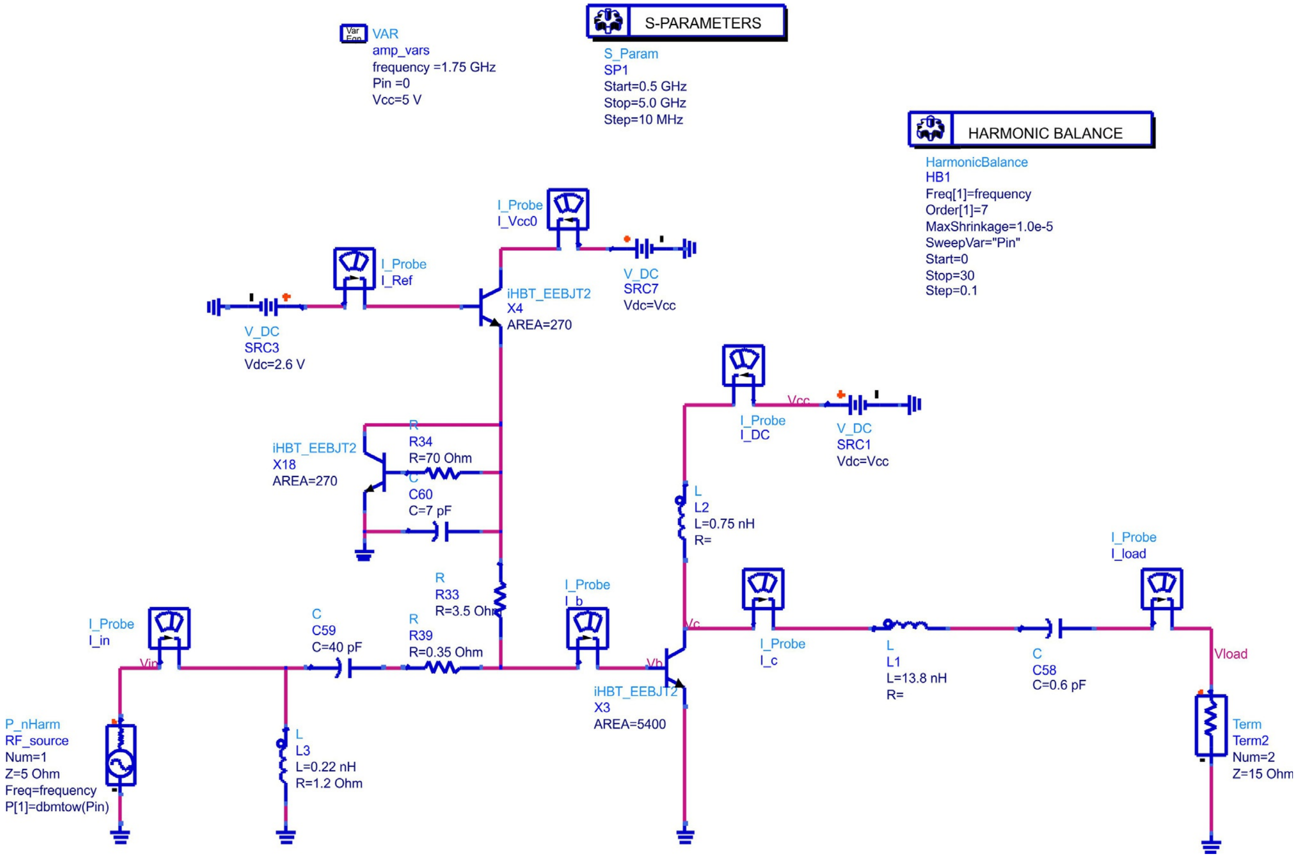

VAR
amp_vars
frequency =1.75 GHz
Pin =0
Vcc=5 V
S-PARAMETERS
S_Param
SP1
Start=0.5 GHz
Stop=5.0 GHz
Step=10 MHz
HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=frequency
Order[1]=7
MaxShrinkage=1.0e-5
SweepVar="Pin"
Start=0
Stop=30
Step=0.1
I_Probe
I_Vcc0
V_DC
SRC7
Vdc=Vcc
I_Probe
I_Ref
iHBT_EEBJT2
X4
AREA=270
V_DC
SRC3
Vdc=2.6 V
Vcc
I_Probe
I_DC
V_DC
SRC1
Vdc=Vcc
iHBT_EEBJT2
X18
AREA=270
R
R34
R=70 Ohm
C
C60
C=7 pF
L
L2
L=0.75 nH
R=
I_Probe
I_load
R
R33
R=3.5 Ohm
I_Probe
I_b
I_Probe
I_in
Vin
C
C59
C=40 pF
R
R39
R=0.35 Ohm
Vc
Vb
I_Probe
I_c
L
L1
L=13.8 nH
R=
C
C58
C=0.6 pF
Vload
iHBT_EEBJT2
X3
AREA=5400
Term
Term2
Num=2
Z=15 Ohm
P_nHarm
RF_source
Num=1
Z=5 Ohm
Freq=frequency
P[1]=dbmtow(Pin)
L
L3
L=0.22 nH
R=1.2 Ohm

FIG. 13.47

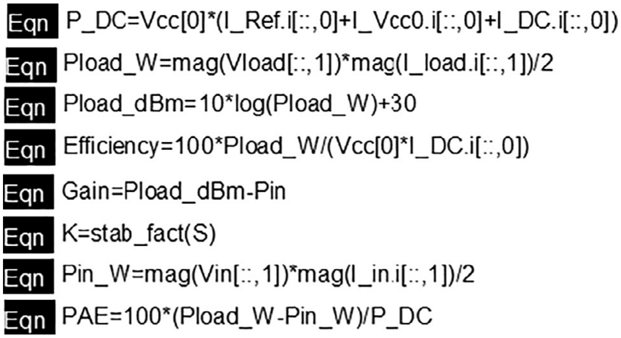
Simulation setup for Class-E second amplifying stage.

current-controlled device, the bipolar transistor requires the DC base driving current, the value of which depends on the output power and device parameters. Because technologically the bipolar device represents a parallel connection of the basic cells, the important issue is to use the ballasting series resistors to avoid the current imbalance and possible device collapse at higher current density levels. Generally, different types of the current-mirror bias circuits can be effectively used to bias a transistor. In our case, the emitter-follower bias circuit that provides the temperature compensation and minimizes the reference current is used.[16] It is very important to provide the proper ratio between the ballasting resistors R_{34} and R_{33}, which is equal to the ratio of the corresponding device areas of $5400/270 = 20$. The emitter-follower bias circuit normally requires only several tens of microamperes of reference current.

Fig. 13.48 shows the measurement equations required to plot the small- and large-signal power-amplifier characteristics. The small-signal frequency dependence of the stability factor K is shown in Fig. 13.49A demonstrating the unconditional stable conditions over entire frequency range with $K > 1$. However, it is not enough just simulating the small-signal performance only. It is important also to verify the potential instability which can occur in the form of injection-locking effect at large-signal mode near operating frequency. The dependences of the real part of the device impedance at the base terminal ReZ_b and the real part of the input impedance ReZ_{in} on the input power P_{in} seen by the source are shown in Fig. 13.49B. It is seen that the real part of the base impedance is slightly negative. To compensate for this negative resistance, it is necessary to connect the resistance of 0.35 Ω in series to the base compromising the stable operation and enough power gain. The real part of the input impedance seen by the source is close to the required 5 Ω at nominal large-signal operation.

As a result, the second power-amplifier stage exhibits a linear power gain of approximately 13 dB and a saturated output power of 33.1 dBm, whose dependences are shown in Fig. 13.50A, with a maximum collector efficiency of 85.3% and a maximum power-added efficiency (*PAE*) of 60.5%, whose dependences on the input power P_{in} are shown in Fig. 13.50B. It is seen that the collector efficiency improvement is achieved at the expense of the significant power gain reduction. However, the maximum *PAE* occurs when the power gain is reduced by approximately 3 dB, which is a result of the contribution of the driving power.

Fig. 13.51 shows the collector and base voltage waveforms corresponding to a Class-E approximation. The collector voltage waveform with a peak factor of approximately 18 V/5 V = 3.6 was achieved



```
Eqn P_DC=Vcc[0]*(I_Ref.i[::,0]+I_Vcc0.i[::,0]+I_DC.i[::,0])
Eqn Pload_W=mag(Vload[::,1])*mag(I_load.i[::,1])/2
Eqn Pload_dBm=10*log(Pload_W)+30
Eqn Efficiency=100*Pload_W/(Vcc[0]*I_DC.i[::,0])
Eqn Gain=Pload_dBm-Pin
Eqn K=stab_fact(S)
Eqn Pin_W=mag(Vin[::,1])*mag(I_in.i[::,1])/2
Eqn PAE=100*(Pload_W-Pin_W)/P_DC
```

FIG. 13.48

Measurement equations.

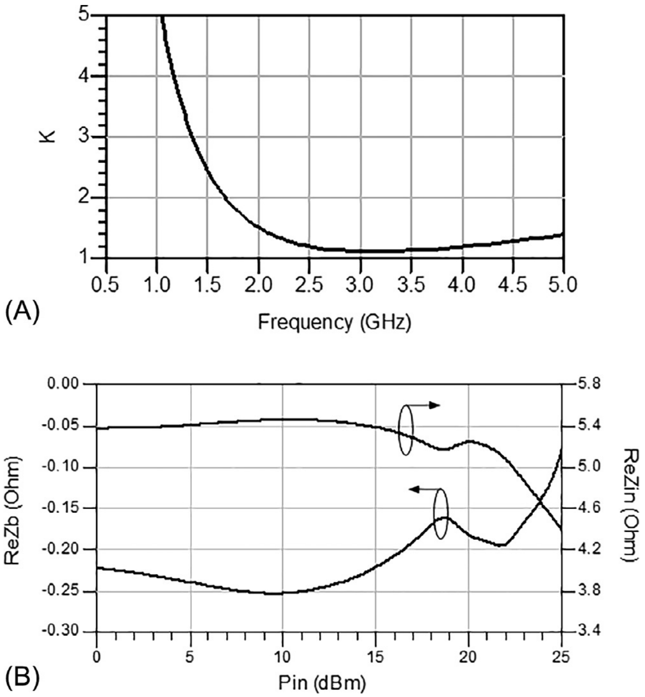


FIG. 13.49

Simulated (A) stability and (B) input impedance.

for a maximum collector efficiency with the base voltage waveform having a flattened top part and causing the device to operate in a switching mode with minimum switching loss.

To match the Class-E load resistance $R = 15\,\Omega$ with a standard load resistance $R_L = 50\,\Omega$, it is necessary to use a matching circuit with the series inductor as a first element to provide high impedance at the second- and higher-order harmonics. Since the ratio of impedances is not so high, we can use the low-pass L-type matching section with design equations given by Eqs. (5.40)–(5.42) in Chapter 5. As a result,

$$Q_L = \sqrt{\frac{50}{15} - 1} \cong 1.5$$

$$L = \frac{Q_L R}{\omega} = 2.1\,\text{nH}$$

$$C = \frac{Q_L}{\omega R} = 2.9\text{pF}.$$

Fig. 13.52 shows the simulation setup of a Class-E second amplifying stage with output matching circuit. Since the loaded quality factor Q_L is sufficiently small, the conditions at the fundamental-frequency and

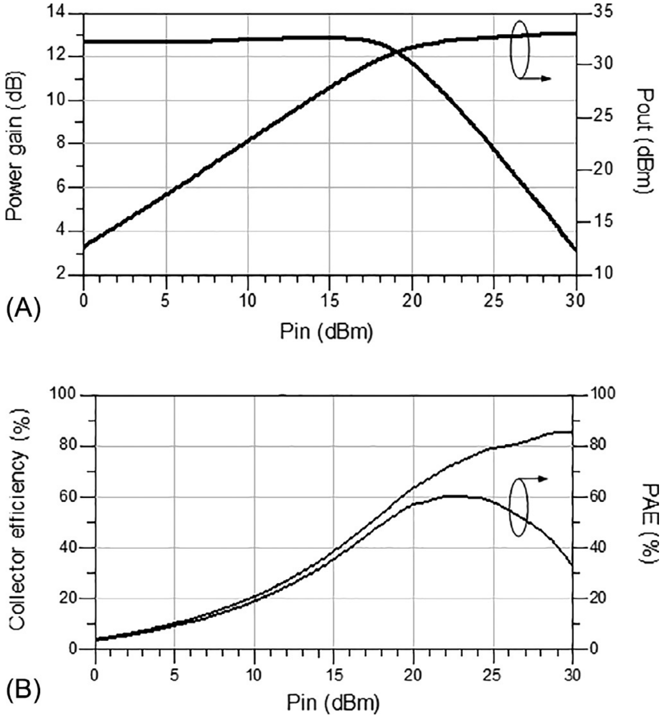


FIG. 13.50

Simulated (A) power gain, output power, and (B) collector and power-added efficiencies.

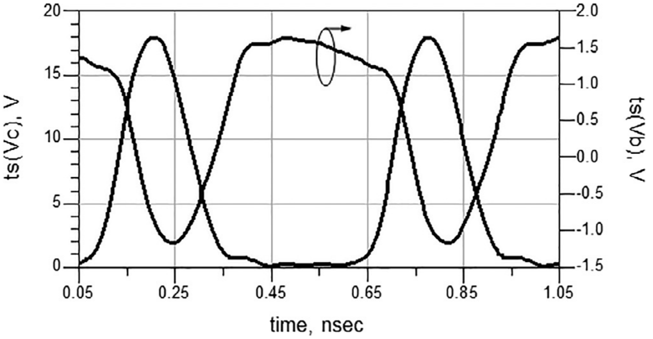


FIG. 13.51

Collector and base voltage waveforms.

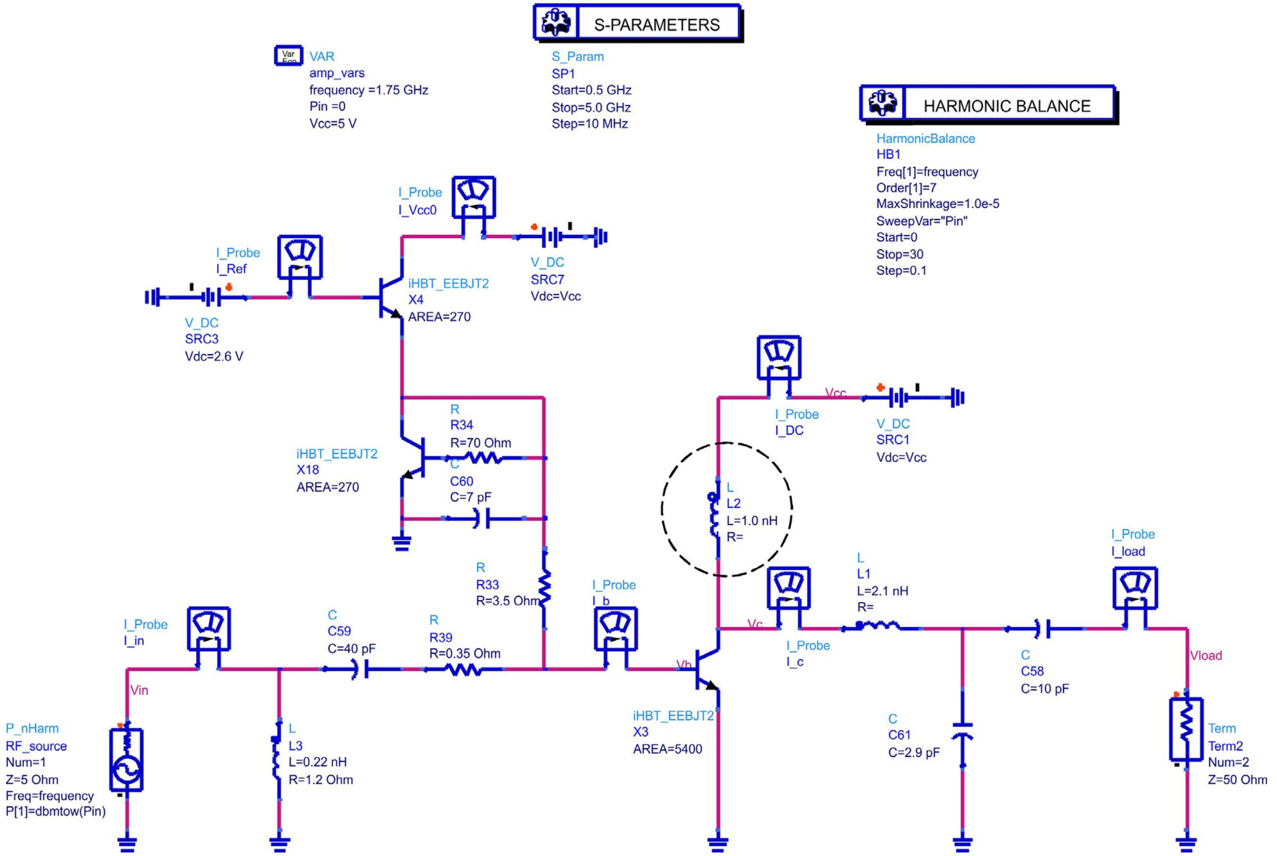

S-PARAMETERS
VAR
amp_vars
frequency =1.75 GHz
Pin =0
Vcc=5 V
S_Param
SP1
Start=0.5 GHz
Stop=5.0 GHz
Step=10 MHz
HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=frequency
Order[1]=7
MaxShrinkage=1.0e-5
SweepVar="Pin"
Start=0
Stop=30
Step=0.1
I_Probe
I_Vcc0
I_Probe
I_Ref
iHBT_EEBJT2
X4
AREA=270
V_DC
SRC7
Vdc=Vcc
V_DC
SRC3
Vdc=2.6 V
R
R34
R=70 Ohm
C
C60
C=7 pF
iHBT_EEBJT2
X18
AREA=270
Vcc
I_Probe
I_DC
V_DC
SRC1
Vdc=Vcc
L
L2
L=1.0 nH
R=
R
R33
R=3.5 Ohm
I_Probe
I_b
L
L1
L=2.1 nH
R=
I_Probe
I_load
I_Probe
I_in
C
C59
C=40 pF
R
R39
R=0.35 Ohm
Vc
Vb
I_Probe
I_c
Vload
Vin
C
C58
C=10 pF
P_nHarm
RF_source
Num=1
Z=5 Ohm
Freq=frequency
P[1]=dbmtow(Pin)
L
L3
L=0.22 nH
R=1.2 Ohm
iHBT_EEBJT2
X3
AREA=5400
C
C61
C=2.9 pF
Term
Term2
Num=2
Z=50 Ohm

FIG. 13.52

Simulation setup for Class-E second amplifying stage with output matching circuit.

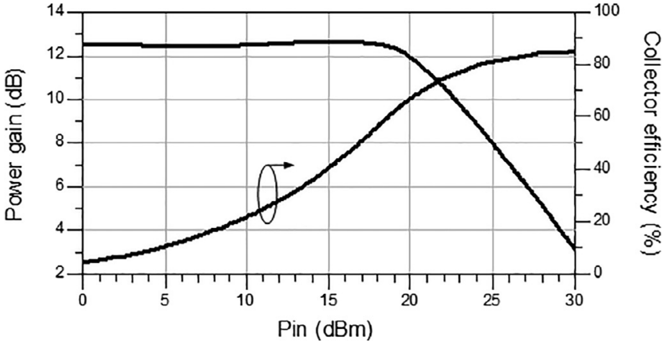


FIG. 13.53

Power gain and collector efficiency.

other harmonic components will be slightly different compared with the ideal case. In this case, the easiest way to maximize collector efficiency is to tune manually the parameters of the basic elements such as the parallel inductor, which is shown inside the dashed circle in Fig. 13.52. The maximum collector efficiency of 84.8% and power gain of approximately 13 dB were achieved, as shown in Fig. 13.53, by tuning the value of the inductance from 0.75 to 1.0 nH. However, a single low-pass L-type matching section can provide a second-harmonic suppression of approximately 20 dB. Consequently, to improve the spectral performance, it is necessary to use the two or more low-pass sections in succession, better with equal quality factors to provide the wider frequency bandwidth.[16]

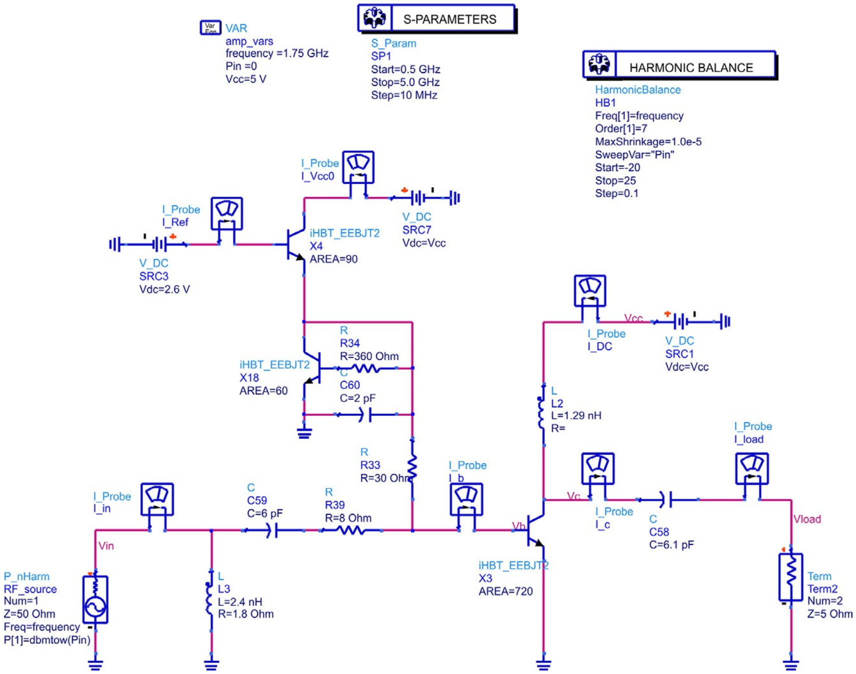
Fig. 13.54 shows the simulation setup of the first amplifying stage designed to operate in a Class-AB mode. Since it is sufficient to provide an output power from the first stage of not more than 200 mW, the device emitter area size was chosen to be 720 μm^2 and the equivalent output resistance is assumed to be 50 Ω, which is closed to the calculated value of $R_{\text{out}}=(V_{\text{cc}}-V_{\text{sat}})^2/2P_{\text{out}}=(4.7\times4.7)/0.4=55.2\,\Omega$. Then, to conjugately match the intermediate load resistance of 5 Ω with the chosen output resistance $R_{\text{out}}=50\,\Omega$, it is convenient to use a high-pass L-type matching section with the shunt inductor as a first element followed by the series capacitor. In this case, the shunt inductor with a bypass capacitor at its end in practical implementation also can serve as a DC power supply path. The parameters of the output matching circuit are calculated as.

$$Q_{\text{L}}=\sqrt{\frac{50}{5}-1}=3$$

$$L=\frac{R_{\text{out}}}{Q_{\text{L}}\omega}=1.5\,\text{nH}$$

$$C=\frac{1}{5Q_{\text{L}}\omega}=6.1\,\text{pF}.$$

To obtain a final value of the shunt inductor, it is necessary to consider the device collector capacitance. In our case, the total output capacitance can be estimated as $C_{\text{out}}=6.6\,\text{pF}\times(720\,\mu\text{m}^2/5400\,\mu\text{m}^2)=0.88\,\text{pF}$ for emitter area of 720 μm^2. To compensate for this capacitance at the fundamental frequency,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frequency =1.75 GHz
Pin =0
Vcc=5 V
S-PARAMETERS
S_Param
SP1
Start=0.5 GHz
Stop=5.0 GHz
Step=10 MHz
HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=frequency
Order[1]=7
MaxShrinkage=1.0e-5
SweepVar="Pin"
Start=-20
Stop=25
Step=0.1
I_Probe
I_Vcc0
V_DC
SRC7
Vdc=Vcc
I_Probe
I_Ref
V_DC
SRC3
Vdc=2.6 V
iHBT_EEBJT2
X4
AREA=90
R
R34
R=360 Ohm
iHBT_EEBJT2
X18
AREA=60
C
C60
C=2 pF
I_Probe
I_DC
Vcc
V_DC
SRC1
Vdc=Vcc
L
L2
L=1.29 nH
R=
I_Probe
I_load
R
R33
R=30 Ohm
I_Probe
I_b
I_Probe
I_in
C
C59
C=6 pF
R
R39
R=8 Ohm
Vc
I_Probe
I_c
C
C58
C=6.1 pF
Vload
Vin
Vb
P_nHarm
RF_source
Num=1
Z=50 Ohm
Freq=frequency
P[1]=dbmtow(Pin)
L
L3
L=2.4 nH
R=1.8 Ohm
iHBT_EEBJT2
X3
AREA=720
Term
Term2
Num=2
Z=5 Ohm

FIG. 13.54

Simulation setup for Class-AB first amplifying stage.

it is necessary to connect the inductor of 9.4 nH in parallel. Hence, the parallel connection of the two inductors with values of 9.4 and 1.5 nH results in a final value of 1.29 nH. The input matching circuit is composed in the form of a high-pass L-type section, the parameters of whose elements can be simulated in a large-signal mode to minimize input return loss as a criterion by using Smith chart tuning procedure. To improve stability factor and simplify the input matching, the resistor of 8 Ω, connected in series to the transistor base terminal, was included.

The small-signal frequency dependence of the stability factor K and S_{11} are shown in Fig. 13.55A demonstrating the unconditional stable conditions over entire frequency range with $K > 1$ and input return loss better than 30 dB at the operating frequency. Under large-signal operation, the first amplifying stage exhibits a linear power gain of approximately 15 dB and a maximum collector efficiency of approximately 72%, the dependences of which on the input power P_{in} are shown in Fig. 13.55B. It is seen that the collector efficiency improvement is achieved at the expense of the significant power gain reduction. However, the sufficiently high efficiency of approximately 65% can be achieved at a 3-dB compression point when the power gain is reduced by 3 dB from its linear value.

The next step is to combine the first amplifying stage with the load impedance of 5 Ω and the second amplifying stage with the source impedance of 5 Ω in a two-stage power amplifier. Fig. 13.56 shows the simulation setup of the two-stage Class-E power amplifier with lumped elements. The main attention should be paid to the interstage matching circuit consisting of the two high-pass matching sections since the impedances are not exactly the same, having also some certain values at the harmonics.

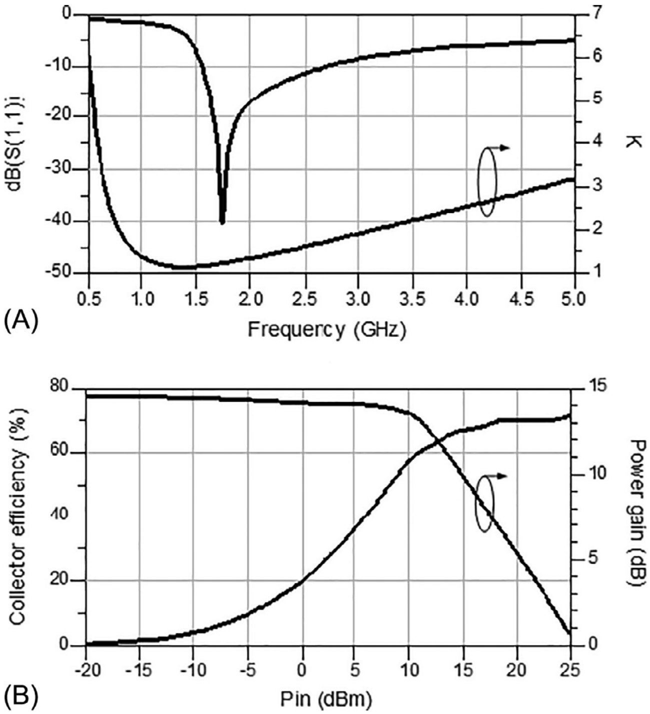


FIG. 13.55

Simulated (A) input return loss and (B) collector efficiency of first amplifying stage.

In this case, it is necessary to provide some tuning of the elements around their initial values shown in a dashed circle. It can be done sufficiently fast even with manual tuning.

Fig. 13.57 shows the measurement equations required to plot the small- and large-signal power amplifier characteristics including all DC power sources. The small-signal frequency dependences of the stability factor K and S_{11} are shown in Fig. 13.58A demonstrating the unconditional stable conditions over entire frequency range with $K > 2$ and input return loss better than 13 dB at the operating frequency. Under large-signal operation, the two-stage parallel-circuit Class-E power amplifier exhibits a linear power gain of more than 29 dB and a maximum *PAE* of approximately 68%, the dependences of which on the input power P_{in} are shown in Fig. 13.58B. The sufficiently high efficiency of approximately 57.5% can be achieved at a 1-dB compression point when the power gain is reduced by 1 dB from its small-signal linear value.

Finally, the lumped inductors must be replaced by the microstrip lines using standard FR4 substrate. The lumped capacitors in the output matching circuit can be implemented as the metal-insulator-metal (MIM) capacitors using a separate die to provide their high-quality factors. To calculate the parameters of the microstrip lines, let us represent the input impedance of a transmission line with arbitrary load impedance as

$$Z_{\text{in}} = Z_0 \frac{Z_{\text{L}} + jZ_0 \tan\theta}{Z_0 + jZ_{\text{L}} \tan\theta} \tag{13.8}$$

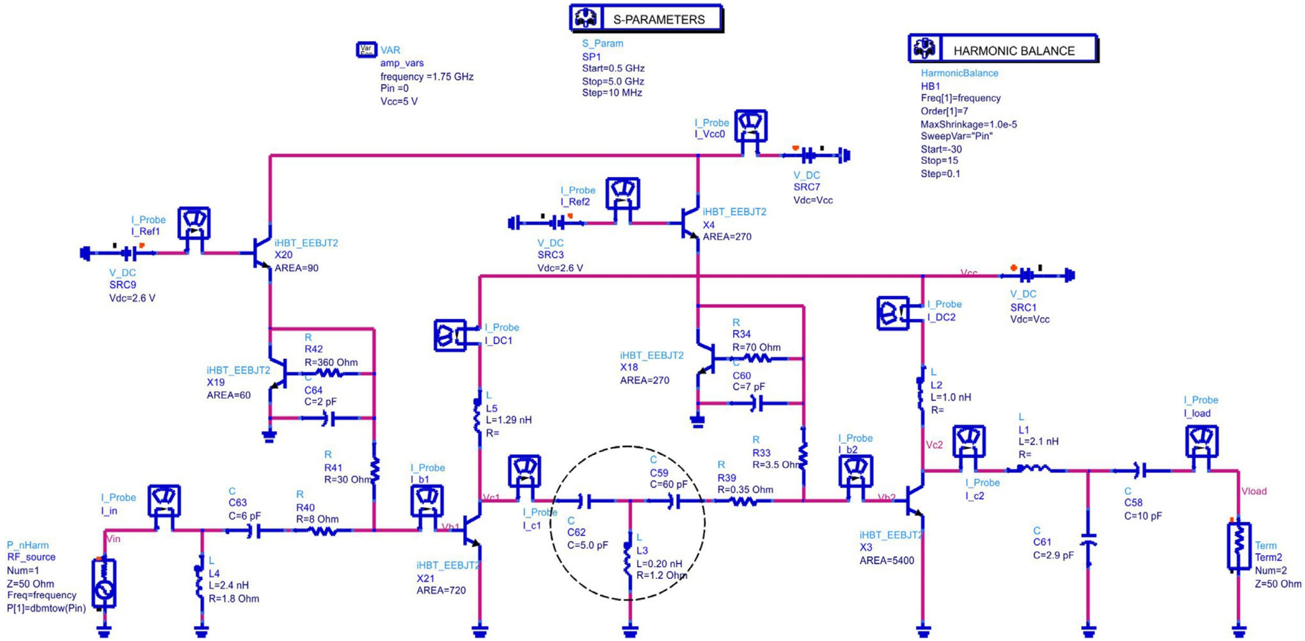
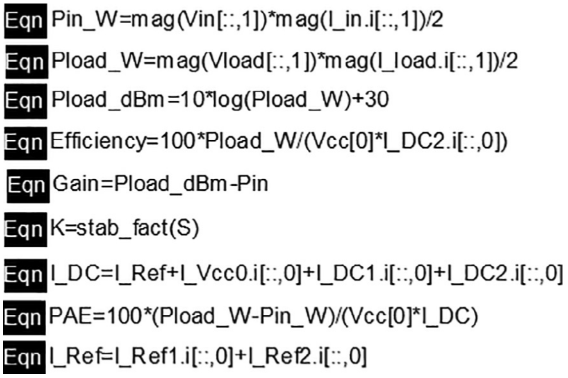

S-PARAMETERS
S_Param
SP1
Start=0.5 GHz
Stop=5.0 GHz
Step=10 MHz
VAR
amp_vars
frequency =1.75 GHz
Pin =0
Vcc=5 V
HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=frequency
Order[1]=7
MaxShrinkage=1.0e-5
SweepVar="Pin"
Start=-30
Stop=15
Step=0.1
I_Probe
I_Vcc0
V_DC
SRC7
Vdc=Vcc
I_Probe
I_Ref2
V_DC
SRC3
Vdc=2.6 V
iHBT_EEBJT2
X4
AREA=270
I_Probe
I_Ref1
V_DC
SRC9
Vdc=2.6 V
iHBT_EEBJT2
X20
AREA=90
Vcc
V_DC
SRC1
Vdc=Vcc
I_Probe
I_DC1
R
R34
R=70 Ohm
C
C60
C=7 pF
iHBT_EEBJT2
X18
AREA=270
I_Probe
I_DC2
R
R42
R=360 Ohm
C
C64
C=2 pF
iHBT_EEBJT2
X19
AREA=60
L
L5
L=1.29 nH
R=
L
L2
L=1.0 nH
R=
R
R41
R=30 Ohm
R
R33
R=3.5 Ohm
Vc2
L
L1
L=2.1 nH
R=
I_Probe
I_load
C
C59
C=60 pF
I_Probe
I_b1
I_Probe
I_b2
R
R39
R=0.35 Ohm
I_Probe
I_c2
I_Probe
I_in
C
C63
C=6 pF
R
R40
R=8 Ohm
Vc1
Vb2
C
C58
C=10 pF
Vload
I_Probe
I_c1
C
C62
C=5.0 pF
Vin
Vb1
L
L3
L=0.20 nH
R=1.2 Ohm
iHBT_EEBJT2
X3
AREA=5400
C
C61
C=2.9 pF
P_nHarm
RF_source
Num=1
Z=50 Ohm
Freq=frequency
P[1]=dbmtow(Pin)
L
L4
L=2.4 nH
R=1.8 Ohm
iHBT_EEBJT2
X21
AREA=720
Term
Term2
Num=2
Z=50 Ohm

FIG. 13.56

Simulation setup for two-stage Class-E power amplifier with lumped elements.



```
Eqn Pin_W=mag(Vin[::,1])*mag(I_in.i[::,1])/2
Eqn Pload_W=mag(Vload[::,1])*mag(I_load.i[::,1])/2
Eqn Pload_dBm=10*log(Pload_W)+30
Eqn Efficiency=100*Pload_W/(Vcc[0]*I_DC2.i[::,0])
Eqn Gain=Pload_dBm-Pin
Eqn K=stab_fact(S)
Eqn I_DC=I_Ref+I_Vcc0.i[::,0]+I_DC1.i[::,0]+I_DC2.i[::,0]
Eqn PAE=100*(Pload_W-Pin_W)/(Vcc[0]*I_DC)
Eqn I_Ref=I_Ref1.i[::,0]+I_Ref2.i[::,0]
```

FIG. 13.57

Measurement equations.

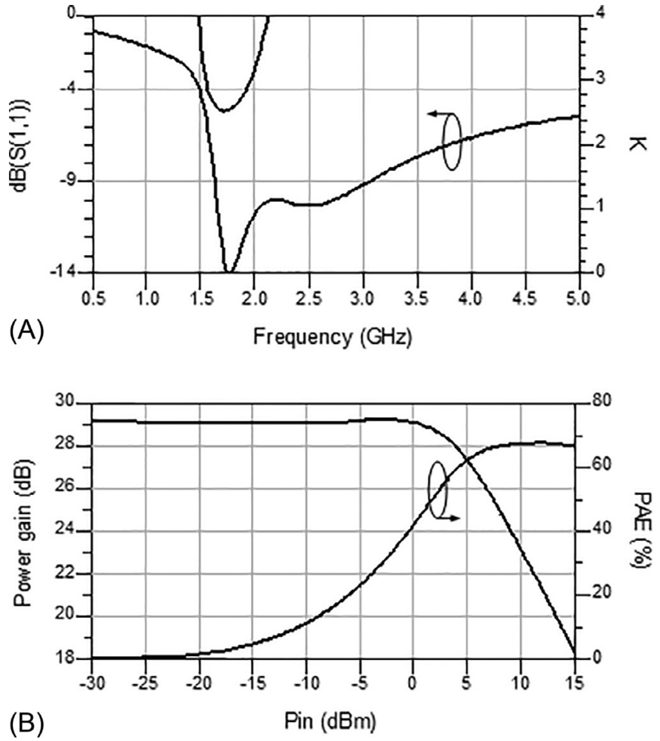
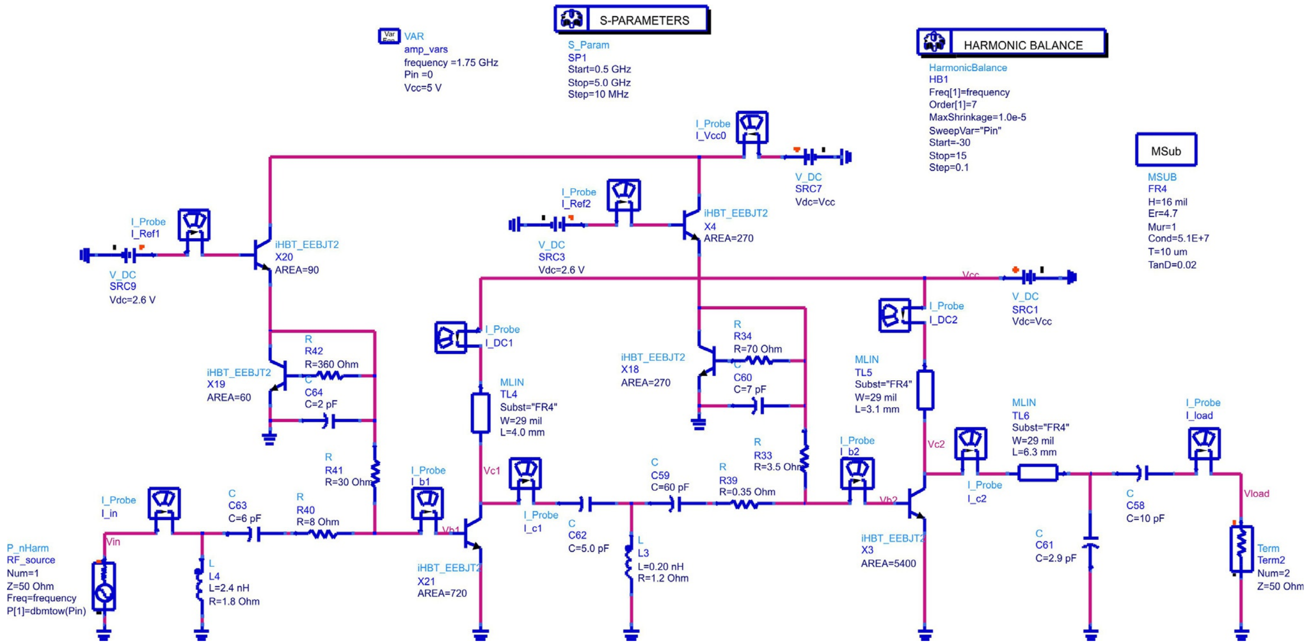


FIG. 13.58

Simulated (A) input return loss and *K*-factor and (B) power gain and *PAE* of two-stage power amplifier with lumped elements.



VAR
amp_vars
frequency =1.75 GHz
Pin =0
Vcc=5 V
S-PARAMETERS
S_Param
SP1
Start=0.5 GHz
Stop=5.0 GHz
Step=10 MHz
HARMONIC BALANCE
HarmonicBalance
HB1
Freq[1]=frequency
Order[1]=7
MaxShrinkage=1.0e-5
SweepVar="Pin"
Start=-30
Stop=15
Step=0.1
MSub
MSUB
FR4
H=16 mil
Er=4.7
Mur=1
Cond=5.1E+7
T=10 um
TanD=0.02
I_Probe
I_Vcc0
V_DC
SRC7
Vdc=Vcc
I_Probe
I_Ref2
V_DC
SRC3
Vdc=2.6 V
iHBT_EEBJT2
X4
AREA=270
I_Probe
I_Ref1
V_DC
SRC9
Vdc=2.6 V
iHBT_EEBJT2
X20
AREA=90
iHBT_EEBJT2
X19
AREA=60
R
R42
R=360 Ohm
C
C64
C=2 pF
R
R41
R=30 Ohm
Vcc
V_DC
SRC1
Vdc=Vcc
I_Probe
I_DC1
MLIN
TL4
Subst="FR4"
W=29 mil
L=4.0 mm
iHBT_EEBJT2
X18
AREA=270
R
R34
R=70 Ohm
C
C60
C=7 pF
R
R33
R=3.5 Ohm
I_Probe
I_DC2
MLIN
TL5
Subst="FR4"
W=29 mil
L=3.1 mm
MLIN
TL6
Subst="FR4"
W=29 mil
L=6.3 mm
I_Probe
I_load
I_Probe
I_in
Vin
P_nHarm
RF_source
Num=1
Z=50 Ohm
Freq=frequency
P[1]=dbmtow(Pin)
L
L4
L=2.4 nH
R=1.8 Ohm
C
C63
C=6 pF
R
R40
R=8 Ohm
I_Probe
I_b1
Vb1
iHBT_EEBJT2
X21
AREA=720
Vc1
I_Probe
I_c1
C
C62
C=5.0 pF
L
L3
L=0.20 nH
R=1.2 Ohm
C
C59
C=60 pF
R
R39
R=0.35 Ohm
I_Probe
I_b2
Vb2
iHBT_EEBJT2
X3
AREA=5400
Vc2
I_Probe
I_c2
C
C61
C=2.9 pF
C
C58
C=10 pF
Vload
Term
Term2
Num=2
Z=50 Ohm

FIG. 13.59

Simulation setup for two-stage Class-E power amplifier with microstrip lines.

where θ is the electrical length, Z_0 is the characteristic impedance, and Z_L is the load impedance.[16] For a short-circuited condition of $Z_L = 0$ or when $Z_0 >> Z_L$, we can write a simple equation

$$Z_{in} = jZ_0 \tan\theta. \tag{13.9}$$

Since the input impedance of a lumped inductance L is written as $Z_{in} = j\omega L$, the electrical length θ can be written as

$$\theta = \tan^{-1}\frac{\omega L}{Z_0}. \tag{13.10}$$

Then, the electrical lengths of the first-stage collector microstrip line, second-stage collector microstrip line, and series microstrip line in an output matching circuit can be respectively calculated as

$$\theta_1 = \tan^{-1}(0.284) = 15.85\,\text{degrees}$$

$$\theta_2 = \tan^{-1}(0.220) = 12.41\,\text{degrees}$$

$$\theta_3 = \tan^{-1}(0.462) = 24.79\,\text{degrees}.$$

Using the LineCalc program, available in Tools displayed by the project menu, results in the following geometrical length of the microstrip lines with a 29-mil width (characteristic impedance of ~50 Ω) implemented into the FR4 substrate with the parameters given in Fig. 13.58:

$$l_1 = 4.0\,\text{mm}$$

$$l_2 = 3.1\,\text{mm}$$

$$l_3 = 6.3\,\text{mm}.$$

Fig. 13.59 shows the simulation setup of the two-stage Class-E power amplifier with microstrip lines. In principle, there is no need to tune any circuit element. In this case, the maximum *PAE* of 67.1% and power gain of 22.5 dB with the output power of 33.6 dBm can be achieved, as shown in Fig. 13.60. At the same time, the output power of 33 dBm and power gain of 27 dB are provided with a *PAE* as high as 62.7%. Some small additional tuning of circuit parameters around their nominal values can probably

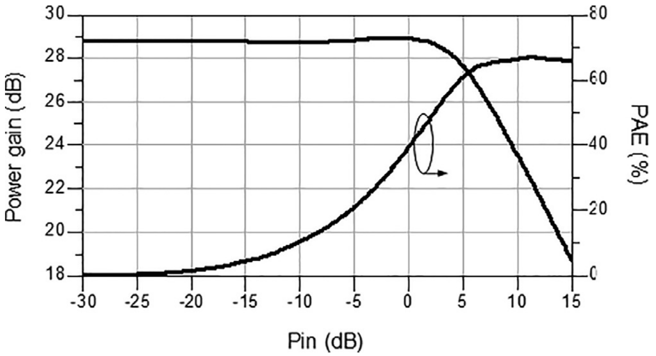


FIG. 13.60

Simulated power gain and *PAE* of two-stage Class-E power amplifier with microstrip lines.

slightly improve the performance. Hence, based on the example described above, you can see how effective a simple analytical approach with quick manual tuning (which can provide high performance and can significantly speed up the entire high-efficiency power-amplifier design procedure) is.

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